Stellaris® LM3S9B96 Development Kit

User's Manual

DK-LM3S9B96-01

Copyright

Texas Instruments
108 Wild Basin, Suite 350
Austin, TX 78746
Main: +1-512-279-8800
Fax: +1-512-279-8879
http://www.luminarymicro.com

Table of Contents

List of Figures

List of Tables

CHAPTER 1

Stellaris® LM3S9B96 Development Board

The Stellaris® LM3S9B96 Development Board provides a platform for developing systems around the advanced capabilities of the LM3S9B96 ARM® Cortex™-M3-based microcontroller.

The LM3S9B96 is a member of the Stellaris Tempest-class microcontroller family. Tempest-class devices include capabilities such as 80 MHz clock speeds, an External Peripheral Interface (EPI) and Audio I^2S interfaces. In addition to new hardware to support these features, the DK-LM3S9B96 board includes a rich set of peripherals found on other Stellaris boards.

The development board includes an on-board in-circuit debug interface (ICDI) that supports both JTAG and SWD debugging. A standard ARM 20-pin debug header supports an array of debugging solutions.

The Stellaris® LM3S9B96 Development Kit accelerates development of Tempest-class microcontrollers. The kit also includes extensive example applications and complete source code.

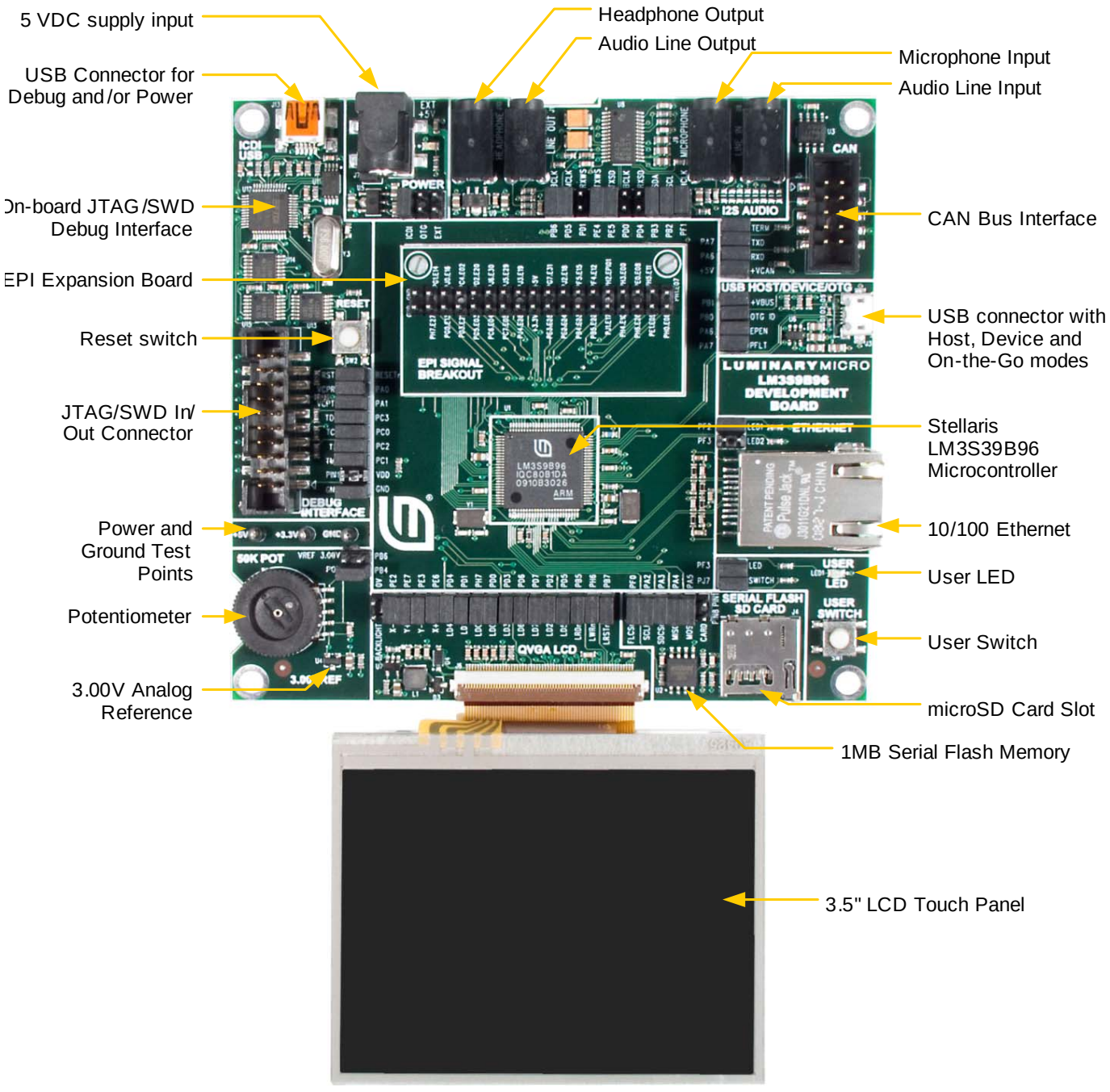
Features

The Stellaris® LM3S9B96 Development Board includes the following features.

- Simple set-up - USB cable provides debugging, communication, and power
- Flexible development platform with a wide range of peripherals
- Color LCD graphics display
  - TFT LCD module with 320 x 240 resolution
  - Resistive touch interface
- 80 MHz LM3S9B96 microcontroller with 256 K Flash, 96 K SRAM, and integrated Ethernet MAC+PHY, USB OTG, and CAN communications
  - – 8 MB SDRAM (plug-in EPI option board)
  - – EPI break-out board (plug-in option board)
- 1 MB serial Flash memory
- Precision 3.00 V voltage reference
- SAFE**RTOS**™ operating system in microcontroller ROM
- I^2S stereo audio codec
  - Line In/Out
  - Headphone Out
  - Microphone In
- Controller Area Network (CAN) Interface
- 10/100 BaseT Ethernet
- USB On-The-Go (OTG) Connector
  - Device, Host, and OTG modes

- User LED and push button
- Thumbwheel potentiometer (can be used for menu navigation)
- MicroSD card slot
- Supports a range of debugging options
  - Integrated In-circuit Debug Interface (ICDI)
  - JTAG, SWD, and SWO all supported
  - Standard ARM® 20-pin JTAG debug connector
- USB Virtual COM Port
- Jumper shunts to conveniently reallocate I/O resources
- Develop using tools supporting the DK-LM3S9B96 from Keil, IAR, Code Sourcery, and Code Red
- Supported by StellarisWare® software including the graphics library, the USB library, and the peripheral driver library

Figure 1-1. DK-LM3S9B96 Development Board



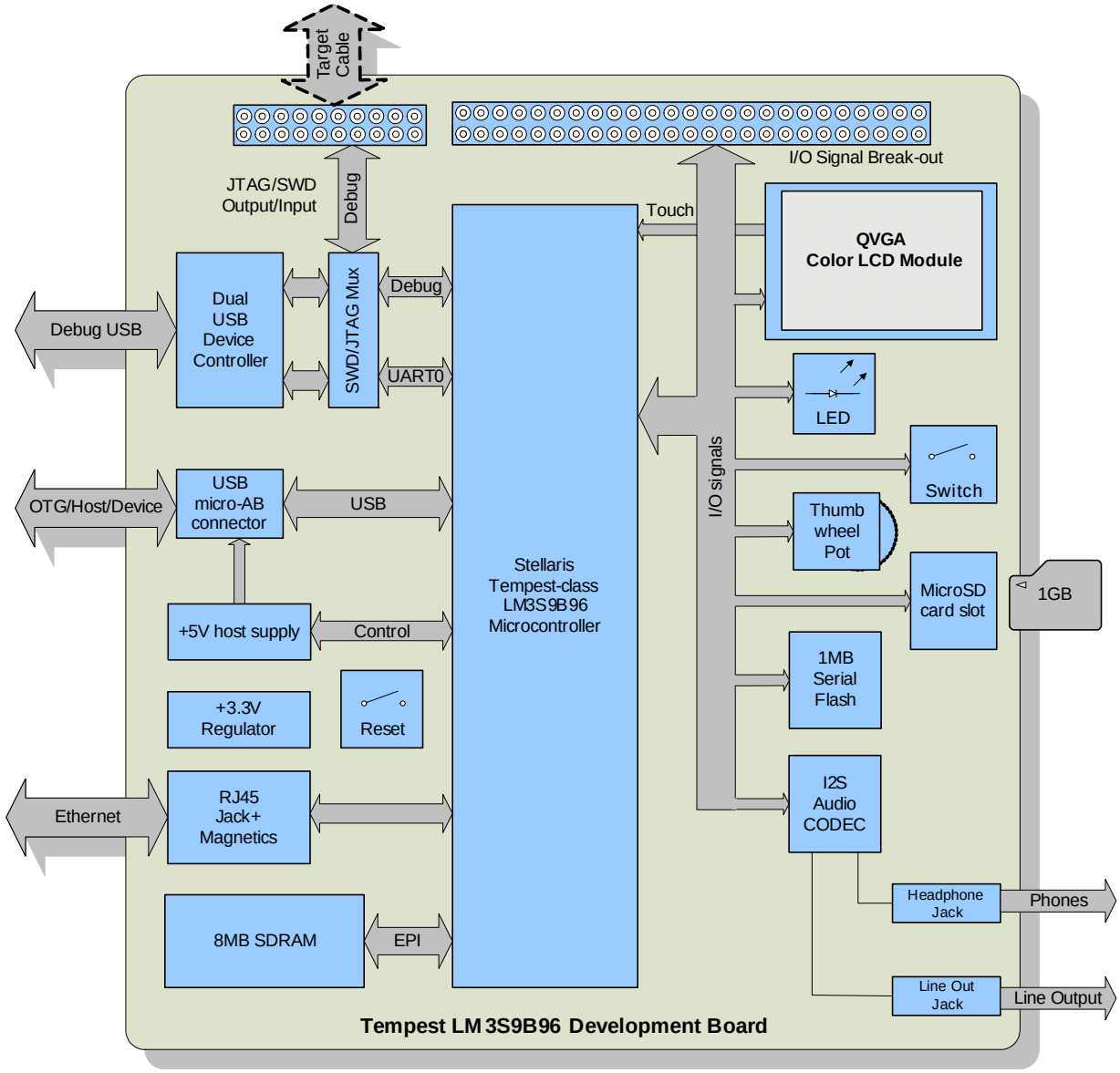
Development Kit Contents

The Stellaris® LM3S9B96 Development Kit contains everything needed to develop and run a range of applications using Stellaris microcontrollers:

- LM3S9B96 development board
- 8 MB SDRAM expansion board
- EPI signal breakout board
- Retractable Ethernet cable
- USB Mini-B cable for debugger use
- USB Micro-B cable for OTG-to-PC connection
- USB Micro-A to USB A adapter for USB Host
- USB Flash memory stick
- microSD Card
- 20-position ribbon cable
- CDs containing evaluation versions of the following tools:
  - StellarisWare with example code for this board
  - ARM RealView® Microcontroller Development Kit (MDK)
  - IAR Embedded Workbench® Kickstart Edition
  - Code Red Technologies Red Suite™
  - CodeSourcery Sourcery G++™ GNU tools.

Block Diagram

Figure 1-2. DK-LM3S9B96 Development Board Block Diagram



Development Board Specifications

- Board supply voltage: 4.75–5.25 Vdc from one of the following sources:
  - Debugger (ICDI) USB cable (connected to a PC)
  - USB Micro-B cable (connected to a PC)
  - DC power jack (2.1 x 5.5mm from external power supply)
- Break-out power output: 3.3 Vdc (100 mA max)

- Dimensions (excluding LCD panel):
  - 4.50” x 4.25” x 0.60” (LxWxH) with SDRAM board
  - 4.50” x 4.25” x 0.75” (LxWxH) with EPI breakout board
- Analog Reference: 3.0 V +/-0.2%
- RoHS status: Compliant

NOTE: When the LM3S9B96 Development Board is used in USB Host mode, the host connector is capable of supplying power to the connected USB device. The available supply current is limited to ~200 mA unless the development board is powered from an external 5 V supply with a =600mA rating.

CHAPTER 2

Hardware Description

In addition to an LM3S9B96 microcontroller, the development board includes a range of useful peripheral features and an integrated in-circuit debug interface (ICDI). This chapter describes how these peripherals operate and interface to the microcontroller

LM3S9B96 Microcontroller Overview

The Stellaris LM3S9B96 is an ARM Cortex-M3-based microcontroller with 256-KB flash memory, 80-MHz operation, Ethernet, USB, EPI, SAFE**RTOS**™ in ROM, and a wide range of peripherals. See the *LM3S9B96 Microcontroller Data Sheet* (order number DS-LM3S9B96) for complete microcontroller details.

The LM3S9B96 microcontroller is factory-programmed with a quickstart demo program. The quickstart program resides in on-chip flash memory and runs each time power is applied, unless the quickstart has been replaced with a user program.

Jumpers and GPIO Assignments

Each peripheral circuit on the development board is interfaced to the LM3S9B96 microcontroller through a 0.1” pitch jumper/shunt. Figure 2-1 on page 14 shows the factory default positions of the jumpers. The jumpers must be in these positions for the quickstart demo program to function correctly.

The development board offers capabilities that the LM3S9B96 cannot support simultaneously due to pin count and GPIO multiplexing limitations. For example, as configured, the board does not support SDRAM and I^2S receive (microphone or line input) functions at the same time. The jumpers associated with I^2S receive are omitted in the default configuration.

Table 2-1 lists all features and peripherals that are disconnected in the factory default configuration. Using these peripherals requires that other peripherals be disconnected. Appendix D, “Microcontroller GPIO Assignments,” on page 37 lists alternative jumper configurations used in conjunction with some of the StellarisWare™ example applications for this board.

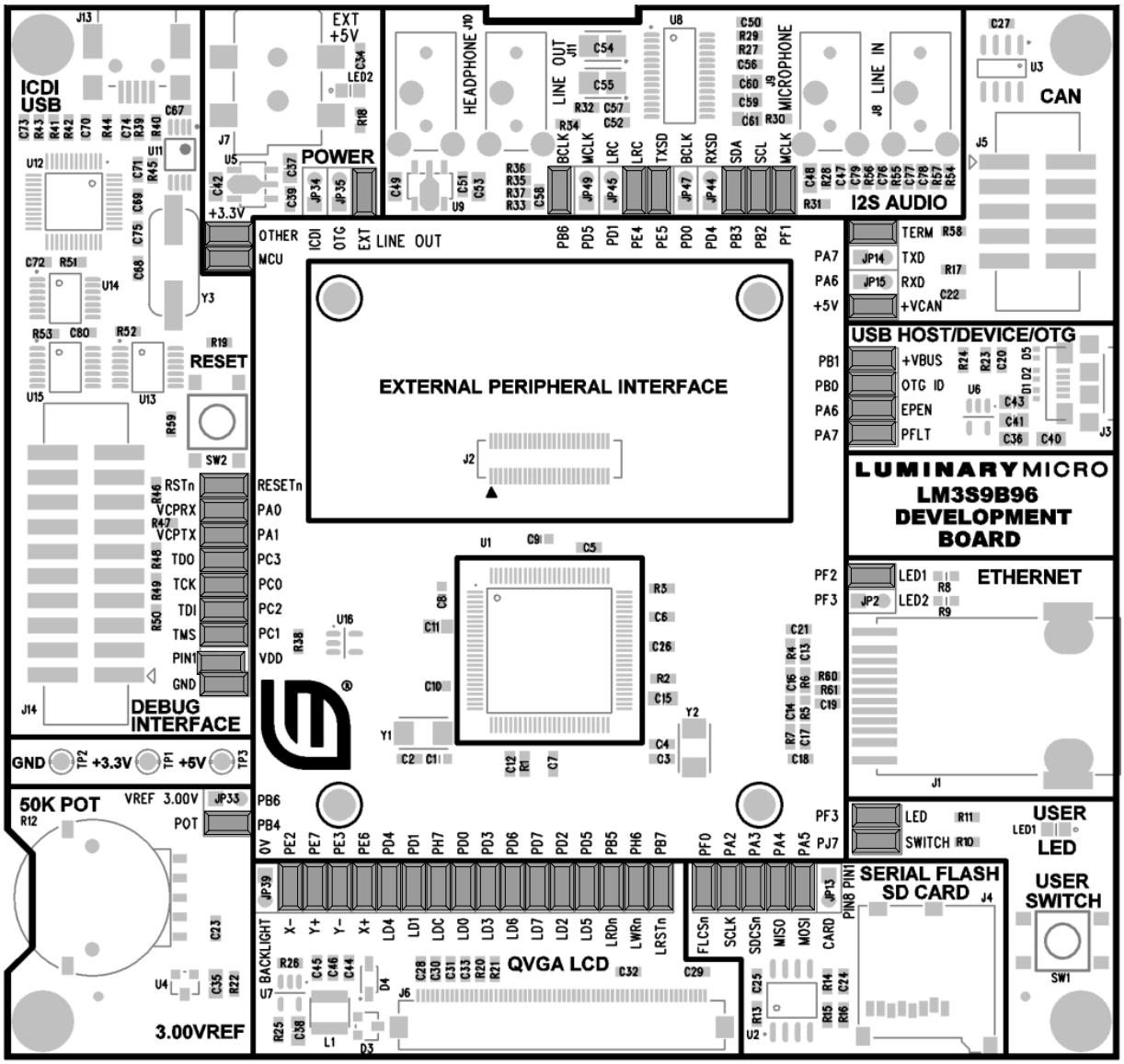
Table 2-1. Board Features and Peripherals that are Disconnected in Factory Default Configuration

Peripheral	Jumpers
I^2S Receive (Audio Input)	JP44, 45, 47, 49
Controller Area Network (CAN)	JP14, 15
Ethernet Yellow Status LED (LED2)	JP2
Analog 3.0V Reference	JP33

See Appendix D, “Microcontroller GPIO Assignments,” on page 37, for a complete list of GPIO assignments. The table lists all default and alternate assignments that are supported by the 0.1” jumpers and PCB routing. The LM3S9B96 has additional internal multiplexing that enables additional configurations which may require discrete wiring between peripherals and GPIO pins.

The ICDI section of the board has a GND-GND jumper that serves no function other than to provide a convenient place to ‘park’ a spare jumper. This jumper may be reused as required.

Figure 2-1. Factory Default Jumper Settings



Clocking

The development board uses a 16.0-MHz (Y2) crystal to complete the LM3S9B96 microcontroller's main internal clock circuit. An internal PLL, configured in software, multiples this clock to higher frequencies for core and peripheral timing.

A 25.0-MHz (Y1) crystal provides an accurate timebase for the Ethernet PHY.

Reset

The RESETn signal into the LM3S9B96 microcontroller connects to the reset switch (SW2) and to the ICDI circuit for a debugger-controlled reset.

External reset is asserted (active low) under any one of the three following conditions:

- Power-on reset (filtered by an R-C network)
- Reset push switch SW2 held down
- By the ICDI circuit (U12 FT2232, U13D 74LVC125A) when instructed by the debugger (this capability is optional, and may not be supported by all debuggers)

The LCD module has special Reset timing requirements requiring a dedicated control line from the microcontroller.

Power Supplies

The development board requires a regulated 5.0 V power source. Jumpers JP34-36 select the power source, with the default source being the ICDI USB connector. Only one +5 V source should be selected at any time to avoid conflict between the power sources.

When using USB in Host mode, the power source should be set to either ICDI or to EXT if a +5 V power supply (not included in the kit) is available.

The development board has two main power rails. A +3.3 V supply powers the microcontroller and most other circuitry. +5 V is used by the OTG USB port and In-circuit Debug Interface (ICDI) USB controller. A low drop-out (LDO) regulator (U5) converts the +5 V power rail to +3.3 V. Both rails are routed to test loops for easy access.

USB

The LM3S9B96's full-speed USB controller supports On-the-Go, Host, and Device configurations. See Table 2-2 for USB-related signals. The 5-pin microAB OTG connector supports all three interfaces in conjunction with the cables included in the kit.

The USB port has additional ESD protection diode arrays (D1, D2,D5) for up to 15 kV of ESD protection.

Table 2-2. USB-Related Signals

Microcontroller Pin	Board Function	Jumper Name
Pin 70 USB0DM	USB Data-	-
Pin 71 USB0DP	USB Data+	-
Pin 73 USB0RBIAS	USB bias resistor	-
Pin 66 USB0ID	OTG ID signal (input to microcontroller)	OTG ID
Pin 67 USB0VBUS	Vbus Level monitoring	+VBUS
Pin 34 USB0EPE	Host power enable (active high)	EPEN
Pin 35 USB0PFLT	Host power fault signal (active low)	PFLT

U6, a fault-protected switch, controls and monitors power to the USB host port. USB0EPEN, the control signal from the microcontroller, has a pull-down resistor to ensure host-port power remains off during reset. The power switch will immediately cut power if the attached USB device draws

more than 1 Amp, or if the switches' thermal limits are exceeded by a device drawing more than 500 mA. USB0PFLT indicates the over-current status back to the microcontroller.

The development board can be either a bus-powered USB device or self-powered USB device depending on the power-supply configuration jumpers.

When using the development board in USB-host mode, power to the EVB should be supplied by the In-circuit Debugger (ICDI) USB cable or by a +5 V source connected to the DC power jack.

Note that the LM3S9B96's USB capabilities are completely independent from the In-Circuit Debug Interface USB functionality.

Debugging

Stellaris microcontrollers support programming and debugging using either JTAG or SWD. JTAG uses the TCK, TMS, TDI, and TDO signals. SWD requires fewer signals (SWCLK, SWDIO, and, optionally, SWO for trace). The debugger determines which debug protocol is used.

Debugging Modes

The LM3S9B96 development board supports a range of hardware debugging configurations. Table 2-3 summarizes these configurations.

Table 2-3. Hardware Debugging Configurations

Mode	Debug Function	Use	Selected by...
1	Internal ICDI	Debug on-board LM3S9B96 microcontroller over Debug USB interface.	Default mode
2	ICDI out to JTAG/ SWD header	The development board is used as a USB to SWD/ JTAG interface to an external target.	Connecting to an external target and starting debug software.
3	In from JTAG/SWD header	For users who prefer an external debug interface (ULINK, JLINK, etc.) with the EVB.	Connecting an external debugger to the JTAG/SWD header

Debug In Considerations

Debug Mode 3 supports board debugging using an external debug interface such as a Segger J-Link or Keil ULINK. Most debuggers use Pin 1 of the Debug connector to sense the target voltage and, in some cases, power the output logic circuit. Installing the VDD/PIN1 jumper will apply 3.3 V power to this pin in order to support external debuggers.

Debug USB Overview

An FT2232 device from Future Technology Devices International Ltd implements USB-to-serial conversion. The FT2232 is factory-configured to implement a JTAG/SWD port (synchronous serial) on channel A and a Virtual COM Port (VCP) on channel B. This feature allows two simultaneous communications links between the host computer and the target device using a single USB cable. Separate Windows drivers for each function are provided on the Documentation and Software CD.

The In-Circuit Debug Interface USB capabilities are completely independent from the LM3S9B96's on-chip USB functionality.

A small serial EEPROM holds the FT2232 configuration data. The EEPROM is not accessible by the LM3S9B96 microcontroller. For full details on FT2232 operation, go to www.ftdichip.com.

USB to JTAG/SWD

The FT2232 USB device performs JTAG/SWD serial operations under the control of the debugger. A simple logic circuit multiplexes SWD and JTAG functions and, when working in SWD mode, provides direction control for the bidirectional data line.

Virtual COM Port

The Virtual COM Port (VCP) allows Windows applications (such as HyperTerminal) to communicate with UART0 on the LM3S9B96 over USB. Once the FT2232 VCP driver is installed, Windows assigns a COM port number to the VCP channel. Table 2-4 shows the debug-related signals.

Table 2-4. Debug-Related Signals

Microcontroller Pin	Board Function	Jumper Name
Pin 77 TDO/SWO	JTAG data out or trace data out	TDO
Pin 78 TDI	JTAG data in	TDI
Pin 79 TMS/SWDIO	JTAG TMS or SWD data in/out	TMS
Pin 80 TCK/SWCLK	JTAG Clock or SWD clock	TCK
Pin 26 PA0/U0RX	Virtual Com port data to LM3S9B96	VCPRX
Pin 27 PA1/U0TX	Virtual Com port data from LM3S9B96	VCPTX
Pin 64 RSTn	System Reset	RSTn

Serial Wire Out (SWO)

The development board supports the Cortex-M3 Serial-Wire Output (SWO) trace capabilities. Under debugger control, on-board logic can route the SWO datastream to the VCP transmit channel. The debugger software can then decode and interpret the trace information received from the Virtual Com Port. The normal VCP connection to UART0 is interrupted when using SWO. Not all debuggers support SWO.

See the *Stellaris LM3S9B96 Microcontroller Data Sheet* for additional information on the Trace Port Interface Unit (TPIU).

Color QVGA LCD Touch Panel

The development board features a TFT Liquid Crystal graphics display with 320 x 240 pixel resolution. The display is protected during shipping by a thin, protective plastic film which should be removed before use.

Features

Features of the LCD module include:

- Kitronix K350QVG-V1-F display
- 320 x RGB x 240 dots
- 3.5" 262 K colors

- Wide temperature range
- White LED backlight
- Integrated RAM
- Resistive touch panel

Control Interface

The Color LCD module has a built-in controller IC with a multi-mode parallel interface. The development board uses an 8-bit 8080 type interface with GPIO Port D providing the data bus. Table 2-4 shows the LCD-related signals.

Table 2-5. LCD-Related Signals

Microcontroller Pin	Board Function	Jumper Name
PE6/ADC1	Touch X+	X+
PE3	Touch Y-	Y-
PE2	Touch X-	X-
PE7/ADC0	Touch Y+	Y+
PB7	LCD Reset	LRSTn
PD0..7	LCD Data Bus 0..7	LD0..7
PH7	LCD Data/Control Select	LDC
PB5	LCD Read Strobe	LRDn
PH6	LCD Write Strobe	LWRn
-	Backlight control	BLON

Backlight

The white LED backlight must be powered for the display to be clearly visible. U7 (FAN5331B) implements a 20 mA constant-current LED power source to the backlight. The backlight is not normally controlled by the microcontroller, however, the control signal is available on a header. A jumper may be installed to disable the backlight by connecting it to GND. Alternatively, a wire may be used to control this signal from a spare microcontroller GPIO line.

Because the FAN5331B operates in a constant current mode, its output voltage will jump up if the LCD should become disconnected. To prevent over-voltage failure of the IC or diode D3, a zener (D4) clamps the voltage. The current will limit to 20 mA, but the total board current will be higher than when the LCD panel is connected. To avoid over-heating the backlighting circuit, install the BLON jumper to completely shut-down the backlighting circuit.

Power

The LCD module has internal bias voltage generators and requires only a single 3.3 V dc supply.

Resistive Touch Panel

The 4-wire resistive touch panel interfaces directly to the microcontroller, using 2 ADC channels and 2 GPIO signals. See the StellarisWare™ source code for additional information on touch panel implementation.

I²S Audio

The LM3S9B96 development board has advanced audio capabilities using an I²S-connected Audio TLV320AIC23 CODEC. The factory default configuration has Audio output (Line Out and/or Headphone output) enabled. Four additional I²S signals are required for Audio input (Line Input and/or Microphone). All four audio interfaces are through 1/8" (3.5mm) stereo jacks. Table 2-6 shows the I²S audio-related signals.

Table 2-6. I²S Audio-Related Signals

Microcontroller Pin	Board Function	Jumper Name
I2C0SDA	CODEC Configuration Data	SDA
I2C0SCL	CODEC Configuration Clock	SCL
I2STXSD	Audio Out Serial Data	TXSD
I2STXWS	Audio Out Framing signal	TXWS
I2STXSCK	Audio Out Bit Clock	BCLK[a]
I2STXMCLK	Audio Out System Clock	MCLK
I2SRXSD	Audio In Serial Data	RXSD[b]
I2SRXWS	Audio In Framing signal	RXWS[b]
I2SRXSCK	Audio In Bit Clock	BCLK[b]
I2SRXMCLK	Audio In System Clock	MCLK[b]

a. Shares GPIO line with Analog voltage reference. Jumper installed by default.
b. Shares GPIO line with LCD data bus – Port D. Jumper omitted by default.

The Audio CODEC has a number of control registers which are configured using the I²C bus signals. CODEC settings can only be written, but not read, using I²C. See the StellarisWare™ example applications for programming information and the TLV320AIX23B data sheet for complete register details.

The Headphone output can be connected directly to any standard headphones. The Line Output is suitable for connection to an external amplifier, including PC desktop speaker sets.

User Switch and LED

The development board provides a user push-switch and LED (see Table 2-7).

Table 2-7. Navigation Switch-Related Signals

Microcontroller Pin	Board Function	Jumper Name
PJ7	User Switch	SWITCH
PF3	User LED	LED[a]

a. Shared with Ethernet Jack Yellow LED. This jumper is installed by default.

CHAPTER 3

External Peripheral Interface (EPI)

The External Peripheral Interface (EPI) is a high-speed 8/16/32-bit parallel bus for connecting external peripherals or memory without glue logic. Supported modes include SDRAM, SRAM, and Flash memories, as well as Host-bus and FIFO modes.

The LM3S9B96 development kit includes an 8 MB SDRAM board in addition to an EPI break-out board. Other EPI expansion boards may be available.

SDRAM Expansion Board

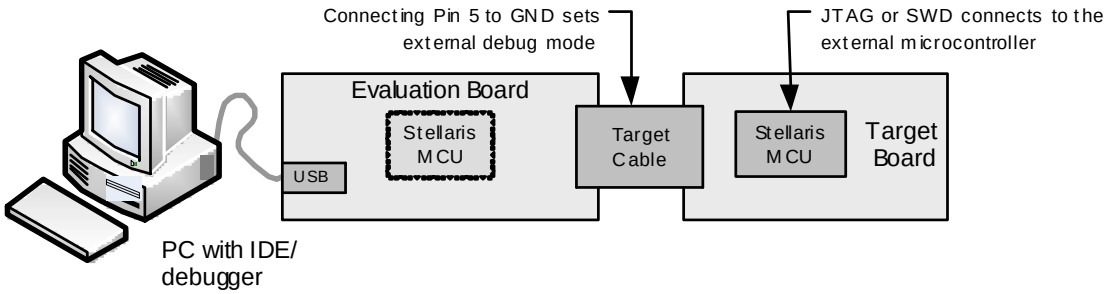
The SDRAM board provides 8 MB of memory (4M x 16) which, once configured, becomes part of the LM3S9B96's memory map at either 0x6000.0000 or 0x8000.0000. The SDRAM interface multiplexes DQ00..14 and AD/BA0..14 without requiring external latches or buffers. Of the 32 EPI signals, only 24 are used in SDRAM mode, with the remaining signals used for non-EPI functions on the board.

CHAPTER 4

Using the In-Circuit Debugger Interface

The Stellaris® LM3S9B96 Development Kit can operate as an In-Circuit Debugger Interface (ICDI). ICDI acts as a USB to the JTAG/SWD adaptor, allowing debugging of any external target board that uses a Stellaris microcontroller. See “Debugging Modes” on page 16 for a description of how to enter Debug Out mode.

Figure 4-1. ICD Interface Mode



The debug interface operates in either serial-wire debug (SWD) or JTAG mode, depending on the configuration in the debugger IDE.

The IDE/debugger does not distinguish between the on-board Stellaris microcontroller and an external Stellaris microcontroller. The only requirement is that the correct Stellaris device is selected in the project configuration.

The Stellaris target board should have a 2x10 0.1” pin header with signals as indicated in Table C-1 on page 35. This applies to both an external Stellaris microcontroller target (Debug Output mode) and to external JTAG/SWD debuggers (Debug Input mode).

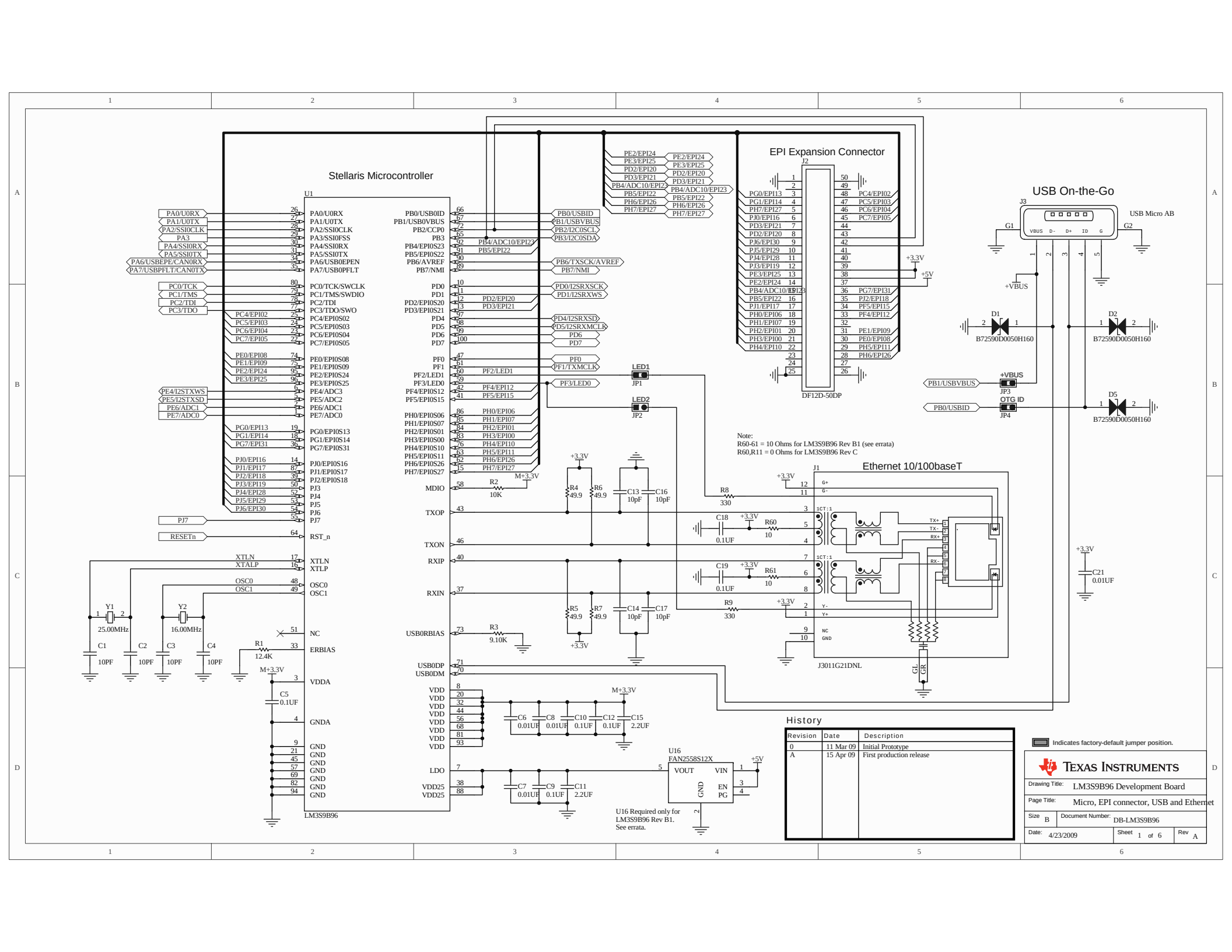
ICDI does not control RST (device reset) or TRST (test reset) signals. Both reset functions are implemented as commands over JTAG/SWD, so these signals are usually not necessary.

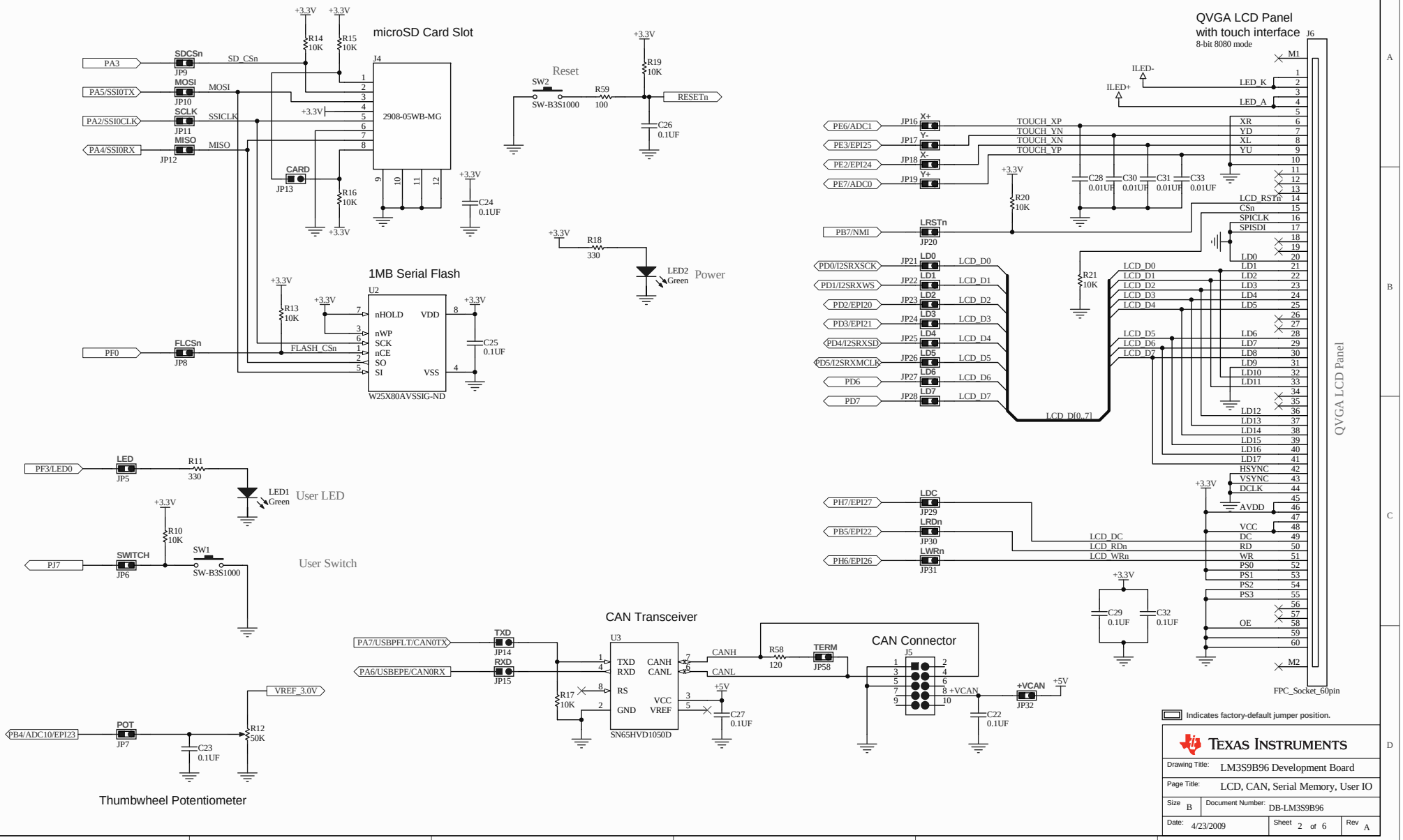
It is recommended that connections be made to all GND pins; however, both targets and external debug interfaces must connect pin 5 and at least one other GND pin to GND. Some external debug interfaces may require a voltage on Pin 1 to set line driver thresholds. The development board ICDI circuit automatically sets Pin 1 high if an external debugger is connected. In other modes this pin is unused.

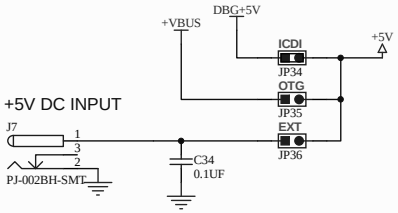
APPENDIX A

Schematics

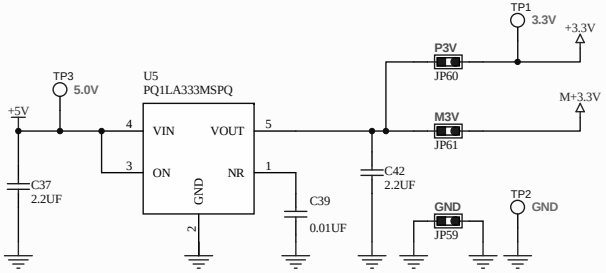
This section contains the schematics for the DK-LM3S9B96 development board.


Stellaris Microcontroller
U1
LM3S9B96
EPI Expansion Connector
J2
DF12D-50DP
USB On-the-Go
J3
USB Micro AB
B72590D0050H160
Ethernet 10/100baseT
J1
J3011G21DNL
LED1
LED2
JP1
JP2
JP3
JP4
OTG ID
+VBUS
Y1
25.00MHz
Y2
16.00MHz
U16
FAN2558S12X
U16 Required only for LM3S9B96 Rev B1. See errata.
Note:
R60-61 = 10 Ohms for LM3S9B96 Rev B1 (see errata)
R60,R11 = 0 Ohms for LM3S9B96 Rev C
History
Revision | Date | Description
0 | 11 Mar 09 | Initial Prototype
A | 15 Apr 09 | First production release
Indicates factory-default jumper position.
TEXAS INSTRUMENTS
Drawing Title: LM3S9B96 Development Board
Page Title: Micro, EPI connector, USB and Ethernet
Size: B
Document Number: DB-LM3S9B96
Date: 4/23/2009
Sheet 1 of 6
Rev A

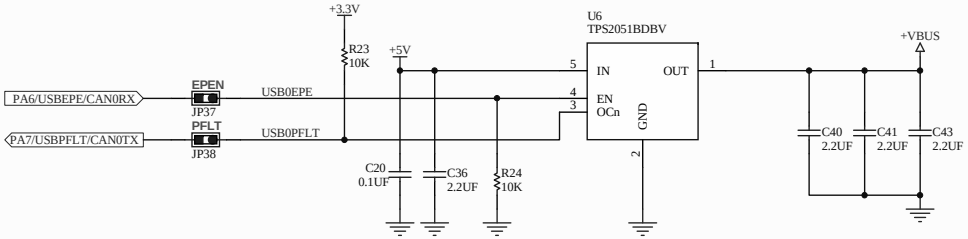

microSD Card Slot
Reset
QVGA LCD Panel
with touch interface
8-bit 8080 mode
1MB Serial Flash
Power
User LED
User Switch
CAN Transceiver
CAN Connector
Thumbwheel Potentiometer
QVGA LCD Panel
FPC_Socket_60pin
Indicates factory-default jumper position.
TEXAS INSTRUMENTS
Drawing Title: LM3S9B96 Development Board
Page Title: LCD, CAN, Serial Memory, User IO
Size B
Document Number: DB-LM3S9B96
Date: 4/23/2009
Sheet 2 of 6
Rev A



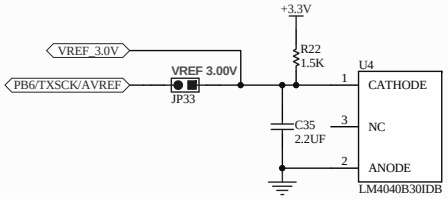
Power Source Selection



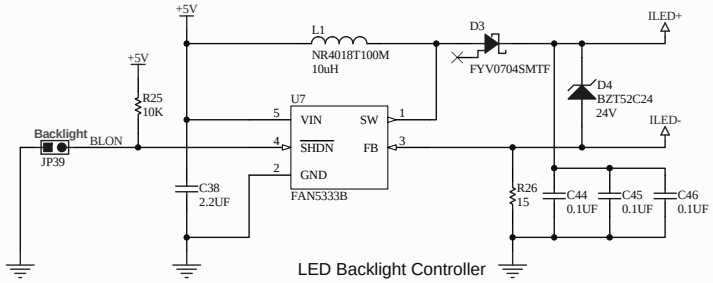
Main +3.3V Supply



VBUS Fault Protected Switch



3.0V 0.2% Voltage Reference

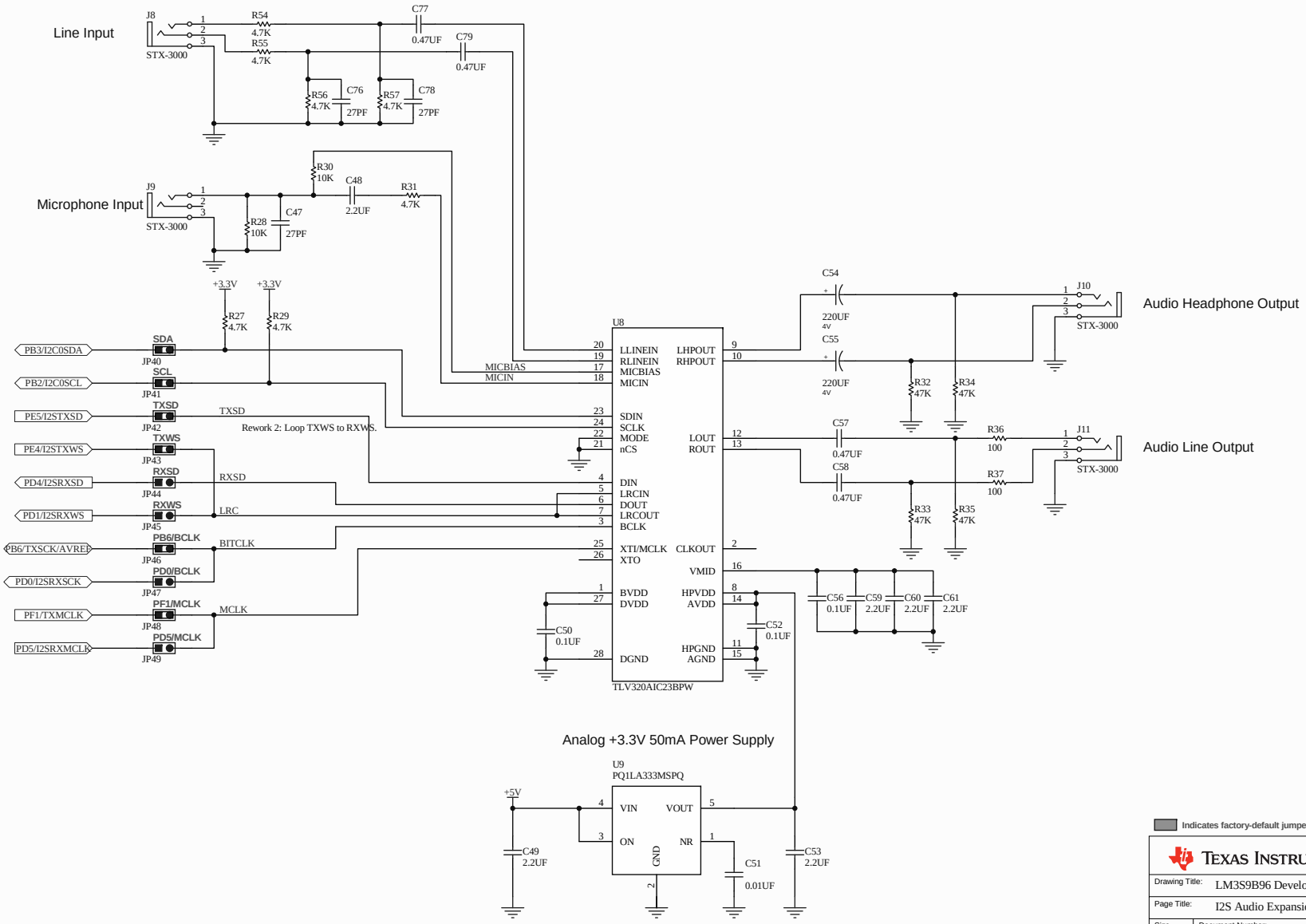


LED Backlight Controller

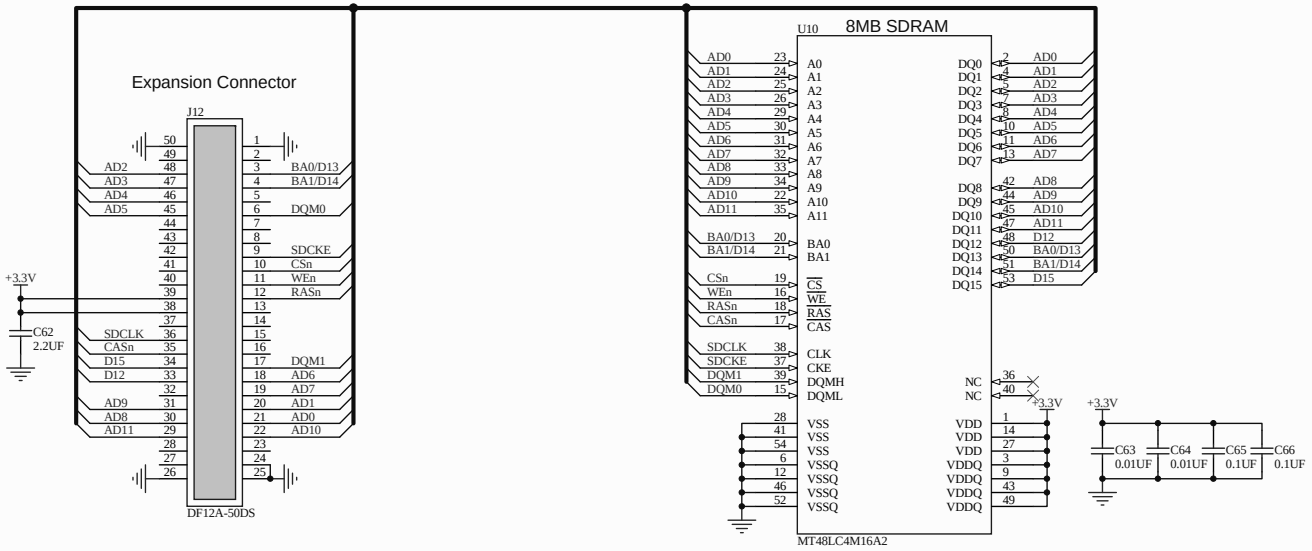
Indicates factory-default jumper position.

TEXAS INSTRUMENTS

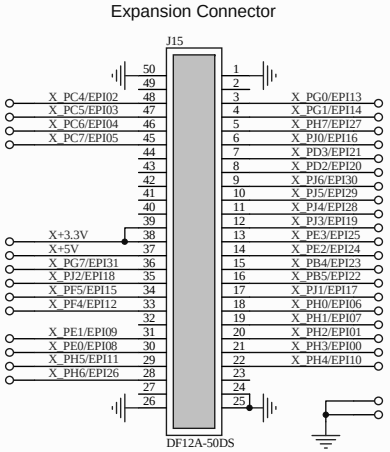
Drawing Title:	LM3S9B96 Development Board
Page Title:	Power Supplies
Size: B	Document Number: DB-LM3S9B96
Date: 4/23/2009	Sheet 3 of 6 — Rev A


Line Input
J8
STX-3000
R54 4.7K
R55 4.7K
C77 0.47UF
C79 0.47UF
R56 4.7K
C76 27PF
R57 4.7K
C78 27PF
Microphone Input
J9
STX-3000
R30 10K
C48 2.2UF
R31 4.7K
R28 10K
C47 27PF
+3.3V
R27 4.7K
R29 4.7K
SDA
SCL
TXSD
TXWS
RXSD
RXWS
PB6/BCLK
PD0/BCLK
PF1/MCLK
PD5/MCLK
JP40
JP41
JP42
JP43
JP44
JP45
JP46
JP47
JP48
JP49
PB3/I2C0SDA
PB2/I2C0SCL
PE5/I2STXSD
PE4/I2STXWS
PD4/I2SRXSD
PD1/I2SRXWS
PB6/TXSCK/AVREF
PD0/I2SRXSCK
PF1/TXMCLK
PD5/I2SRXMCLK
TXSD
Rework 2: Loop TXWS to RXWS.
RXSD
LRC
BITCLK
MCLK
MICBIAS
MICIN
U8
LLINEIN
RLINEIN
MICBIAS
MICIN
SDIN
SCLK
MODE
nCS
DIN
LRCIN
DOUT
LRCOUT
BCLK
XTI/MCLK
XTO
BVDD
DVDD
DGND
LHPOUT
RHPOUT
LOUT
ROUT
CLKOUT
VMID
HPVDD
AVDD
HPGND
AGND
TLV320AIC23BPW
C50 0.1UF
C52 0.1UF
C54 220UF 4V
C55 220UF 4V
C56 0.1UF
C59 2.2UF
C60 2.2UF
C61 2.2UF
R32 47K
R34 47K
R33 47K
R35 47K
C57 0.47UF
C58 0.47UF
R36 100
R37 100
J10
J11
STX-3000
Audio Headphone Output
Audio Line Output
Analog +3.3V 50mA Power Supply
U9
PQ1LA333MSPQ
+5V
VIN
VOUT
ON
NR
GND
C49 2.2UF
C51 0.01UF
C53 2.2UF
Indicates factory-default jumper position.
Texas Instruments
Drawing Title: LM3S9B96 Development Board
Page Title: I2S Audio Expansion Board
Size B
Document Number: DB-LM3S9B96
Date: 4/23/2009
Sheet 4 of 6
Rev A

SDRAM Expansion Board

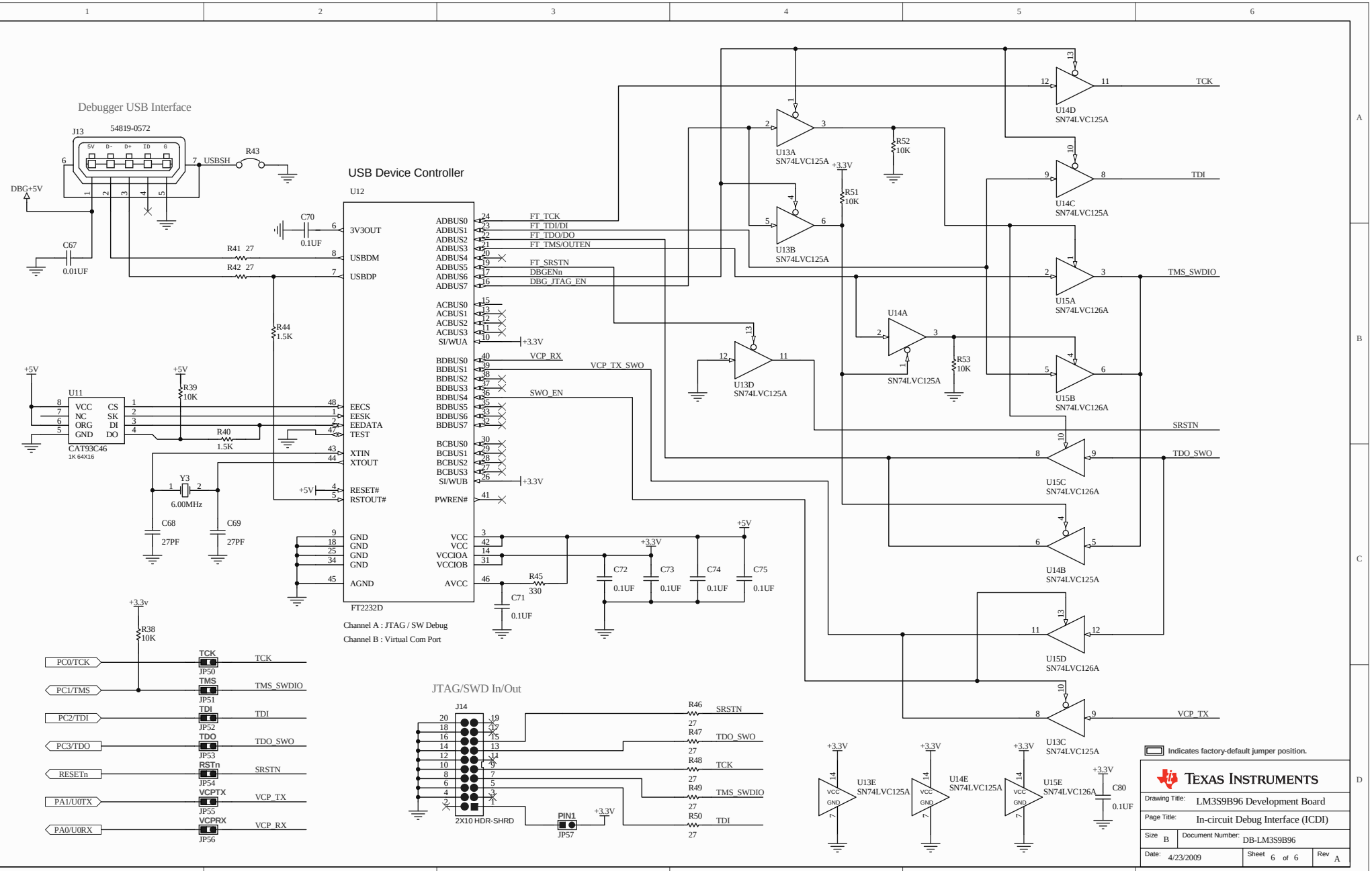


EPI Signal Breakout Board



Drawing Title:	LM3S9B96 Development Board
Page Title:	EPI and SDRAM Expansion Boards
Size: B	Document Number: DB-LM3S9B96
Date: 4/23/2009	Sheet 5 of 6
	Rev A

Texas Instruments

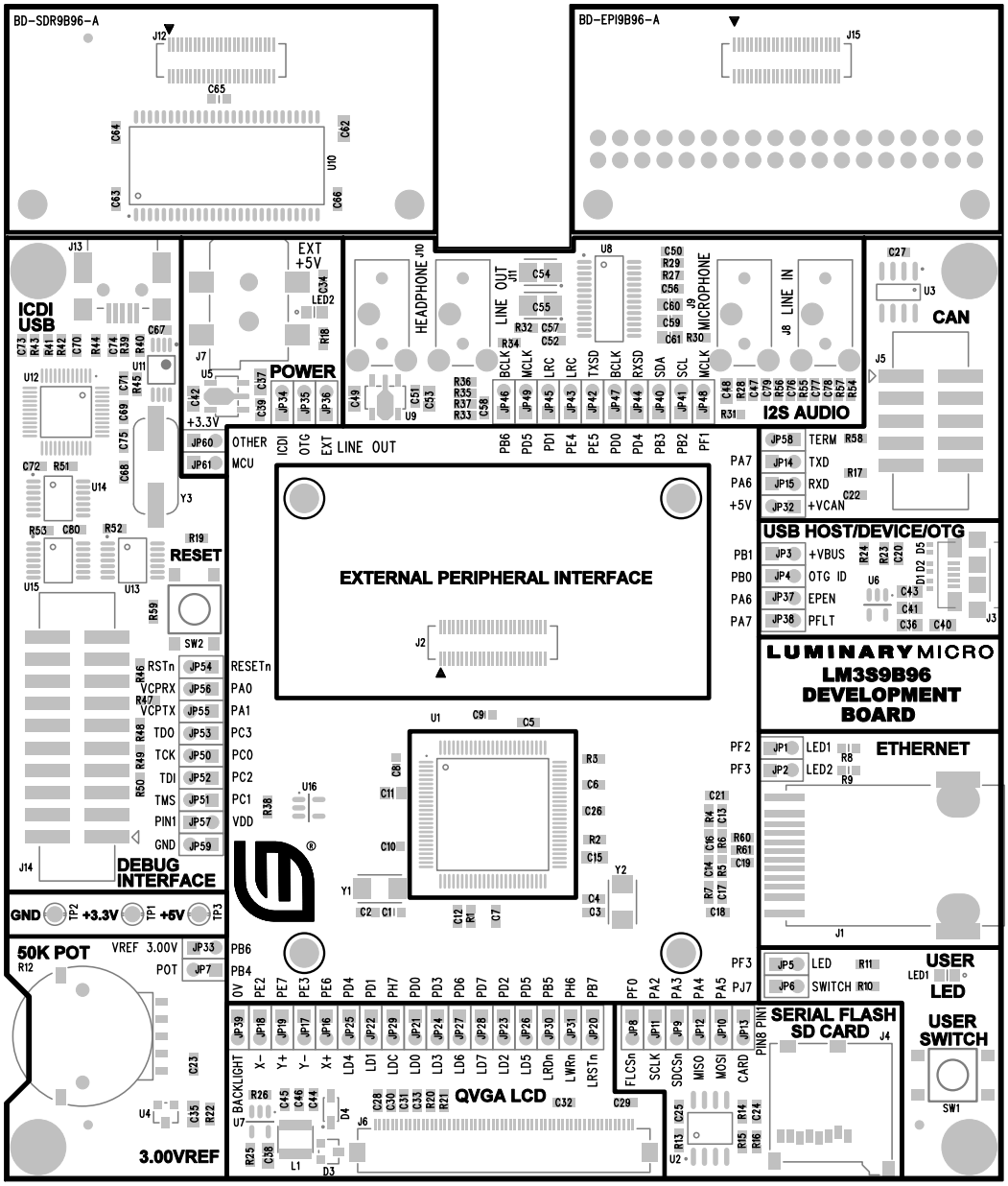

Debugger USB Interface
USB Device Controller
JTAG/SWD In/Out
Channel A : JTAG / SW Debug
Channel B : Virtual Com Port
Indicates factory-default jumper position.
TEXAS INSTRUMENTS
Drawing Title: LM3S9B96 Development Board
Page Title: In-circuit Debug Interface (ICDI)
Size B
Document Number: DB-LM3S9B96
Date: 4/23/2009
Sheet 6 of 6
Rev A

Component Locations

This appendix contains details on component locations, including:

- Component placement plot for top (Figure B-1)

Figure B-1. Component placement plot for top



A P P E N D I X C

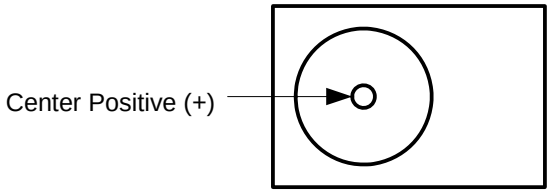
Connection Details

This appendix contains the following sections:

- DC Power Jack (see page 35)
- ARM Target Pinout (see page 35)

DC Power Jack

The EVB provides a DC power jack for connecting an external +5 V regulated (+/-5%) power source.



The socket is 5.5 mm dia with a 2.1 mm pin.

ARM Target Pinout

In ICDI input and output mode, the Stellaris® LM3S9B96 Development Kit supports ARM's standard 20-pin JTAG/SWD configuration. The same pin configuration can be used for debugging over serial-wire debug (SWD) and JTAG interfaces.

Table C-1. Debug Interface Pin Assignments

Function	Pin Number
TDI	5
TDO/SWO	13
TMS/SWDIO	7
TCK/SWCLK	9
System Reset	15
VDD	1
GND	4, 6, 8, 10, 12, 14, 16, 18, 20
No Connect	2, 3, 11, 17, 19

Insert Jumper VDD/PIN1 Jumper (JP57) only when using the development board with an external debug interface such as a ULINK or JLINK.

A P P E N D I X D

Microcontroller GPIO Assignments

Table D-1 shows the pin assignments for the LM3S9B96 microcontroller.

Table D-1. Microcontroller GPIO Assignments

LM3S9B96 GPIO Pin		Development Board Use			
Number	**Description**	**Default Function**	**Default Use**	**Alt. Function**	**Alternate Use**
26	PA0	U0Rx	Virtual Com Port		
27	PA1	U0Tx	Virtual Com Port		
28	PA2	SSI0Clk	SPI		
29	PA3	SSI0Fss	SD Card CSn		
30	PA4	SSI0Rx	SPI		
31	PA5	SSI0Tx	SPI		
34	PA6	USB0EPEN	USB Pwr Enable	CAN0RX	
35	PA7	USB0PFLT	USB Pwr Fault	CAN0TX	
66	PB0	USB0ID	USB OTG ID		
67	PB1	USB0VBUS	USB Vbus		
72	PB2	I2C0SCL	Audio I2C		
65	PB3	I2C0SDA	Audio I2C		
92	PB4	ADC10	Potentiometer	EPI0S23	EPI Breakout
91	PB5	PB5	LCD RDn	EPI0S22	EPI Breakout
90	PB6	PB6	I2STXSCK	AVREF	Ext Volt Ref
89	PB7	PB7	LCD RST		
80	PC0	TCK/SWCLK	JTAG		
79	PC1	TMS/SWDIO	JTAG		
78	PC2	TDI	JTAG		
77	PC3	TDO/SWO	JTAG		
25	PC4	EPI0S2	SDRAM D02		EPI0S02
24	PC5	EPI0S3	SDRAM D03		EPI0S03
23	PC6	EPI0S4	SDRAM D04		EPI0S04
22	PC7	EPI0S5	SDRAM D05		EPI0S05
10	PD0	PD0	LCD Data 0	I2SRXSCK	I2S Audio In

Table D-1. Microcontroller GPIO Assignments (Continued)

LM3S9B96 GPIO Pin		Development Board Use			
Number	**Description**	**Default Function**	**Default Use**	**Alt. Function**	**Alternate Use**
11	PD1	PD1	LCD Data 1	I2S0RXWS	I2S Audio In
12	PD2	PD2	LCD Data 2	EPI0S20	EPI Breakout
13	PD3	PD3	LCD Data 3	EPI0S21	EPI Breakout
97	PD4	PD4	LCD Data 4	I2SRXSD	I2S Audio In
98	PD5	PD5	LCD Data 5	I2SRXMCLK	I2S Audio In
99	PD6	PD6	LCD Data 6		
100	PD7	PD7	LCD Data 7		
74	PE0	EPI0S8	SDRAM D8		EPI0S08
75	PE1	EPI0S9	SDRAM D9		EPI0S09
95	PE2	PE2	Touch XN		EPI0S24
96	PE3	PE3	Touch YN		EPI0S25
6	PE4	I2STXWS	I2S Audio Out		
5	PE5	I2STXSD	I2S Audio Out		
2	PE6	ADC1	ADC Touch XP		
1	PE7	ADC0	ADC Touch YP		
47	PF0	PF0	Flash CSn		
61	PF1	I2STXMCLK	I2S Audio Out		
60	PF2	LED1	Green Enet LED		
59	PF3	PF3	User LED	LED0	Yw Enet LED
42	PF4	EPI0S12	SDRAM D12		
41	PF5	EPI0S15	SDRAM D15		
19	PG0	EPI0S13	SDRAM D13		
18	PG1	EPI0S14	SDRAM D14		
36	PG7	EPI0S31	SDRAM CLK		
86	PH0	EPI0S06	SDRAM D06		
85	PH1	EPI0S07	SDRAM D07		
84	PH2	EPI0S01	SDRAM D01		
83	PH3	EPI0S00	SDRAM D00		
76	PH4	EPI0S10	SDRAM D10		
63	PH5	EPI0S11	SDRAM D11		

Table D-1. Microcontroller GPIO Assignments (Continued)

LM3S9B96 GPIO Pin		Development Board Use			
Number	**Description**	**Default Function**	**Default Use**	**Alt. Function**	**Alternate Use**
62	PH6	EPI0S26	LCD_WRn	EPI0S26	EPI Breakout
15	PH7	EPI0S27	LCD_DC	EPI0S27	EPI Breakout
14	PJ0	EPI0S16	SDRAM DQM		
87	PJ1	EPI0S17	SDRAM DQM		
39	PJ2	EPI0S18	SDRAM CAS		
50	PJ3	EPI0S19	SDRAM RAS		
52	PJ4	EPI0S28	SDRAM WEn		
53	PJ5	EPI0S29	SDRAM CSn		
54	PJ6	EPI0S30	SDRAM SDCKE		
55	PJ7	PJ7	User Switch		

APPENDIX E

References

In addition to this document, the following references are included on the Stellaris Family Development Kit documentation CD-ROM and are also available for download at www.luminarymicro.com:

- *Stellaris LM3S9B96 Data Sheet*, publication number DS-LM3S9B96
- *Kitronix LCD Data Sheet*
- StellarisWare Driver Library
- *StellarisWare Driver Library User's Manual*, publication number SW-DRL-UG

Additional references include:

- *FT2232D Dual USB/UART FIFO IC Data sheet*, version 0.91, 2006, Future Technology Devices International Ltd.
- *Texas Instruments TLV320AIC23BPM Audio CODEC Data Sheet*

Important Notice

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265