

# LCD segment driver

## BU9706KS

The BU9706KS is a 40-output LCD segment driver provided with a 40-bit shift register and a 40-bit latch.

As the 40-bit shift register can be divided into two 20-bit sections, it can be used efficiently, based on the number of segments and the character configuration.

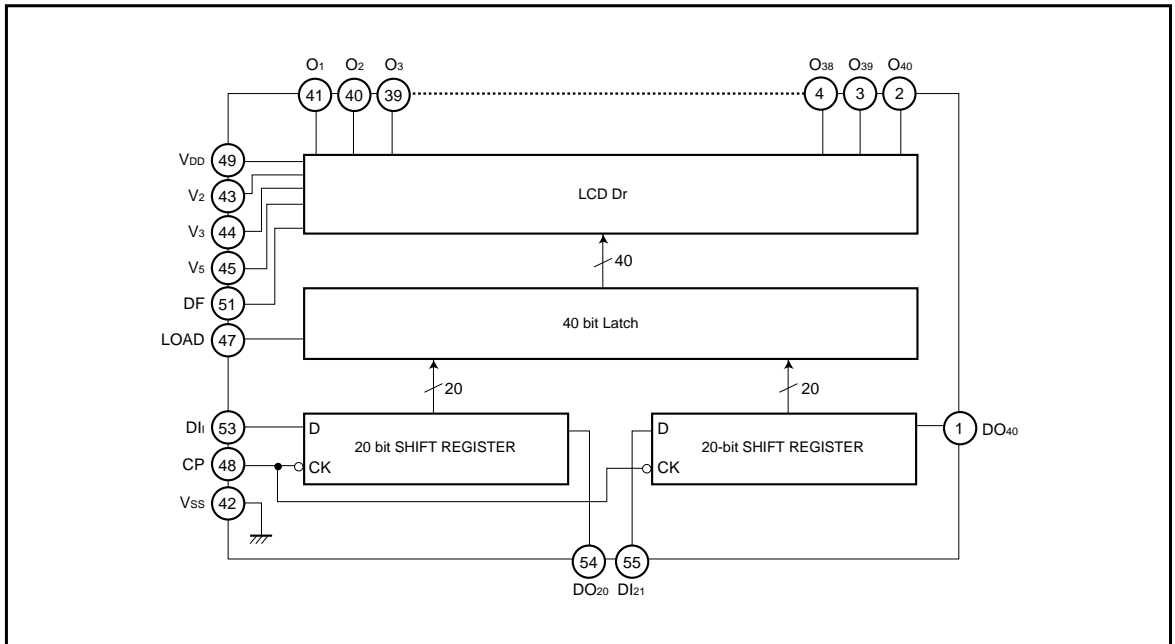
Also, by using a number of BU9706KS drivers, it is possible to configure an LCD segment driver of more than 80 bits.

As the liquid crystal drive voltage can be set externally to any value, it can be used as a driver IC for both static and dynamic drive in various types of liquid crystal display panels.

### ●Features

- 1) 40-bit shift register and 40-bit latch enable serial input - parallel output.
- 2) Shift register can be divided into two 20-bit sections.
- 3) Power supply voltage: 3.5 to 6V.
- 4) LCD drive voltage: 3 to 6V.
- 5) Can accommodate duty of 1 / 8 to 1 / 16.
- 6) Can be used as a driver IC for static drive by setting the liquid crystal drive voltage externally ( $V_3 = V_{DD}$ ,  $V_2 = V_5 = V_{SS}$ , connect DF as LCD common).

### ●Block diagram



●Absolute maximum ratings (Ta = 25°C, Vss = 0V)

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>DD</sub>	- 0.3 ~ + 6.5	V
LCD power supply voltage*	V <sub>DD</sub> - V <sub>5</sub>	0 ~ + 6.5	V
Input voltage	V <sub>IN</sub>	V <sub>SS</sub> - 0.3 ~ V <sub>DD</sub> + 0.3	V
Power dissipation	P <sub>d</sub>	500	mW
Operating temperature	T <sub>opr</sub>	- 20 ~ + 70	°C
Storage temperature	T <sub>stg</sub>	- 55 ~ + 125	°C

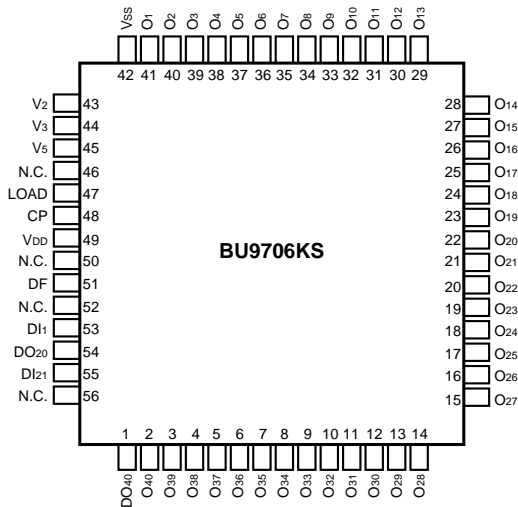
\* The LCD power supply voltage must satisfy the condition of V<sub>DD</sub> > V<sub>2</sub> ≧ V<sub>3</sub> > V<sub>5</sub> ≧ V<sub>SS</sub>.

●Recommended operating conditions (Ta = 25°C, Vss = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V <sub>DD</sub>	3.5	—	6.0	V
LCD power supply voltage*	V <sub>DD</sub> - V <sub>5</sub>	3.0	—	6.0	V
Input voltage	V <sub>IN</sub>	0	—	V <sub>DD</sub>	V

\* The LCD power supply voltage must satisfy the condition of V<sub>DD</sub> > V<sub>2</sub> ≧ V<sub>3</sub> > V<sub>5</sub> ≧ V<sub>SS</sub>.

●Pin assignments



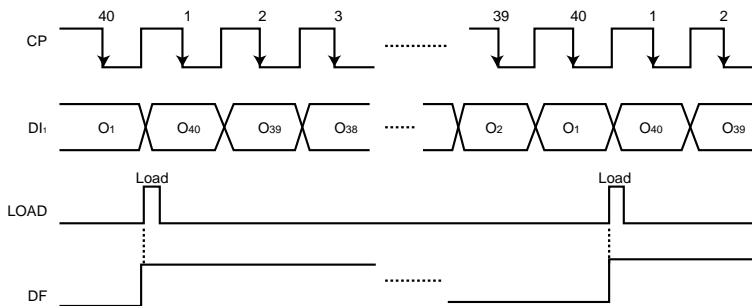
●Pin descriptions

Pin No.	Pin name	I / O	Function
2 ~ 41	O <sub>40</sub> ~ O <sub>1</sub>	O	Output pin for the liquid crystal driver. V <sub>DD</sub> , V <sub>2</sub> , V <sub>3</sub> or V <sub>5</sub> is output depending on the latch content and the DF signal. Refer to the truth table for the output level.
43 ~ 45	V <sub>2</sub> ~ V <sub>5</sub>	—	Power supply pin for liquid crystal drive
49	V <sub>DD</sub>	—	Logic power supply pin and liquid crystal drive power supply pin
42	V <sub>SS</sub>	—	Logic power supply pin
53	DI <sub>1</sub>	I	Data input pin for the shift register (1 to 20 bits). Data is read to the first bit of the shift register at the clock signal falling edge.
54	DO <sub>20</sub>	O	Data output pin for the shift register (1 to 20 bits). Data is output in synchronization with the clock signal falling edge. A 40-bit shift register is accomplished by connecting pins 54 and 55.
55	DI <sub>21</sub>	I	Data input pin for the shift register (21 to 40 bits). Data is read to the 21st bit of the shift register at the clock signal falling edge.
1	DO <sub>40</sub>	O	Data output pin for the shift register (21 to 40 bits). Data is output in synchronization with the clock signal falling edge. It is used to configure an LCD driver with more than 40 bits by connecting it to the DI pin of the BU9706KS at the next stage.
48	CP	I	Clock signal input pin for the shift register. The contents of the shift register are shifted by 1 bit only at the clock signal falling edge.
47	LOAD	I	Latch signal input pin for the 40-bit latch. The contents of the shift register are transferred to O <sub>1</sub> to O <sub>40</sub> at LOAD = "H" and the data is latched at LOAD = "L". While LOAD = "L", the latched data is held even if the contents of the shift register change.
51	DF	I	Input pin for the signal which produces AC for LCD drive.

●LCD drive output pin truth table

Latch data	DF	O <sub>n</sub> terminal voltage
H	H	V <sub>5</sub>
H	L	V <sub>DD</sub>
L	H	V <sub>3</sub>
L	L	V <sub>2</sub>

●Timing chart



- Shifted at CP input falling.
- When the LOAD input state becomes "H", the contents of the shift register are transferred to the segment outputs O<sub>1</sub> to O<sub>40</sub>, and when it is "L", the data is latched.

Fig.1

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V<sub>DD</sub> = 5 V)

## DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input high level voltage*1	V <sub>IH</sub>	4.0	—	—	V	—
Input low level voltage*1	V <sub>IL</sub>	—	—	1.0	V	—
Input high level current*1	I <sub>IH</sub>	—	—	1	μA	V <sub>IH</sub> = V <sub>DD</sub>
Input low level current*1	I <sub>IL</sub>	—	—	-1	μA	V <sub>IL</sub> = 0V
Output high level voltage*2	V <sub>OH</sub>	4.2	—	—	V	I <sub>o</sub> = -40μA
Output low level voltage*2	V <sub>OL</sub>	—	—	0.4	V	I <sub>o</sub> = 0.4mA
ON resistance*3*4	R <sub>ON</sub>	—	—	5	kΩ	V <sub>IN</sub> - V <sub>O</sub>  *5 = 0.25V
Current dissipation	I <sub>DD</sub>	—	—	0.5	mA	CP = DC No load

\*1 Applied to DF, LOAD, CP, DI1 and DI21 pins

\*2 Applied to DO20 and DO40 pins

\*3 Applied to O1 to O40 pins

\*4 V<sub>DD</sub> = 5V, V<sub>2</sub> = 2 / 3 V<sub>DD</sub>, V<sub>3</sub> = 1 / 3 V<sub>DD</sub>, V<sub>5</sub> = 0V

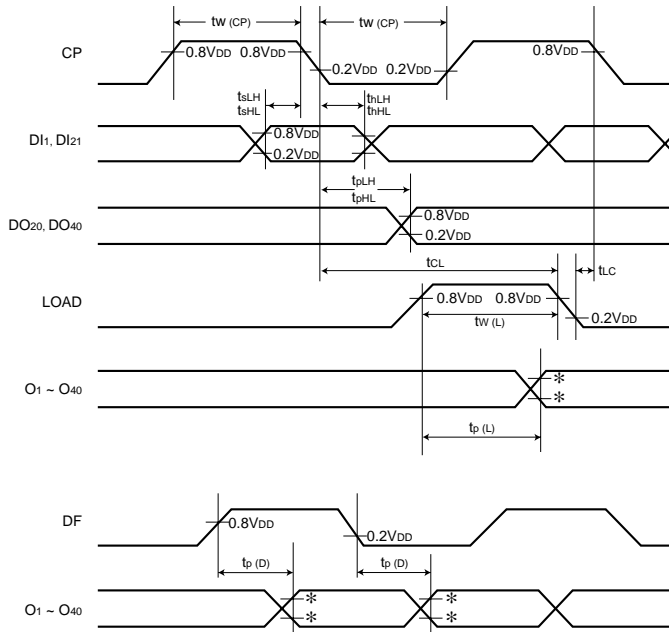
\*5 V<sub>IN</sub> = V<sub>DD</sub>, V<sub>2</sub>, V<sub>3</sub>, V<sub>5</sub>, V<sub>o</sub> = O<sub>n</sub> pin voltage

## AC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Propagation delay time 1	t <sub>pLH</sub> , t <sub>pHL</sub>	—	—	250	ns	CP → DO <sub>n</sub> delay time
Propagation delay time 2*	t <sub>p(L)</sub>	—	—	250	ns	Load → O <sub>n</sub> delay time
Propagation delay time 3*	t <sub>p(D)</sub>	—	—	250	ns	DF → O <sub>n</sub> delay time
DI → CP setup time	t <sub>sLH</sub> , t <sub>sHL</sub>	50	—	—	ns	—
CP → DI hold time	t <sub>hLH</sub> , t <sub>hHL</sub>	50	—	—	ns	—
CP pulse width	t <sub>w(CP)</sub>	125	—	—	ns	—
Load pulse width	t <sub>w(L)</sub>	125	—	—	ns	—
CP → load time	t <sub>CL</sub>	250	—	—	ns	—
LOAD → CP time	t <sub>LC</sub>	0	—	—	ns	—
Maximum clock frequency	f <sub>CP</sub>	3.3	—	—	MHz	DUTY = 50%

\* V<sub>DD</sub> = 5V, V<sub>2</sub> = 2 / 3V<sub>DD</sub>, V<sub>3</sub> = 1 / 3V<sub>DD</sub>, V<sub>5</sub> = 0V

○ Not designed for radiation resistance.



\*  $t_p(L)$  and  $t_p(D)$  are times required before the O<sub>1</sub> to O<sub>40</sub> output amplitude becomes 80% and 20% respectively.

Fig.2 AC characteristics waveform

●Application example

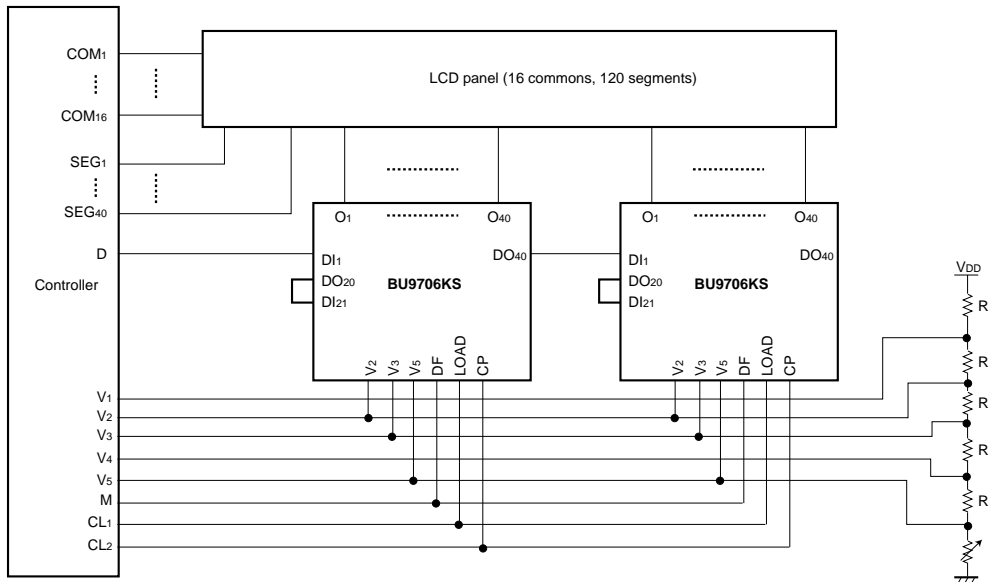
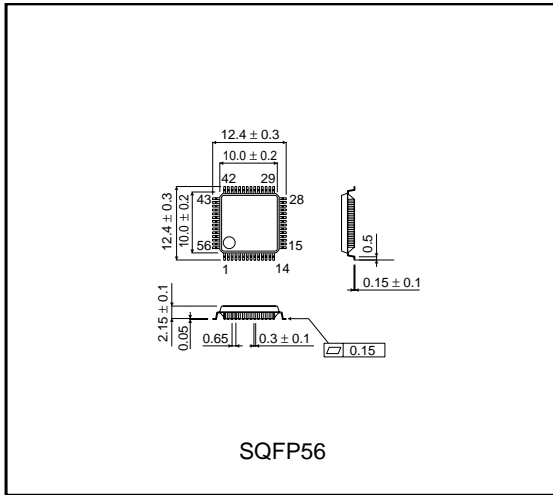


Fig.3

●External dimensions (Units: mm)



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