LCD Module Technical Specification

Type No. **T-51638D084-FW-A-AA**
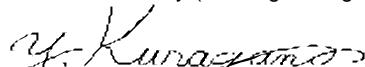
Approved by (Production Engineering

Checked by (Quality Assurance Division)

Checked by (ACI Engineering Division)

Prepared by (Production Engineering Group)

CONTENTS

1. OVERVIEW

T-51638D084-FW-A-AA is 8.4" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs, control circuit, and backlight unit.

By applying 6 bit digital data, 640×480, 262,144-color images are displayed on the 8.4" diagonal screen. Input power voltage is single 3.3V for LCD driving.

Inverter for backlight is not included in this module. General specifications are summarized in the following table:

ITEM	SPECIFICATION
Display Area (mm)	170.9(H) $\times$ 128.2 (V) (8.4-inch diagonal)
Number of Dots	640×3 (H) $\times$ 480 (V)
Pixel Pitch (mm)	0.267 (H) $\times$ 0.267 (V)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	normally white
Number of Colors	262,144
Contrast ratio	450
Optimum Viewing Angle(Contrast ratio)	6 o'clock
Brightness (cd/m²)	450
Module Size (mm)	199.5 (W) $\times$ 149.0 (H) $\times$ 11.5 (D)
Module Mass (g)	360(Typ)
Backlight Unit	CCFL, 2-tubes, edge-light, replaceable
Surface Treatment	Anti-glare and hard-coating 3H

Characteristic value without any note is typical value.

The LCD product described in this specification is designed and manufactured for the standard use in OA equipment and consumer products, such as computers, communication equipment, industrial robots, AV equipment and so on.

Do not use the LCD product for the equipment that require the extreme high level of reliability, such as aerospace applications, submarine cables, nuclear power control systems and medical or other equipment for life support.

OPTREX assumes no responsibility for any damage resulting from the use of the LCD product in disregard of the conditions and handling precautions in this specification.

If customers intend to use the LCD product for the above items or other no standard items, please contact our sales persons in advance.

2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN.	MAX.	UNIT
Power Supply Voltage for LCD	VCC	0	4.0	V
Logic Input Voltage	VI	0	6.0	V
Lamp Voltage	VL	0	1500	Vrms
Lamp Current	IL	0	8.0	mArms
Lamp Frequency	FL	--	80	kHz
Operation Temperature *1)	T_{op}	0	60	°C
Storage Temperature *1)	T_{stg}	-20	65	°C

[Note]

*1) Top,Tstg ≤ 40°C : 90%RH max. without condensation

Top,Tstg > 40°C : Absolute humidity shall be less than the value of 90%RH at 40°C without condensation.

3. ELECTRICAL CHARACTERISTICS

(1) TFT- LCD　　　　　　　　　　　　　　　　　Ambient Temperature: Ta = 25°C
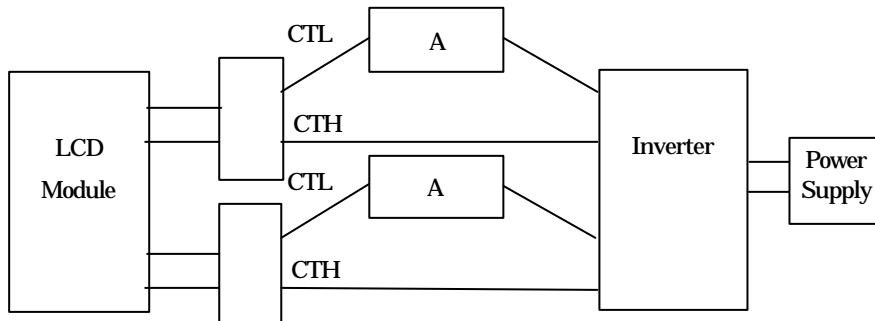
ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT	Remarks
Power Supply Voltages for LCD		VCC	3.0	3.3	3.6	V	Note A) (See next page)
Power Supply Currents for LCD		ICC	--	240	400	mA	Note B) (See next page)
Permissive input ripple Voltage		VRP	--	--	100	mVp-p	VCC=+3.3V
Logic Input Voltage	High	VIH	2.4	--	5.5	V	VCC=MAX
	Low	VIL	0	--	0.8	V	VCC=MIN

(2) Backlight　　　　　　　　　　　　　　　　　　　　　　　　　　Ta = 25°C

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	Remarks
Lamp Voltage	VL	--	450	--	Vrms	IL = 6.5 mArms
Lamp Current	IL	3.0	6.5	7.0	mArms	*1)
Lamp Frequency	FL	30	--	60	kHz	*2)
Starting Lamp Voltage	VS	670	--	--	Vrms	
Lamp Life Time	LT	50000	--	--	h	

*1) Lamp Current measurement method (The current meter is inserted in low voltage line.)
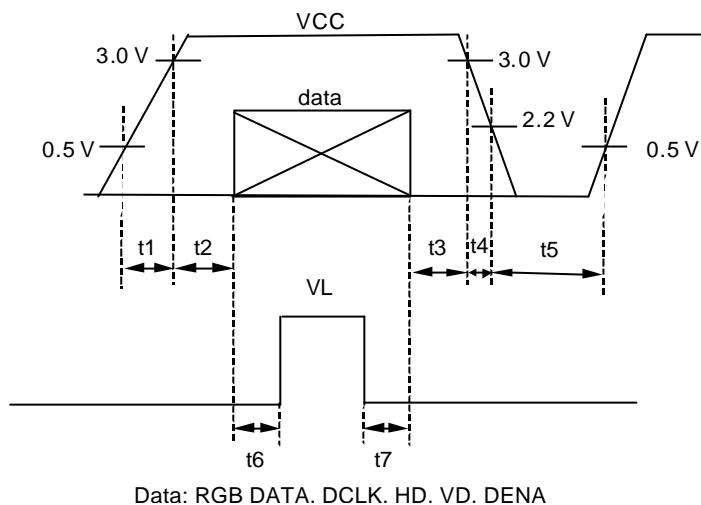
*2) Lamp frequency of inverter may produce interference with horizontal synchronous frequency, and this may cause horizontal beat on the display. Therefore, please adjust lamp frequency, and keep inverter as far from module as possible or use electronic shielding between inverter and module to avoid the interference.

[Note]

A) Power and signals sequence:
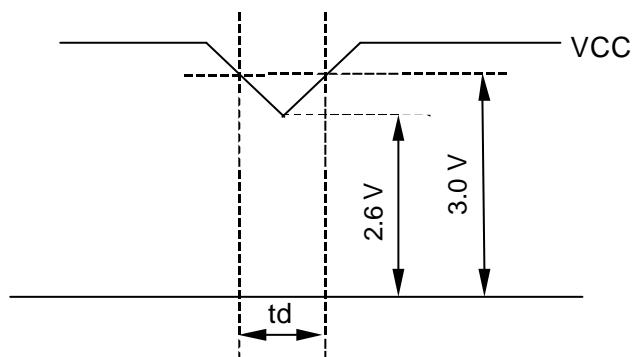
t1 ≤ 10 ms	400 ms ≤ t5
0 < t2 ≤ 50 ms	200 ms ≤ t6
0 < t3 ≤ 50 ms	0 ≤ t7
0 ≤ t4 ≤ 50 ms	

Data: RGB DATA. DCLK. HD. VD. DENA

VCC-dip conditions:

1) When 2.6 V≤ VCC < 3.0 V, td ≤ 10 ms

2) When VCC < 2.6 V

   VCC-dip conditions should also follow the power and signals sequence.

B) Typical current condition:

   64- gray- bar-pattern
   480 line mode
   VCC = +3.3 V, f_H=31.5 kHz, f_V=60 Hz, f_{CLK}= 25 MHz
   Normal value, not peak value

4. INTERFACE PIN CONNECTION

CN 1(INTERFACE SIGNAL)

Used connector: DF9B-31P-1V(Hirose)

Corresponding connector: DF9B-31S-1V(Hirose)

Pin No.	Symbol	Function
1	GND	
2	DCLK	Clock signal for sampling catch data signal
3	HD	Horizontal sync signal
4	VD	Vertical sync signal
5	GND	
6	R0	Red data signal(LSB)
7	R1	Red data signal
8	R2	Red data signal
9	R3	Red data signal
10	R4	Red data signal
11	R5	Red data signal(MSB)
12	GND	
13	G0	Green data signal(LSB)
14	G1	Green data signal
15	G2	Green data signal
16	G3	Green data signal
17	G4	Green data signal
18	G5	Green data signal(MSB)
19	GND	
20	B0	Blue data signal(LSB)
21	B1	Blue data signal
22	B2	Blue data signal
23	B3	Blue data signal
24	B4	Blue data signal
25	B5	Blue data signal(MSB)
26	GND	
27	DENA	Data enable signal(to settle the viewing area)
28	VCC	3.3 V Power Supply
29	VCC	3.3 V Power Supply
30	TEST	This pin should be open. Test signal output for only internal test use.
31	REV	Reverse scan control. L = Normal, H = Reverse

*) The shielding case is connected with GND

CN 2 , CN 3 (BACKLIGHT)

Backlight-side connector: BHR-02(8.0)VS-1N(JST)

Inverter-side connector: SM02(8.0)B-BHS(JST)

Pin No.	Symbol	Function
1	CTH	VBLH(High Voltage)
3	CTL	VBLL(Low Voltage)

[Note]VBLH-VBLL = VL

5. INTERFACE TIMING

(1) Timing Specifications
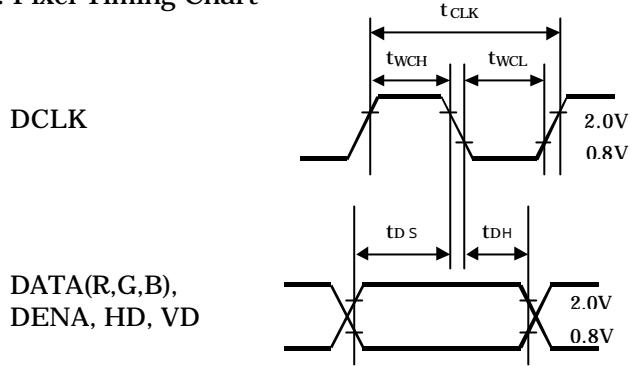
| ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT
DCLK *1), *4)	Frequency	f_{CLK}	20	25	30	MHz
	Period	t_{CLK}	33.3	40	50	ns
	Low Width	t_{WCL}	10	--	--	ns
	High Width	t_{WCH}	10	--	--	ns
DATA (R,G,B,DENA, HD, VD) *1)	Set up time	t_{DS}	5	--	--	ns
	Hold time	t_{DH}	5	--	--	ns
DENA *3)	Horizontal Active Time	t_{HA}	640	640	640	t_{CLK}
	Horizontal Front Porch	t_{HFP}	0	16	--	t_{CLK}
	Horizontal Back Porch	t_{HBP}	19	144	--	t_{CLK}
	Vertical Active Time	t_{VA}	480	480	480	t_H
	Vertical Front Porch	t_{VFP}	1	10	--	t_H
	Vertical Back Porch	t_{VBP}	8	35	--	t_H
HD *2), *4)	Frequency	f_H	27	31.5	38	kHz
	Period	t_H	26.3	31.7	37.0	µs
	Low Width	t_{WHL}	5	96	--	t_{CLK}
VD *2)	Frequency	f_V	55	60	70	Hz
	Period	t_V	14.2	16.7	18.2	ms
	Low Width	t_{WVL}	2	2	--	t_H

[Note]
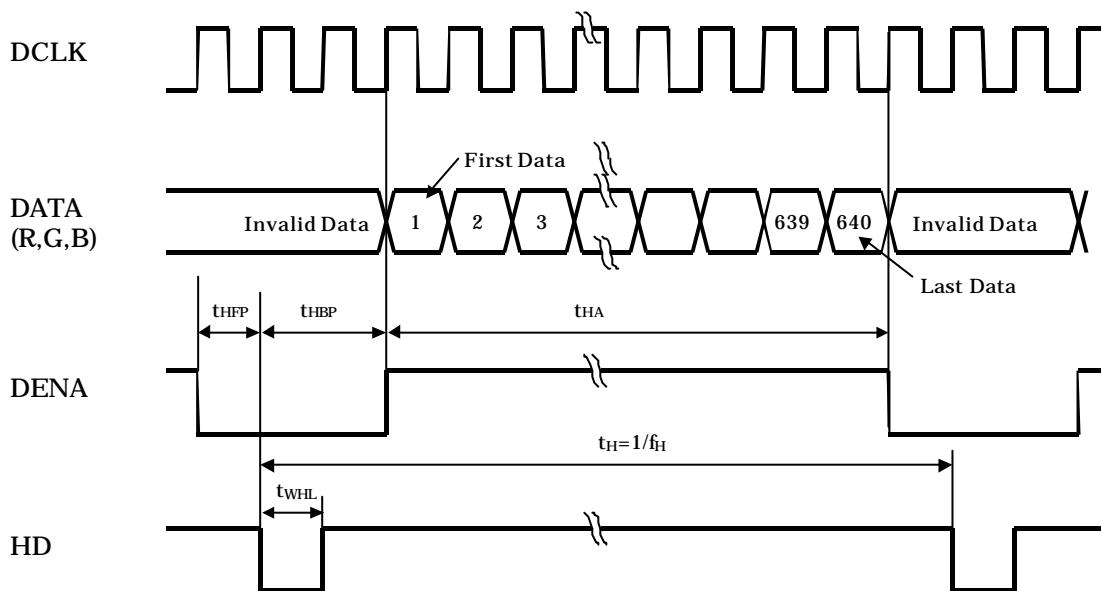
*1) DATA is latched at fall edge of DCLK in this timing specification.

*2) Polarities of HD and VD are negative in this specification.

*3) DENA (Data Enable) should always be positive polarity as shown in the timing specification.

*4) DCLK should appear during all invalid period, and HD should appear during invalid period of frame cycle.

(2) Timing Chart

a. Pixel Timing Chart

t_{CLK}

t_{WCH} t_{WCL}

DCLK

2.0V
0.8V

t_D t_D

DATA(R,G,B),
DENA, HD, VD

2.0V
0.8V
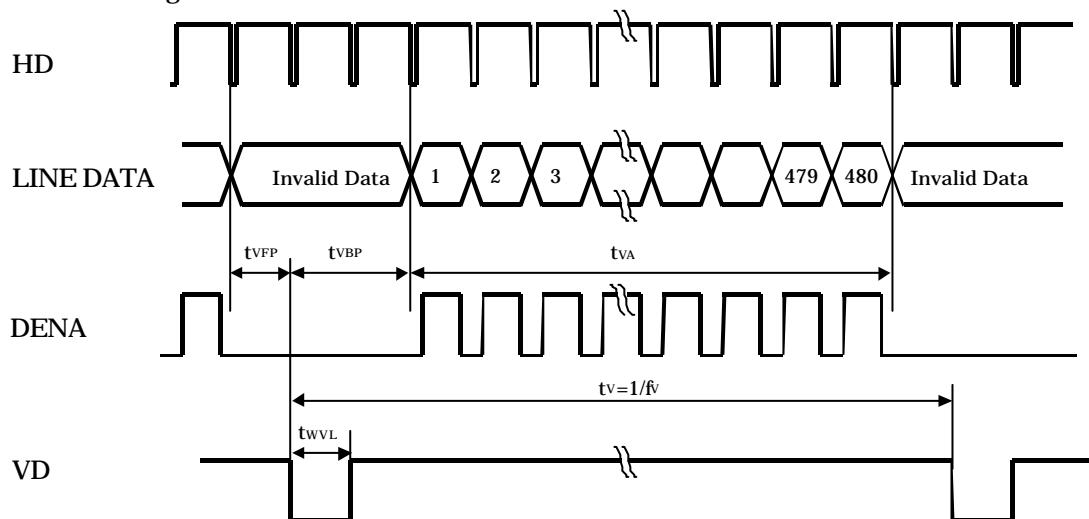
b. Horizontal Timing Chart

DCLK

First Data

DATA
(R,G,B)

Invalid Data | 1 | 2 | 3 | 639 | 640 | Invalid Data

Last Data

t_{HFP} t_{HBP} t_{HA}

DENA

$t_H=1/f_H$

t_{WHL}

HD

c. Vertical Timing Chart

HD

LINE DATA

Invalid Data | 1 | 2 | 3 | 479 | 480 | Invalid Data

t_{VFP} t_{VBP} t_{VA}

DENA

$t_V=1/f_V$

t_{WVL}

VD

(3) Color Data Assignment

COLOR	INPUT DATA	R DATA						G DATA						B DATA					
		R5 MSB	R4	R3	R2	R1	R0 LSB	G5 MSB	G4	G3	G2	G1	G0 LSB	B5 MSB	B4	B3	B2	B1	B0 LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	BLUE(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	GREEN(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	BLUE(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
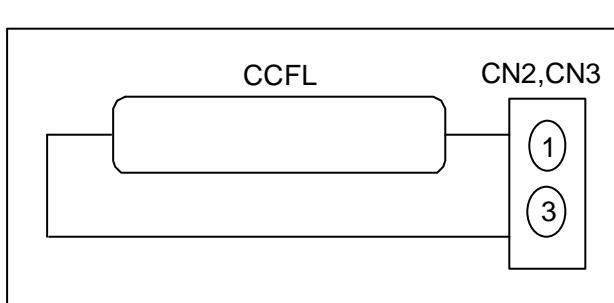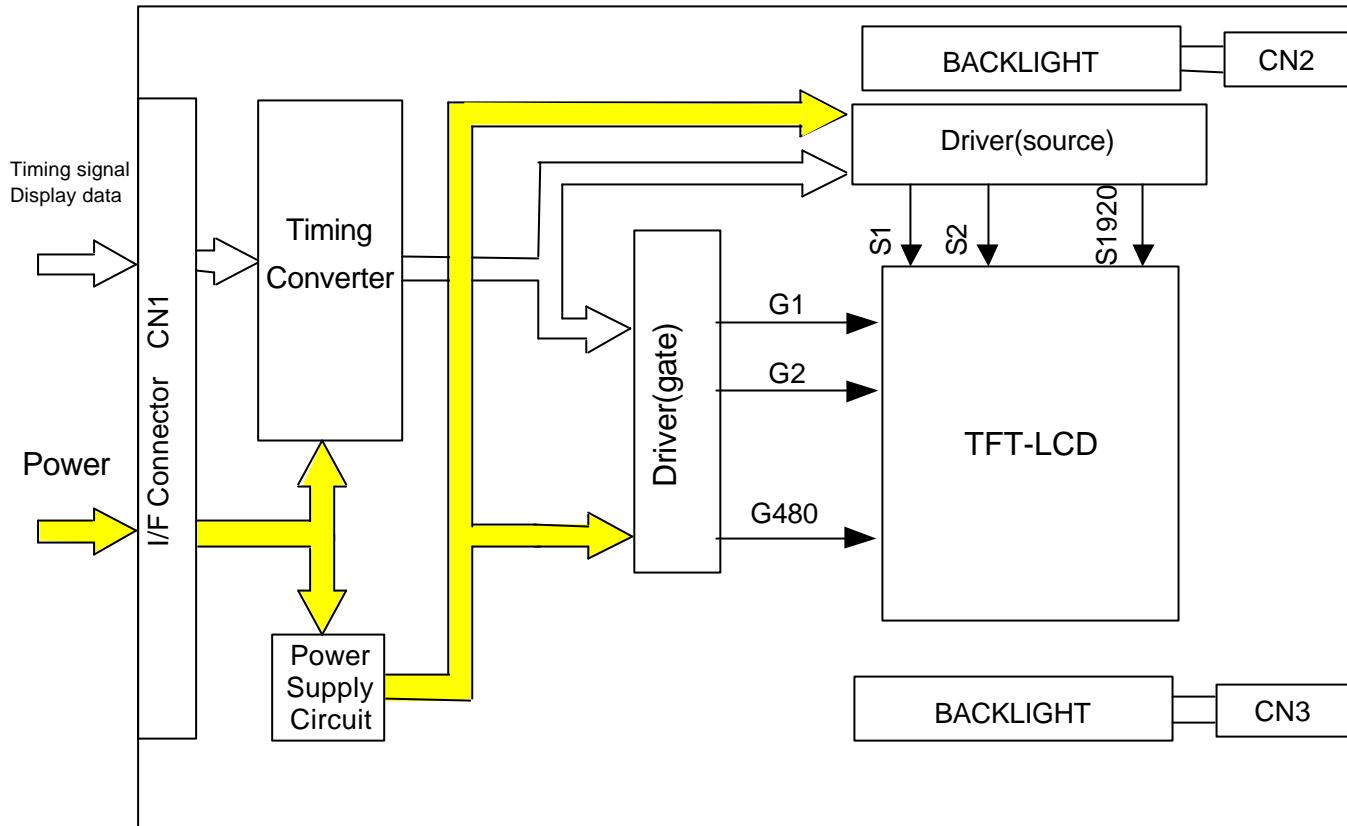
[Note]1) Definition of gray scale

Color (n) --- n indicates gray scale level.

Higher n means brighter level.
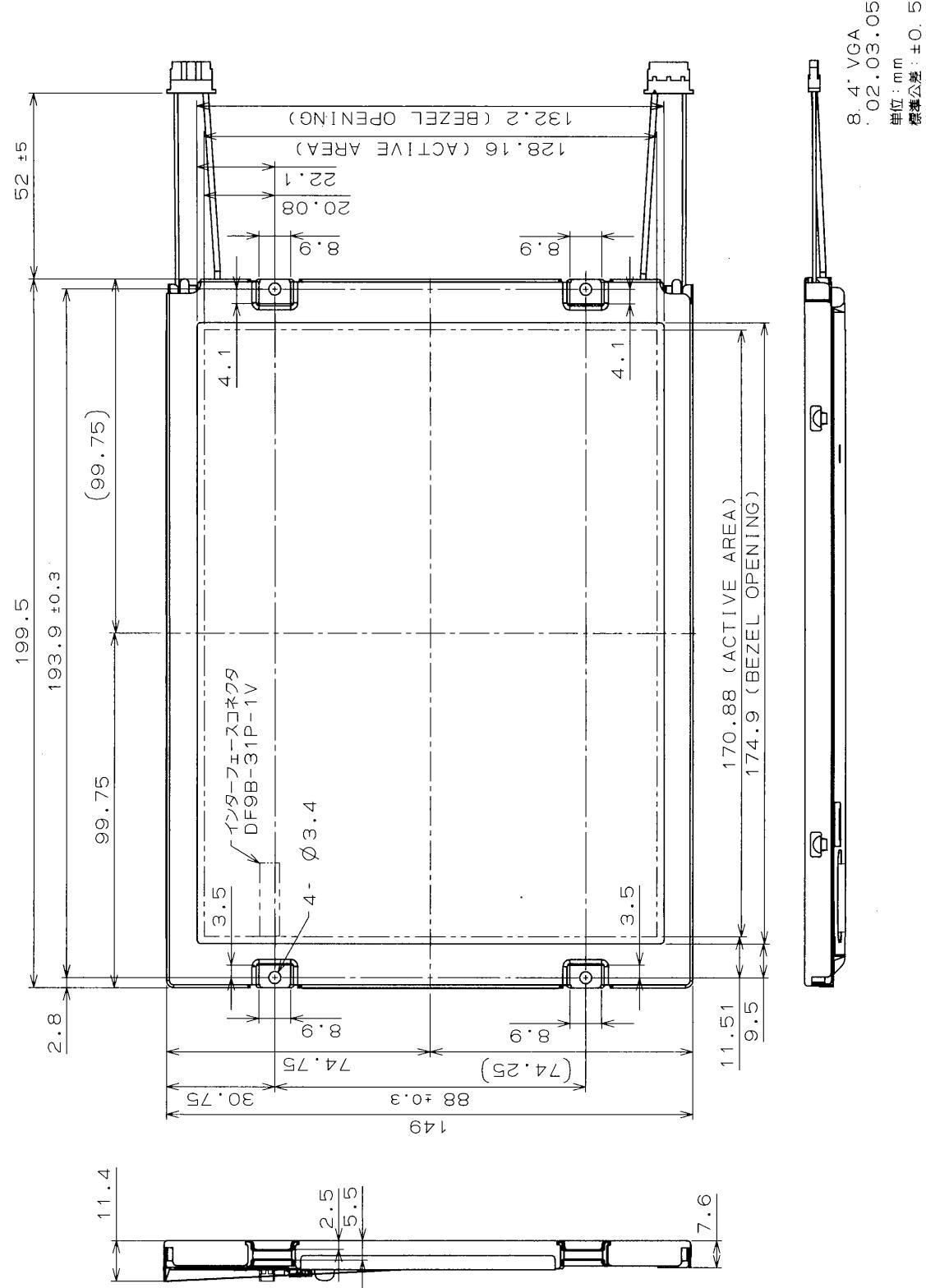
2) Data   1:High, 0: Low

6. BLOCK DIAGLAM
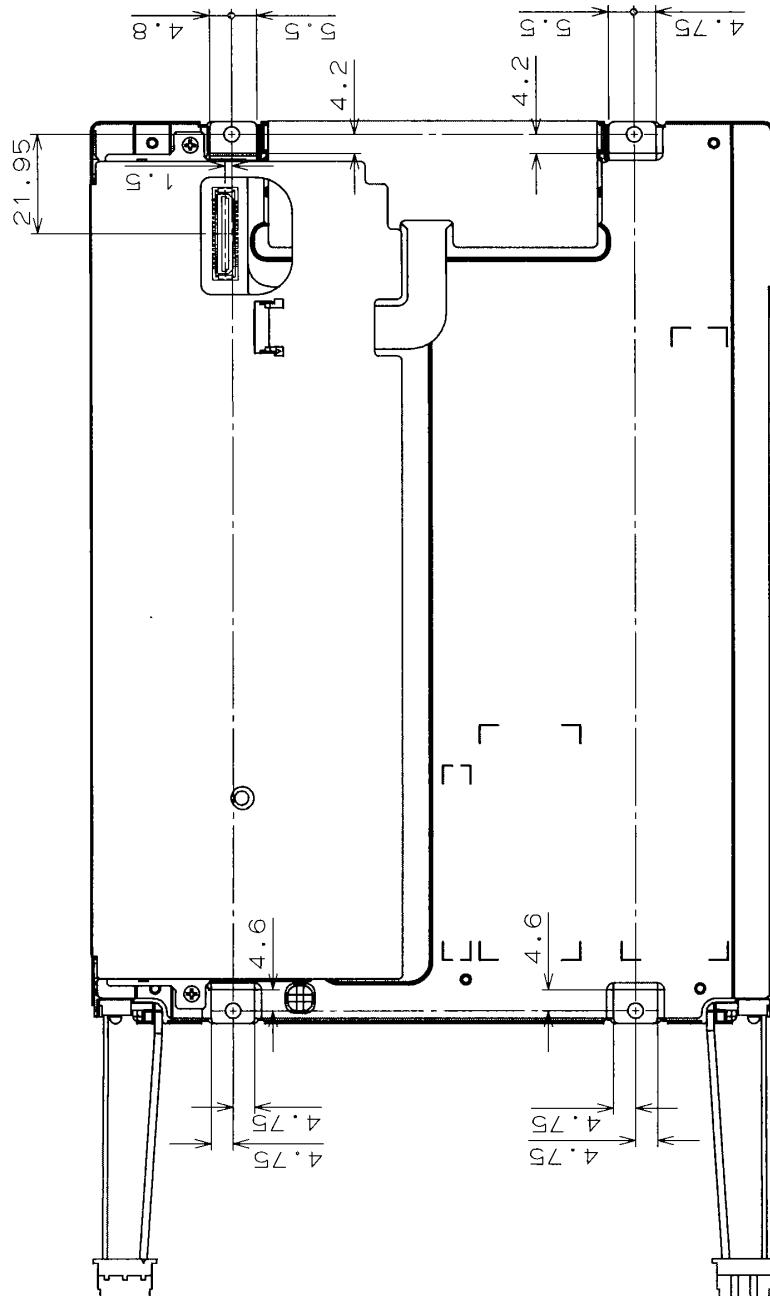
7. MECHANICAL SPECIFICATIONS

(1) Front Side

Tolerance is ±0.5mm unless noted.

(2) Rear Side

Tolerance is ±0.5mm unless noted.

[Note]
  We recommend you referring to the detailed drawing for your design.
  Please contact our company sales representative when you need the detailed drawing.

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8. OPTICAL CHARACTERISTICS

Ta = 25°C, VCC = 3.3 V, Input Signals: Typ. Values shown in Section 5

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	Remarks
Contrast Ratio		CR	θ = φ = 0°	--	450	--	--	*1)*3)
Luminance		Lw	θ = φ = 0°	--	450	--	cd/m²	*2)*3)
Response Time		tr	θ = φ = 0°	--	8	--	ms	*3)*4)
		tf	θ = φ = 0°	--	27	--	ms	*3)*4)
Viewing Angle	Horizontal	φ	CR ≥ 10	--	-65~65	--	°	*3)
	Vertical	θ		--	-60~50	--	°	*3)
Image Sticking		tis	2 h	--	--	2	s	*5)
Color Coordinates	Red	Rx	θ = φ = 0°	0.542	0.572	0.602	--	*3)
		Ry		0.302	0.332	0.362		
	Green	Gx		0.285	0.315	0.345		
		Gy		0.493	0.523	0.553		
	Blue	Bx		0.125	0.155	0.185		
		By		0.118	0.148	0.178		
	White	Wx		0.283	0.313	0.343		
		Wy		0.294	0.324	0.354		

[Note]

These items are measured using CS1000(MINOLTA) for color coordinates, and CS1000 or BM-5A(TOPCON) for others under the dark room condition (no ambient light) after more than 30 minutes from turning on the lamp unless noted.
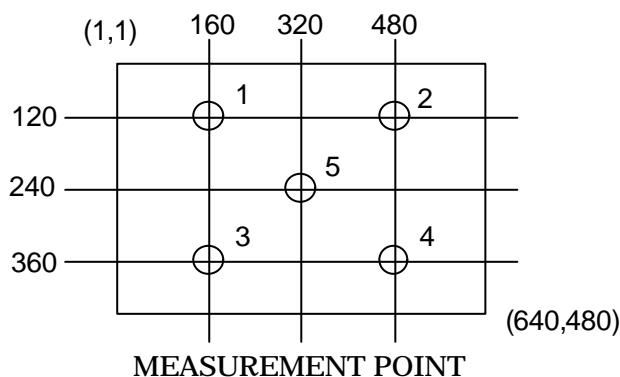
Condition: IL = 6.5 mArms, FL = 60kHz

*1) Definition of Contrast Ratio
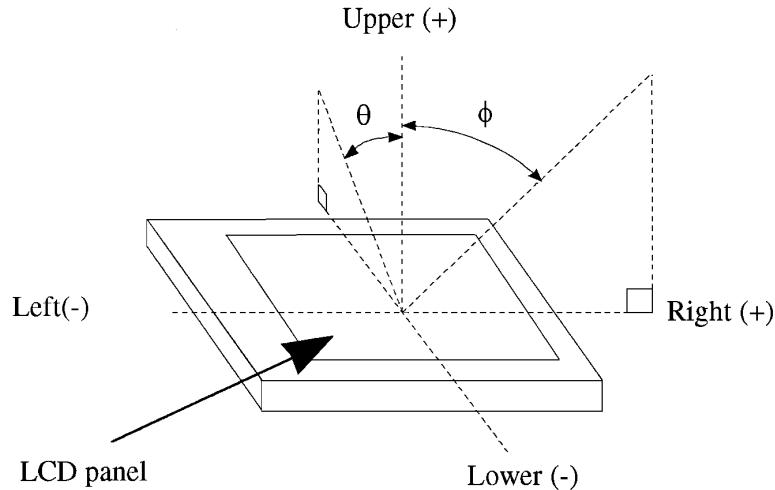
   CR=ON (White) Luminance / OFF(Black) Luminance: average of 5 points shown in a figure below

*2) Definition of Luminance
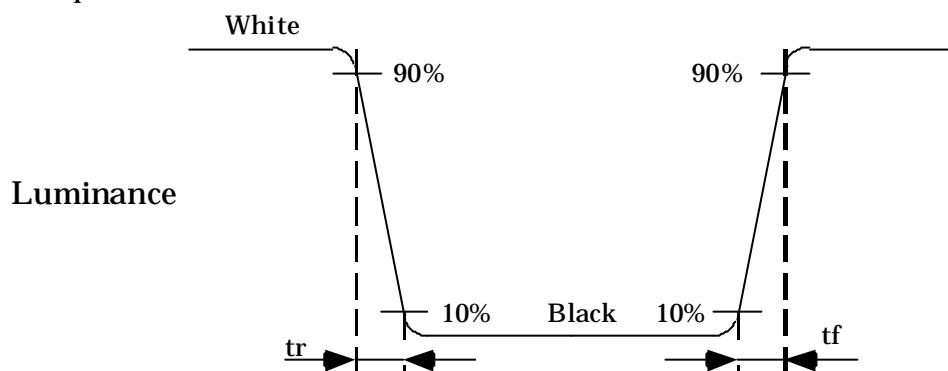
   Lw= ON (White) Luminance: average of 5 points shown in a figure below


MEASUREMENT POINT

*3) Definition of Viewing Angle (θ , φ)

Upper (+)

θ   φ

Left(-)   Right (+)

LCD panel   Lower (-)
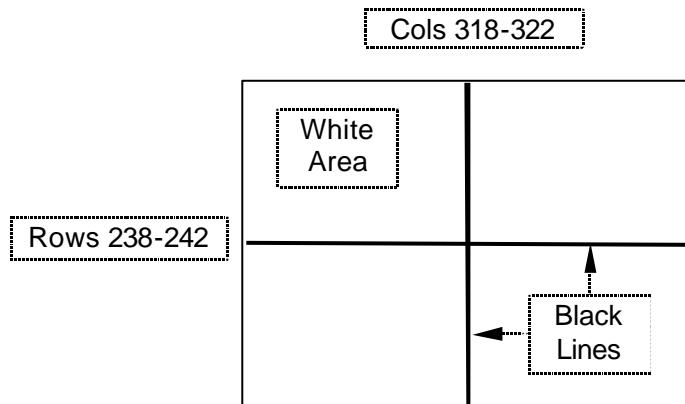
*4) Definition of Response Time

White

90%   90%

Luminance

10%   Black   10%

tr   tf

*5) Image Sticking

Continuously display the test pattern shown in the figure below for two-hours. Then display a completely white screen. The previous image shall not persist more than two seconds at 25°C.

TEST PATTERN FOR IMAGE STICKING TEST

Cols 318-322

White Area

Rows 238-242

Black Lines

9. RELIABILITY TEST CONDITION

(1) Temperature and Humidity

TEST ITEM	CONDITIONS
HIGH TEMPERATURE HIGH HUMIDITY OPERATION	40°C, 90%RH, 240 h
HIGH TEMPERATURE STORAGE	65°C, 96 h
LOW TEMPERATURE STORAGE	-20°C, 96 h
THERMAL SHOCK(NON-OPERARION)	BETWEEN -20°C (1h) and 65°C(1h), 5 CYCLES

(2) Shock & Vibration

ITEM	CONDITIONS
SHOCK (NON-OPERATION)	Shock level: 1470m/s^2 (150G) Waveform: half sinusoidal wave, 2ms Number of shocks: one shock input in each direction of three mutually perpendicular axis for a total of six shock inputs
VIBRATION (NON-OPERATION)	Vibration level: 9.8m/s^2 (1.0G)(Zero to Peak) Waveform: sinusoidal Frequency range: 5 to 500Hz Frequency sweep rate: 0.5 octave /min Duration: one sweep from 5 to 500 Hz in each of three mutually perpendicular axis(each x,y,z axis: 1 hour, total 3 hours)

(3) Judgment standard

The judgment of the above tests should be made as follow:
    Pass: Normal display image with no obvious non-uniformity and no line defect.
        Partial transformation of the module parts should be ignored.

    Fail: No display image, obvious non-uniformity, or line defects.