National Semiconductor

January 1995

ADC10662/ADC10664 10-Bit 360 ns A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative, patented multistep* conversion technique, the 10-bit ADC10662 and ADC10664 are 2- and 4-input CMOS analog-to-digital converters offering sub-microsecond conversion times yet dissipating a maximum of only 235 mW. The ADC10662 and ADC10664 perform a 10-bit conversion in two lower-resolution ''flashes'', thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches. In addition to standard static performance specifications (Linearity, Full-Scale Error, etc.) dynamic performance (THD, S/N) is guaranteed.

The analog input voltage to the ADC10662 and ADC10664 is sampled and held by an internal sampling circuit. Input signals at frequencies from dc to over 250 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

The ADC10662 and ADC10664 include a ''speed-up'' pin. Connecting an external resistor between this pin and ground reduces the typical conversion time to as little as 360 ns.

For ease of interface to microprocessors, the ADC10662 and ADC10664 have been designed to appear as a memory location or I/O port without the need for external interface logic.

Features

- Built-in sample-and-hold
- Single +5V supply
- 2- or 4-input multiplexer options
- No external clock required

Key Specifications

- Conversion time to 10 bits — 360 ns typical, 466 ns max over temperature
- Sampling Rate — 1.5 MHz (min)
- Low power dissipation — 235 mW (max)
- Total harmonic distortion (50 kHz) — −60 dB (max)
- No missing codes over temperature

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications

Ordering Information

ADC10662

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC10662CIN	N24A Molded DIP
ADC10662CIWM	M24B Small Outline

ADC10664

Industrial ($-40°C \leq T_A \leq +85°C$)	Package
ADC10664CIN	N28B Molded DIP
ADC10664CIWM	M28B Small Outline

*U.S. Patent Number 4918449

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

 TL/H/11192

RRD-B30M75/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ = AV_{CC} = DV_{CC}$)	−0.3V to +6V
Voltage at Any Input or Output	−0.3V to V^+ + 0.3V
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	875 mW
ESD Susceptability (Note 5)	2000V
Soldering Information (Note 6)	
N Package (10 Sec)	260°C
SO Package:	
Vapor Phase (60 Sec)	215°C
Infrared (15 Sec)	220°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC10662CIN, ADC10662CIWM, ADC10664CIN, ADC10664CIWM	$-40°C \le T_A \le +85°C$
Supply Voltage Range	4.5V to 5.5V

Converter Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = +5V$, $V_{REF(-)}$ = GND, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{Min}$ to T_{Max};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limit)
	Resolution			**10**	Bits
	Integral Linearity Error		±0.5	±1.0/±**1.5**	LSB
	Offset Error			±**1**	LSB (max)
	Full-Scale Error			±**1**	LSB (max)
	Total Unadjusted Error		±0.5	±1.5/±**2.0**	LSB
	Missing Codes			**0**	(max)
	Power Supply Sensitivity	$V^+ = 5V \pm 5\%$, $V_{REF} = 4.5V$ $V^+ = 5V \pm 10\%$, $V_{REF} = 4.5V$	±1/16 ±1/8		LSB LSB
THD	Total Harmonic Distortion (Note 10)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P} f_{IN} = 100 kHz, 4.85 V_{P-P} f_{IN} = 240 kHz, 4.85 V_{P-P}	**−68** **−66** **−62** **−58**	**−60**	dB dB (max) dB dB
SNR	Signal-to-Noise Ratio (Note 10)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P} f_{IN} = 100 kHz, 4.85 V_{P-P}	**61** **60** **60**	**58**	dB dB (min) dB
ENOB	Effective Number of Bits (Note 10)	f_{IN} = 1 kHz, 4.85 V_{P-P} f_{IN} = 50 kHz, 4.85 V_{P-P}	**9.6** **9.5**	**9**	Bits Bits (min)
R_{REF}	Reference Resistance		650	**400** **900**	Ω (min) Ω (max)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**V^+ + 0.05**	V (max)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**GND − 0.05**	V (min)
$V_{REF(+)}$	$V_{REF(+)}$ Input Voltage			**$V_{REF(-)}$**	V (min)
$V_{REF(-)}$	$V_{REF(-)}$ Input Voltage			**$V_{REF(+)}$**	V (max)
V_{IN}	Input Voltage			**V^+ + 0.05**	V (max)
V_{IN}	Input Voltage			**GND − 0.05**	V (min)
	OFF Channel Input Leakage Current ON Channel Input Leakage Current	$\overline{CS} = V^+$, $V_{IN} = V^+$ $\overline{CS} = V^+$, $V_{IN} = V^+$	0.01 ±1	**3** **−3**	μA (max) μA (max)

DC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $V_{REF(+)} = 5V$ $V_{REF(-)} =$ GND, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage	$V^+ = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V^+ = 4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN(1)} = 5V$	0.005	**3.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN(0)}$ 0V	−0.005	**−3.0**	μA (max)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = -360\ \mu A$ $V^+ = 4.5V$, $I_{OUT} = -10\ \mu A$		**2.4** **4.25**	V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V^+ = 4.5V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Current	$V_{OUT} = 5V$ $V_{OUT} = 0V$	0.1 −0.1	**50** **−50**	μA (max) μA (max)
DI_{CC}	DV_{CC} Supply Current	$\overline{CS} = \overline{S}/H = \overline{RD} = 0$	1.0	**2**	mA (max)
AI_{CC}	AV_{CC} Supply Current	$\overline{CS} = \overline{S}/H = \overline{RD} = 0$	30	**45**	mA (max)

AC Electrical Characteristics

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, $V_{REF(-)} =$ GND, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$.

Symbol	Parameter	Conditions		Typical (Note 7)	Limit (Note 8)	Units (Limits)
t_{CONV}	Mode 1 Conversion Time from Rising Edge of $\overline{S}/H$ to Falling Edge of $\overline{INT}$	CIN, CIWM Suffixes		360	**466**	ns (max)
t_{CRD}	Mode 2 Conversion Time	CIN, CIWM Suffixes		470	**610**	ns (max)
t_{ACC1}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 1; $C_L = 100$ pF		30	**50**	ns (max)
t_{ACC2}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Mode 2; $C_L = 100$ pF	CIN, CIWM Suffixes	475	**616**	ns (max)
t_{SH}	Minimum Sample Time	Mode 1 *(Figure 1)* ; (Note 9)			**150**	ns (max)
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to High-Z State)	$R_L = 1k$, $C_L = 10$ pF		30	**60**	ns (max)
t_{INTH}	Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$C_L = 100$ pF		25	**50**	ns (max)
t_P	Delay from End of Conversion to Next Conversion				**50**	ns (max)

AC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = +5V$, $t_r = t_f = 20$ ns, $V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, and Speed Adjust pin connected to ground through a 14.0 kΩ resistor (Mode 1) or an 8.26 kΩ resistor (Mode 2) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = +25°C$. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	Limit (Note 8)	Units (Limits)
t_{MS}	Multiplexer Control Setup Time		10	**75**	ns (max)
t_{MH}	Multiplexer Hold Time		10	**40**	ns (max)
C_{VIN}	Analog Input Capacitance		35		pF (max)
C_{OUT}	Logic Output Capacitance		5		pF (max)
C_{IN}	Logic Input Capacitance		5		pF (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditons.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < GND$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. In most cases, the maximum derated power dissipation will be reached only during fault conditions. For these devices, T_{JMAX} for a board-mounted device can be found from the tables below:

ADC10662

Suffix	θ_{JA} (°C/W)
CIN	60
CIWM	82

ADC10664

Suffix	θ_{JA} (°C/W)
CIN	53
CIWM	78

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: See AN-450 ''Surface Mounting Methods and Their Effect on Product Reliability'' or the section titled ''Surface Mount'' found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Typicals represent most likely parametric norm.

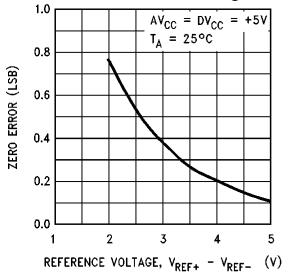
Note 8: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 9: Accuracy may degrade if t_{SH} is shorter than the value specified. See curves of Accuracy vs t_{SH}.

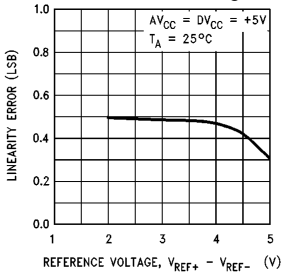
Note 10: THD, SNR, and ENOB are tested in Mode 1. Measuring these quantities in Mode 2 yields similar values.

Typical Performance Characteristics

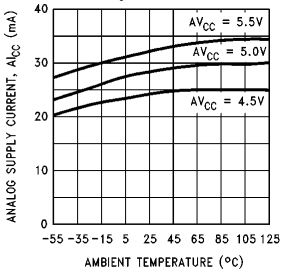
Zero (Offset) Error vs Reference Voltage



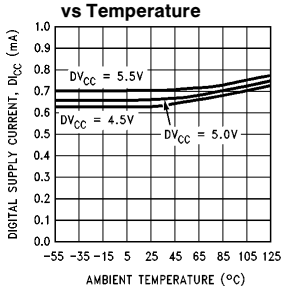
Linearity Error vs Reference Voltage



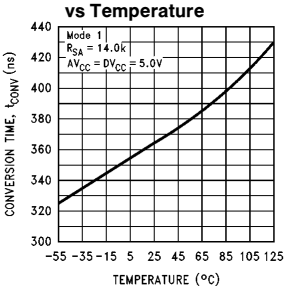
Analog Supply Current vs Temperature



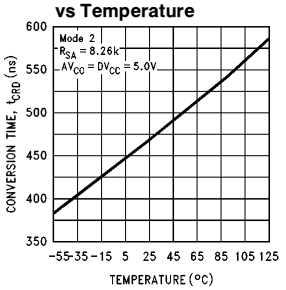
Digital Supply Current vs Temperature



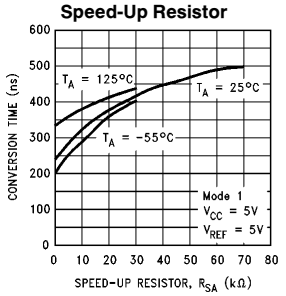
Conversion Time vs Temperature



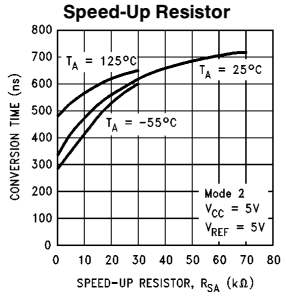
Conversion Time vs Temperature



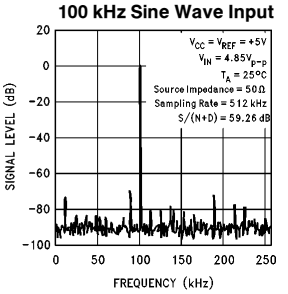
Conversion Time vs Speed-Up Resistor



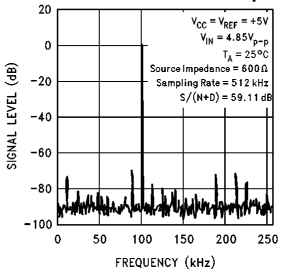
Conversion Time vs Speed-Up Resistor



Spectral Response with 100 kHz Sine Wave Input



Spectral Response with 100 kHz Sine Wave Input



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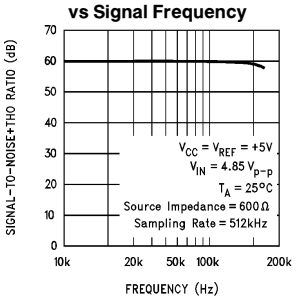
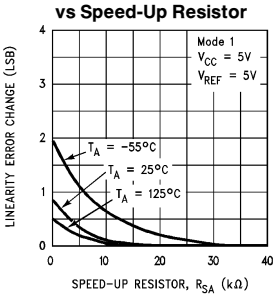
Typical Performance Characteristics (Continued)

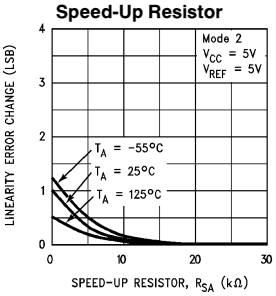
Signal-to-Noise + THD Ratio vs Signal Frequency



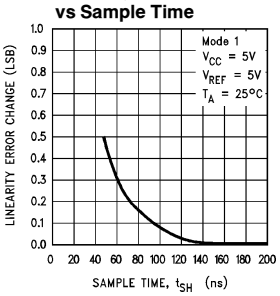
Linearity Change vs Speed-Up Resistor



Linearity Change vs Speed-Up Resistor



Linearity Error Change vs Sample Time



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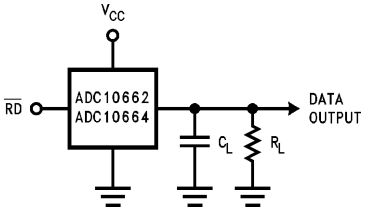
TRI-STATE Test Circuits and Waveforms



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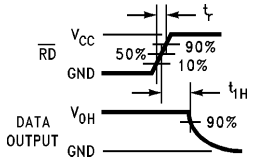

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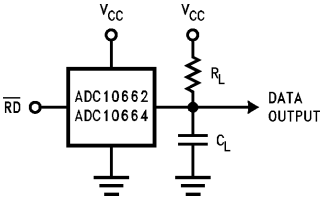

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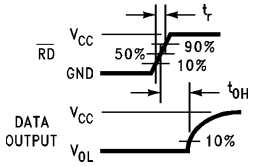

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Timing Diagrams

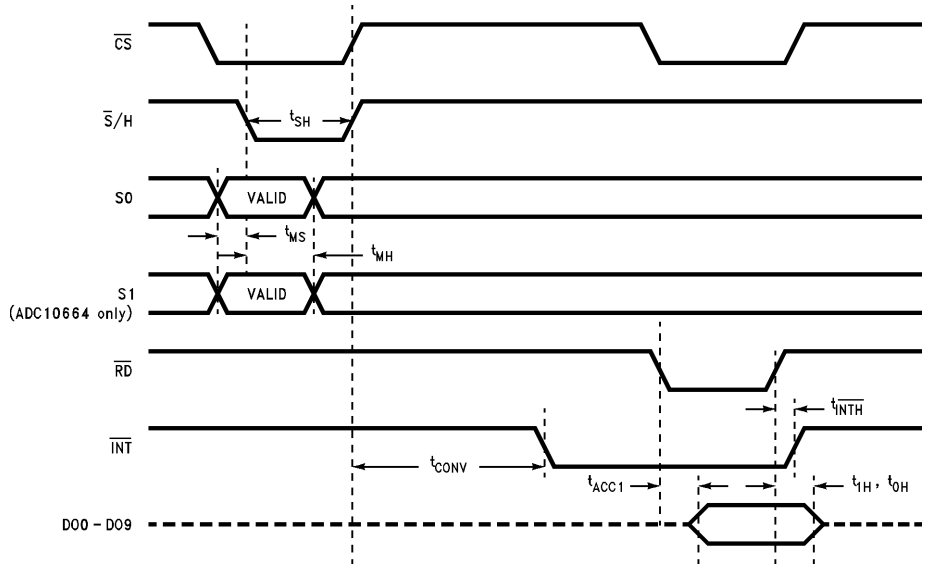

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FIGURE 1. Mode 1. The conversion time (t_{CONV}) is set by the internal timer.

Timing Diagrams (Continued)

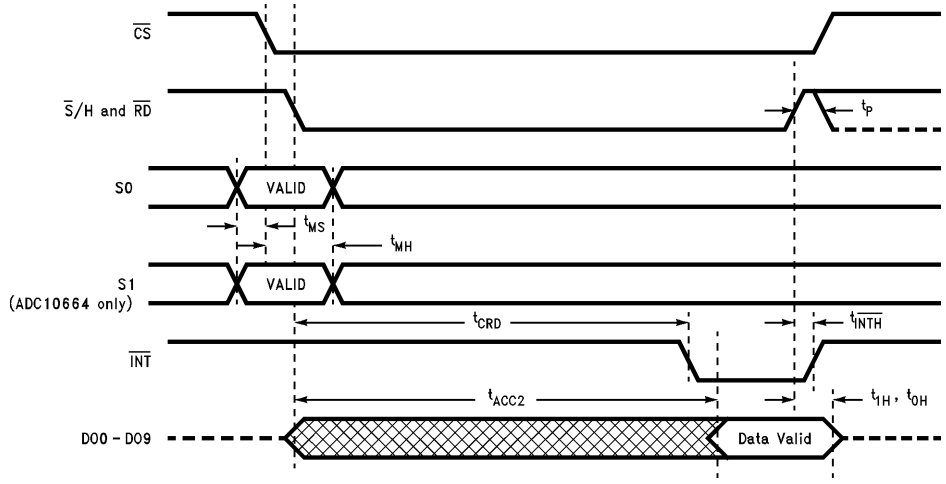

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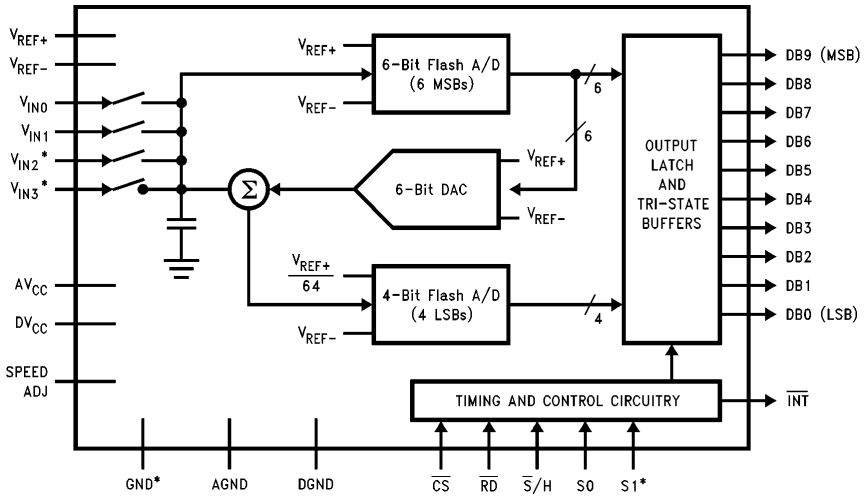
FIGURE 2. Mode 2 ($\overline{RD}$ Mode). The conversion time (t_{CRD}) includes the sampling time and is determined by the internal timer.

Simplified Block Diagram



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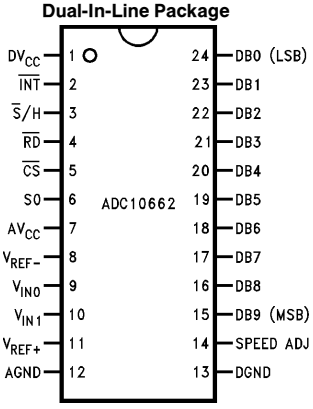
*ADC10664 Only

Connection Diagrams

Dual-In-Line Package



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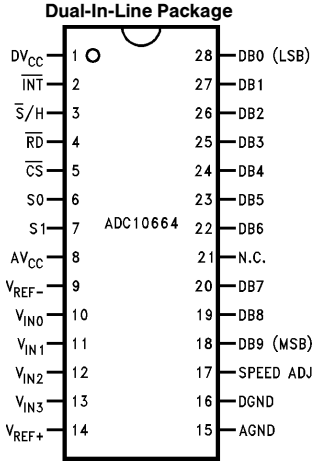
Top View

Dual-In-Line Package



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Top View

Pin Descriptions

DV_{CC}, AV_{CC} These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor to ground.

$\overline{INT}$ This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.

$\overline{S}$/H This is the Sample/Hold control input. When this pin is forced low (and $\overline{CS}$ is low), it causes the analog input signal to be sampled and initiates a new conversion.

$\overline{RD}$ This is the active low Read control input. When this $\overline{RD}$ and $\overline{CS}$ are low, any data present in the output registers will be placed on the data bus.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$ and $\overline{S}$/H pins.

S0, S1 These pins select the analog input that will be connected to the A/D during the conversion. The input is selected based on the state of S0 and S1 when $\overline{S}$/H makes its High-to-Low transition (See the Timing Diagrams). The ADC10664 includes both S0 and S1. The ADC10662 includes just S0.

V_{REF-}, V_{REF+} These are the reference voltage inputs. They may be placed at any voltage between GND and V_{CC}, but V_{REF+} must be greater than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to (V_{REF+} − 1 LSB) produces an output code of 1023.

V_{IN0}, V_{IN1}, V_{IN2}, V_{IN3} These are the analog input pins. The ADC10662 has two inputs (V_{IN0} and V_{IN1}) and the ADC10664 has four inputs (V_{IN0}, V_{IN1}, V_{IN2} and V_{IN3}). The impedance of the source should be less than 500Ω for best accuracy and conversion speed. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV above V_{CC} or 50 mV below ground.

GND, AGND, DGND These are the power supply ground pins. The ADC10662 and ADC10664 have separate analog and digital ground pins (AGND and DGND) for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. Both pins should be returned to the same potential.

DB0–DB9 These are the TRI-STATE output pins.

SPEED ADJ By connecting a resistor between this pin and ground, the conversion time can be reduced. The specifications listed in the table of Electrical Characteristics apply for a speed adjust resistor (R_{SA}) equal to 14.0 kΩ (Mode 1) or 8.26 kΩ (Mode 2). See the Typical Performance Curves and the table of Electrical Characteristics.

Functional Description

The ADC10662 and ADC10664 digitize an analog input signal to 10 bits accuracy by performing two lower-resolution ''flash'' conversions. The first flash conversion provides the six most significant bits (MSBs) of data, and the second flash conversion provides the four least significant bits LSBs).

Figure 3 is a simplified block diagram of the converter. Near the center of the diagram is a string of resistors. At the bottom of the string of resistors are 16 resistors, each of which has a value 1/1024 the resistance of the whole resistor string. These lower 16 resistors (the **LSB Ladder**) therefore have a voltage drop of 16/1024, or 1/64 of the total reference voltage ($V_{REF+} - V_{REF-}$) across them. The remainder of the resistor string is made up of eight groups of eight resistors connected in series. These comprise the **MSB Ladder**. Each section of the MSB Ladder has 1/8 of the total reference voltage across it, and each of the LSB resistors has 1/64 of the total reference voltage across it. Tap points across these resistors can be connected, in groups of sixteen, to the sixteen comparators at the right of the diagram.

On the left side of the diagram is a string of seven resistors connected between V_{REF+} and V_{REF-}. Six comparators compare the input voltage with the tap voltages on this resistor string to provide a low-resolution ''estimate'' of the input voltage. This estimate is then used to control the multiplexer that connects the MSB Ladder to the sixteen comparators on the right. Note that the comparators on the left needn't be very accurate; they simply provide an estimate of the input voltage. Only the sixteen comparators on the right and the six on the left are necessary to perform the initial six-bit flash conversion, instead of the 64 comparators that would be required using conventional half-flash methods.

To perform a conversion, the estimator compares the input voltage with the tap voltages on the seven resistors on the left. The estimator decoder then determines which MSB Ladder tap points will be connected to the sixteen comparators on the right. For example, assume that the estimator determines that V_{IN} is between 11/16 and 13/16 of V_{REF}. The estimator decoder will instruct the comparator MUX to connect the 16 comparators to the taps on the MSB ladder between 10/16 and 14/16 of V_{REF}. The 16 comparators will then perform the first flash conversion. Note that since the comparators are connected to ladder voltages that extend beyond the range indicated by the estimator circuit, errors in the estimator as large as 1/16 of the reference voltage (64 LSBs) will be corrected. This first flash conversion produces the six most significant bits of data—four bits in the flash itself, and 2 bits in the estimator.

The remaining four LSBs are now determined using the same sixteen comparators that were used for the first flash conversion. The MSB Ladder tap voltage just below the input voltage (as determined by the first flash) is subtracted from the input voltage and compared with the tap points on the sixteen LSB Ladder resistors. The result of this second, four-bit flash conversion is then decoded, and the full 10-bit result is latched.

Note that the sixteen comparators used in the first flash conversion are reused for the second flash. Thus, the multistep conversion technique used in the ADC10662 and ADC10664 needs only a small fraction of the number of comparators that would be required for a traditional flash converter, and far fewer than would be used in a conventional half-flash approach. This allows the ADC10662 and ADC10664 to perform high-speed conversions without excessive power drain.

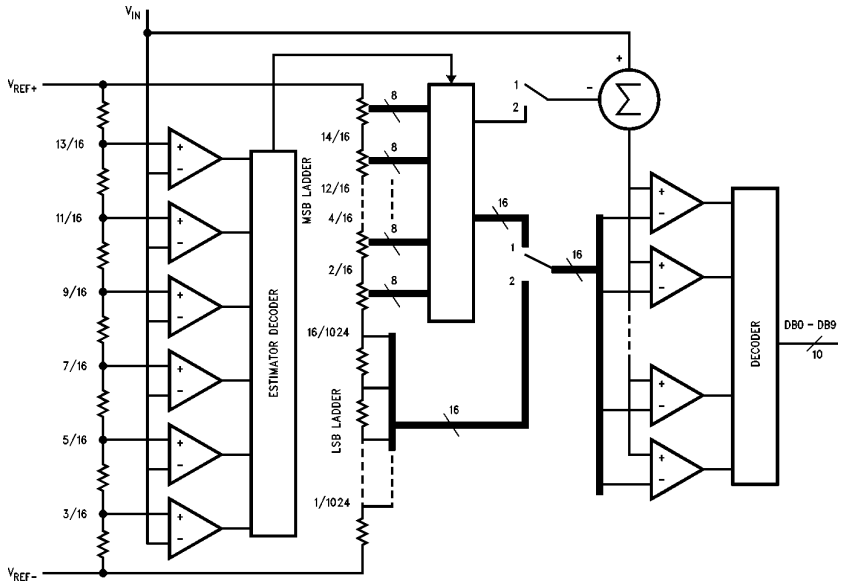

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FIGURE 3. Block Diagram of the Multistep Converter Architecture

Applications Information

1.0 MODES OF OPERATION

The ADC10662 and ADC10664 have two basic digital interface modes. *Figure 1* and *Figure 2* are timing diagrams for the two modes. The ADC10662 and ADC10664 have input multiplexers that are controlled by the logic levels on pins S_0 and S_1 when $\overline{S}/H$ goes low. Table I is a truth table showing how the input channnels are assigned.

Mode 1

In this mode, the $\overline{S}/H$ pin controls the start of conversion. $\overline{S}/H$ is pulled low for a minimum of 150 ns. This causes the comparators in the ''coarse'' flash converter to become active. When $\overline{S}/H$ goes high, the result of the coarse conversion is latched and the ''fine'' conversion begins. After 360 ns (typical), $\overline{INT}$ goes low, indicating that the conversion results are latched and can be read by pulling $\overline{RD}$ low. Note that $\overline{CS}$ must be low to enable $\overline{S}/H$ or $\overline{RD}$. $\overline{CS}$ is internally ''ANDed'' with $\overline{S}/H$ and $\overline{RD}$; the input voltage is sampled when $\overline{CS}$ and $\overline{S}/H$ are low, and data is read when $\overline{CS}$ and $\overline{RD}$ are low. $\overline{INT}$ is reset high on the rising edge of $\overline{RD}$.

TABLE I. Input Multiplexer Programming

ADC10664

S_1	S_0	Channel
0	0	V_{IN0}
0	1	V_{IN1}
1	0	V_{IN2}
1	1	V_{IN3}

(a)

ADC10662

S_0	Channel
0	V_{IN0}
1	V_{IN1}

(b)

Mode 2

In Mode 2, also called ''$\overline{RD}$ mode'', the $\overline{S}/H$ and $\overline{RD}$ pins are tied together. A conversion is initiated by pulling both pins low. The A/D converter samples the input voltage and causes the coarse comparators to become active. An internal timer then terminates the coarse conversion and begins the fine conversion. 470 ns (typical) after $\overline{S}/H$ and $\overline{RD}$ are pulled low, $\overline{INT}$ goes low, indicating that the conversion is completed. Approximately 20 ns later the data appearing on the TRI-STATE output pins will be valid. Note that data will appear on these pins throughout the conversion, but until $\overline{INT}$ goes low the data at the output pins will be the result of the previous conversion.

2.0 REFERENCE CONSIDERATIONS

The ADC10662 and ADC10664 each have two reference inputs. These inputs, V_{REF+} and V_{REF-}, are fully differential and define the zero to full-scale range of the input signal. The reference inputs can be connected to span the entire supply voltage range ($V_{REF-} = 0V$, $V_{REF+} = V_{CC}$) for ratiometric applications, or they can be connected to different voltages (as long as they are between ground and V_{CC}) when other input spans are required. Reducing the overall V_{REF} span to less than 5V increases the sensitivity of the converter (e.g., if $V_{REF} = 2V$, then 1 LSB = 1.953 mV). Note, however, that linearity and offset errors become larger when lower reference voltages are used. See the Typical Performance Curves for more information. For this reason, reference voltages less than 2V are not recommended.

In most applications, V_{REF-} will simply be connected to ground, but it is often useful to have an input span that is offset from ground. This situation is easily accommodated by the reference configuration used in the ADC10662 and ADC10664. V_{REF-} can be connected to a voltage other than ground as long as the voltage source connected to this pin is capable of sinking the converter's reference current (12.5 mA Max @ $V_{REF} = 5V$). If V_{REF-} is connected to a voltage other than ground, bypass it with multiple capacitors.

Since the resistance between the two reference inputs can be as low as 400Ω, the voltage source driving the reference inputs should have low output impedance. Any noise on either reference input is a potential cause of conversion errors, so each of these pins must be supplied with a clean, low noise voltage source. Each reference pin should be bypassed with a 10 μF tantalum and a 0.1 μF ceramic.

3.0 THE ANALOG INPUT

The ADC10662 and ADC10664 sample the analog input voltage once every conversion cycle. When this happens, the input is briefly connected to an impedance approximately equal to 600Ω in series with 35 pF. Short-duration current spikes can therefore be observed at the analog input during normal operation. These spikes are normal and do not degrade the converter's performance.

Large source impedances can slow the charging of the sampling capacitors and degrade conversion accuracy. Therefore, only signal sources with output impedances less than 500Ω should be used if rated accuracy is to be achieved at the minimum sample time (250 ns maximum). If the sampling time is increased, the source impedance can be larger. If a signal source has a high output impedance, its output should be buffered with an operational amplifier. The operational amplifier's output should be well-behaved when driving a switched 35 pF/600Ω load. Any ringing or voltage shifts at the op amp's output during the sampling period can result in conversion errors.

Correct conversion results will be obtained for input voltages greater than GND − 50 mV and less than V^+ + 50 mV. Do not allow the signal source to drive the analog input pin more than 300 mV higher than AV_{CC} and DV_{CC}, or more than 300 mV lower than GND. If an analog input pin is forced beyond these voltages, the current flowing through the pin should be limited to 5 mA or less to avoid permanent damage to the IC. The sum of all the overdrive currents into all pins must be less than 20 mA. When the input signal is expected to extend more than 300 mV beyond the power supply limits, some sourt of protection scheme should be used. A simple network using diodes and resistors is shown in *Figure 4*.

Applications Information (Continued)

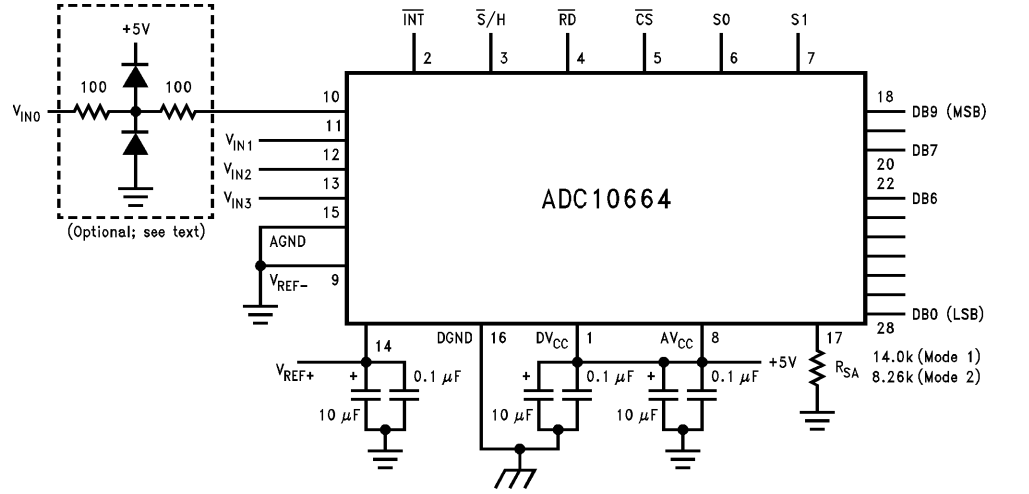

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FIGURE 4. Typical Connection. Note the multiple bypass capacitors on the reference and power supply pins. If V_{REF-} is not grounded, it should also be bypassed to analog ground using multiple capacitors (see 5.0 "Power Supply Considerations"). AGND and DGND should be at the same potential. V_{IN0} is shown with an input protection network.

4.0 INHERENT SAMPLE-AND-HOLD

Because the ADC10662 and ADC10664 sample the input signal once during each conversion, they are capable of measuring relatively fast input signals without the help of an external sample-hold. In a non-sampling successive-approximation A/D converter, regardless of speed, the input signal must be stable to better than ±1/2 LSB during each conversion cycle or significant errors will result. Consequently, even for many relatively slow input signals, the signals must be externally sampled and held constant during each conversion if a SAR with no internal sample-and-hold is used.

Because they incorporate a direct sample/hold control input, the ADC10662 and ADC10664 are suitable for use in DSP-based systems. The $\overline{S}$/H input allows synchronization of the A/D converter to the DSP system's sampling rate and to other ADC10662s, and ADC10664s.

The ADC10662 and ADC10664 can perform accurate conversions of input signals with frequency components from DC to over 250 kHz.

5.0 POWER SUPPLY CONSIDERATIONS

The ADC10662 and ADC10664 are designed to operate from a +5V (nominal) power supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply pins should be connected to the same voltage source, and each should be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor. Depending on the circuit board layout and other system considerations, more bypassing may be necessary.

The ADC10662 and ADC10664 have separate analog and digital ground pins for separate bypassing of the analog and digital supplies. Their ground pins should be connected to the same potential, and all grounds should be "clean" and free of noise.

In systems with multiple power supplies, careful attention to power supply sequencing may be necessary to avoid overdriving inputs. The A/D converter's power supply pins should be at the proper voltage before digital or analog signals are applied to any of the other pins.

6.0 LAYOUT AND GROUNDING

In order to ensure fast, accurate conversions from the ADC10662 and ADC10664, it is necessary to use appropriate circuit board layout techniques. The analog ground return path should be low-impedance and free of noise from other parts of the system. Noise from digital circuitry can be especially troublesome, so digital grounds should always be separate from analog grounds. For best performance, separate ground planes should be provided for the digital and analog parts of the system.

All bypass capacitors should be located as close to the converter as possible and should connect to the converter and to ground with short traces. The analog input should be isolated from noisy signal traces to avoid having spurious signals couple to the input. Any external component (e.g., a filter capacitor) connected across the converter's input should be connected to a very clean ground return point. Grounding the component at the wrong point will result in reduced conversion accuracy.

7.0 DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but conventional DC integral and differential nonlinearity specifications don't accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynam-

Applications Information (Continued)

ic characteristics such as signal-to-noise ratio (SNR) and total harmonic distortion (THD), are quantitative measures of this capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. The resulting spectral plot might look like the ones shown in the typical performance curves. The large peak is the fundamental frequency, and the noise and distortion components (if any are present) are visible above and below the fundamental frequency. Harmonic distortion components appear at whole multiples of the input frequency. Their amplitudes are combined as the square root of the sum of the squares and compared to the fundamental amplitude to yield the THD specification. Guaranteed limits for THD are given in the table of Electrical Characteristics.

Signal-to-noise ratio is the ratio of the amplitude at the fundamental frequency to the rms value at all other frequencies, excluding any harmonic distortion components. Guaranteed limits are given in the Electrical Characteristics table. An alternative definition of signal-to-noise ratio includes the distortion components along with the random noise to yield a signal-to-noise-plus-distortion ration, or S/(N + D).

The THD and noise performance of the A/D converter will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. One way of describing the A/D's performance as a function of signal frequency is to make a plot of ''effective bits'' versus frequency. An ideal A/D converter with no linearity errors or self-generated noise will have a signal-to-noise ratio equal to (6.02n + 1.8) dB, where n is the resolution in bits of the A/D converter. A real A/D converter will have some amount of noise and distortion, and the effective bits can be found by:

$$\text{n (effective)} = \frac{\text{S/(N + D) (dB)} - 1.8}{6.02}$$

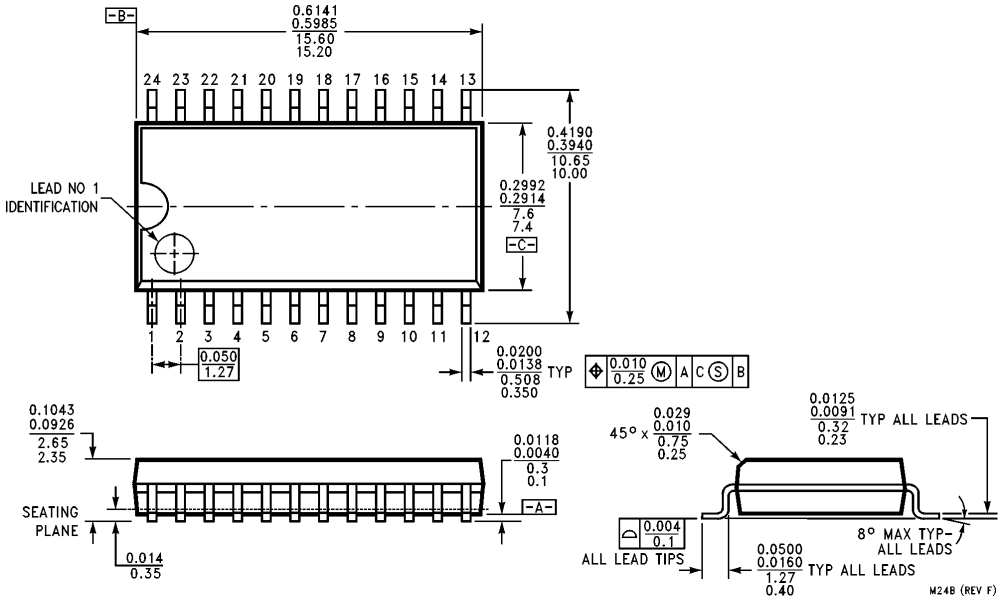
where S/(N + D) is the ratio of signal to noise and distortion, which can vary with frequency.

As an example, an ADC10662 with a 4.85 V_{P-P}, 100 kHz sine wave input signal will typically have a signal-to-noise-plus-distortion ratio of 59.2 dB, which is equivalent to 9.53 effective bits. As the input frequency increases, noise and distortion gradually increase, yielding a plot of effective bits or S/(N + D) as shown in the typical performance curves.

8.0 SPEED ADJUST

The speed adjust pin is connected to an on-chip current source that determines the converter's internal timing. By connecting a resistor between the speed adjust pin and ground as shown in *Figure 4*, the internal programming current is increased, which reduces the conversion time. The ADC10662 and ADC10664 are specified and guaranteed for operation with R_{SA} = 14.0 kΩ (Mode 1) or R_{SA} = 8.26k (Mode 2). Smaller resistors will result in faster conversion times, but linearity will begin to degrade as R_{SA} becomes smaller (see curves).

Physical Dimensions inches (millimeters)



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NS Package Number M24B

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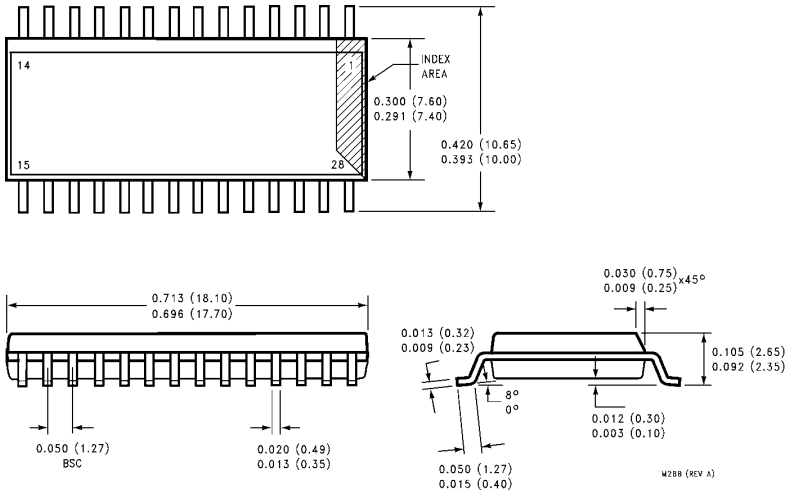

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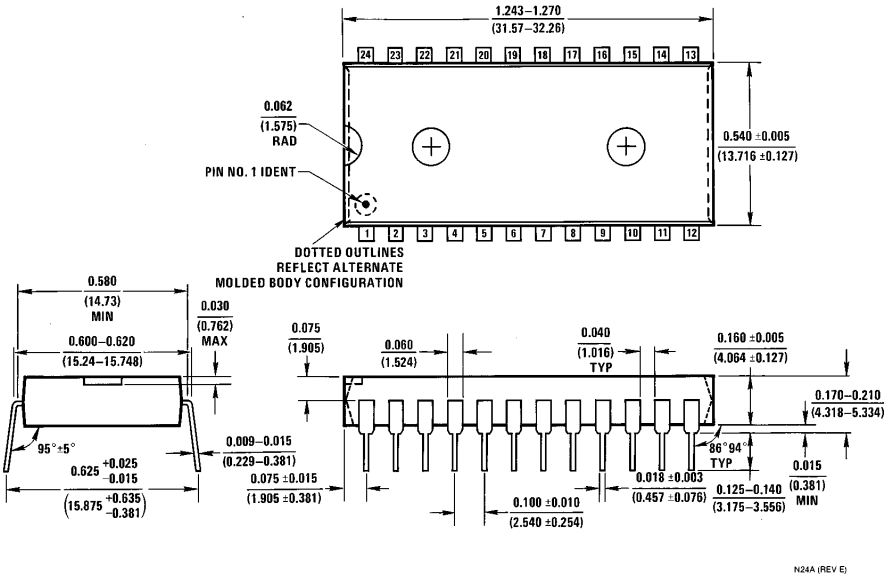
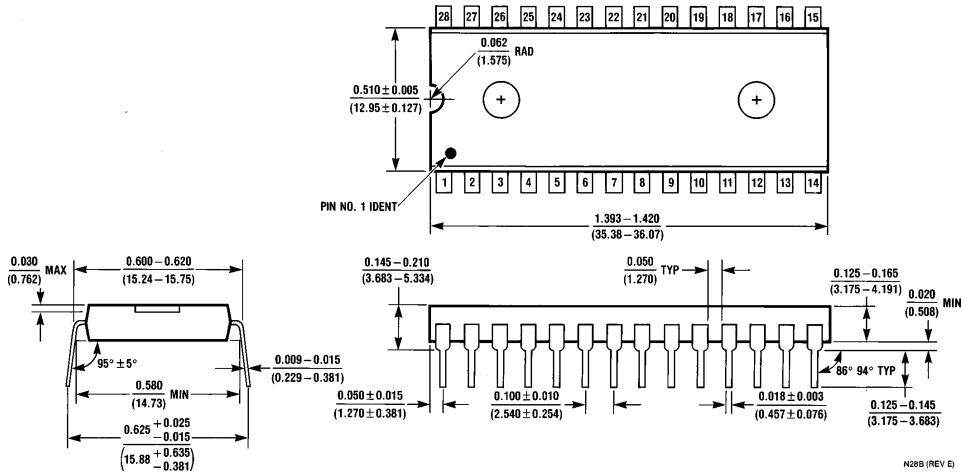


Order Number ADC10662CIN
NS Package Number N24A

Physical Dimensions inches (millimeters) (Continued)



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