PRELIMINARY

CYP15G0401DXA

Quad HOTLink II™ Transceiver

Features

- 2nd generation HOTLink® technology
- Fibre Channel and Gigabit Ethernet compliant 8B/10B-coded or 10-bit unencoded
- ESCON, DVB-ASI Compliant
- SMPTE-292M, SMPTE-259M Compliant
- 8-bit encoded data transport
  - Aggregate throughput of 9.6 GBits/second
- 10-bit unencoded data transport
  - Aggregate throughput of 12 GBits/second
- Selectable parity check/generate
- Selectable multi-channel bonding options
  - Four 8-bit channels
  - Two 16-bit channels
  - One 32-bit channel
  - N x 32-bit channel support (inter-chip)
- Selectable input clocking options
- Selectable output clocking options
- MultiFrame™ Receive Framer provides alignment to
  - Bit, byte, half-word, word, multi-word
  - Comma or Full K28.5 detect
  - Single or Multi-byte Framer for byte alignment
  - Low-latency option
- Skew alignment support for multiple bytes of offset
- Synchronous LVTTL parallel input interface
- Synchronous LVTTL parallel output interface
- 200-to-1500 MBaud serial signaling rate
- Internal PLLs with *no* external PLL components
- Dual differential PECL-compatible serial inputs per channel
  - Internal DC-restoration
- Dual differential PECL-compatible serial outputs per channel
  - Source matched for 50Ω transmission lines
  - No external bias resistors required
  - Signaling-rate controlled edge-rates
- Compatible with
  - Fiber-optic modules
  - Copper cables
  - Circuit board traces
- JTAG boundary scan
- Built-In Self-Test (BIST) for at-speed link testing
- Per-channel Link Quality Indicator
  - Analog signal detect
  - Digital signal detect
  - Frequency range detect
- Low Power 2.8W @ 3.3V Typical
- Single 3.3V supply
- 256-ball Thermally Enhanced BGA
- 0.25µ BiCMOS technology

Functional Description

The CYP15G0401DXA Quad HOTLink II™ Transceiver is a point-to-point or point-to-multipoint communications building block allowing the transfer of data over high-speed serial links (optical fiber, balanced, and unbalanced copper transmission lines) at signaling speeds ranging from 200-to-1500 MBaud per serial link. The multiple channels in each device may be combined to allow transport of wide buses across significant distances with minimal concern for offsets in clock phase or link delay.

Each transmit channel accepts parallel characters in an Input Register, encodes each character for transport, and converts it to serial data. Each receive channel accepts serial data and converts it to parallel data, decodes the data into characters,

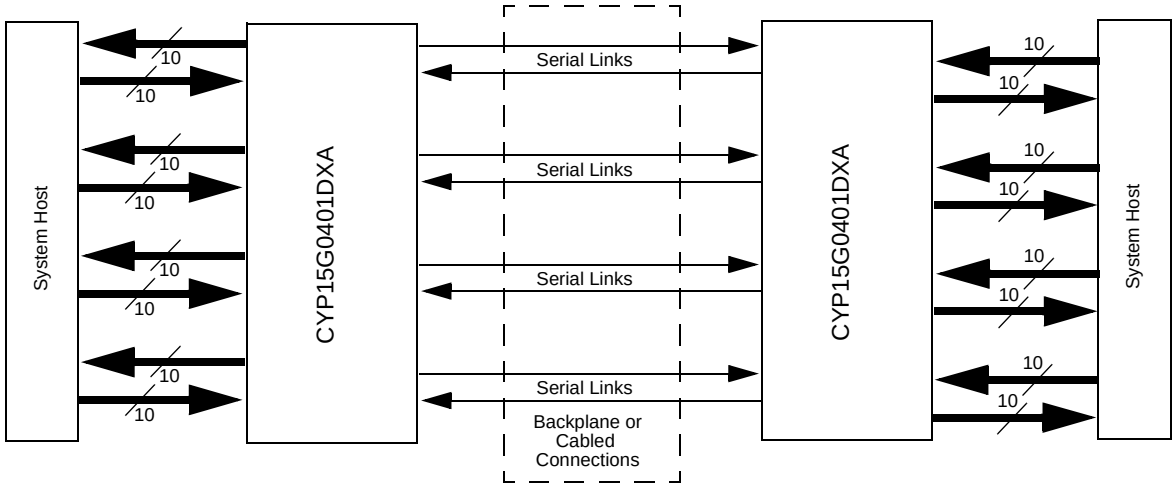


Figure 1. HOTLink II™ System Connections

and presents these characters to an Output Register. *Figure 1* illustrates typical connections between independent host systems and corresponding CYP15G0401DXA parts. As a second-generation HOTLink device, the CYP15G0401DXA extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data, command, and BIST) with other HOTLink devices.

The transmit (TX) section of the CYP15G0401DXA Quad HOTLink II consists of four byte-wide channels that can be operated independently or bonded to form wider buses. Each channel can accept either 8-bit data characters or pre-encoded 10-bit transmission characters. Data characters are passed from the Transmit Input Register to an embedded 8B/10B Encoder to improve their serial transmission characteristics. These encoded characters are then serialized and output from dual Positive ECL (PECL) compatible differential transmission-line drivers at a bit-rate of either 10- or 20-times the input reference clock.

The receive (RX) section of the CYP15G0401DXA Quad HOTLink II consists of four byte-wide channels that can be operated independently or synchronously bonded for greater bandwidth. Each channel accepts a serial bit-stream from one of two PECL-compatible differential line receivers and, using a completely integrated PLL Clock Synchronizer, recovers the timing information necessary for data reconstruction. Each recovered bit-stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are then written to an internal Elasticity Buffer, and presented to the destination host system. The integrated 8B/10B Encoder/Decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

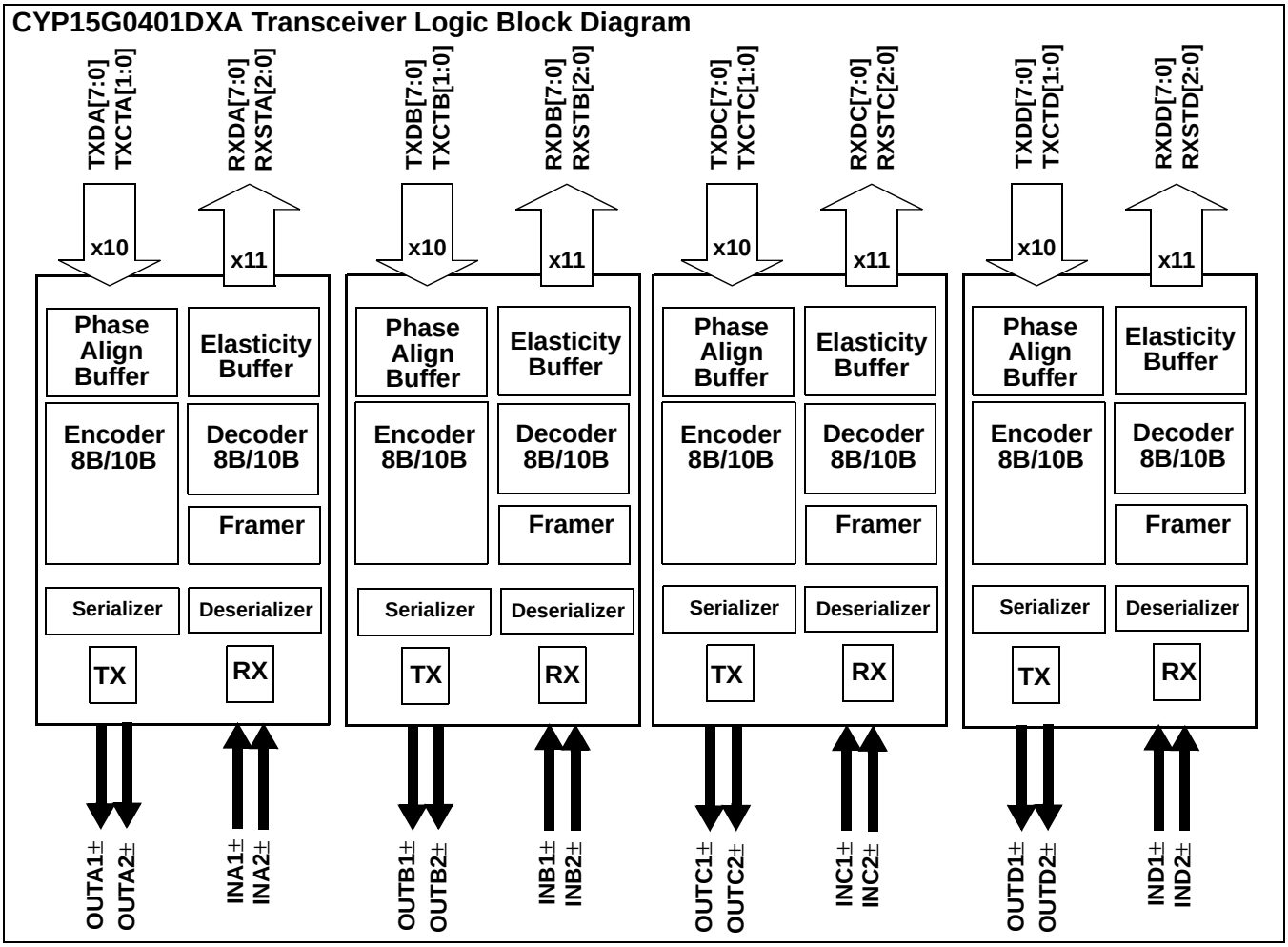
For those systems using buses wider than a single byte, the four independent receive paths can be bonded together to allow synchronous delivery of data across a two-byte-wide (16-bit) path, or across all four bytes (32-bit). Multiple CYP15G0401DXA devices may be bonded together to provide synchronous transport of buses wider than 32 bits.

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. In addition to clocking the transmit path, the receive interface may be configured to present data relative to a recovered clock or to a local reference clock.

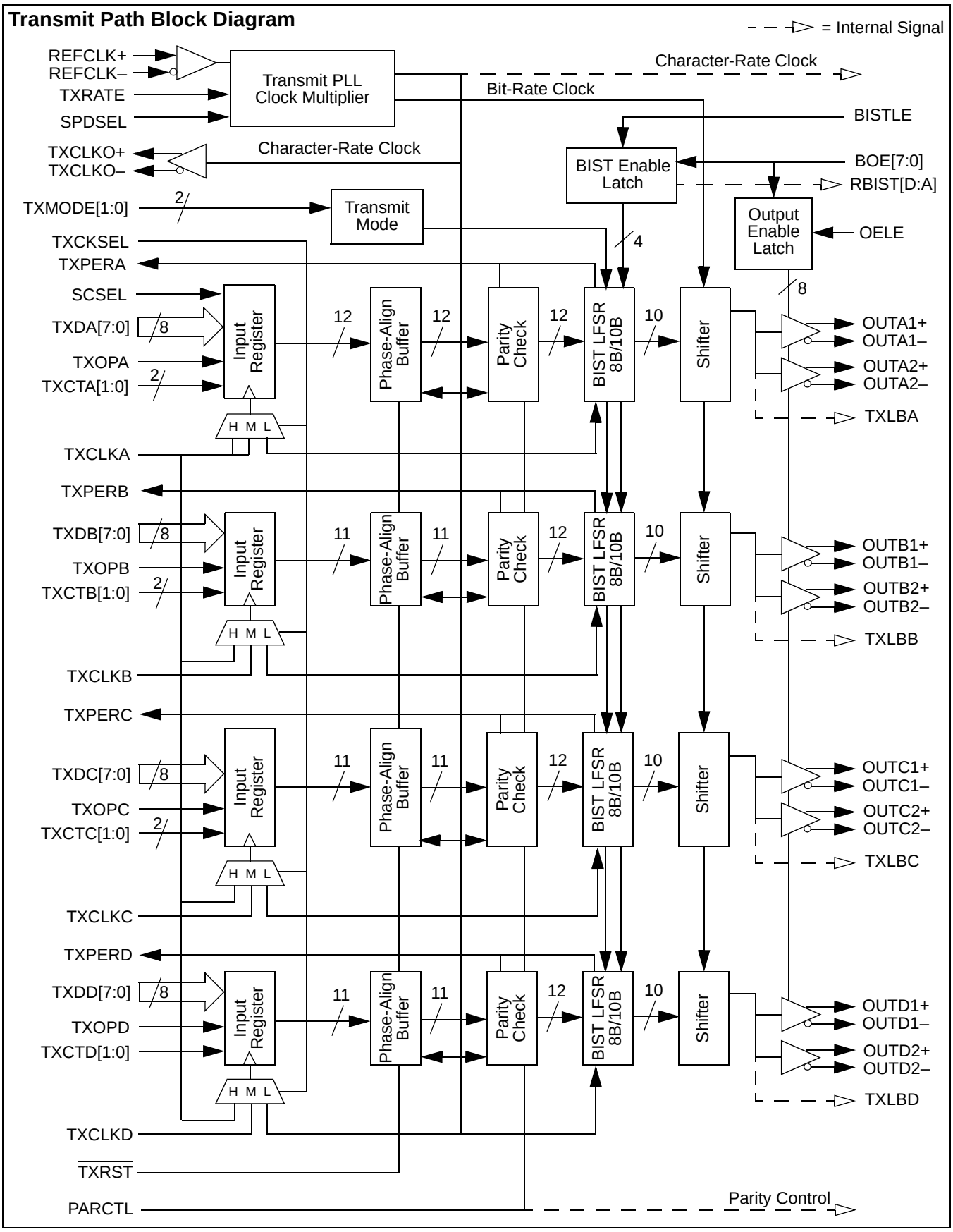
Each transmit and receive channel contains an independent Built-In Self-Test pattern generator and checker. This BIST hardware allows at-speed testing of the high-speed serial data paths in each transmit and receive section, and across the interconnecting links.

HOTLink II devices are ideal for a variety of applications where parallel interfaces can be replaced with high-speed, point-to-point serial links. Some applications include interconnecting backplanes on basestations, switches, routers, servers and video transmission systems.

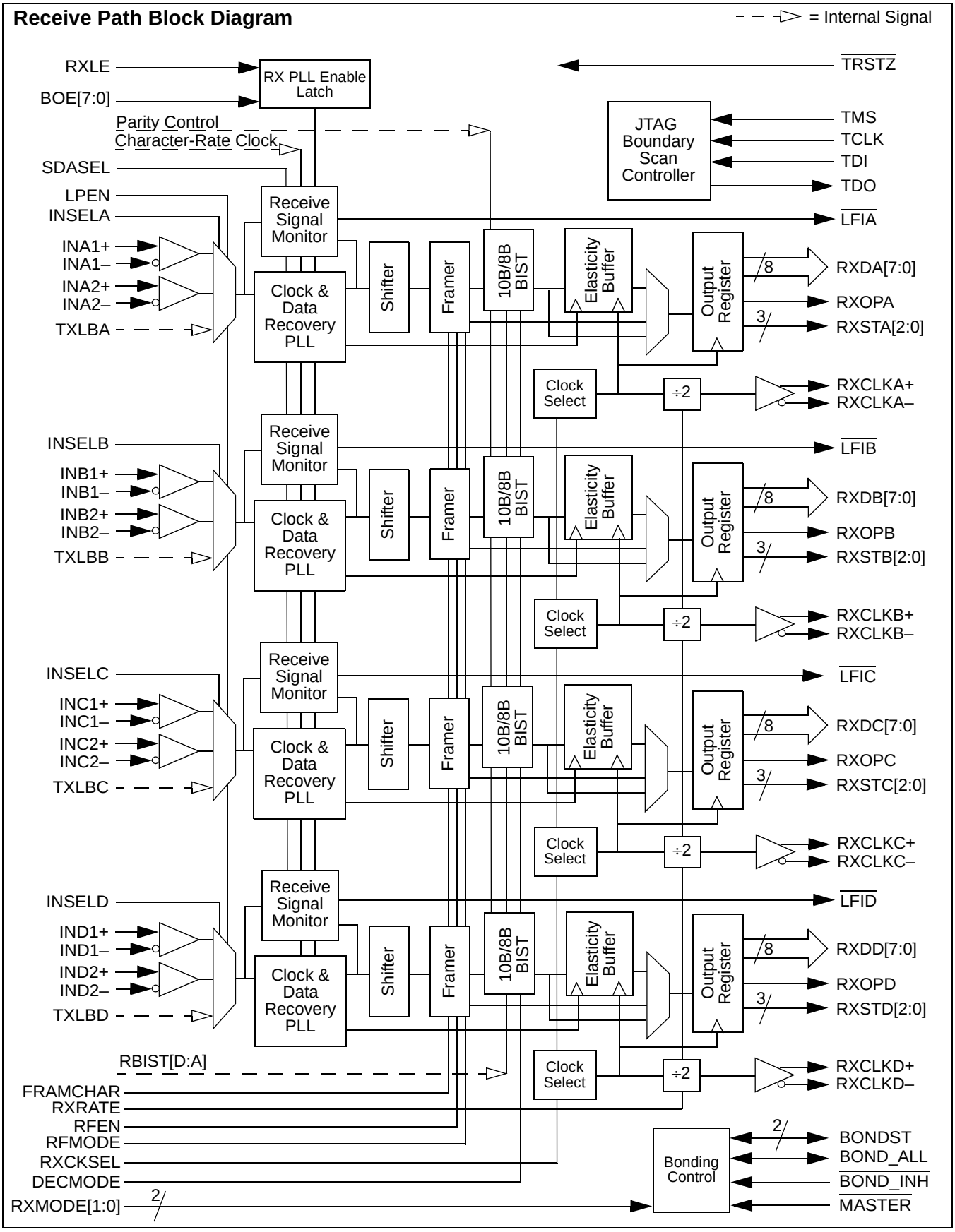
CYP15G0401DXA Transceiver Logic Block Diagram



Transmit Path Block Diagram



Receive Path Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	INC1–	OUT C1–	INC2–	OUT C2–	**V_{CC}**	IND1–	OUT D1–	**GND**	IND2–	OUT D2–	INA1–	OUT A1–	**GND**	INA2–	OUT A2–	**V_{CC}**	INB1–	OUT B1–	INB2–	OUT B2–
B	INC1+	OUT C1+	INC2+	OUT C2+	**V_{CC}**	IND1+	OUT D1+	**GND**	IND2+	OUT D2+	INA1+	OUT A1+	**GND**	INA2+	OUT A2+	**V_{CC}**	INB1+	OUT B1+	INB2+	OUT B2+
C	TDI	TMS	INSELC	INSELB	**V_{CC}**	PAR CTL	SDA SEL	**GND**	BOE[7]	BOE[5]	BOE[3]	BOE[1]	**GND**	TX MODE [0]	RX MODE [0]	**V_{CC}**	TX RATE	RX RATE	LPEN	TDO
D	TCLK	$\overline{\text{TRSTZ}}$	INSELD	INSELA	**V_{CC}**	RF MODE	SPD SEL	**GND**	BOE[6]	BOE[4]	BOE[2]	BOE[0]	**GND**	TX MODE [1]	RX MODE [1]	**V_{CC}**	$\overline{\text{BOND}}$ INH	RXLE	RFEN	$\overline{\text{MAS}}$ TER
E	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
F	TX PERC	TX OPC	TX DC[0]	RXCK SEL													BISTLE	RX STB[1]	RXOPB	RX STB[0]
G	TX DC[7]	TXCK SEL	TX DC[4]	TX DC[1]													DEC MODE	OELE	FRAM CHAR	RX DB[1]
H	**GND**	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**
J	TX CTC[1]	TX DC[5]	TX DC[2]	TX DC[3]													RX STB[2]	RX DB[0]	RX DB[5]	RX DB[2]
K	RX DC[2]	RXCLK C–	TX CTC[0]	$\overline{\text{LFIC}}$													RX DB[3]	RX DB[4]	RX DB[7]	RX CLK B+
L	RX DC[3]	RXCLK C+	TX CLKC	TX DC[6]													RX DB[6]	$\overline{\text{LFIB}}$	RX CLK B–	TX DB[6]
M	RX DC[4]	RX DC[5]	RX DC[7]	RX DC[6]													TX CTB[1]	TX CTB[0]	TX DB[7]	TX CLKB
N	**GND**	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**
P	RX DC[1]	RX DC[0]	RX STC[0]	RX STC[1]													TX DB[5]	TX DB[4]	TX DB[3]	TX DB[2]
R	RX STC[2]	RX OPC	TX PERD	TX OPD													TX DB[1]	TX DB[0]	TX OPB	TX PERB
T	**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**
U	TX DD[0]	TX DD[1]	TX DD[2]	TX CTD[1]	**V_{CC}**	RX DD[2]	RX DD[1]	**GND**	RX OPD	BOND _ALL	REF CLK–	TXDA[1]	**GND**	TXDA[4]	TX CTA[0]	**V_{CC}**	RX DA[2]	RXOPA	RX STA[2]	RX STA[1]
V	TX DD[3]	TX DD[4]	TX CTD[0]	RX DD[6]	**V_{CC}**	RX DD[3]	RX STD[0]	**GND**	RX STD[2]	BOND ST[0]	REF CLK+	BOND ST[1]	**GND**	TXDA[3]	TXDA[7]	**V_{CC}**	RX DA[7]	RX DA[3]	RX DA[0]	RX STA[0]
W	TX DD[5]	TX DD[7]	$\overline{\text{LFID}}$	RXCLK D–	**V_{CC}**	RX DD[4]	RX STD[1]	**GND**	TX CLK O–	$\overline{\text{TXRST}}$	TXOPA	SCSEL	**GND**	TXDA[2]	TXDA[6]	**V_{CC}**	$\overline{\text{LFIA}}$	RX CLK A–	RX DA[4]	RX DA[1]
Y	TX DD[6]	TX CLKD	RX DD[7]	RXCLK D+	**V_{CC}**	RX DD[5]	RX DD[0]	**GND**	TX CLK O+	N/C	TX CLKA	TX PERA	**GND**	TXDA[0]	TXDA[5]	**V_{CC}**	TX CTA[1]	RX CLK A+	RX DA[6]	RX DA[5]

Pin Configuration (Bottom View)

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
OUT B2–	INB2–	OUT B1–	INB1–	**V_{CC}**	OUT A2–	INA2–	**GND**	OUT A1–	INA1–	OUT D2–	IND2–	**GND**	OUT D1–	IND1–	**V_{CC}**	OUT C2–	INC2–	OUT C1–	INC1–	A
OUT B2+	INB2+	OUT B1+	INB1+	**V_{CC}**	OUT A2+	INA2+	**GND**	OUT A1+	INA1+	OUT D2+	IND2+	**GND**	OUT D1+	IND1+	**V_{CC}**	OUT C2+	INC2+	OUT C1+	INC1+	B
TDO	LPEN	RX RATE	TX RATE	**V_{CC}**	RX MODE [0]	TX MODE [0]	**GND**	BOE[1]	BOE[3]	BOE[5]	BOE[7]	**GND**	SDA SEL	PAR CTL	**V_{CC}**	INSELB	INSELC	TMS	TDI	C
$\overline{\text{MAS TER}}$	RFEN	RXLE	$\overline{\text{BOND INH}}$	**V_{CC}**	RX MODE [1]	TX MODE [1]	**GND**	BOE[0]	BOE[2]	BOE[4]	BOE[6]	**GND**	SPD SEL	RF MODE	**V_{CC}**	INSELA	INSELD	$\overline{\text{TRSTZ}}$	TCLK	D
V_{CC}	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**	E
RX STB[0]	RXOPB	RX STB[1]	BISTLE													RXCK SEL	TX DC[0]	TX OPC	TX PERC	F
RX DB[1]	FRAM CHAR	OELE	DEC MODE													TX DC[1]	TX DC[4]	TXCK SEL	TX DC[7]	G
GND	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**	H
RX DB[2]	RX DB[5]	RX DB[0]	RX STB[2]													TX DC[3]	TX DC[2]	TX DC[5]	TX CTC[1]	J
RX CLK B+	RX DB[7]	RX DB[4]	RX DB[3]													$\overline{\text{LFIC}}$	TX CTC[0]	RXCLK C–	RX DC[2]	K
TX DB[6]	RX CLK B–	$\overline{\text{LFIB}}$	RX DB[6]													TX DC[6]	TX CLKC	RXCLK C+	RX DC[3]	L
TX CLKB	TX DB[7]	TX CTB[0]	TX CTB[1]													RX DC[6]	RX DC[7]	RX DC[5]	RX DC[4]	M
GND	**GND**	**GND**	**GND**													**GND**	**GND**	**GND**	**GND**	N
TX DB[2]	TX DB[3]	TX DB[4]	TX DB[5]													RX STC[1]	RX STC[0]	RX DC[0]	RX DC[1]	P
TX PERB	TX OPB	TX DB[0]	TX DB[1]													TX OPD	TX PERD	RX OPC	RX STC[2]	R
V_{CC}	**V_{CC}**	**V_{CC}**	**V_{CC}**													**V_{CC}**	**V_{CC}**	**V_{CC}**	**V_{CC}**	T
RX STA[1]	RX STA[2]	RXOPA	RX DA[2]	**V_{CC}**	TX CTA[0]	TXDA[4]	**GND**	TXDA[1]	REF CLK–	BOND _ALL	RX OPD	**GND**	RX DD[1]	RX DD[2]	**V_{CC}**	TX CTD[1]	TX DD[2]	TX DD[1]	TX DD[0]	U
RX STA[0]	RX DA[0]	RX DA[3]	RX DA[7]	**V_{CC}**	TXDA[7]	TXDA[3]	**GND**	BOND ST[1]	REF CLK+	BOND ST[0]	RX STD[2]	**GND**	RX STD[0]	RX DD[3]	**V_{CC}**	RX DD[6]	TX CTD[0]	TX DD[4]	TX DD[3]	V
RX DA[1]	RX DA[4]	RX CLK A–	$\overline{\text{LFIA}}$	**V_{CC}**	TXDA[6]	TXDA[2]	**GND**	SCSEL	TXOPA	$\overline{\text{TXRST}}$	TX CLK O–	**GND**	RX STD[1]	RX DD[4]	**V_{CC}**	RXCLK D–	$\overline{\text{LFID}}$	TX DD[7]	TX DD[5]	W
RX DA[5]	RX DA[6]	RX CLK A+	TX CTA[1]	**V_{CC}**	TXDA[5]	TXDA[0]	**GND**	TX PERA	TX CLKA	N/C	TX CLK O+	**GND**	RX DD[0]	RX DD[5]	**V_{CC}**	RXCLK D+	RX DD[7]	TX CLKD	TX DD[6]	Y

Pin Descriptions

CYP15G0401DXA Quad HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
Transmit Path Data Signals		
TXPERA TXPERB TXPERC TXPERD	LVTTL Output, changes relative to REFCLK↑ [1]	**Transmit Path Parity Error**. Active HIGH. Asserted (HIGH) if parity checking is enabled and a parity error is detected at the Encoder. This output is HIGH for one transmit character clock period to indicate detection of a parity error in the character presented to the Encoder. If a parity error is detected, the character in error is replaced with a C0.7 character to force a corresponding bad-character detection at the remote end of the link. This replacement takes place regardless of the encoded/non-encoded state of the interface. When BIST is enabled for the specific transmit channel, BIST progress is presented on these outputs. Once every 511 character times (plus a 16-character Word Sync Sequence when the receive channels are clocked by a common clock), the associated TXPERx signal will pulse HIGH for one transmit-character clock period to indicate a complete pass through the BIST sequence. These outputs also provide indication of a transmit Phase-Align Buffer underflow or overflow. When the transmit Phase-Align Buffers are enabled (TXCKSEL ≠ LOW, or TXCKSEL = LOW and TXRATE = HIGH), if an underflow or overflow condition is detected, TXPERx for the channel in error is asserted and remains asserted until either an atomic Word Sync Sequence is transmitted or $\overline{\text{TXRST}}$ is sampled LOW to re-center the transmit Phase-Align Buffers.
TXCTA[1:0] TXCTB[1:0] TXCTC[1:0] TXCTD[1:0]	LVTTL Input, synchronous, sampled by the selected TXCLKx↑ or REFCLK↑ [1]	**Transmit Control**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL, and are passed to the Encoder or Transmit Shifter. They identify how the associated TXDx[7:0] characters are interpreted. When the Encoder is bypassed, these inputs are interpreted as data bits. When the Encoder is enabled, these inputs determine if the TXDx[7:0] character is encoded as Data, a Special Character code, or replaced with other Special Character codes. See *Table 1* for details.
TXDA[7:0] TXDB[7:0] TXDC[7:0] TXDD[7:0]	LVTTL Input, synchronous, sampled by the selected TXCLKx↑ or REFCLK↑ [1]	**Transmit Data Inputs**. These inputs are captured on the rising edge of the transmit interface clock as selected by TXCKSEL and passed to the Encoder or Transmit Shifter. When the Encoder is enabled (TXMODE[1:0] ≠ LL), TXDx[7:0] specify the specific data or command character to be sent.
TXOPA TXOPB TXOPC TXOPD	LVTTL Input, synchronous, internal pull-up, sampled by the respective TXCLKx↑ or REFCLK↑ [1]	**Transmit Path Odd Parity**. When parity checking is enabled (PARCTL ≠ LOW), the parity captured at these inputs is XORed with the data on the associated TXDx bus to verify the integrity of the captured character.

Note:
1. When REFCLK is configured for half-rate operation (TXRATE = HIGH), these inputs are sampled (or the outputs change) relative to both the rising and falling edges of REFCLK.

Pin Descriptions (continued)

CYP15G0401DXA Quad HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
$\overline{\text{TXRST}}$	LVTTL Input, asynchronous, internal pull-up, sampled by TXCLKA↑ or REFCLK↑ [1]	**Transmit Clock Phase Reset**. Active LOW. When sampled LOW, the transmit Phase-Align Buffers are allowed to adjust their data-transfer timing (relative to the selected input clock) to allow clean transfer of data from the Input Register to the Encoder or Transmit Shifter. When $\overline{\text{TXRST}}$ is sampled deasserted (HIGH), the internal phase relationship between the associated TXCLKx and the internal character-rate clock is fixed and the device operates normally. When configured for half-rate REFCLK sampling of the transmit character stream (TXCKSEL = LOW and TXRATE = HIGH), assertion of $\overline{\text{TXRST}}$ is only used to clear Phase-Align buffer faults caused by highly asymmetric REFCLK periods or REFCLKs with excessive cycle-to-cycle jitter. During this alignment period, one or more characters may be added to or lost from all the associated transmit paths as the transmit Phase-Align Buffers are adjusted. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive rising edges of TXCLKA (or one REFCLK↑) to ensure the reset operation is initiated correctly on all channels. This input is ignored when both TXCKSEL and TXRATE are LOW. In all other configurations, TXRST should be asserted during device initialization to ensure proper operation of the Phase-Align and Elasticity Buffers.
SCSEL	LVTTL Input, synchronous, internal pull-down, sampled by TXCLKA↑ or REFCLK↑ [1]	**Special Character Select**. Used in some transmit modes along with TXCTx[1:0] to encode special characters or to initiate a Word Sync Sequence. When the transmit paths are configured for independent inputs clocks (TXCKSEL = MID), SCSEL is captured relative to TXCLKA↑.
Transmit Path Clock and Clock Control		
TXCKSEL	3-Level Select [2], static control input	**Transmit Clock Select**. Selects the clock source, used to write data into the transmit Input Register of the transmit channel(s). When LOW, all four Input Registers are clocked by REFCLK↑ [1]. When MID, TXCLKx↑ is used as the Input Register clock for TXDx[7:0] and TXCTx[1:0]. When HIGH, TXCLKA↑ is used to clock data into the Input Register of each channel.
TXCLKO±	LVTTL Output	**Transmit Clock Output**. This true and complement output clock is synthesized by the transmit PLL and operates synchronous to the internal transmit character clock. It operates at either the same frequency as REFCLK, or at twice the frequency of REFCLK (as selected by TXRATE). TXCLKO± is always equal to the transmit VCO bit-clock frequency ÷10. This output clock has no direct phase relationship to REFCLK or any recovered character clock.
TXRATE	LVTTL Input, static control input, internal pull-down	**Transmit PLL Clock Rate Select**. When TXRATE = HIGH, the Transmit PLL multiplies REFCLK by 20 to generate the serial bit-rate clock. When TXRATE = LOW, the transmit PLL multiples REFCLK by 10 to generate the serial bit-rate clock. See *Table 11* for a list of operating serial rates. When REFCLK is selected to clock the receive parallel interfaces (RXCKSEL = LOW), the TXRATE input also determines if the clocks on the RXCLKA± and RXCLKC± outputs are full or half-rate. When TXRATE = HIGH, these output clocks are half-rate clocks and follow the frequency and duty cycle of the REFCLK input. When TXRATE = LOW, these output clocks are full-rate clocks and follow the frequency and duty cycle of the REFCLK input.

Note:

2. 3-Level select inputs are used for static configuration. They are ternary (not binary) inputs that make use of non-standard logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC}. When not connected or allowed to float, a 3-Level select input will self-bias to the MID level.

Pin Descriptions (continued)

CYP15G0401DXA Quad HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
TXCLKA TXCLKB TXCLKC TXCLKD	LVTTL Clock Input, internal pull-down	**Transmit Path Input Clocks**. These clocks must be frequency-coherent to TXCLKO±, but may be offset in phase. The internal operating phase of each input clock (relative to REFLCK or TXCLKO±) is adjusted when TXRST = LOW and locked when TXRST = HIGH.
Transmit Path Mode Control		
TXMODE[1:0]	3-Level Select [2] static control inputs	**Transmit Operating Mode**. These inputs are interpreted to select one of nine operating modes of the transmit path. See *Table 3* for a list of operating modes.
Receive Path Data Signals		
RXDA[7:0] RXDB[7:0] RXDC[7:0] RXDD[7:0]	LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [1] input	**Parallel Data Output**. These outputs change following the rising edge of the selected receive interface clock.
RXSTA[2:0] RXSTB[2:0] RXSTC[2:0] RXSTD[2:0]	LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [1] input	**Parallel Status Output**. These outputs change following the rising edge of the selected receive interface clock. When the Decoder is bypassed, RXSTx[1:0] become the two low-order bits of the 10-bit received character, while RXSTx[2] = HIGH indicates the presence of a Comma character in the Output Register. When the Decoder is enabled (DECMODE = HIGH), RXST[1:0] provide status of the received signal. See *Table 21* for a list of Receive Character status.
RXOPA RXOPB RXOPC RXOPD	3-state, LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [1] input	**Receive Path Odd Parity**. When parity generation is enabled (PARCTL ≠ LOW), the parity output at these pins is valid for the data on the associated RXDx bus bits. When parity generation is disabled (PARCTL = LOW) these output drivers are disabled (High-Z).
Receive Path Clock and Clock Control		
RXRATE	LVTTL Input, static control input, internal pull-down	**Receive Clock Rate Select**. When LOW, the RXCLKx± recovered clock outputs are complementary clocks operating at the recovered character rate. Data for the associated receive channels should be latched on the rising edge of RXCLKx+ or falling edge of RXCLKx–. When HIGH, the RXCLKx± recovered clock outputs are complementary clocks operating at half the character rate. Data for the associated receive channels should be latched alternately on the rising edge of RXCLKx+ and RXCLKx–. When operated with REFCLK clocking of the received parallel data outputs (RXCKSEL = LOW), RXRATE must be LOW.
FRAMCHAR	3-Level Select [2], static control input	**Framing Character Select**. Used to select the character or portion of a character used for character framing of the received data streams. When MID, the Framer looks for both positive and negative disparity versions of the 8-bit Comma character. When HIGH, the Framer looks for both positive and negative disparity versions of the K28.5 character. The LOW selection is reserved for component test.
RFEN	LVTTL Input, asynchronous, internal pull-down	**Reframe Enable for all channels**. Active HIGH. When HIGH, the framers in all four channels are enabled to frame per the presently enabled framing mode and selected framing character.
RXMODE[1:0]	3-Level Select [2], static control inputs	**Receive Operating Mode**. These inputs are interpreted to select one of nine operating modes of the receive path. See *Table 15* for details.

Pin Descriptions (continued)

CYP15G0401DXA Quad HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
RXCLKA± RXCLKB± RXCLKC± RXCLKD±	3-state, LVTTL Output clock or static control input	**Receive Character Clock Output or Clock Select Input**. When the Receive Elasticity Buffers are disabled (RXCKSEL = MID), these true and complement clocks are the Receive interface clocks which are used to control timing of data output transfers. These clocks are output continuously at either the dual-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATE. When configured such that all output data paths are clocked by REFCLK instead of a recovered clock (RXCKSEL = LOW), the RXCLKA± and RXCLKC± output drivers present a buffered form of REFCLK, and RXCLKB+ and RXCLKD+ are static control inputs used to select the master channel for bonding and status control. RXCLKA± and RXCLKC± are buffered forms of REFCLK that are slightly different in phase. This phase difference allows the user to select the optimal setup/hold timing for their specific interface. When dual-channel bonding is enabled and a recovered clock is used to present data (RXCKSEL = HIGH), RXCLKA± drives the recovered clock from either receive channel A or receive channel B as selected by RXCLKB+, and RXCLKC± drives the recovered clock from either receive channel C or receive channel D as selected by RXCLKD+. When quad-channel bonding is enabled and a recovered clock is used to present data (RXCKSEL = HIGH), both RXCLKA± and RXCLKC± output the recovered clock from receive channel A, B, C, or D, as selected by RXCLKB+ and RXCLKD+.
RXCKSEL	3-Level Select [2], static control input	**Receive Clock Mode**. Selects the receive clock source used to transfer data to the Output Registers. When LOW, all four Output Registers are clocked by REFCLK. RXCLKB± and RXCLKD± outputs are disabled (High-Z), and RXCLKA± and RXCLKC± present buffered and delayed forms of REFCLK. This clocking mode is required for channel bonding across multiple devices. When MID, each RXCLKx± output follows the recovered clock for the respective channel, as selected by RXRATE. When HIGH, and channel bonding is enabled in dual-channel mode (RX modes 3 and 5), RXCLKA± outputs the recovered clock from either receive channel A or receive channel B as selected by RXCLKB+, and RXCLKC± outputs the recovered clock from either receive channel C or receive channel D as selected by RXCLKD+. These output clocks may operate at the character-rate or half the character-rate as selected by RXRATE. When HIGH and channel bonding is enabled in quad channel mode (RX modes 6 and 8), or if the receive channels are operated in independent mode (RX modes 0 and 2), RXCLKA± and RXCLKC± output the recovered clock from receive channel A, B, C, or D, as selected by RXCLKB+ and RXCLKD+. This output clock may operate at the character-rate or half the character-rate as selected by RXRATE.
DECMODE	3-Level Select [2], static control input	**Decoder Mode Select**. This input selects the behavior of the Decoder block. When LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. When MID, the Cypress decoder table for Special Code characters is used. When HIGH, the alternate decoder table for Special Code characters is used. See *Table 26* for a list of the Special Codes supported in both encoded modes.

Pin Descriptions (continued)

CYP15G0401DXA Quad HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
RFMODE	3-Level Select [2], static control input	**Reframe Mode Select**. Used to select the type of character framing used to adjust the character boundaries (based on detection of one or more framing characters in the received serial bit stream). This signal operates in conjunction with the presently enabled channel bonding mode, and the type of framing character selected. When LOW, the Low-Latency Framer is selected. This will frame on each occurrence of the selected framing character(s) in the received data stream. This mode of framing stretches the recovered clock for one or multiple cycles to align that clock with the recovered data. When MID, the Cypress-mode Multi-Byte parallel Framer is selected. This requires a pair of the selected framing character(s), on identical 10-bit boundaries, within a span of 50 bits, before the character boundaries are adjusted. The recovered character clock remains in the same phasing regardless of character offset. When HIGH, the alternate mode Multi-Byte parallel Framer is selected. This requires detection of the selected framing character(s) of the allowed disparities in the received serial bit stream, on identical 10-bit boundaries, on four directly adjacent characters. The recovered character clock remains in the same phasing regardless of character offset.
Device Control Signals		
PARCTL	3-Level Select [2], static control input	**Parity Check/Generate Control**. Used to control the different parity check and generate functions. When LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z). When MID, and the 8B/10B Encoder and Decoder are enabled (TXMODE[1] ≠ LOW, DECMODE ≠ LOW), TXDx[7:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] outputs and presented on RXOPx. When the Encoder and Decoder are disabled (TXMODE[1] = LOW, DECMODE = LOW), theTXDx[7:0] and TXCTx[1:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] and RXSTx[1:0] outputs and presented on RXOPx. When HIGH, parity checking and generation are enabled. The TXDx[7:0] and TXCTx[1:0] inputs are checked (along with TXOPx) for valid ODD parity, and ODD parity is generated for the RXDx[7:0] and RXSTx[2:0] outputs and presented on RXOPx.
SPDSEL	3-Level Select [2], static control input	**Serial Rate Select**. This input specifies the operating bit-rate range of both transmit and receive PLLs. LOW = 200–400 MBd, MID = 400–800 MBd, HIGH = 800–1500 MBd.
REFCLK±	Differential LVPECL or single-ended LVTTL Input Clock	**Reference Clock**. This clock input is used as the timing reference for the transmit and receive PLLs. This input clock may also be selected to clock the transmit and receive parallel interfaces. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLK input, and leave the alternate REFCLK input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs. When TXCKSEL = LOW, REFCLK is also used as the clock for the parallel transmit data (input) interface. When RXCKSEL = LOW, REFCLK is also used as the clock for the parallel receive data (output) interface.
$\overline{\text{TRSTZ}}$	LVTTL Input, internal pull-up	**Device Reset**. Active LOW. Initializes all state machines and counters in the device. When sampled LOW by the rising edge of REFLCK, this input resets the internal state machines and sets the Elasticity Buffer pointers to a nominal offset. When the reset is removed ($\overline{\text{TRSTZ}}$ sampled HIGH by REFCLK↑), the status and data outputs will become deterministic in less than 16 REFCLK cycles. The BISTLE, OELE, and RXLE latches are reset by $\overline{\text{TRSTZ}}$. If the Elasticity Buffer or the Phase-Align Buffer are used, $\overline{\text{TRSTZ}}$ should be applied after power up to initialize the internal pointers into these memory arrays.

Pin Descriptions (continued)

CYP15G0401DXA Quad HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
Analog I/O and Control		
OUTA1± OUTB1± OUTC1± OUTD1±	CML Differential Output	**Primary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules. These outputs must be AC-coupled for PECL-compatible connections.
OUTA2± OUTB2± OUTC2± OUTD2±	CML Differential Output	**Secondary Differential Serial Data Outputs**. These PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules. These outputs must be AC-coupled for PECL compatible connections.
INA1± INB1± INC1± IND1±	LVPECL Differential Input	**Primary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx1± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = HIGH.
INA2± INB2± INC2± IND2±	LVPECL Differential Input	**Secondary Differential Serial Data Inputs**. These inputs accept the serial data stream for deserialization and decoding. The INx2± serial streams are passed to the receiver Clock and Data Recovery (CDR) circuits to extract the data content when INSELx = LOW.
INSELA INSELB INSELC INSELD	LVTTL Input, asynchronous	**Receive Input Selector**. Determines which external serial bit stream is passed to the receiver Clock and Data Recovery circuit. When HIGH, the INx1± input is selected. When LOW, the INx2± input is selected.
SDASEL	3-Level Select [2], static configuration input	**Signal Detect Amplitude Level Select**. Allows selection of one of three predefined amplitude trip points for a valid signal indication, as listed in *Table 12*.
LPEN	LVTTL Input, asynchronous, internal pull-down	**All-Port Loop-Back Enable**. Active HIGH. When asserted (HIGH), the transmit serial data from each channel is internally routed to the associated receiver Clock and Data Recovery (CDR) circuit. All enabled serial drivers are forced to differential logic “1”. All serial data inputs are ignored.
OELE	LVTTL Input, asynchronous, internal pull-up	**Serial Driver Output Enable Latch Enable**. Active HIGH. When OELE = HIGH, the signals on the BOE[7:0] inputs directly control the OUTxy± differential drivers. When the BOE[x] input is HIGH, the associated OUTxy± differential driver is enabled. When the BOE[x] input is LOW, the associated OUTxy± differential driver is powered down. When OELE returns LOW, the last values present on BOE[7:0] are captured in the internal Output Enable Latch. The specific mapping of BOE[7:0] signals to transmit output enables is listed in *Table 10*. If the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable all outputs.
BISTLE	LVTTL Input, asynchronous, internal pull-up	**Transmit and Receive BIST Latch Enable**. Active HIGH. When BISTLE = HIGH, the signals on the BOE[7:0] inputs directly control the transmit and receive BIST enables. When the BOE[x] input is LOW, the associated transmit or receive channel is configured to generate or compare the BIST sequence. When the BOE[x] input is HIGH, the associated transmit or receive channel is configured for normal data transmission or reception. When BISTLE returns LOW, the last values present on BOE[7:0] are captured in the internal BIST Enable Latch. The specific mapping of BOE[7:0] signals to transmit and receive BIST enables is listed in *Table 10*. When the latch is closed, if the device is reset ($\overline{\text{TRSTZ}}$ is sampled LOW), the latch is reset to disable BIST on all transmit and receive channels.

Pin Descriptions (continued)

CYP15G0401DXA Quad HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
RXLE	LVTTL Input, asynchronous, internal pull-up	**Receive Channel Power-Control Latch Enable**. Active HIGH. When RXLE = HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the receive PLLs and analog circuitry. When the BOE[7:0] input is HIGH, the associated receive channel A through D PLL and analog circuitry are active. When the BOE[7:0] input is LOW, the associated receive channel A through D PLL and analog circuitry are powered down. When RXLE returns LOW, the last values present on BOE[7:0] are captured in the internal RX PLL Enable Latch. The specific mapping of BOE[7:0] signals to the associated receive channel enables is listed in *Table 10*. When the device is reset ($\overline{\text{TRSTZ}}$ = LOW), the latch is reset to disable all receive channels.
BOE[7:0]	LVTTL Input, asynchronous, internal pull-up	**BIST, Serial Output, and Receive Channel Enables**. These inputs are passed to and through the Output Enable Latch when OELE is HIGH, and captured in this latch when OELE returns LOW. These inputs are passed to and through the BIST Enable Latch when BISTLE is HIGH, and captured in this latch when BISTLE returns LOW. These inputs are passed to and through the Receive Channel Enable Latch when RXLE is HIGH, and captured in this latch when RXLE returns LOW.
$\overline{\text{LFIA}}$ $\overline{\text{LFIB}}$ $\overline{\text{LFIC}}$ LFID	LVTTL Output, synchronous to the selected RXCLKx↑ output or REFCLK↑ [1] input, asynchronous to Receive channel enable/disable	**Link Fault Indication Output**. Active LOW. $\overline{\text{LFIx}}$ is the logical OR of four internal conditions: 1. Received serial data frequency outside expected range 2. Analog amplitude below expected levels 3. Transition density lower than expected 4. Receive Channel disabled
Bonding Control		
BONDST[1:0]	Bidirectional Open Drain, internal pull-up	**Bonding Status**. These signals are only used when multiple devices are bonded together. They communicate the status of the present internal bonding and Elasticity Buffer management events to the slave devices. These outputs change at the same character rate as the receive output data buses, but are connected only to all the slave CYP15G0401DXA devices. When $\overline{\text{MASTER}}$ = LOW, these are output signals and present the Elasticity Buffer status from the selected receive channel of the device configured as the master. Receive master channel selection is performed using the RXCKB+ and RXCKD+ inputs. These status outputs indicate one of four possible conditions, on a synchronous basis, to the slave devices. These condition are: 00—Reserved 01—Add one K28.5 immediately following the next framing character received 10—Delete next framing character received 11—Normal data These outputs are driven only when the device is configured as a master, all four channels are bonded together, and the receive parallel interface is clocked by REFCLK↑.
$\overline{\text{MASTER}}$	LVTTL Input, static configuration input, internal pull-down	**Master Device Select**. When LOW, the present device is configured as the master, and BONDST[1:0] are outputs. When HIGH, the present device is configured as a slave, and BONDST[1:0] are inputs. $\overline{\text{MASTER}}$ is only interpreted when configured for quad channel bonding, and the receive parallel interface is clocked by REFCLK↑.

Pin Descriptions (continued)

CYP15G0401DXA Quad HOTLink II™ Transceiver

Name	I/O Characteristics	Signal Description
BOND_ALL	Bidirectional Open Drain, Internal pull-up	**All Channels Bonded Indicator**. Active HIGH, wired AND. After bonding resolution is completed and when HIGH, all receive channels have detected valid framing. This output is LOW during the bonding resolution process. This output is driven only when configured for four channel bonding, and the receive parallel interface is clocked by REFCLK↑.
$\overline{\text{BOND\_INH}}$	LVTTL Input, static configuration input, Internal pull-up	**Parallel Bond Inhibit**. Active LOW. When asserted (LOW), this signal inhibits the adjustment of character offsets in all receive channels if the Bonding Sequence has *not* been detected in all bonded channels. When HIGH, all channels that have detected the Bonding Sequence are allowed to align their Receive Elasticity Buffer pipelines. For any channels to bond, the selected master channel must be a member of the group. When multiple devices are used together, the $\overline{\text{BOND\_INH}}$ input on all parts must be configured the same.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select**. Used to control access to the JTAG Test Modes. If maintained high for $\geq$5 TCLK cycles, the JTAG test controller is reset. The TAP controller is also reset automatically upon application of power to the device.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock**
TDO	3-State LVTTL Output	**Test Data Out**. JTAG data output buffer which is High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In**. JTAG data input port.
Power		
V_{CC}		**+3.3V Power**
GND		**Signal and Power Ground for all internal circuits**

CYP15G0401DXA HOTLink II Operation

The CYP15G0401DXA is a highly configurable device designed to support reliable transfer of large quantities of data, using high-speed serial links, from one or multiple sources to one or multiple destinations. This device supports four single-byte or single-character channels that may be combined to support transfer of wider buses.

CYP15G0401DXA Transmit Data Path

Operating Modes

The transmit path of the CYP15G0401DXA supports four character-wide data paths. These data paths are used in multiple operating modes as controlled by the TXMODE[1:0] inputs.

Input Register

Within these operating modes, the bits in the Input Register for each channel support different bit assignments, based on if the character is unencoded, encoded with two control bits, or encoded with three control bits. These assignments are shown in *Table 1*.

Table 1. Input Register Bit Assignments[3]

Signal Name	Unencoded	Encoded	
		2-bit Control	3-bit Control
TXDx[0] (LSB)	DINx[0]	TXDx[0]	TXDx[0]
TXDx[1]	DINx[1]	TXDx[1]	TXDx[1]
TXDx[2]	DINx[2]	TXDx[2]	TXDx[2]
TXDx[3]	DINx[3]	TXDx[3]	TXDx[3]
TXDx[4]	DINx[4]	TXDx[4]	TXDx[4]
TXDx[5]	DINx[5]	TXDx[5]	TXDx[5]
TXDx[6]	DINx[6]	TXDx[6]	TXDx[6]
TXDx[7]	DINx[7]	TXDx[7]	TXDx[7]
TXCTx[0]	DINx[8]	TXCTx[0]	TXCTx[0]
TXCTx[1] (MSB)	DINx[9]	TXCTx[1]	TXCTx[1]
SCSEL	N/A	N/A	SCSEL

Note:
3. The TXOPx inputs are also captured in the associated Input Register, but their interpretation is under the separate control of PARCTL.

Each Input Register captures a minimum of eight data bits and two control bits on each input clock cycle. When the Encoder is bypassed, the control bits are part of the pre-encoded 10-bit character.

When the Encoder is enabled (TXMODE[1] ≠ LOW), the TXCTx[1:0] bits are interpreted along with the associated TXDx[7:0] character to generate the specific 10-bit transmission character. When TXMODE[0] ≠ HIGH, an additional special character select (SCSEL) input is also captured and interpreted. This SCSEL input is used to modify the encoding of the associated characters. When the transmit Input Registers are clocked by a common clock (TXCLKA↑ or REFCLK↑), this SCSEL input can be changed on a clock-by-clock basis and affects all four channels.

When operated with a separate input clock on each transmit channel, this SCSEL input is sampled synchronous to TXCLKA↑. While the value on SCSEL still affects all channels, it is interpreted when the character containing it is read from the transmit Phase-Align Buffer (where all four paths are internally clocked synchronously).

Phase-Align Buffer

Data from the Input Registers are passed either to the Encoder or to the associated Phase-Align Buffer. When the transmit paths are operated synchronous to REFCLK↑ (TXCKSEL = LOW and TXRATE = LOW), the Phase-Align Buffers are bypassed and data is passed directly to the Parity Check and Encoder blocks to reduce latency.

When an Input-Register clock with an uncontrolled phase relationship to REFCLK is selected (TXCKSEL ≠ LOW) or if data is captured on both edges of REFCLK (TXRATE = HIGH), the Phase-Align Buffers are enabled. These buffers are used to absorb clock phase differences between the presently selected input clock and the internal character clock.

Initialization of these Phase-Align Buffers takes place when the $\overline{\text{TXRST}}$ input is sampled LOW by TXCLKA↑. When $\overline{\text{TXRST}}$ is returned HIGH, the present input clock phase relative to REFCLK is set. $\overline{\text{TXRST}}$ is an asynchronous input, but is sampled internally to synchronize it to the internal transmit path state machines. $\overline{\text{TXRST}}$ must be sampled LOW by a minimum of two consecutive TXCLKA↑ clocks to ensure the reset operation is initiated correctly on all channels.

Once set, the input clocks are allowed to skew in time up to half a character period in either direction relative to REFCLK; i.e., ±180°. This time shift allows the delay paths of the character clocks (relative to REFCLK) to change due to operating voltage and temperature, while not affecting the design operation.

If the phase offset, between the initialized location of the input clock and REFCLK↑, exceeds the skew handling capabilities of the Phase-Align Buffer, an error is reported on the associated TXPERx output. This output indicates a continuous error until the Phase-Align Buffer is reset. While the error remains active, the transmitter for the associated channel will output a continuous C0.7 character to indicate to the remote receiver that an error condition is present in the link.

In specific transmit modes it is also possible to reset the Phase-Align Buffers individually and with minimal disruption of the serial data stream. When the transmit interface is configured for generation of atomic Word Sync Sequences (TXMODE[1] = MID) and a Phase-Align Buffer error is present, the transmission of a Word Sync Sequence will re-center the Phase-Align Buffer and clear the error condition.

> **NOTE:** One or more K28.5 characters may be added or lost from the data stream during this reset operation. When used with non-Cypress devices that require a complete 16-character Word Sync Sequence for proper Receive Elasticity Buffer alignment, it is recommend that the sequence be followed by a second Word Sync Sequence to ensure proper operation.

Parity Support

In addition to the ten data and control bits that are captured at each transmit Input Register, a TXOPx input is also available on each channel. This allows the CYP15G0401DXA to support ODD parity checking for each channel. Parity checking is available for all operating modes (including Encoder Bypass). The specific mode of parity checking is controlled by the PARCTL input, and operates per *Table 2*.

Table 2. Input Register Bits Checked for Parity[4]

Signal Name	Transmit Parity Check Mode (PARCTL)			
	LOW	MID		HIGH
		TXMODE[1] = LOW	TXMODE[1] ≠ LOW	
TXDx[0]		X[5]	X	X
TXDx[1]		X	X	X
TXDx[2]		X	X	X
TXDx[3]		X	X	X
TXDx[4]		X	X	X
TXDx[5]		X	X	X
TXDx[6]		X	X	X
TXDx[7]		X	X	X
TXCTx[0]		X		X
TXCTx[1]		X		X
TXOPx		X	X	X

Notes:
4. Transmit path parity errors are reported on the associated TXPERx output.
5. Bits marked as X are XORed together. Result must be a logic-1 for parity to be valid.

When PARCTL is MID (open) and the Encoders are enabled (TXMODE[1] ≠ LOW), only the TXD[7:0] data bits are checked for ODD parity along with the associated TXOPx bit. When PARCTL = HIGH with the Encoder enabled (or MID with the Encoder bypassed), the TXDx[7:0] and TXCTx[1:0] inputs are checked for ODD parity along with the associated TXOPx bit. When PARCTL = LOW, parity checking is disabled.

When parity checking and the Encoder are both enabled (TXMODE[1] ≠ LOW), the detection of a parity error causes a C0.7 character of proper disparity to be passed to the Transmit Shifter. When the Encoder is bypassed (TXMODE[1] = LOW), detection of a parity error causes a positive disparity version of a C0.7 transmission character to be passed to the Transmit Shifter.

Encoder

The character, received from the Input Register or Phase-Align Buffer and Parity Check Logic, is then passed to the Encoder logic. This block interprets each character and any associated control bits, and outputs a 10-bit transmission character.

Depending on the configured operating mode, the generated transmission character may be

- the 10-bit pre-encoded character accepted in the Input Register
- the 10-bit equivalent of the 8-bit Data character accepted in the Input Register
- the 10-bit equivalent of the 8-bit Special Character code accepted in the Input Register
- the 10-bit equivalent of the C0.7 SVS character if parity checking was enabled and a parity error was detected
- the 10-bit equivalent of the C0.7 SVS character if a Phase-Align Buffer overflow or underflow error is present
- a character that is part of the 511-character BIST sequence
- a K28.5 character generated as an individual character or as part of the 16-character Word Sync Sequence.

The selection of the specific characters generated are controlled by the TXMODE[1:0], SCSEL, TXCTx[1:0], and TXDx[7:0] inputs for each character.

Data Encoding

Raw data, as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee

- a minimum transition density (to allow the serial receive PLL to extract a clock from the data stream)
- a DC-balance in the signaling (to prevent baseline wander)
- run-length limits in the serial data (to limit the bandwidth requirements of the serial link.)
- the remote receiver a way of determining the correct character boundaries (framing).

When the Encoder is enabled (TXMODE[1] ≠ LOW), the characters to be transmitted are converted from Data or Special Character codes to 10-bit transmission characters (as selected by their respective TXCTx[1:0] and SCSEL inputs), using an integrated 8B/10B Encoder. When directed to encode the character as a Special Character code, it is encoded using the Special Character encoding rules listed in *Table 26*. When directed to encode the character as a Data character, it is encoded using the Data Character encoding rules in *Table 25*.

The 8B/10B Encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 (Fibre Channel), IEEE 802.3z (Gigabit Ethernet), the IBM® ESCON® and FICON™ channels, Digital Video Broadcast (DVB-ASI), and ATM Forum standards for data transport.

Many of the Special Character codes listed in *Table 26* may be generated by more than one input character. The CYP15G0401DXA is designed to support two independent (but non-overlapping) Special Character code tables. This allows the CYP15G0401DXA to operate in mixed environments with other Cypress HOTLink devices using the enhanced Cypress command code set, and the reduced command sets of other non-Cypress devices. Even when used in an environment that normally uses non-Cypress Special Character codes, the selective use of Cypress command codes can permit operation where running disparity and error handling must be managed.

Following conversion of each input character from 8 bits to a 10-bit transmission character, it is passed to the Transmit Shifter and is shifted out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

Transmit Modes

The operating mode of the transmit path is set through the TXMODE[1:0] inputs. These 3-level select inputs allow one of nine transmit modes to be selected. Within each of these operating modes, the actual characters generated by the Encoder logic block are controlled by TXMODE[1:0] and other control signals. The transmit modes are listed in *Table 3*.

The encoded modes (TX Modes 3 through 8) support multiple encoding tables. These encoding tables vary by the specific combinations of SCSEL, TXCTx[1], and TXCTx[0] that are used to control the generation of data and control characters. These multiple encoding forms allow maximum flexibility in interfacing to legacy applications, while also supporting numerous extensions in capabilities.

Table 3. Transmit Operating Modes

TX Mode		Operating Mode		
Mode Number	TXMODE [1:0]	Word Sync Sequence Support	SCSEL Control	TXCTx Function
0	LL	None	None	Encoder Bypass
1	LM	None	None	Reserved for test
2	LH	None	None	Reserved for test
3	ML	Atomic	Special Character	Encoder Control
4	MM	Atomic	Word Sync	Encoder Control
5	MH	Atomic	None	Encoder Control
6	HL	Interruptible	Special Character	Encoder Control
7	HM	Interruptible	Word Sync	Encoder Control
8	HH	Interruptible	None	Encoder Control

TX Mode 0—Encoder Bypass

When the Encoder is bypassed, the character captured from the TXDx[7:0] and TXCTx[1:0] inputs is passed directly to the Transmit Shifter without modification. If parity checking is enabled (PARCTL ≠ LOW) and a parity error is detected, the 10-bit character is replaced with the 1001111000 pattern (+C0.7 character).

With the Encoder bypassed, the TXCTx[1:0] inputs are considered part of the data character and do not perform a control function that would otherwise modify the interpretation of the TXDx[7:0] bits. The bit usage and mapping of these control bits when the Encoder is bypassed is shown in *Table 4*.

Table 4. Encoder Bypass Mode (TXMODE[1:0] = LL)

Signal Name	Bus Weight	10Bit Name
TXDx[0] (LSB)	2^0	a[6]
TXDx[1]	2^1	b
TXDx[2]	2^2	c
TXDx[3]	2^3	d
TXDx[4]	2^4	e
TXDx[5]	2^5	i
TXDx[6]	2^6	f
TXDx[7]	2^7	g
TXCTx[0]	2^8	h
TXCTx[1] (MSB)	2^9	j

Note:
6. LSB is shifted out first.

In Encoder Bypass mode the SCSEL input is ignored. All clocking modes interpret the data the same, with no internal linking between channels.

TX Modes 1 and 2—Factory Test Modes

These modes enable specific factory test configurations. They are not considered normal operating modes of the device. Entry or configuration of the device into these modes will not damage the device

TX Mode 3— Word Sync and SCSEL Control of Special Codes

When configured in TX Mode 3, the SCSEL input is captured along with the associated TXCTx[1:0] data control inputs. These bits combine to control the interpretation of the TXDx[7:0] bits and the characters generated by them. These bits are interpreted as listed in *Table 5*.

Table 5. TX Modes 3 and 6 Encoding

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
1	0	1	Special character code
X	1	1	16-character Word Sync Sequence

When TXCKSEL = MID, all transmit channels capture data into their Input Registers using independent TXCLKx clocks. The SCSEL input is sampled only by TXCLKA↑. When the character (accepted in the Channel-A Input Register) has passed through the Phase-Align Buffer and any selected parity validation, the level captured on SCSEL is passed to the Encoder of the remaining channels during this same cycle.

To avoid the possible ambiguities that may arise due to the uncontrolled arrival of SCSEL relative to the characters in the alternate channels, SCSEL is often used as static control input.

Word Sync Sequence

When TXCTx[1:0] = 11, a 16-character sequence of K28.5 characters, known as a Word Sync Sequence, is generated on the associated channel. This sequence of K28.5 characters may start with either a positive or negative disparity K28.5 (as determined by the current running disparity and the 8B/10B coding rules). The disparity of the second and third K28.5 characters in this sequence are reversed from what normal 8B/10B coding rules would generate. The remaining K28.5 characters in the sequence follow all 8B/10B coding rules. The disparity of the generated K28.5 characters in this sequence follow a pattern of either ++−−+−+−+−+−+−+− or −−++−+−+−+−+−+−+.

When TXMODE[1] = MID (open, TX modes 3, 4, and 5), the generation of this character sequence is an atomic (non-interruptible) operation. Once it has been successfully started, it cannot be stopped until all 16 characters have been generated. The content of the associated Input Registers is ignored for the duration of this 16-character sequence. At the end of this sequence, if the TXCTx[1:0] = 11 condition is sampled again, the sequence restarts and remains uninterruptible for the following 15 character clocks.

If parity checking is enabled, the character used to start the Word Sync Sequence must also have correct ODD parity. Once the sequence is started, parity is not checked on the following 15 characters in the Word Sync Sequence.

When TXMODE[1] = HIGH (TX modes 6, 7, and 8), the generation of the Word Sync Sequence becomes an interruptible

operation. In TX Mode 6, this sequence is started as soon as the TXCTx[1:0] = 11 condition is detected on a channel. In order for the sequence to continue on that channel, the TXCTx[1:0] inputs must be sampled as 00 for the remaining 15 characters of the sequence.

If at any time a sample period exists where TXCTx[1:0] ≠ 00, the Word Sync Sequence is terminated, and a character representing the associated data and control bits is generated by the Encoder. This resets the Word Sync Sequence state machine such that it will start at the beginning of the sequence at the next occurrence of TXCTx[1:0] = 11.

When parity checking is enabled and TXMODE[1] = HIGH, all characters (including those in the middle of a Word Sync Sequence) must have correct parity. The detection of a character with incorrect parity during a Word Sync Sequence will interrupt that sequence and force generation of a C0.7 SVS character. Any interruption of the Word Sync Sequence causes the sequence to terminate.

When TXCKSEL = LOW, the Input Registers for all four transmit channels are clocked by REFCLK[1]. When TXCKSEL = HIGH, the Input Registers for all four transmit channels are clocked with TXCLKA↑. In these clock modes all four sets of TXCTx[1:0] inputs operate synchronous to the SCSEL input.

NOTE: When operated in any configuration where receive channels are bonded together, TXCKSEL must be either LOW or HIGH (not MID) to ensure that associated characters are transmitted in the same character cycle.

TX Mode 4—Atomic Word Sync and SCSEL Control of Word Sync Sequence Generation

When configured in TX Mode 4, the SCSEL input is captured along with the associated TXCTx[1:0] data control inputs. These bits combine to control the interpretation of the TXDx[7:0] bits and the characters generated by them. These bits are interpreted as listed in *Table 6*.

Table 6. TX Modes 4 and 7 Encoding

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	X	0	Encoded data character
0	0	1	K28.5 fill character
0	1	1	Special character code
1	X	1	16-character Word Sync Sequence

When TXCKSEL = MID, all transmit channels operate independently. The SCSEL input is sampled only by TXCKA↑. When the character accepted in the Channel-A Input Register has passed any selected validation and is ready to be passed to the Encoder, the level captured on SCSEL is passed to the Encoders of the remaining channels during this same cycle.

Changing the state of SCSEL will change the relationship of the characters to other channels. SCSEL should either be used as a static configuration input, or changed only when the state of TXCTx[1:0] on the alternate channels are such that SCSEL is ignored during the change.

TX Mode 4 also supports an Word Sync Sequence. Unlike TX Mode 3, this sequence starts when SCSEL and TXCTx[0] are both high. With the exception of the combination of control bits used to initiate the sequence, the generation and operation of this Word Sync Sequence is the same as for TX Mode 3.

TX Mode 5—Atomic Word Sync generation without SCSEL.

When configured in TX Mode 5, the SCSEL signal is not used. In addition to the standard character encodings, two additional encoding mappings are controlled by the Channel Bonding selection made through the RXMODE[1:0] inputs.

For non-bonded operation, the TXCTx[1:0] inputs for each channel control the characters generated by that channel. The specific characters generated by these bits are listed in *Table 7*.

Table 7. TX Modes 5 and 8 Encoding, Non-Bonded

SCSEL	TXCTx[1]	TXCTx[0]	Characters Generated
X	0	0	Encoded data character
X	0	1	K28.5 fill character
X	1	0	Special character code
X	1	1	16-character Word Sync Sequence

TX Mode 5 also has the capability of generating an atomic Word Sync Sequence. For the sequence to be started, the TXCTx[1:0] inputs must both be sampled HIGH. The generation and operation of this Word Sync Sequence is the same as TX Mode 3.

Two additional encoding maps are provided for use when receive channel bonding is enabled. When dual-channel bonding is enabled (RXMODE[1] = MID), the CYP15G0401DXA is configured such that channels A and B are bonded together to form a two-character-wide path, and channels C and D are bonded together to form a second two-character-wide path.

When operated in this two-channel bonded mode, the TXCTA[0] and TXCTB[0] inputs control the interpretation of the data on both the A and B channels, while the TXCTC[0] and TXCTD[0] inputs control the interpretation of the data on both the C and D channels. The characters on each half of these bonded channels are controlled by the associated TXCTx[1] bit. The specific characters generated by these control bit combinations are listed in *Table 8*.

Note especially that any time TXCTB[0] is sampled HIGH, both channels A and B start generating an atomic Word Sync Sequence, regardless of the state of any of the other bits in the A or B Input Registers. In a similar fashion, anytime TXCTD[0] is sampled HIGH, both the C and D channels start generation of an atomic Word Sync Sequence.

When RXMODE[1] = HIGH, the CYP15G0401DXA is configured for quad-channel bonding, such that channels A, B, C, and D are bonded together to form a four-character-wide path. When operated in this mode, the TXCTA[0] and TXCTB[0] inputs control the interpretation of the data on all four channels. The characters generated on these bonded channels are controlled by the associated TXCTx[1] bit. The specific characters generated by these bits are listed in *Table 9*.

Unlike dual-channel bonded modes, when all four channels are bonded together, the TXCTC[0] and TXCTD[0] inputs are ignored.

Table 8. TX Modes 5 and 8, Dual-Channel Bonded

SCSEL	TXCTA[1]	TXCTA[0]	TXCTB[1]	TXCTB[0]	TXCTC[1]	TXCTC[0]	TXCTD[1]	TXCTD[0]	Characters Generated
X	0	0	X	0	X	X	X	X	Encoded data character on channel A
X	0	1	X	0	X	X	X	X	K28.5 fill character on channel A
X	1	0	X	0	X	X	X	X	Special character code on channel A
X	1	1	X	0	X	X	X	X	16-character word sync on channel A
X	X	0	0	0	X	X	X	X	Encoded data character on channel B
X	X	1	0	0	X	X	X	X	K28.5 fill character on channel B
X	X	0	1	0	X	X	X	X	Special character code on channel B
X	X	1	1	0	X	X	X	X	16-character word sync on channel B
X	X	X	X	1	X	X	X	X	16-character word sync on channels A and B
X	X	X	X	X	0	0	X	0	Encoded data character on channel C
X	X	X	X	X	0	1	X	0	K28.5 fill character on channel C
X	X	X	X	X	1	0	X	0	Special character code on channel C
X	X	X	X	X	1	1	X	0	16-character word sync on channel C
X	X	X	X	X	X	0	0	0	Encoded data character on channel D
X	X	X	X	X	X	1	0	0	K28.5 fill character on channel D
X	X	X	X	X	X	0	1	0	Special character code on channel D
X	X	X	X	X	X	1	1	0	16-character word sync on channel D
X	X	X	X	X	X	X	X	1	16-character word sync on channels C and D

Table 9. TX Modes 5 and 8, Quad-Channel Bonded

SCSEL	TXCTA[1]	TXCTA[0]	TXCTB[1]	TXCTB[0]	TXCTC[1]	TXCTC[0]	TXCTD[1]	TXCTD[0]	Characters Generated
X	0	0	X	0	X	X	X	X	Encoded data character on channel A
X	0	1	X	0	X	X	X	X	K28.5 fill character on channel A
X	1	0	X	0	X	X	X	X	Special character code on channel A
X	1	1	X	0	X	X	X	X	16-character word sync on channel A
X	X	0	0	0	X	X	X	X	Encoded data character on channel B
X	X	1	0	0	X	X	X	X	K28.5 fill character on channel B
X	X	0	1	0	X	X	X	X	Special character code on channel B
X	X	1	1	0	X	X	X	X	16-character word sync on channel B
X	X	0	X	0	0	X	X	X	Encoded data character on channel C
X	X	1	X	0	0	X	X	X	K28.5 fill character on channel C
X	X	0	X	0	1	X	X	X	Special character code on channel C
X	X	1	X	0	1	X	X	X	16-character word sync on channel C
X	X	0	X	0	X	X	0	X	Encoded data character on channel D
X	X	1	X	0	X	X	0	X	K28.5 fill character on channel D
X	X	0	X	0	X	X	1	X	Special character code on channel D
X	X	1	X	0	X	X	1	X	16-character word sync on channel D
X	X	X	X	1	X	X	X	X	16-character word sync on channels A, B, C, and D

Transmit BIST

Each transmit channel contains an internal pattern generator that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in *Table 10* (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to identical LFSR in the attached Receiver(s).

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator in the associated transmit channel (or the BIST checker in the associated receive channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH to open the latch. A device reset ($\overline{\text{TRSTZ}}$ sampled LOW), presets the BIST Enable Latch to disable BIST on all channels.

All data and data-control information present at the associated TXDx[7:0] and TXCTx[1:0] inputs are ignored when BIST is active on that channel. If the receive channels are configured for common clock operation (RXCKSEL ≠ MID) each pass is preceded by a 16-character Word Sync Sequence to allow Elasticity Buffer alignment and management of clock-frequency variations.

Serial Output Drivers

The serial interface Output Drivers use high-performance differential CML (Current Mode Logic) to provide source-matched drivers for the transmission lines. These Serial Drivers accept data from the Transmit Shifters. These outputs have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

When configured for local loopback (LPEN = HIGH), all enabled Serial Drivers are configured to drive a static differential logic-1.

Each Serial Driver can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the OELE latch-enable signal. When OELE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Serial Output Enable Latch to control the Serial Driver. The BOE[7:0] input associated with a specific OUTxy± driver is listed in *Table 10*.

When OELE is HIGH and BOE[x] is HIGH, the associated Serial Driver is enabled. When OELE is HIGH and BOE[x] is LOW, the associated Serial Driver is disabled and internally powered down. If both Serial Drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch, and remain there until OELE returns HIGH to enable the latch. A device reset ($\overline{\text{TRSTZ}}$ sampled LOW) clears this latch and disables all Serial Drivers.

NOTE: When a disabled transmit channel (i.e., both outputs disabled) is re-enabled, the data on the Serial Drivers may not meet all timing specifications for up to 10 ms.

Table 10. Output Enable, BIST, and Receive Channel Enable Signal Map

BOE Input	Output Controlled (OELE)	BIST Channel Enable (BISTLE)	Receive PLL Channel Enable (RXLE)
BOE[7]	OUTD2±	Transmit D	X
BOE[6]	OUTD1±	Receive D	Receive D
BOE[5]	OUTC2±	Transmit C	X
BOE[4]	OUTC1±	Receive C	Receive C
BOE[3]	OUTB2±	Transmit B	X
BOE[2]	OUTB1±	Receive B	Receive B
BOE[1]	OUTA2±	Transmit A	X
BOE[0]	OUTA1±	Receive A	Receive A

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the REFCLK input, and multiples that clock by 10 or 20 (as selected by TXRATE) to generate a bit-rate clock for use by the Transmit Shifter. It also provides a character-rate clock used by the transmit paths.

This clock multiplier PLL can accept a REFCLK input between 20 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYP15G0401DXA clock multiplier (controlled by TXRATE) and by the level on the SPDSEL input.

SPDSEL is a 3-level select[2] (ternary) input that selects one of three operating ranges for the serial data outputs and inputs. The operating serial signaling-rate and allowable range of REFCLK frequencies are listed in *Table 11*.

Table 11. Operating Speed Settings

SPDSEL	TXRATE	REFCLK Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	reserved	200–400
	0	20–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The REFCLK± input is a differential input with each input internally biased to 1.4V. If the REFCLK+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point.

When both the REFCLK+ and REFCLK– inputs are connected, the clock source must be a differential clock. This can be either a differential LVPECL clock that is DC- or AC-coupled, or a differential LVTTL or LVCMOS clock.

By connecting the REFCLK– input to an external voltage source or resistive voltage divider, it is possible to adjust the reference point of the REFCLK+ input for alternate logic levels. When doing so it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

CYP15G0401DXA Receive Data Path

Serial Line Receivers

Two differential Line Receivers, INx1± and INx2±, are available on each channel for accepting serial data streams. The active Serial Line Receiver on a channel is selected using the associated INSELx input. The Serial Line Receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL family, not limited to 100K PECL) or AC-coupled to +5V powered optical modules. The common -mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

The local loopback input (LPEN) allows the serial transmit data to be routed internally back to the Clock and Data Recovery circuit associated with each channel. When configured for local loopback, all transmit Serial Driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers.

Signal Detect/Link Fault

Each selected Line Receiver (i.e., that routed to the clock and data recovery PLL) is simultaneously monitored for

- analog amplitude
- transition density
- Range Controls report the received data stream inside normal frequency range (± 200 ppm)
- receive channel enabled.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the $\overline{LFIx}$ (Link Fault Indicator) output associated with each receive channel, which changes synchronous to the selected receive interface clock.

Table 12. Analog Amplitude Detect Valid Signal Levels

SDASEL	Typical signal with peak amplitudes above
LOW	140 mV p-p differential
MID (Open)	280 mV p-p differential
HIGH	420 mV p-p differential

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable. This allows operation with highly attenuated signals, or in high-noise environments. This adjustment is made through the SDASEL signal, a 3-level select[2] input, which sets the trip point for the detection of a valid signal at one of three levels, as listed in *Table 12*. This control input affects the analog monitors for all receive channels.

The Analog Signal Detect Monitors are active for the Line Receiver selected by the associated INSELx input. When the channel is configured for local loopback (LPEN = HIGH), no line receivers are selected, and the $\overline{LFIx}$ output for each channel reports only the receive VCO frequency out-of-range and transition density status of the associated transmit signal. When local loopback is active, the Analog Signal Detect Monitors are disabled.

Transition Density

The Transition Detection logic checks for the absence of any transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received on a channel, the Transition Detection logic for that channel will assert $\overline{LFIx}$. The $\overline{LFIx}$ output remains asserted until at least one transition is detected in each of three adjacent received characters.

Range Controls

The receive-VCO Range-Control Monitor tracks the frequency of the received signal relative to REFCLK. It also determines if the receive Clock/Data Recovery circuits should align the receive-VCO clock to the data stream or to the local REFCLK input. This prevents the receive VCO from tracking an out-of-specification received signal.

When the Range-Control Monitor for a channel indicates that the signaling rate is within specification, the phase detector in the receive PLL is configured to track the transitions in the received data stream. In this mode the $\overline{LFIx}$ output for the associated channel is HIGH, unless one of the other status monitors indicates that the received signal is out of specification. If the Range-Control Monitor indicates that the received data stream signaling-rate is out of specification, the phase detector is configured to track the local REFCLK input, and the associated $\overline{LFIx}$ output is asserted LOW.

The specific trip points for this compare function are listed in *Table 13*. Because the compare function operates with two asynchronous clocks, there is a small uncertainty in the measurement. The switch points are asymmetric to provide hysteresis to the operation.

Table 13. Receive Signaling Rate Range Control criteria

Current RX PLL Tracking Source	Frequency Difference Between Transmit Character Clock & RX VCO	Next RX PLL Tracking Source
Selected data stream ($\overline{LFIx}$ = HIGH)	<1708 ppm	Data Stream
	1708–1953 ppm	Indeterminate
	>1953 ppm	REFCLK
REFCLK ($\overline{LFIx}$ = LOW)	<488 ppm	Data Stream
	488–732 ppm	Indeterminate
	>732 ppm	REFCLK

Receive Channel Enabled

The CYP15G0401DXA contains four receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the BOE[7:0] inputs, as controlled by the RXLE latch-enable signal. When RXLE is HIGH, the signals present on the BOE[7:0] inputs are passed through the Receive Channel Enable Latch to control the PLLs and logic of the associated receive channel. The BOE[7:0] input associated with a specific receive channel is listed in *Table 10*.

When RXLE is HIGH and BOE[x] is HIGH, the associated receive channel is enabled to receive and decode a serial stream. When RXLE is HIGH and BOE[x] is LOW, the associ-

ated receive channel is disabled and powered down. If a single channel of a bonded-pair or bonded-quad is disabled, the other receive channels may not bond correctly. If the disabled channel is selected as the master channel for insert/delete or recovered clock select, these functions will not work correctly. Any disabled channel indicates an asserted LFIx output. When RXLE returns LOW, the values present on the BOE[7:0] inputs are latched in the Receive Channel Enable Latch, and remain there until RXLE returns HIGH to opened the latch again.

NOTE: When a disabled receive channel is re-enabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 10 ms.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate Clock/Data Recovery (CDR) block within each receive channel. The clock extraction function is performed by embedded phase-locked loops (PLLs) that track the frequency of the transitions in the incoming bit streams and align the phase of their internal bit-rate clocks to the transitions in the selected serial data streams.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) reference clock from the REFCLK input. This REFCLK input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency. (rather than a harmonic of the bit-rate)
- to reduce PLL acquisition time
- and to limit unlocked frequency excursions of the CDR VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR will attempt to recover a bit stream from it. If the frequency of the recovered data stream is outside the limits set by the Range Control Monitors, the PLL will track REFCLK instead of the data stream. When the frequency of the selected data stream returns to a valid frequency, the CDR PLL tracks the received data stream. The frequency of REFCLK is required to be within ±200 ppm of the frequency of the clock that drives the REFCLK input of the *remote* transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the $\overline{\text{LFIx}}$ output can be used to select an alternate data stream. When an LFIx indication is detected, external logic can toggle selection of the associated INx1± and INx2± inputs through the associated INSELx input. When a port switch takes place, it is necessary for the receive PLL for that channel to reacquire the new serial stream and frame to the incoming character boundaries. If channel bonding is also enabled, a channel alignment event is also required before the output data may be considered usable.

Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for one or more Comma or K28.5 characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

Framing Character

The CYP15G0401DXA allows selection of either of two combinations of framing characters to support requirements of different interfaces. The selection of the framing character is made through the FRAMCHAR input.

The specific bit combinations of these framing characters are listed in *Table 14*. When the specific bit combination of the selected framing character is detected by the Framer, the boundaries of the characters present in the received data stream are known.

Table 14. Framing Character Selector

FRAMCHAR	Bits detected in Framer	
	Character Name	Bits Detected
MID (Open)	Comma+ or Comma–	00111110XX [7] or 11000001XX
HIGH	–K28.5 or +K28.5	0011111010 or 1100000101

Note:

7. The standard definition of a Comma contains only seven bits. However, since all valid Comma characters within the 8B/10B character set also have the 8th bit as an inversion of the 7th bit, the compare pattern is extended to a full eight bits to reduce the possibility of a framing error.

Framer

The Framer on each channel operates in one of three different modes, as selected by the RFMODE input. In addition, the Framer itself may be enabled or disabled through the RFEN input. When RFEN = LOW, the framers in all four receive paths are disabled, and no combination of bits in a received data stream will alter the character boundaries. When RFEN = HIGH, the Framer selected by RFMODE is enabled on all four channels.

When RFMODE = LOW, the Low-Latency Framer is selected. This Framer operates by stretching the recovered character clock until it aligns with the received character boundaries. In this mode the Framer starts its alignment process on the first detection of the selected framing character. To reduce the impact on external circuits that make use of a recovered clock, the clock period is not stretched by more than two bit-periods in any one clock cycle. When operated with a character-rate output clock (RXRATE = LOW), the output of properly framed characters may be delayed by up to nine character-clock cycles from the detection of the selected framing character. When operated with a half-character-rate output clock (RXRATE = HIGH), the output of properly framed characters may be delayed by up to 14 character-clock cycles from the detection of the selected framing character.

NOTE: When Receive BIST is enabled on a channel, the Low-Latency Framer must not be enabled. The BIST sequence contains an aliased K28.5 framing character, which would cause the Receiver to update its character boundaries incorrectly.

When RFMODE = MID (open) the Cypress-mode Multi-Byte Framer is selected. The required detection of multiple framing characters makes the associated link much more robust to incorrect framing due to aliased SYNC characters in the data stream. In this mode, the Framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock does not contain any significant phase changes or hops

during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

When RFMODE = HIGH, the Alternate-mode Multi-Byte Framer is enabled. Like the Cypress-mode Multi-Byte Framer, multiple framing characters must be detected before the character boundary is adjusted. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, on identical 10-bit boundaries, before character framing is adjusted.

Framing for all channels is enabled when RFEN = HIGH. If RFEN = LOW, the Framer for each channel is disabled. When the framers are disabled, no changes are made to the recovered character boundaries on any channel, regardless of the presence of framing characters in the data stream.

10B/8B Decoder Block

The Decoder logic block performs three primary functions:

- decoding the received transmission characters back into Data and Special Character codes,
- comparing generated BIST patterns with received characters to permit at-speed link and device testing,
- and generation of ODD parity on the decoded characters.

10B/8B Decoder

The framed parallel output of each Deserializer Shifter is passed to the 10B/8B Decoder where, if the Decoder is enabled (DECMODE ≠ LOW), it is transformed from a 10-bit transmission character back to the original Data and Special Character codes. This block uses the 10B/8B Decoder patterns in *Table 25* and *Table 26* of this data sheet. Valid data characters are indicated by a 000b bit-combination on the associated RXSTx[2:0] status bits, and Special Character codes are indicated by a 001b bit-combination on these same status outputs. Framing characters, invalid patterns, disparity errors, and synchronization status are presented as alternate combinations of these status bits.

The 10B/8B Decoder operates in two normal modes, and can also be bypassed. The operating mode for the Decoder is controlled by the DECMODE input.

When DECMODE = LOW, the Decoder is bypassed and raw 10-bit characters are passed to the Output Register. In this mode, channel bonding is not possible, the Receive Elasticity Buffers are bypassed, and RXCKSEL must be MID. This clock mode generates separate RXCLKx± outputs for each receive channel.

When DECMODE = MID (or open), the 10-bit transmission characters are decoded using *Table 25* and *Table 26*. Received Special Code characters are decoded using the Cypress column of *Table 26*.

When DECMODE = HIGH, the 10-bit transmission characters are decoded using *Table 25* and *Table 26*. Received Special Code characters are decoded using the Alternate column of *Table 26*.

In all settings where the Decoder is enabled, the receive paths may be operated as separate channels or bonded to form various multi-channel buses.

Receive BIST Operation

The Receiver interfaces contain internal pattern generators that can be used to validate both device and link operation. These generators are enabled by the associated BOE[x] signals listed in *Table 10* (when the BISTLE latch enable input is HIGH). When enabled, a register in the associated receive channel becomes a pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received data stream, the associated Receiver checks each character in the Decoder with each character generated by the LFSR and indicates compare errors and BIST status at the RXSTx[2:0] bits of the Output Register.

When the BISTLE signal is HIGH, any BOE[x] input that is LOW enables the BIST generator/checker in the associated Receive channel (or the BIST generator in the associated Transmit channel). When BISTLE returns LOW, the values of all BOE[x] signals are captured in the BIST Enable Latch. These values remain in the BIST Enable Latch until BISTLE is returned HIGH. All captured signals in the BIST Enable Latch are set HIGH (i.e., BIST is disabled) following a device reset (TRSTZ is sampled LOW).

When BIST is first recognized as being enabled in the Receiver, the LFSR is preset to the BIST-loop start-code of D0.0. This D0.0 character is sent only once per BIST loop. The status of the BIST progress and any character mismatches is presented on the RXSTx[2:0] status outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXSTx[2:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. These same status values are presented when the Decoder is bypassed and BIST is enabled on a receive channel.

The specific status reported by the BIST state machine are listed in *Table 21*. These same codes are reported on the receive status outputs regardless of the state of DECMODE.

The specific patterns checked by each receiver are described in detail in the Cypress application note “HOTLink Built-In Self-Test.” The sequence compared by the CYP15G0401DXA is identical to that in the CY7B933 and CY7C924DX, allowing interoperable systems to be built when used at compatible serial signaling rates.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

When the receive paths are configured for common clock operation (RXCKSEL ≠ MID) each pass must be preceded by a 16-character Word Sync Sequence to allow output buffer alignment and management of clock frequency variations. This is automatically generated by the transmitter when its local RXCKSEL ≠ MID.

The BIST state machine requires the characters to be correctly framed for it to detect the BIST sequence. If the Low Latency Framer is enabled (RFMODE = LOW), the Framer will misalign to an aliased SYNC character within the BIST sequence.

If the Alternate Multi-Byte Framer is enabled (RFMODE = HIGH) and the Receiver outputs are clocked relative to a recovered clock, it is generally necessary to frame the Receiver before BIST is enabled. If the Receiver outputs are clocked relative to REFCLK (RXCKSEL = LOW), the transmitter precedes every 511 character BIST sequence with a 16-character Word Sync Sequence.

Receive Elasticity Buffer

Each receive channel contains an Elasticity Buffer that is designed to support multiple clocking modes. These buffers allow data to be read using an Elasticity Buffer read-clock that is asynchronous in both frequency and phase from the Elasticity Buffer write clock, or to use a read clock that is frequency coherent but with uncontrolled phase relative to the Elasticity Buffer write clock.

Each Elasticity Buffer is a minimum of 10-characters deep, and supports a 12-bit wide data path. It is capable of supporting a decoded character, three status bits, and a parity bit for each character present in the buffer. The write clock for these buffers is always the recovered clock for the associated read channel.

The read clock for the Elasticity Buffers may come from one of three selectable sources. It may be a

- character-rate REFCLK
- recovered clock from the same receive channel
- recovered clock from an alternate receive channel

These Elasticity Buffers are also used to align the output data streams when multiple channels are bonded together.

Receive Modes

The operating mode of the receive path is set through the RXMODE[1:0] inputs. These RXMODE[1:0] inputs are only interpreted when the Decoder is enabled (DECMODE ≠ LOW). These modes determine the type (if any) of channel bonding and status reporting. The different receive modes are listed in *Table 15*.

Table 15. Receive Operating Modes

RX Mode		Operating Mode	
Mode Number	RXMODE [1:0]	Channel Bonding	RXSTx Status Reporting
0	LL	Independent	Status A
1	LM		Reserved for test
2	LH	Independent	Status B
3	ML	Dual	Status A
4	MM		Reserved for test
5	MH	Dual	Status B
6	HL	Quad	Status A
7	HM		Reserved for test
8	HH	Quad	Status B

Independent Channel Modes

In independent channel modes (RX Modes 0 and 2, where RXMODE[1] = LOW), all four receive paths may be clocked in any clock mode selected by RXCKSEL.

When RXCKSEL = LOW, all four receive channels are clocked by REFCLK. RXCLKB± and RXCLKD± outputs are disabled (High-Z), and the RXCLKA± and RXCLKC± outputs present a buffered and delayed form of REFCLK. In this mode, the Receive Elasticity Buffers are enabled. For REFCLK clocking, the Elasticity Buffers must be able to insert K28.5 characters and delete framing characters as appropriate.

The insertion of a K28.5 or deletion of a framing character can occur at any time on any channel, however, the actual timing on these insertions and deletions is controlled in part by the how the transmitter sends its data. Insertion of a K28.5 character can only occur when the receiver has a framing character in the Elasticity Buffer. Likewise, to delete a framing character, one must also be in the Elasticity Buffer. To prevent a receive buffer overflow or underflow on a receive channel, a minimum density of framing characters must be present in the received data streams.

Prior to reception of valid data, at least one Word Sync Sequence (or that portion necessary to align the receive buffers) must be received to allow the Receive Elasticity Buffer to be centered. The Elasticity Buffer may also be centered by a device reset operation initiated through the $\overline{\text{TRSTZ}}$ input, however, following such an event the CYP15G0401DXA will normally require a framing event before it will correctly decode characters.

When RXCKSEL = MID (or open), each received channel Output Register is clocked by the recovered clock for that channel. Since no characters may be added or deleted, the receiver Elasticity Buffer is bypassed.

When RXCKSEL = HIGH, all channels are clocked by the selected recovered clock. This selection is made using the RXCLKB+ and RXCLKD+ signals as inputs per *Table 16*. This selected clock is always output on RXCLKA± and RXCLKC±. In this mode the Receive Elasticity Buffers are enabled. When data is output using a recovered clock (RXCKSEL = HIGH), the receive channels are not allowed to insert and delete characters, except as necessary for Elasticity Buffer alignment.

Table 16. Independent and Quad Channel Bonded Recovered Clock Select

RXCLKB+	RXCLKD+	RXCLKA±/RXCLKC± Clock Source
0	0	RXCLKA
0	1	RXCLKB
1	0	RXCLKC
1	1	RXCLKD

Prior to delivery of valid data, a Word Sync Sequence (or that portion necessary to align the receive buffers) must be received to center the Elasticity Buffers. The Elasticity buffer may also be centered by a device reset operation initiated by $\overline{\text{TRSTZ}}$ input, however, following such an event the CYP15G0401DXA also requires a framing event before it will correctly decode characters. Since the Elasticity buffer is not allowed to insert or delete framing characters, the transmit clocks on all received channels must all be from a common source.

Dual-Channel Bonded Modes

In dual-channel bonded modes (RX Modes 3 and 5, where RXMODE[1] = MID or open), the associated receive channel pair Output Registers must be clocked by a common clock. This mode does not operate when RXCKSEL = MID.

Proper operation in this mode requires that the associated transmit data streams are clocked from a common reference with no long-term character slippage between the bonded channels. In dual-channel mode this means that channels A and B must be clocked from a common reference, and channels C and D must be clocked from a common reference.

Prior to the deliver of valid data, a Word Sync Sequence (or that portion necessary to align the receive buffers) must be received on the bonded channels (within the allowable inter-channel skew window) to allow the Receive Elasticity Buffers to be centered. While normal characters may be output prior to this alignment event, they are not necessarily aligned to the same word boundaries as when they were transmitted.

When RXCKSEL = LOW, all four receive channels are clocked by REFCLK. RXCLKB± and RXCLKD± outputs are disabled (High-Z), and RXCLKA± and RXCLKC± present a buffered and delayed form of REFCLK. In this mode, the Receive Elasticity Buffers are enabled. For REFCLK clocking, the Elasticity Buffers must be able to insert K28.5 characters and delete framing characters as appropriate. While these insertions and deletions can take place at any time, they must occur at the same time on both channels that are bonded together. This is necessary to keep the data in the bonded channel-pairs properly aligned. This insert and delete process is controlled by the channel selected using the RXCLKB+ and RXCLKD+ inputs as listed in *Table 17*.

When RXCKSEL = HIGH, the A and B channels are clocked by the selected recovered clock, and the C and D channels are clocked by the selected recovered clock, as shown in *Table 17*. The output clock for the channel A/B bonded-pair is output continuously on RXCLKA±. The clock source for this output is selected from the recovered clock for channel A or channel B using the RXCLKB+ input. The output clock for the channel C/D bonded-pair is output continuously on RXCLKC±. The clock source for this output is selected from the recovered clock for channel C or channel D using the RXCLKD+ input.

Table 17. Dual-Channel Bonded Recovered Clock Select

RXCLKB+	RXCLKD+	Clock Source	
		RXCLKA±	RXCLKC±
0	X	RXCLKA	
1	X	RXCLKB	
X	0		RXCLKC
X	1		RXCLKD

When data is output using a recovered clock (RXCKSEL = HIGH), receive channels are not allowed to insert and delete characters, except as necessary for Elasticity Buffer alignment.

Quad Channel Modes

In quad-channel modes (RX modes 6 and 7, where RXMODE[1] = HIGH), all four receive channel Output Registers must be clocked by a common clock. This mode does not operate when RXCKSEL = MID.

Proper operation in this mode requires that the four transmit data streams are clocked from a common reference with no long-term character slippage between the bonded channels. In quad-channel modes this means that the transmit channels A, B, C, and D must all be clocked from a common reference.

Prior to the delivery of valid data, at least one Word Sync Sequence (or that portion necessary to align the receive buffers) must be received on all four bonded channels (within the allowable inter-channel skew window) to allow the Receive Elasticity Buffers to be centered and aligned.

When RXCKSEL = LOW, all four receive channels are clocked by the internal derivative of REFCLK. RXCLKB± and RXCLKD± outputs are disabled (High-Z), and RXCLKA± and RXCLKC± present a buffered and delayed form of REFCLK. In this mode the Receive Elasticity Buffers are enabled. For REFCLK clocking, the Elasticity Buffers must be able to insert K28.5 characters and delete framing characters as appropriate. While these insertions and deletions can take place at any time, they must occur at the same time on all four channels. This is necessary to keep the data in the four bonded channels properly aligned. This insert and delete process is controlled by the channel selected using the RXCLKB+ and RXCLKD+ inputs as listed in *Table 16*.

When RXCKSEL = HIGH, all four receive-channel Output Registers are clocked by the selected recovered clock. The clock select for quad channel mode is the same as that for independent channel operation. This selection is made using the RXCLKB+ and RXCLKD+ inputs, as shown in *Table 16*. The output clock for the four bonded channels is output continuously on RXCLKA± and RXCLKC±.

When data is output using a recovered clock (RXCKSEL = HIGH), receive channels are not allowed to insert and delete characters, except as necessary for Elasticity Buffer alignment.

Multi-Device Bonding

When configured for quad-channel bonding (RXMODE[1] = HIGH) it is also possible to bond channels across multiple devices. This form of channel bonding is only possible when RXCKSEL = LOW, selecting REFCLK as the output clock for all channels on all devices.

In this mode, the BONDST[1:0] signals are used to pass channel bonding status between the different devices. This is necessary to keep the data on all bonded devices in common alignment. One device must be selected as the controlling device by driving the MASTER pin on that device LOW. All other devices must have their MASTER pin HIGH to prevent having multiple active drivers on the BONDST bus. Within the master device, a single receive channel is selected as the controlling channel for generation of the different BONDST[1:0] status. This selection is made using the RXCLKB+ and RXCLKD+ inputs, as shown in *Table 16*. This allows the master channel selection to be changed through external control of the MASTER, RXCLKB+, and RXCLKD+ inputs.

NOTE: Any change in the master device or channel should be followed by assertion of TRSTZ to properly initialize the device.

Power Control

The CYP15G0401DXA supports user control of the powered up or down state of each transmit and receive channel. The receive channels are controlled by the RXLE signal and the

values present on the BOE[7:0] bus. The transmit channels are controlled by the OELE signal and the values present on the BOE[7:0] bus. Powering down unused channels will save power and reduce system heat generation. Controlling system power dissipation will improve the system performance.

Receive Channels

When RXLE is HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the receive PLLs and analog circuits. When a BOE[7:0] input is HIGH, the associated receive channel [A through D] PLL and analog logic are active. When a BOE[7:0] input is LOW, the associated receive channel [A through D] PLL and analog circuits are powered down. When RXLE returns LOW, the last values present on the BOE[7:0] inputs are captured. The specific BOE[7:0] input signal associated with a receive channel is listed in *Table 10*.

If a single channel of a bonded-pair or quad is disabled, this may prevent the other receive channels from bonding.

If the disabled channel has been selected as the master channel for insert/delete functions, or for recovered clock select, these functions will not operate. Any disabled receive channel will indicate a constant LFIx output.

When a disabled receive channel is re-enabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 10 ms.

Transmit Channels

When OELE is HIGH, the signals on the BOE[7:0] inputs directly control the power enables for the Serial Drivers. When a BOE[x] input is HIGH, the associated Serial Driver is enabled. When a BOE[x] input is LOW, the associated Serial Driver is disabled and powered down. If both Serial Drivers of a channel are disabled, the internal logic for that channel is powered down. When OELE returns LOW, the values present on the BOE[7:0] inputs are latched in the Output Enable Latch.

Device Reset State

When the CYP15G0401DXA is reset by assertion of $\overline{\text{TRSTZ}}$, the Transmit Enable and Receive Enable Latches are both cleared, and the BIST Enable Latch is preset. In this state, all transmit and receive channels are disabled, and BIST is disabled on all channels.

Following a device reset, it is necessary to enable the transmit and receive channels used for normal operation. This can be done by sequencing the appropriate values on the BOE[7:0] inputs while the OELE and RXLE signals are raised and lowered. For systems that do not require dynamic control of power, or want the part to power up in a fixed configuration, it is also possible to strap the RXLE and OELE control signals HIGH to permanently enable their associated latches. Connection of the associated BOE[7:0] signals HIGH will then enable the respective transmit and receive channels as soon as the $\overline{\text{TRSTZ}}$ signal is deasserted.

Output Bus

Each receive channel presents a 12-signal output bus consisting of

- an 8-bit data bus,
- a 3-bit status bus,
- and a parity bit.

The signals present on this output bus are modified by the present operating mode of the CYP15G0401DXA as selected by DECMODE. The bits are assigned as per *Table 18*.

Table 18. Output Register Bit Assignments[8]

Signal Name	DECMODE = LOW	DECMODE = MID or HIGH
RXSTx[2] (LSB)	COMDETx	RXSTx[2]
RXSTx[1]	DOUTx[0]	RXSTx[1]
RXSTx[0]	DOUTx[1]	RXSTx[0]
RXDx[0]	DOUTx[2]	RXDx[0]
RXDx[1]	DOUTx[3]	RXDx[1]
RXDx[2]	DOUTx[4]	RXDx[2]
RXDx[3]	DOUTx[5]	RXDx[3]
RXDx[4]	DOUTx[6]	RXDx[4]
RXDx[5]	DOUTx[7]	RXDx[5]
RXDx[6]	DOUTx[8]	RXDx[6]
RXDx[7] (MSB)	DOUTx[9]	RXDx[7]

Note:
8. The RXOPx outputs are also driven from the associated Output Register, but their interpretation is under the separate control of PARCTL.

When the 10B/8B Decoder is bypassed (DECMODE = LOW), the framed 10-bit character and a single status bit are presented at the receiver Output Register. The status output indicates if the character in the Output Register is one of the selected framing characters. The bit usage and mapping of the external signals to the raw 10B transmission character is shown in *Table 19*.

Table 19. Decoder Bypass Mode (DECMODE = LOW)

Signal Name	Bus Weight	10-bit Name
RXSTx[2] (LSB)	COMDETx	
RXSTx[1]	2^0	a
RXSTx[0]	2^1	b
RXDx[0]	2^2	c
RXDx[1]	2^3	d
RXDx[2]	2^4	e
RXDx[3]	2^5	i
RXDx[4]	2^6	f
RXDx[5]	2^7	g
RXDx[6]	2^8	h
RXDx[7] (MSB)	2^9	j

The COMDETx status outputs operate the same regardless of the bit combination selected for character framing by the FRAMCHAR input. They are HIGH when the character in the Output Register contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.

When the Low-Latency Framer and half-rate receive port clocking are also enabled (RFMODE = LOW, RXRATE = HIGH, and RXCKSEL ≠ LOW), the Framer will stretch the recovered clock to the nearest 20-bit boundary such that the

rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

When the Cypress or Alternate Mode Framer is enabled and half-rate receive port clocking is also enabled (RFMODE ≠ LOW and RXRATE = HIGH), the output clock is not modified when framing is detected, but a single pipeline stage may be added or subtracted from the data stream by the Framer logic such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

This adjustment only occurs when the Framer is enabled (RFEN = HIGH). When the Framer is disabled, the clock boundaries are not adjusted, and COMDETx may be asserted during the rising edge of RXCLK– (if an odd number of characters were received following the initial framing).

Parity Generation

In addition to the eleven data and status bits that are presented by each channel, an RXOPx parity output is also available on each channel. This allows the CYP15G0401DXA to support ODD parity generation for each channel. To handle a wide range of system environments, the CYP15G0401DXA supports different forms of parity generation, including no parity. When the decoders are enabled (DECMODE ≠ LOW), parity can be generated on

- the RXDx[7:0] character
- the RXDx[7:0] character and RXSTx[2:0] status

When the decoders are bypassed (DECMODE = LOW), parity can be generated on

- the RXDx[7:0] and RXSTx[1:0] bits
- the RXDx[7:0] and RXSTx[2:0] bits

These modes differ in the number bits which are included in the parity calculation. Only ODD parity is provided which ensures that at least one bit of the data bus is always a logic-1. Those bits covered by parity generation are listed in *Table 20*.

Parity generation is enabled through the 3-level select PARCTL input. When PARCTL = LOW, parity checking is disabled, and the RXOPx outputs are all disabled (High-Z).

When PARCTL = MID (open) and the decoders are enabled (DECMODE ≠ LOW), ODD parity is generated for the received and decoded character in the RXDx[7:0] signals and is presented on the associated RXOPx output.

When PARCTL = MID and the decoders are bypassed (DECMODE = LOW), ODD parity is generated for the received and decoded character in the RXDx[7:0] and RXSTx[1:0] bit positions.

When PARCTL = HIGH, ODD parity is generated for the RXDx[7:0] and the associated RXSTx[2:0] status bits.

When the Output Register clocking is such that the decoded character is passed through the Receive Elasticity Buffer prior to the addition of the RXSTx[2:0] status bits, the output parity calculation becomes a two-step process. The first parity calculation takes place as soon as the character is framed and decoded. This generates proper parity for the data portion of the decoded character which is then written to the Elasticity Buffer. If the parity calculation also includes the associated RXSTx[2:0] status bits (PARCTL = HIGH), a second parity calculation is made prior to loading the data and status bits into the receive Output Register. This is necessary because the status bits associated with a character in the Output Register are not determined until after the character is read from the Receive Elasticity Buffer.

This second parity calculation is based only on the content of the status bits, and the singular parity bit associated with the character read from the Elasticity Buffer.

Table 20. Output Register Parity Generation

Signal Name	Receive Parity Generate Mode (PARCTL)			
	LOW[9]	MID		HIGH
		DECMODE = LOW	DECMODE ≠ LOW	
RXSTx[2]				X[10]
RXSTx[1]		X		X
RXSTx[0]		X		X
RXDx[0]		X	X	X
RXDx[1]		X	X	X
RXDx[2]		X	X	X
RXDx[3]		X	X	X
RXDx[4]		X	X	X
RXDx[5]		X	X	X
RXDx[6]		X	X	X
RXDx[7]		X	X	X

Notes:
9. Receive path parity output drivers (RXOPx) are disabled (High-Z) when PARCTL = LOW
10. When the Decoder is bypassed (DECMODE = LOW) and BIST is not enabled (Receive BIST Latch output is HIGH), RXSTx[2] is driven to a logic-0, except when the character in the output buffer is a framing character.

Receive Status Bits

When the 10B/8B Decoder is enabled (DECMODE ≠ LOW), each character presented at the Output Register includes three associated status bits. These bits are used to identify

- if the contents of the data bus are valid,
- the type of character present,
- the state of receive BIST operations (regardless of the state of DECMODE),
- character violations,
- and channel bonding status.

These conditions normally overlap; e.g., a valid data character received with incorrect running disparity is not reported as a valid data character. It is instead reported as a Decoder violation of some specific type. This implies a hierarchy or priority level to the various status bit combinations. The hierarchy and value of each status is listed in *Table 21*.

Within these status decodes, there are three modes of status reporting. The two data status reporting modes (Type A and Type B) are selectable through the RXMODE[0] input. These status types allow compatibility with legacy systems, while allowing full reporting in new systems. The third status mode is used for reporting receive BIST status and progress. These status values are generated in part by the Receive Synchronization State Machine, and are listed in *Table 21*.

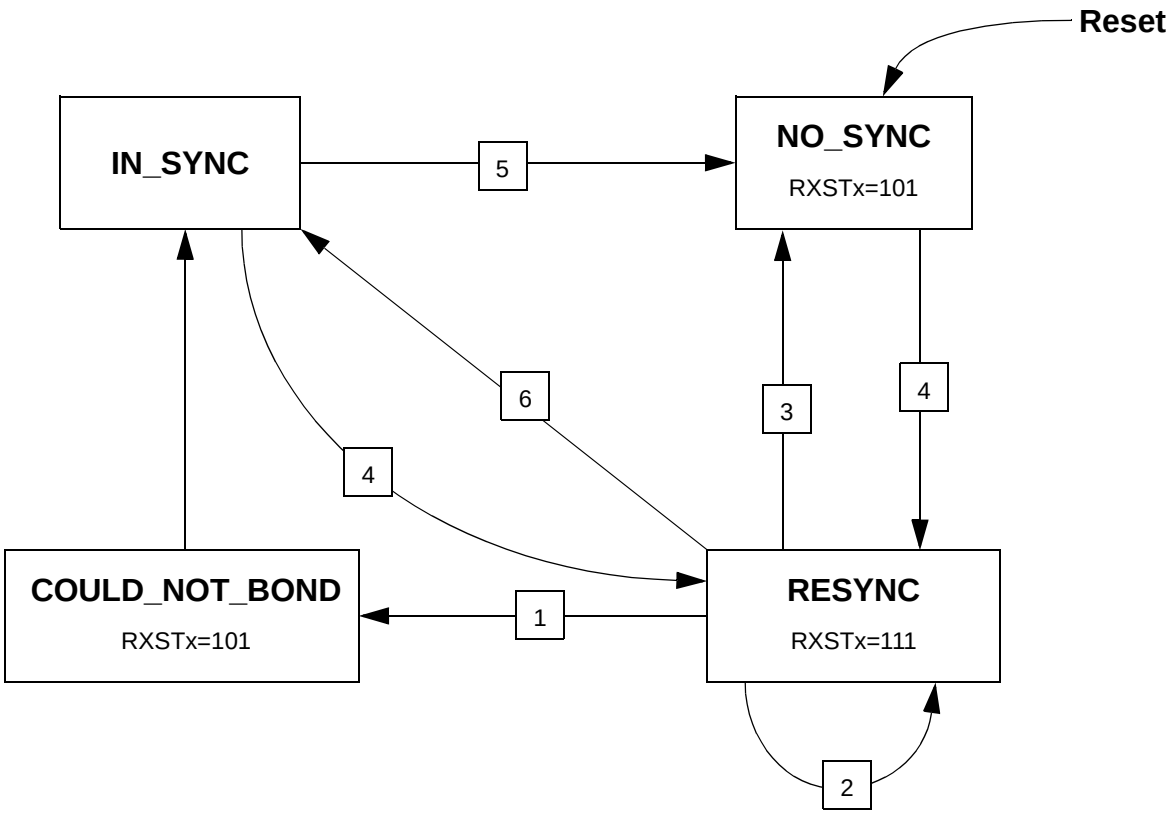
Table 21. Receive Character Status Bits

RXSTx[2:0]	Priority	Description		
		RX Status A	RX Status B	Receive BIST Status (Receive BIST = Enabled)
000	7	**Normal Character Received.** The valid Data character on the output bus meets all the formatting requirements of Data characters listed in *Table 25*.		**BIST Data Compare.** Character compared correctly
001	7	**Special Code Detected.** The valid special character on the output bus meets all the formatting requirements of the Special Code characters listed in *Table 26*, but is not the presently selected framing character or a decoder violation indication.		**BIST Command Compare.** Character compared correctly
010	2	**Receive Elasticity Buffer Underrun/Overrun Error.** The receive buffer was not able to add/drop a K28.5 or framing character.	**Channel Lock Detected.** Asserts when the bonded channels have detected RESYNC within the allotted window. Presented only on the last cycle before aligned data is presented.	**BIST Last Good.** Last Character of BIST sequence detected and valid.
011	5	**Framing Character Detected.** This indicates that a character matching the patterns identified as a framing character (as selected by FRAMCHAR) was detected. The decoded value of this character is present in the associated output bus.		
100	4	**Codeword Violation.** The character on the output bus is a C0.7. This indicates that the received character cannot be decoded into any valid character.		**BIST Last Bad.** Last Character of BIST sequence detected invalid.
101	1	**Loss of Sync.** The character on the bus is invalid, due to an event that has caused the receive channels to lose synchronization. When channel bonding is enabled, this indicates that one or more channels have either lost bit synchronization (loss of character framing), or that the bonded channels are no longer in proper character alignment. When the channels are operated independently (with the decoder enabled), this indicates a PLL Out of Lock condition.	**Loss of Sync.** The character on the bus is invalid, due to an event that has caused the receive channels to lose synchronization. When channel bonding is enabled, this indicates that one or more channels have either lost bit synchronization (loss of character framing), or that the bonded channels are no longer in proper character alignment. When the channels are operated independently (with the decoder enabled), this indicates a loss of character framing. Also used to indicate Receive Elasticity Buffer underflow/overflow errors.	**BIST Start.** Receive BIST is enabled on this channel, but character compares have not yet commenced. This also indicates a PLL Out of Lock condition, and Elasticity Buffer overflow/underflow conditions.
110	6	**Running Disparity Error.** The character on the output bus is a C4.7, C1.7, or C2.7.		**BIST Error.** While comparing characters, a mismatch was found in one or more of the decoded character bits.
111	3	**Resync.** The receiver state machine is in the Resynchronization state. In this state the data on the output bus reflects the presently decoded FRAMCHAR.		**BIST Wait.** The receiver is comparing characters. but has not yet found the start of BIST character to enable the LFSR.

Receive Synchronization State Machine

Each receive channel contains a Receive Synchronization State Machine. This machine handles loss and recovery of bit, channel, and word framing, and part of the control for channel bonding. This state machine is enabled whenever the receive channels are configured for channel bonding (RXMODE[1] ≠ LOW). Separate forms of the state machine exist for the two different types of status reporting.

When operated without channel bonding (RXMODE[1] = LOW, RX Modes 0 and 2), these state machines are disabled and characters are decoded directly. In RX Mode 0 the RESYNC (111b) status is never reported. In RX Mode 2, neither the RESYNC (111b) nor Channel Lock Detected (010b) status are reported.

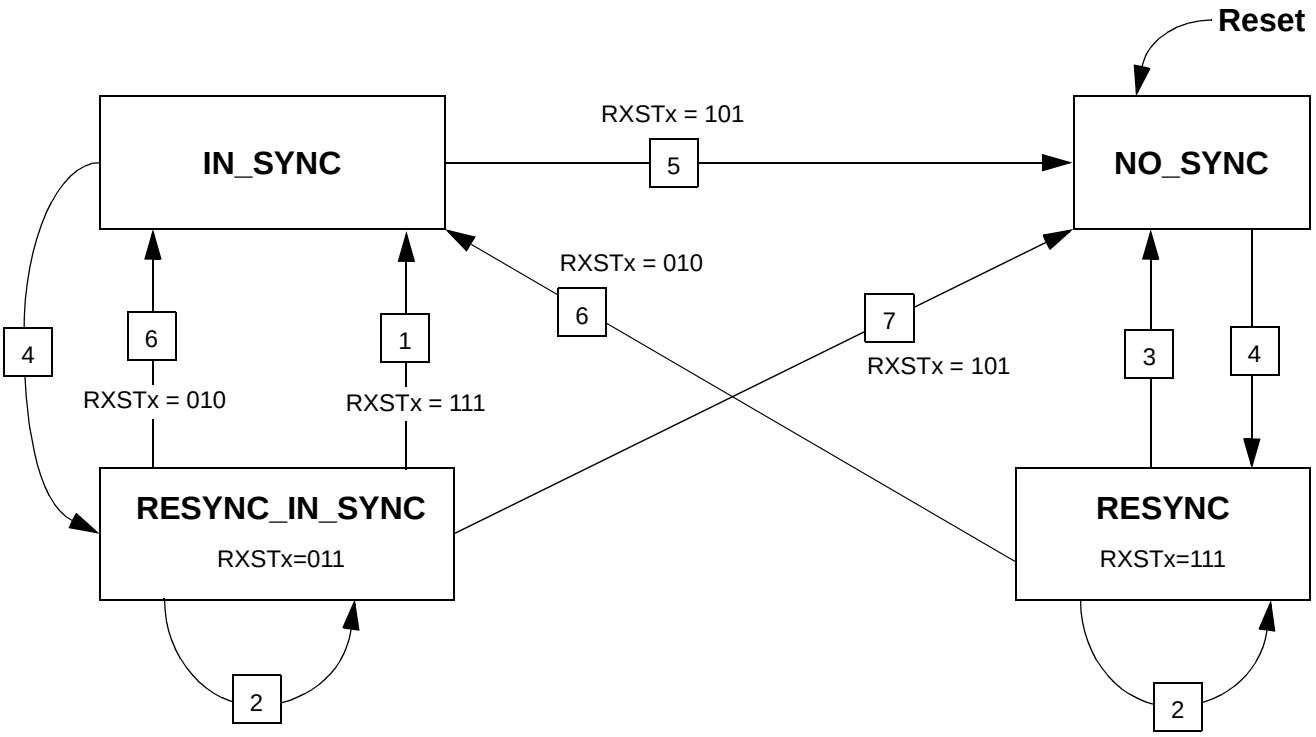


#	State Transition Conditions
1	($\overline{\text{BOND\_INH}}$ = LOW) AND (Deskew Window Expired)
2	FRAMCHAR Detected
3	(Elasticity Buffer Under/Overrun) OR (RX PLL Loss of Lock) OR (Any Decoder Error)
4	Four Consecutive FRAMCHAR Detected
5	(Elasticity Buffer Under/Overrun) OR (RX PLL Loss of Lock) OR (Four Consecutive Decoder Errors) OR (Invalid Minus Valid = 4)
6	Valid Character other than a FRAMCHAR

Figure 2. Status Type-A Receive State Machine

Status Type-A Receive State Machine

This machine has four primary states: NO_SYNC, RESYNC, COULD_NOT_BOND, and IN_SYNC, as shown in *Figure 2*. The IN_SYNC state can respond with multiple status types, while others can respond with only one type.



#	Condition
1	($\overline{\text{BOND\_INH}}$ = LOW OR Master Channel Did Not Bond) AND (Deskew Window Expired) OR (Decoder Error)
2	FRAMCHAR Detected
3	(Elasticity Buffer Under/Overrun) OR (RX PLL Loss of Lock) OR (Any Decoder Error) OR ($\overline{\text{BOND\_INH}}$ = LOW) OR (Master Channel Did Not Bond) AND (Deskew Window Expired))
4	Four Consecutive FRAMCHAR Detected
5	(Elasticity Buffer Under/Overrun) OR (RX PLL Loss of Lock) OR (Four Consecutive Decoder Errors) OR (Invalid Minus Valid = 4)
6	(Last FRAMCHAR Before a Valid Character) AND (Bonded to $\overline{\text{MASTER}}$ Channel)
7	(Elasticity Buffer Under/Overrun) OR (RX PLL Loss of Lock)

Figure 3. Status Type-B Receive State Machine

Status Type-B Receive State Machine

This machine has four primary states: NO_SYNC, RESYNC, IN_SYNC, and COULD_NOT_BOND, as shown in *Figure 3*. Some of these state can respond with only one status value, while others can respond with multiple status types.

BIST Status State Machine

When a receive path is enabled to look for and compare the received data stream with the BIST pattern, the RXSTx[2:0] bits identify the present state of the BIST compare operation.

The BIST state machine has multiple states, as shown in *Figure 4* and *Table 21*. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than 16, the state machine is forced to the WAIT_FOR_BIST state where it monitors the interface for the first character (D0.0) of the next BIST sequence. Also, if the Elasticity Buffer ever hits an overflow/underflow condition, the status is forced to the BIST_START until the buffer is re-centered (approximately nine character periods).

To ensure compatibility between the source and destination systems when operating in BIST modes, the sending and receiving ends of the link must use the same receive clock setup. (RXCKSEL = MID or RXCKSEL ≠ MID).

JTAG Support

The CYP15G0401DXA contains a JTAG port to allow system level diagnosis of device interconnect. Of the available JTAG modes, only boundary scan is supported. This capability is present only on the LVTTL inputs and outputs and the REFCLK± clock input. The high-speed serial inputs and outputs are not part of the JTAG test chain.

JTAG ID

The JTAG device ID for the CYP15G0401DXA is '0C800069'x.

3-Level Select Inputs

Each 3-Level select input reports as two bits in the scan register. These bits report the LOW, MID, and HIGH state of the associated input as 00, 10, and 11 respectively.

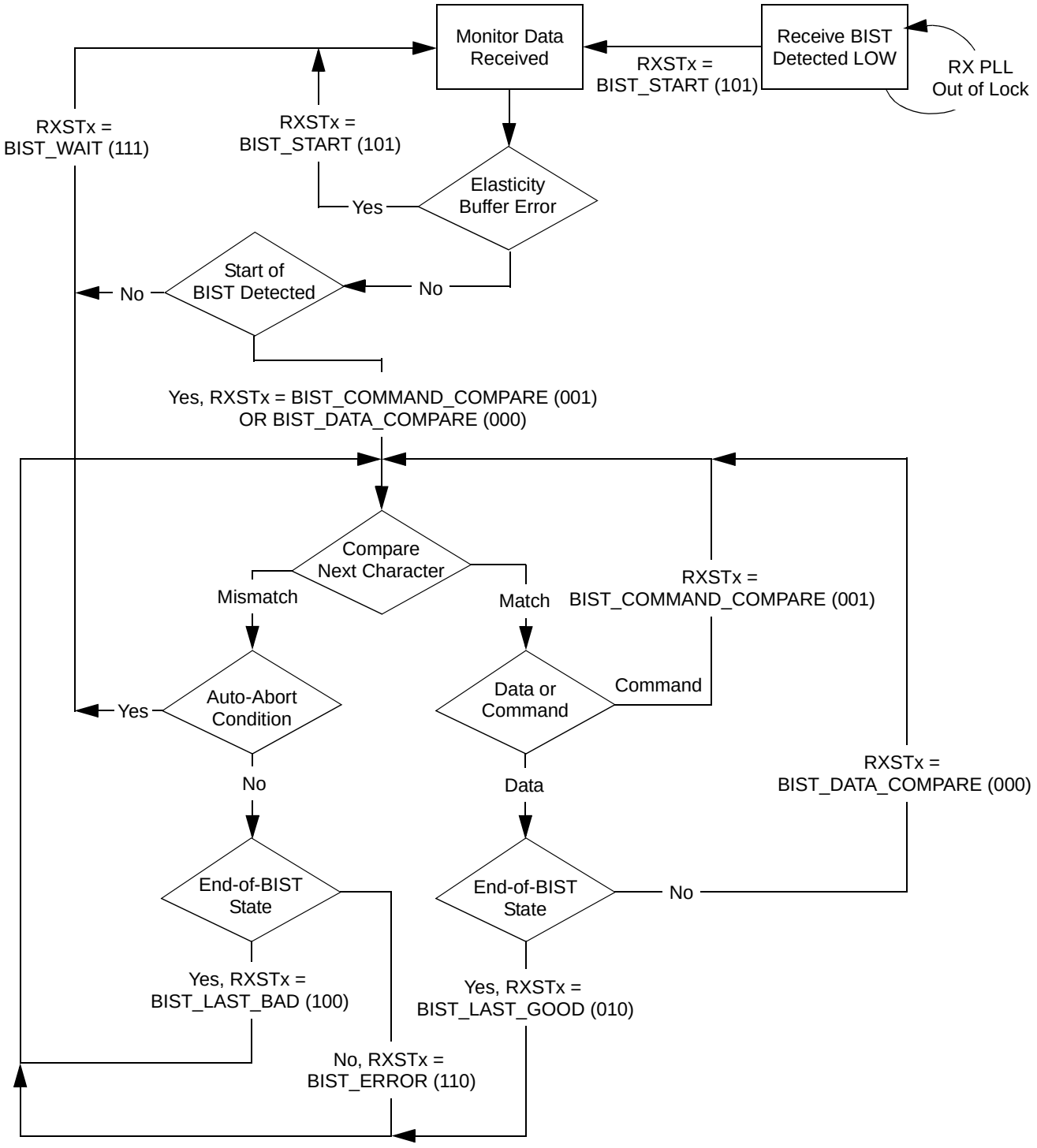


Figure 4. Receive BIST State Machine

Maximum Ratings

(Above which the useful life may be impaired. User guidelines only, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied.... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +3.8V

DC Voltage Applied to LVTTL Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V

Output Current into LVTTL Outputs (LOW) ..... 60 mA

DC Input Voltage ..... –0.5V to V_{CC} + 0.5V

Static Discharge Voltage ..... > 2000 V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ±5%
Industrial	–40°C to +85°C	+3.3V ±5%

CYP15G0401DXA DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
LVTTL Compatible Outputs					
V_{OHT}	Output HIGH Voltage	I_{OH} = –4 mA, V_{CC} = Min.	2.4	V_{CC}	V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA, V_{CC} = Min.	0	0.4	V
I_{OST}	Output Short Circuit Current	V_{OUT} = 0V[11]	–50	–15	mA
I_{OZL}	High-Z Output Leakage Current		–20	20	µA
LVTTL Compatible Inputs					
V_{IHT}	Input HIGH Voltage		2.0	V_{CC} + 0.3	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK Input, V_{IN} = V_{CC}		1.5	mA
		Other Inputs, V_{IN} = V_{CC}		+40	µA
I_{ILT}	Input LOW Current	REFCLK Input, V_{IN} = 0.0V		–1.5	mA
		Other Inputs, V_{IN} = 0.0V		–40	µA
I_{IHPDT}	Input HIGH Current with internal pull-down	V_{IN} = V_{CC}		+200	µA
I_{ILPUT}	Input LOW Current with internal pull-up	V_{IN} = 0.0V		–200	µA
LVDIFF Inputs: REFCLK±					
V_{DIFF}[12]	Input Differential Voltage		400	V_{CC}	mV
V_{IHHP}	Highest Input HIGH Voltage		1.2	V_{CC}	V
V_{ILLP}	Lowest Input LOW Voltage		0.0	V_{CC}/2	V
V_{COMREF}[13]	Common Mode Range		1.0	V_{CC} – 1.2V	V
3-Level Inputs					
V_{IHH}	Three-Level Input HIGH Voltage	Min. ≤ V_{CC} ≤ Max.	0.87 * V_{CC}	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage	Min. ≤ V_{CC} ≤ Max.	0.47 * V_{CC}	0.53 * V_{CC}	V
V_{ILL}	Three-Level Input LOW Voltage	Min. ≤ V_{CC} ≤ Max.	0.0	0.13 * V_{CC}	V
I_{IHH}	Input HIGH Current	V_{IN} = V_{CC}		200	µA
I_{IMM}	Input MID Current	V_{IN} = V_{CC}/2	–50	50	µA
I_{ILL}	Input LOW Current	V_{IN} = GND		–200	µA
Differential CML Serial Outputs: OUTA1±, OUTA2±, OUTB1±, OUTB2±, OUTC1±, OUTC2±, OUTD1±, OUTD2±					
V_{OHC}	Output HIGH Voltage (V_{CC} referenced)	100Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
		150Ω differential load	V_{CC} – 0.5	V_{CC} – 0.2	V
V_{OLC}	Output LOW Voltage (V_{CC} referenced)	100Ω differential load	V_{CC} – 1.1	V_{CC} – 0.7	V
		150Ω differential load	V_{CC} – 1.1	V_{CC} – 0.7	V
V_{ODIF}	Output Differential Voltage |(OUT+) – (OUT–)|	100Ω differential load	450	800	mV
		150Ω differential load	560	1000	mV

Notes:

11. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
12. This is the minimum difference in voltage between the true and complement inputs required to ensure detection of a logic-1 or logic-0. A logic-1 exists when the true (+) input is more positive than the complement (–) input. A logic-0 exists when the complement (–) input is more positive than true (+) input.
13. The common mode range defines the allowable range of REFCLK+ and REFCLK– when REFCLK+ = REFCLK–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.

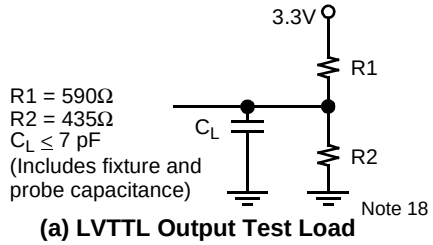
CYP15G0401DXA DC Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		Min.	Max.	Unit
Differential Serial Line Receiver Inputs: INA1±, INA2±, INB1±, INB2±, INC1±, INC2±, IND1±, IND2±						
V_{DIFFS}[12]	Input Differential Voltage |(IN+) – (IN–)|			100	1200	mV
V_{IHE}	Highest Input HIGH Voltage				V_{CC}	V
V_{ILE}	Lowest Input LOW Voltage			V_{CC} – 2.0		V
I_{IHE}	Input HIGH Current	$V_{IN} = V_{IHE}$ Max.			1350	µA
I_{ILE}	Input LOW Current	$V_{IN} = V_{ILE}$ Min.		–700		µA
V_{COM}[14]	Common mode Input range	((V_{CC} – 2.0) + 0.05) Min., (Min. V_{CC} – 0.05) Max.		+1.25	+3.1	V
Miscellaneous				**Typ.**	**Max.**	
I_{CC}[15]	Max Power Supply Current	REFCLK = Max.	Commercial	860	1100	mA
			Industrial	TBD	TBD	mA
I_{CC}[16]	Typ Power Supply Current	REFCLK = 125 MHz		750		mA

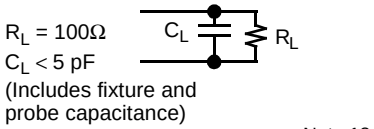
Capacitance[17]

Parameter	Description	Test Conditions	Max.	Unit
C_{INTTL}	TTL Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	7	pF
C_{INPECL}	PECL input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 3.3V	4	pF

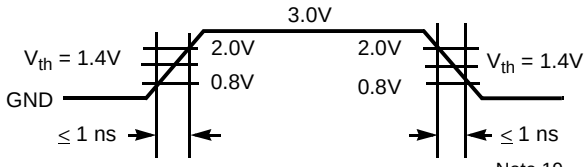
Test Loads and Waveforms



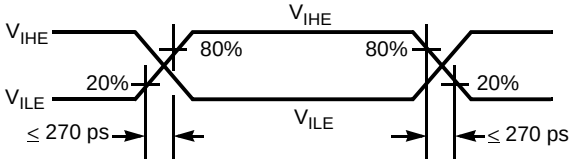
(a) LVTTL Output Test Load



(b) CML Output Test Load



(c) LVTTL Input Test Waveform



(d) CML/LVPECL Input Test Waveform

Notes:

14. The common mode range defines the allowable range of INPUT+ and INPUT– when INPUT+ = INPUT–. This marks the zero-crossing between the true and complement inputs as the signal switches between a logic-1 and a logic-0.
15. Maximum I_{CC} is measured with V_{CC} = MAX, RFEN = LOW, T_A = 25°C, with all channels and Serial Line Drivers enabled, sending a continuous alternating 01 pattern, and outputs unloaded.
16. Typical I_{CC} is measured under similar conditions except with V_{CC} = 3.3V, T_A = 25°C, RFEN = LOW, with all channels enabled and one Serial Line Driver per transmit channel sending a continuous alternating 01 pattern. The redundant outputs on each channel are powered down and the parallel outputs are unloaded.
17. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
18. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.
19. The LVTTL switching threshold is 1.4V. All timing references are made relative to the point where the signal edges crosses the threshold voltage.

CYP15G0401DXA Transmitter LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max	Unit
f_{TS}	TXCLKx Clock Frequency	20	150	MHz
t_{TXCLK}	TXCLKx Period	6.66	50	ns
t_{TXCLKH}[17]	TXCLKx HIGH Time	2.2		ns
t_{TXCLKL}[17]	TXCLKx LOW Time	2.2		ns
t_{TXCLKR}[17, 20, 21]	TXCLKx Rise Time	0.3	1.7	ns
t_{TXCLKF}[17, 20, 21]	TXCLKx Fall Time	0.3	1.7	ns
t_{TXDS}	Transmit Data Set-Up Time to TXCLKx↑ (TXCKSEL ≠ LOW)	1.7		ns
t_{TXDH}	Transmit Data Hold Time from TXCLKx↑ (TXCKSEL ≠ LOW)	0.8		ns
f_{TOS}	TXCLKO Clock Frequency = 1x or 2x REFCLK Frequency	20	150	MHz
t_{TXCLKO}	TXCLKO Period	6.66	50	ns
$t_{TXCLKOD+}$	TXCLKO+ Duty Cycle with 65% HIGH time	–1.0	+0.0	ns
$t_{TXCLKOD–}$	TXCLKO– Duty Cycle with 35% HIGH time	–0.0	+1.0	ns

CYP15G0401DXA Receiver LVTTL Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{RS}	RXCLKx Clock Output Frequency	10	150	MHz
t_{RXCLKP}	RXCLKx Period	6.66	50	ns
t_{RXCLKH}	RXCLKx HIGH Time (RXRATE = LOW)	2.33[17]	26.5	ns
	RXCLKx HIGH Time (RXRATE = HIGH)	5.66	51	ns
t_{RXCLKL}	RXCLKx LOW Time (RXRATE = LOW)	2.33[17]	26	ns
	RXCLKx LOW Time (RXRATE = HIGH)	5.2	51	ns
t_{RXCLKD}	RXCLKx Duty Cycle centered at 50%	–1.0	+1.0	ns
t_{RXCLKR}[17]	RXCLKx Rise Time	0.3	1.2	ns
t_{RXCLKF}[17]	RXCLKx Fall Time	0.3	1.2	ns
$t_{RXDV–}$[22]	Status and Data Valid Time to RXCLKx (RXCKSEL HIGH or MID)	5UI – 1.5		ns
	Status and Data Valid Time to RXCLKx (HALF RATE RECOVERED CLOCK)	–1.5		ns
t_{RXDV+}[22]	Status and Data Valid Time From RXCLKx (RXCKSEL HIGH or MID)	5UI – 1.8		ns
	Status and Data Valid Time From RXCLKx (HALF RATE RECOVERED CLOCK)	–1.5		ns

Notes:

20. The ratio of rise time to falling time must not vary by greater than 2:1.
21. For a given operating frequency, neither rise or fall specification can be greater than 20% of the clock-cycle period or the data sheet maximum time.
22. Parallel data output specifications are only valid if all inputs or outputs are loaded with similar DC and AC loads.

CYP15G0401DXA REFCLK Switching Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
f_{REF}	REFCLK Clock Frequency	20	150	MHz
t_{REFCLK}	REFCLK Period	6.6	50	ns
t_{REFH}	REFCLK HIGH Time (TXRATE = HIGH)	5.9		ns
	REFCLK HIGH Time (TXRATE = LOW)	2.9[17]		ns
t_{REFL}	REFCLK LOW Time (TXRATE = HIGH)	5.9		ns
	REFCLK LOW Time (TXRATE = LOW)	2.9[17]		ns
t_{REFD}[23]	REFCLK Duty Cycle	30	70	%
t_{REFR}[17, 20, 21]	REFCLK Rise Time (20% - 80%)		2	ns
t_{REFF}[17, 20, 21]	REFCLK Fall Time (20% - 80%)		2	ns
t_{TREFDS}	Transmit Data Setup Time to REFCLK (TXCKSEL = LOW)	1.7		ns
t_{TREFDH}	Transmit Data Hold Time from REFCLK (TXCKSEL = LOW)	0.8		ns
t_{RREFDA}	Receive Data Access Time from REFCLK (RXCKSEL = LOW)		9.5	ns
t_{RREFDV}	Receive Data Valid Time from REFCLK (RXCKSEL = LOW)	4.0		ns
$t_{REFADV–}$	Received Data Valid Time to RXCLKA (RXCKSEL = LOW)	10UI – 4.7		ns
$t_{REFADV+}$	Received Data Valid Time from RXCLKA (RXCKSEL = LOW)	1.0		ns
$t_{REFCDV–}$	Received Data Valid Time to RXCLKC (RXCKSEL = LOW)	10UI – 4.3		ns
$t_{REFCDV+}$	Received Data Valid Time from RXCLKC (RXCKSEL = LOW)	0.2		ns
t_{REFRX}[24]	REFCLK Frequency Referenced to Received Clock Period	–0.02	+0.02	%

CYP15G0401DXA Transmit Serial Outputs and TX PLL Characteristics Over the Operating Range

Parameter	Description	Condition	Min.	Max.	Unit
t_B	Bit Time		5000	660	ps
t_{RISE}[17]	CML Output Rise Time 20% - 80% (CML Test Load)	SPDSEL = HIGH	50	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	200	1000	ps
t_{FALL}[17]	CML Output Fall Time 80% - 20% (CML Test Load)	SPDSEL = HIGH	50	270	ps
		SPDSEL = MID	100	500	ps
		SPDSEL = LOW	200	1000	ps
t_{DJ}[17, 25, 27]	Deterministic Jitter (peak-peak)	0.2 – 1.5Gbps		TBD	UI
t_{RJ}[17, 26, 27]	Random Jitter (σ)	0.2 – 1.5Gbps		TBD	ps
t_{TXLOCK}	Transmit PLL lock to REFCLK		TBD	TBD	ns

Notes:

23. The duty cycle specification is a simultaneous condition with the t_{REFH} and t_{REFL} parameters. This means that at faster character rates the REFCLK duty cycle cannot be as large as 30% - 70%,
24. REFCLK has no phase or frequency relationship with the recovered clock(s) and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within ±200 PPM (±0.02%) of the transmitter PLL reference (REFCLK) frequency, necessitating a ±100-PPM crystal.
25. While sending continuous K28.5s, outputs loaded to a balanced 100Ω load, measured at the cross point of differential outputs, over the operating range.
26. While sending continuous K28.7s, after 100,000 samples measured at the cross point of differential outputs, time referenced to REFCLK input, over the operating range.
27. Total jitter is calculated at an assumed BER of 1E –12. Hence: Total Jitter (t_J) = (t_{RJ} * 14) + t_{DJ}.

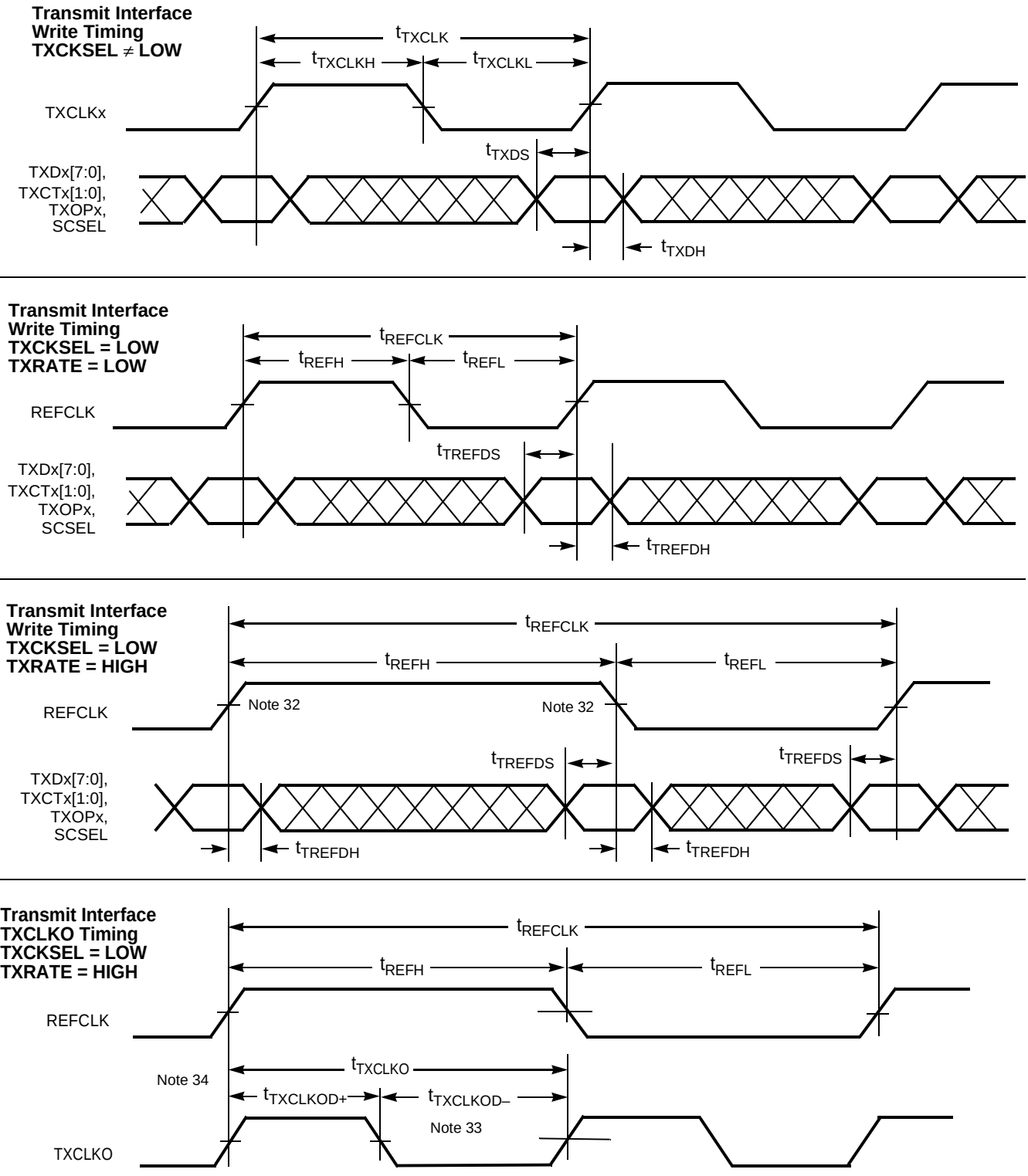
CYP15G0401DXA Receive Serial Inputs and CDR PLL Characteristics Over the Operating Range

Parameter	Description	Min.	Max.	Unit
t_{RXLOCK}	Receive PLL lock to input data stream (cold start)		10	ms
	Receive PLL lock to input data stream		2500	UI
$t_{RXUNLOCK}$	Receive PLL Unlock Rate	TBD	TBD	ns
t_{SA}	Static Alignment [17, 28]	TBD	TBD	ps
t_{jtol}	Jitter Tolerance[17, 29, 30, 31]	TBD	TBD	UI

Notes:

28. Static alignment is a measure of the alignment of the Receiver sampling point to the center of a bit. Static alignment is measured by sliding one bit edge in 3,000 nominal transitions until a character error occurs.
29. Receiver UI (Unit Interval) is calculated as 1 / (f_{REF} * 20) (when RXRATE = HIGH) or 1 / (f_{REF} * 10) (when RXRATE = LOW) if no data is being received, or 1 / (f_{REF} * 20) (when RXRATE = HIGH) or 1 / (f_{REF} * 10) (when RXRATE = LOW) of the remote transmitter if data is being received. In an operating link this is equivalent to t_B.
30. All measurements were done using a CJTPAT.
31. Measured at a datarate of 1.25Gbps.

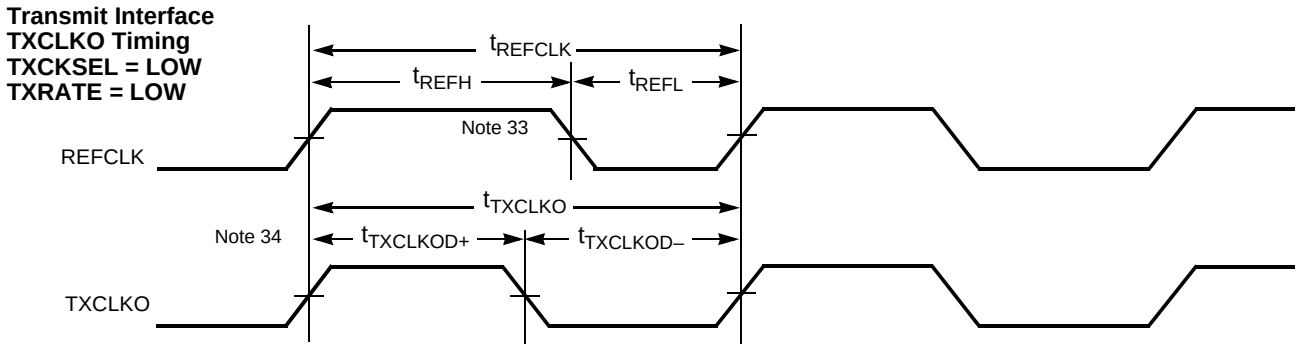
CYP15G0401DXA HOTLink II Transmitter Switching Waveforms



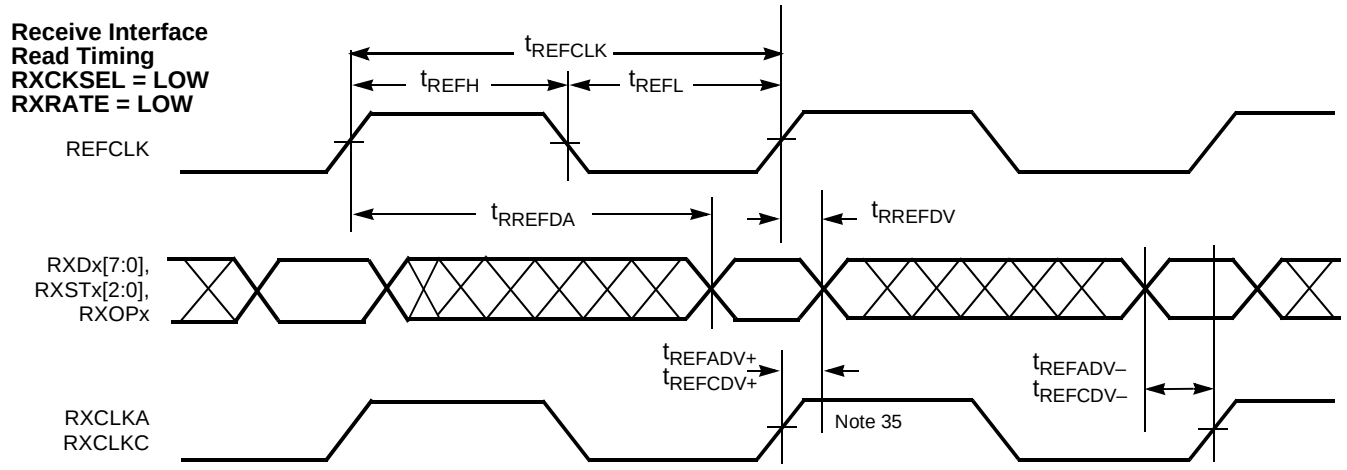
Notes:

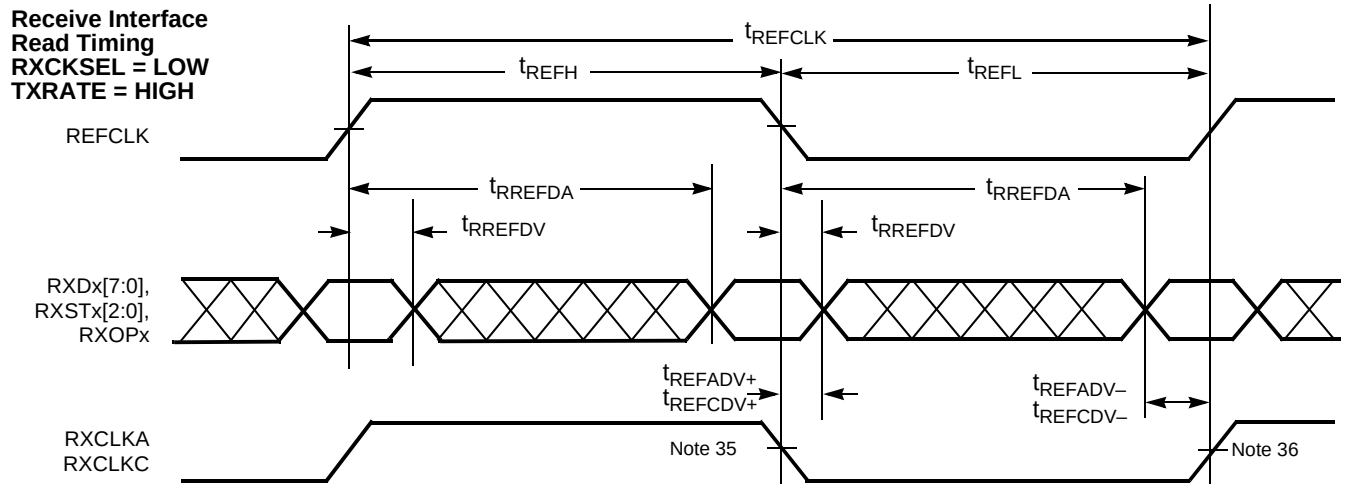
32. When REFCLK is configured for half-rate operation (TXRATE = HIGH) and data is captured using REFCLK instead of a TXCLKx clock (TXCKSEL = LOW), data is captured using both the rising and falling edges of REFCLK.
33. The TXCLKO output remains at the character rate regardless of the state of TXRATE and does not follow the duty cycle of REFCLK.
34. The rising edge of TXCLKO output has no direct phase relationship to the REFCLK input.

CYP15G0401DXA HOTLink II Transmitter Switching Waveforms (continued)



Switching Waveforms for the CYP15G0401DXA HOTLink II Receiver



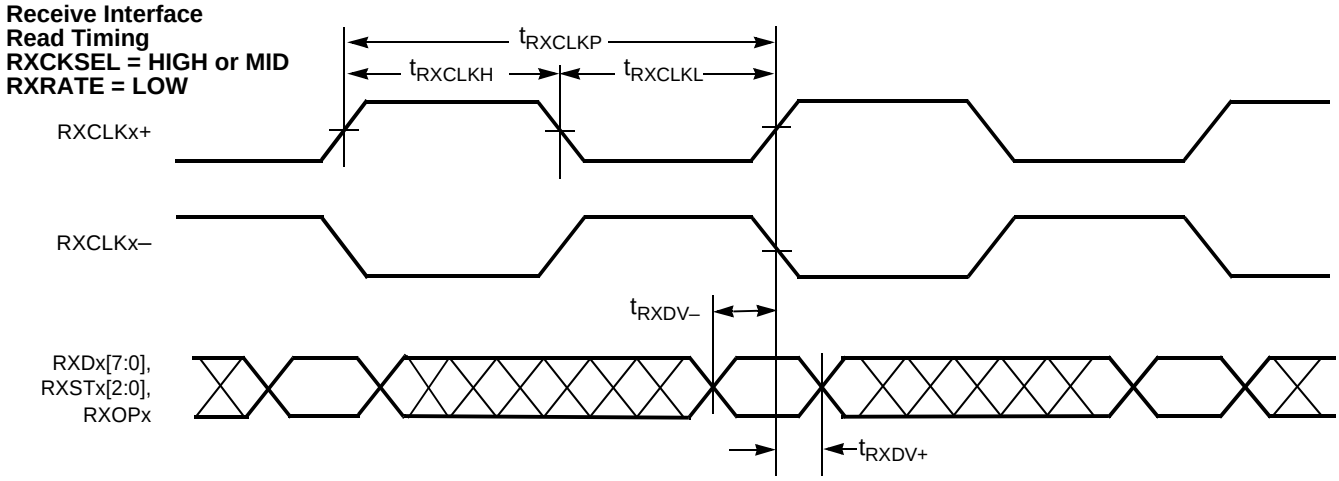


Note:

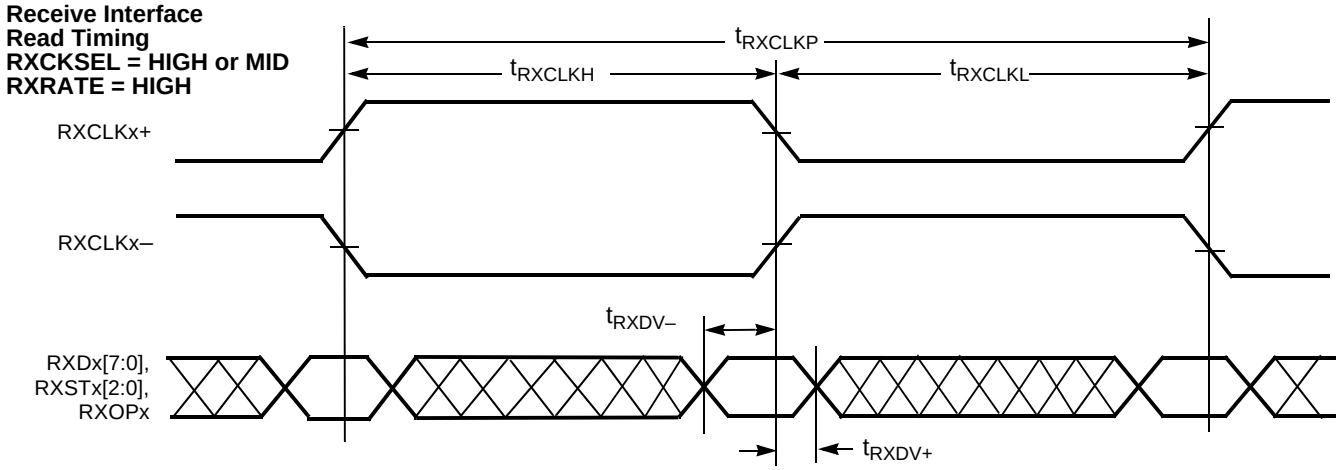
35. RXCLKA and RXCLKC are delayed in phase from REFCLK, and are different in phase from each other.
36. When operated with a half-rate REFCLK, the setup and hold specifications for data relative to RXCLKA and RXCLKC are relative to both rising and falling edges of the respective clock output

Switching Waveforms for the CYP15G0401DXA HOTLink II Receiver (continued)

Receive Interface Read Timing RXCKSEL = HIGH or MID RXRATE = LOW



Receive Interface Read Timing RXCKSEL = HIGH or MID RXRATE = HIGH



Static Alignment

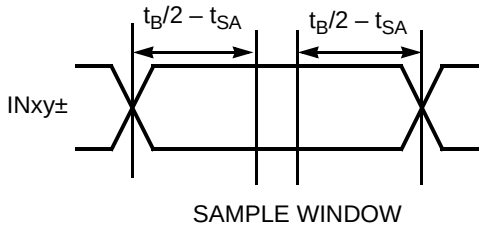


Table 22. Package Coordinate Signal Allocation

Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type	Ball ID	Signal Name	Signal Type
A01	INC1–	CML IN	C04	INSELB	LVTTL IN	E19	VCC	POWER
A02	OUTC1–	CML OUT	C05	VCC	POWER	E20	VCC	POWER
A03	INC2–	CML IN	C06	PARCTL	3-LEVEL SEL	F01	TXPERC	LVTTL OUT
A04	OUTC2–	CML OUT	C07	SDASEL	3-LEVEL SEL	F02	TXOPC	LVTTL IN PU
A05	VCC	POWER	C08	GND	GROUND	F03	TXDC[0]	LVTTL IN
A06	IND1–	CML IN	C09	BOE[7]	LVTTL IN PU	F04	RXCKSEL	3-LEVEL SEL
A07	OUTD1–	CML OUT	C10	BOE[5]	LVTTL IN PU	F17	BISTLE	LVTTL IN PU
A08	GND	GROUND	C11	BOE[3]	LVTTL IN PU	F18	RXSTB[1]	LVTTL OUT
A09	IND2–	CML IN	C12	BOE[1]	LVTTL IN PU	F19	RXOPB	LVTTL 3-S OUT
A10	OUTD2–	CML OUT	C13	GND	GROUND	F20	RXSTB[0]	LVTTL OUT
A11	INA1–	CML IN	C14	TXMODE[0]	3-LEVEL SEL	G01	TXDC[7]	LVTTL IN
A12	OUTA1–	CML OUT	C15	RXMODE[0]	3-LEVEL SEL	G02	TXCKSEL	3-LEVEL SEL
A13	GND	GROUND	C16	VCC	POWER	G03	TXDC[4]	LVTTL IN
A14	INA2–	CML IN	C17	TXRATE	LVTTL IN PD	G04	TXDC[1]	LVTTL IN
A15	OUTA2–	CML OUT	C18	RXRATE	LVTTL IN PD	G17	DECMODE	3-LEVEL SEL
A16	VCC	POWER	C19	LPEN	LVTTL IN PD	G18	OELE	LVTTL IN PU
A17	INB1–	CML IN	C20	TDO	LVTTL 3-S OUT	G19	FRAMCHAR	3-LEVEL SEL
A18	OUTB1–	CML OUT	D01	TCLK	LVTTL IN PD	G20	RXDB[1]	LVTTL OUT
A19	INB2–	CML IN	D02	$\overline{\text{TRSTZ}}$	LVTTL IN PU	H01	GND	GROUND
A20	OUTB2–	CML OUT	D03	INSELD	LVTTL IN	H02	GND	GROUND
B01	INC1+	CML IN	D04	INSELA	LVTTL IN	H03	GND	GROUND
B02	OUTC1+	CML OUT	D05	VCC	POWER	H04	GND	GROUND
B03	INC2+	CML IN	D06	RFMODE	3-LEVEL SEL	H17	GND	GROUND
B04	OUTC2+	CML OUT	D07	SPDSEL	3-LEVEL SEL	H18	GND	GROUND
B05	VCC	POWER	D08	GND	GROUND	H19	GND	GROUND
B06	IND1+	CML IN	D09	BOE[6]	LVTTL IN PU	H20	GND	GROUND
B07	OUTD1+	CML OUT	D10	BOE[4]	LVTTL IN PU	J01	TXCTC[1]	LVTTL IN
B08	GND	GROUND	D11	BOE[2]	LVTTL IN PU	J02	TXDC[5]	LVTTL IN
B09	IND2+	CML IN	D12	BOE[0]	LVTTL IN PU	J03	TXDC[2]	LVTTL IN
B10	OUTD2+	CML OUT	D13	GND	GROUND	J04	TXDC[3]	LVTTL IN
B11	INA1+	CML IN	D14	TXMODE[1]	3-LEVEL SEL	J17	RXSTB[2]	LVTTL OUT
B12	OUTA1+	CML OUT	D15	RXMODE[1]	3-LEVEL SEL	J18	RXDB[0]	LVTTL OUT
B13	GND	GROUND	D16	VCC	POWER	J19	RXDB[5]	LVTTL OUT
B14	INA2+	CML IN	D17	$\overline{\text{BOND\_INH}}$	LVTTL IN PU	J20	RXDB[2]	LVTTL OUT
B15	OUTA2+	CML OUT	D18	RXLE	LVTTL IN PU	K01	RXDC[2]	LVTTL OUT
B16	VCC	POWER	D19	RFEN	LVTTL IN PD	K02	RXCLKC–	LVTTL OUT
B17	INB1+	CML IN	D20	$\overline{\text{MASTER}}$	LVTTL IN PD	K03	TXCTC[0]	LVTTL IN
B18	OUTB1+	CML OUT	E01	VCC	POWER	K04	$\overline{\text{LFIC}}$	LVTTL OUT
B19	INB2+	CML IN	E02	VCC	POWER	K17	RXDB[3]	LVTTL OUT
B20	OUTB2+	CML OUT	E03	VCC	POWER	K18	RXDB[4]	LVTTL OUT
C01	TDI	LVTTL IN PU	E04	VCC	POWER	K19	RXDB[7]	LVTTL OUT
C02	TMS	LVTTL IN PU	E17	VCC	POWER	K20	RXCLKB+	LVTTL I/O PD
C03	INSELC	LVTTL IN	E18	VCC	POWER	L01	RXDC[3]	LVTTL OUT

Table 22. Package Coordinate Signal Allocation (continued)

Ball ID	Signal Name	Signal Type
L02	RXCLKC+	LVTTL I/O PD
L03	TXCLKC	LVTTL IN PD
L04	TXDC[6]	LVTTL IN
L17	RXDB[6]	LVTTL OUT
L18	$\overline{\text{LFIB}}$	LVTTL OUT
L19	RXCLKB–	LVTTL I/O PD
L20	TXDB[6]	LVTTL IN
M01	RXDC[4]	LVTTL OUT
M02	RXDC[5]	LVTTL OUT
M03	RXDC[7]	LVTTL OUT
M04	RXDC[6]	LVTTL OUT
M17	TXCTB[1]	LVTTL IN
M18	TXCTB[0]	LVTTL IN
M19	TXDB[7]	LVTTL IN
M20	TXCLKB	LVTTL IN PD
N01	GND	GROUND
N02	GND	GROUND
N03	GND	GROUND
N04	GND	GROUND
N17	GND	GROUND
N18	GND	GROUND
N19	GND	GROUND
N20	GND	GROUND
P01	RXDC[1]	LVTTL OUT
P02	RXDC[0]	LVTTL OUT
P03	RXSTC[0]	LVTTL OUT
P04	RXSTC[1]	LVTTL OUT
P17	TXDB[5]	LVTTL IN
P18	TXDB[4]	LVTTL IN
P19	TXDB[3]	LVTTL IN
P20	TXDB[2]	LVTTL IN
R01	RXSTC[2]	LVTTL OUT
R02	RXOPC	LVTTL 3-S OUT
R03	TXPERD	LVTTL OUT
R04	TXOPD	LVTTL IN PU
R17	TXDB[1]	LVTTL IN
R18	TXDB[0]	LVTTL IN
R19	TXOPB	LVTTL IN PU
R20	TXPERB	LVTTL OUT
T01	VCC	POWER
T02	VCC	POWER
T03	VCC	POWER
T04	VCC	POWER
T17	VCC	POWER
T18	VCC	POWER
T19	VCC	POWER
T20	VCC	POWER
U01	TXDD[0]	LVTTL IN
U02	TXDD[1]	LVTTL IN
U03	TXDD[2]	LVTTL IN
U04	TXCTD[1]	LVTTL IN
U05	VCC	POWER
U06	RXDD[2]	LVTTL OUT
U07	RXDD[1]	LVTTL OUT
U08	GND	GROUND
U09	RXOPD	LVTTL 3-S OUT
U10	BOND_ALL	OPEN DR
U11	REFCLK–	PECL IN
U12	TXDA[1]	LVTTL IN
U13	GND	GROUND
U14	TXDA[4]	LVTTL IN
U15	TXCTA[0]	LVTTL IN
U16	VCC	POWER
U17	RXDA[2]	LVTTL OUT
U18	RXOPA	LVTTL OUT
U19	RXSTA[2]	LVTTL OUT
U20	RXSTA[1]	LVTTL OUT
V01	TXDD[3]	LVTTL IN
V02	TXDD[4]	LVTTL IN
V03	TXCTD[0]	LVTTL IN
V04	RXDD[6]	LVTTL OUT
V05	VCC	POWER
V06	RXDD[3]	LVTTL OUT
V07	RXSTD[0]	LVTTL OUT
V08	GND	GROUND
V09	RXSTD[2]	LVTTL OUT
V10	BONDST[0]	OPEN DR
V11	REFCLK+	PECL IN
V12	BONDST[1]	OPEN DR
V13	GND	GROUND
V14	TXDA[3]	LVTTL IN
V15	TXDA[7]	LVTTL IN
V16	VCC	POWER
V17	RXDA[7]	LVTTL OUT
V18	RXDA[3]	LVTTL OUT
V19	RXDA[0]	LVTTL OUT
V20	RXSTA[0]	LVTTL OUT
W01	TXDD[5]	LVTTL IN
W02	TXDD[7]	LVTTL IN
W03	$\overline{\text{LFID}}$	LVTTL OUT
W04	RXCLKD–	LVTTL OUT
W05	VCC	POWER
W06	RXDD[4]	LVTTL OUT
W07	RXSTD[1]	LVTTL OUT
W08	GND	GROUND
W09	TXCLKO–	LVTTL OUT
W10	$\overline{\text{TXRST}}$	LVTTL IN PU
W11	TXOPA	LVTTL IN PU
W12	SCSEL	LVTTL IN PD
W13	GND	GROUND
W14	TXDA[2]	LVTTL IN
W15	TXDA[6]	LVTTL IN
W16	VCC	POWER
W17	$\overline{\text{LFIA}}$	LVTTL OUT
W18	RXCLKA–	LVTTL OUT
W19	RXDA[4]	LVTTL OUT
W20	RXDA[1]	LVTTL OUT
Y01	TXDD[6]	LVTTL IN
Y02	TXCLKD	LVTTL IN
Y03	RXDD[7]	LVTTL OUT
Y04	RXCLKD+	LVTTL I/O PD
Y05	VCC	POWER
Y06	RXDD[5]	LVTTL OUT
Y07	RXDD[0]	LVTTL OUT
Y08	GND	GROUND
Y09	TXCLKO+	LVTTL OUT
Y10	N/C	NO CONNECT
Y11	TXCLKA	LVTTL IN PD
Y12	TXPERA	LVTTL OUT
Y13	GND	GROUND
Y14	TXDA[0]	LVTTL IN
Y15	TXDA[5]	LVTTL IN
Y16	VCC	POWER
Y17	TXCTA[1]	LVTTL IN
Y18	RXCLKA+	LVTTL I/O PD
Y19	RXDA[6]	LVTTL OUT
Y20	RXDA[5]	LVTTL OUT

X3.230 Codes and Notation Conventions

Information to be transmitted over a serial link is encoded eight bits at a time into a 10-bit Transmission Character and then sent serially, bit by bit. Information received over a serial link is collected ten bits at a time, and those Transmission Characters that are used for data characters are decoded into the correct eight-bit codes. The 10-bit Transmission Code supports all 256 8-bit combinations. Some of the remaining Transmission Characters (Special Characters) are used for functions other than data transmission.

The primary use of a Transmission Code is to improve the transmission characteristics of a serial link. The encoding defined by the Transmission Code ensures that sufficient transitions are present in the serial bit stream to make clock recovery possible at the Receiver. Such encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of information. In addition, some Special Characters of the Transmission Code selected by Fibre Channel Standard contain a distinct and easily recognizable bit pattern that assists the receiver in achieving character alignment on the incoming bit stream.

Notation Conventions

The documentation for the 8B/10B Transmission Code uses letter notation for the bits in an 8-bit byte. Fibre Channel Standard notation uses a bit notation of A, B, C, D, E, F, G, H for the 8-bit byte for the raw 8-bit data, and the letters a, b, c, d, e, i, f, g, h, j for encoded 10-bit data. There is a correspondence between bit A and bit a, B and b, C and c, D and d, E and e, F and f, G and g, and H and h. Bits i and j are derived, respectively, from (A,B,C,D,E) and (F,G,H).

The bit labeled A in the description of the 8B/10B Transmission Code corresponds to bit 0 in the numbering scheme of the FC-2 specification, B corresponds to bit 1, as shown below.

FC-2 bit designation—	7	6	5	4	3	2	1	0
HOTLink D/Q designation—	7	6	5	4	3	2	1	0
8B/10B bit designation—	H	G	F	E	D	C	B	A

To clarify this correspondence, the following example shows the conversion from an FC-2 Valid Data Byte to a Transmission Character.

```
FC-2  45H
      Bits: 7654 3210
            0100 0101
```

Converted to 8B/10B notation, note that the order of bits has been reversed):

```
Data Byte Name  D5.2
                Bits: ABCDE FGH
                      10100 010
```

Translated to a transmission Character in the 8B/10B Transmission Code:

```
                Bits: abcdei fghj
                      101001 0101
```

Each valid Transmission Character of the 8B/10B Transmission Code has been given a name using the following convention: cxx.y, where c is used to show whether the Transmission Character is a Data Character (c is set to D, and SC/D = LOW) or a Special Character (c is set to K, and SC/D = HIGH). When c is set to D, xx is the decimal value of the binary number composed of the bits E, D, C, B, and A in that order, and the y is the decimal value of the binary number composed of the bits H, G, and F in that order. When c is set to K, xx and y are derived by comparing the encoded bit patterns of the Special Character to those patterns derived from encoded Valid Data bytes and selecting the names of the patterns most similar to the encoded bit patterns of the Special Character.

Under the above conventions, the Transmission Character used for the examples above, is referred to by the name D5.2. The Special Character K29.7 is so named because the first six bits (abcdei) of this character make up a bit pattern similar to that resulting from the encoding of the unencoded 11101 pattern (29), and because the second four bits (fghj) make up a bit pattern similar to that resulting from the encoding of the unencoded 111 pattern (7).

NOTE: This definition of the 10-bit Transmission Code is based on the following references, which describe the same 10-bit transmission code.

A.X. Widmer and P.A. Franaszek. “A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code” IBM Journal of Research and Development, 27, No. 5: 440-451 (September, 1983).

U.S. Patent 4,486,739. Peter A. Franaszek and Albert X. Widmer. “Byte-Oriented DC Balanced (0.4) 8B/10B Partitioned Block Transmission Code” (December 4, 1984).

Fibre Channel Physical and Signaling Interface (ANS X3.230-1994 ANSI FC-PH Standard).

IBM Enterprise Systems Architecture/390 ESCON I/O Interface (document number SA22-7202).

8B/10B Transmission Code

The following information describes how the tables are used for both generating valid Transmission Characters (encoding) and checking the validity of received Transmission Characters (decoding). It also specifies the ordering rules to be followed when transmitting the bits within a character and the characters within any higher-level constructs specified by a standard.

Transmission Order

Within the definition of the 8B/10B Transmission Code, the bit positions of the Transmission Characters are labeled a, b, c, d, e, i, f, g, h, j. Bit “a” is transmitted first followed by bits b, c, d, e, i, f, g, h, and j in that order.

Note that bit i is transmitted between bit e and bit f, rather than in alphabetical order.

Valid and Invalid Transmission Characters

The following tables define the valid Data Characters and valid Special Characters (K characters), respectively. The tables are used for both generating valid Transmission Characters and checking the validity of received Transmission Characters. In the tables, each Valid-Data-byte or Special-Character-code entry has two columns that represent two Transmission Characters. The two columns correspond to the current value of the running disparity. Running disparity is a binary parameter with either a negative (–) or positive (+) value.

After powering on, the Transmitter may assume either a positive or negative value for its initial running disparity. Upon transmission of any Transmission Character, the transmitter will select the proper version of the Transmission Character based on the current running disparity value, and the Transmitter calculates a new value for its running disparity based on the contents of the transmitted character. Special Character

codes C1.7 and C2.7 can be used to force the transmission of a specific Special Character with a specific running disparity as required for some special sequences in X3.230.

After powering on, the Receiver may assume either a positive or negative value for its initial running disparity. Upon reception of any Transmission Character, the Receiver decides whether the Transmission Character is valid or invalid according to the following rules and tables and calculates a new value for its Running Disparity based on the contents of the received character.

The following rules for running disparity are used to calculate the new running-disparity value for Transmission Characters that have been transmitted and received.

Running disparity for a Transmission Character is calculated from sub-blocks, where the first six bits (abcdei) form one sub-block and the second four bits (fghj) form the other sub-block. Running disparity at the beginning of the 6-bit sub-block is the running disparity at the end of the previous Transmission Character. Running disparity at the beginning of the 4-bit sub-block is the running disparity at the end of the 6-bit sub-block. Running disparity at the end of the Transmission Character is the running disparity at the end of the 4-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

1. Running disparity at the end of any sub-block is positive if the sub-block contains more ones than zeros. It is also positive at the end of the 6-bit sub-block if the 6-bit sub-block is 000111, and it is positive at the end of the 4-bit sub-block if the 4-bit sub-block is 0011.
2. Running disparity at the end of any sub-block is negative if the sub-block contains more zeros than ones. It is also negative at the end of the 6-bit sub-block if the 6-bit sub-block is 111000, and it is negative at the end of the 4-bit sub-block if the 4-bit sub-block is 1100.
3. Otherwise, running disparity at the end of the sub-block is the same as at the beginning of the sub-block.

Use of the Tables for Generating Transmission Characters

The appropriate entry in *Table 25* for the Valid Data byte or *Table 26* for Special Character byte identify which Transmission Character is to be generated. The current value of the Transmitter's running disparity is used to select the Transmission Character from its corresponding column. For each Transmission Character transmitted, a new value of the running disparity is calculated. This new value is used as the Transmitter's current running disparity for the next Valid Data byte or Special Character byte to be encoded and transmitted. *Table 23* shows naming notations and examples of valid transmission characters.

Use of the Tables for Checking the Validity of Received Transmission Characters

The column corresponding to the current value of the Receiver's running disparity is searched for the received Transmission Character. If the received Transmission Character is found in the proper column, then the Transmission Character is valid and the associated Data byte or Special Character code is determined (decoded). If the received Transmission Character is not found in that column, then the Transmission Character is invalid. This is called a code violation. Independent of the Transmission Character's validity, the received Transmission Character is used to calculate a new value of running disparity. The new value is used as the Receiver's current running disparity for the next received Transmission Character.

Table 23. Valid Transmission Characters

Data			
	D_{IN} or Q_{OUT}		
Byte Name	765	43210	Hex Value
D0.0	000	00000	00
D1.0	000	00001	01
D2.0	000	00010	02
. .	. .	. .	. .
D5.2	010	00101	45
. .	. .	. .	. .
D30.7	111	11110	FE
D31.7	111	11111	FF

Detection of a code violation does not necessarily show that the Transmission Character in which the code violation was detected is in error. Code violations may result from a prior error that altered the running disparity of the bit stream which did not result in a detectable error at the Transmission Character in which the error occurred. *Table 24* shows an example of this behavior.

Table 24. Code Violations Resulting from Prior Errors

	RD	Character	RD	Character	RD	Character	RD
Transmitted data character	–	D21.1	–	D10.2	–	D23.5	+
Transmitted bit stream	–	101010 1001	–	010101 0101	–	111010 1010	+
Bit stream after error	–	101010 1011	+	010101 0101	+	111010 1010	+
Decoded data character	–	D21.0	+	D10.2	+	Code Violation	+

Table 25. Valid Data Characters (TXCTx[0] = 0, RXSTx[2:0] = 000)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.0	000 00000	100111 0100	011000 1011	D0.1	001 00000	100111 1001	011000 1001
D1.0	000 00001	011101 0100	100010 1011	D1.1	001 00001	011101 1001	100010 1001
D2.0	000 00010	101101 0100	010010 1011	D2.1	001 00010	101101 1001	010010 1001
D3.0	000 00011	110001 1011	110001 0100	D3.1	001 00011	110001 1001	110001 1001
D4.0	000 00100	110101 0100	001010 1011	D4.1	001 00100	110101 1001	001010 1001
D5.0	000 00101	101001 1011	101001 0100	D5.1	001 00101	101001 1001	101001 1001
D6.0	000 00110	011001 1011	011001 0100	D6.1	001 00110	011001 1001	011001 1001
D7.0	000 00111	111000 1011	000111 0100	D7.1	001 00111	111000 1001	000111 1001
D8.0	000 01000	111001 0100	000110 1011	D8.1	001 01000	111001 1001	000110 1001
D9.0	000 01001	100101 1011	100101 0100	D9.1	001 01001	100101 1001	100101 1001
D10.0	000 01010	010101 1011	010101 0100	D10.1	001 01010	010101 1001	010101 1001
D11.0	000 01011	110100 1011	110100 0100	D11.1	001 01011	110100 1001	110100 1001
D12.0	000 01100	001101 1011	001101 0100	D12.1	001 01100	001101 1001	001101 1001
D13.0	000 01101	101100 1011	101100 0100	D13.1	001 01101	101100 1001	101100 1001
D14.0	000 01110	011100 1011	011100 0100	D14.1	001 01110	011100 1001	011100 1001
D15.0	000 01111	010111 0100	101000 1011	D15.1	001 01111	010111 1001	101000 1001
D16.0	000 10000	011011 0100	100100 1011	D16.1	001 10000	011011 1001	100100 1001
D17.0	000 10001	100011 1011	100011 0100	D17.1	001 10001	100011 1001	100011 1001
D18.0	000 10010	010011 1011	010011 0100	D18.1	001 10010	010011 1001	010011 1001
D19.0	000 10011	110010 1011	110010 0100	D19.1	001 10011	110010 1001	110010 1001
D20.0	000 10100	001011 1011	001011 0100	D20.1	001 10100	001011 1001	001011 1001
D21.0	000 10101	101010 1011	101010 0100	D21.1	001 10101	101010 1001	101010 1001
D22.0	000 10110	011010 1011	011010 0100	D22.1	001 10110	011010 1001	011010 1001
D23.0	000 10111	111010 0100	000101 1011	D23.1	001 10111	111010 1001	000101 1001
D24.0	000 11000	110011 0100	001100 1011	D24.1	001 11000	110011 1001	001100 1001
D25.0	000 11001	100110 1011	100110 0100	D25.1	001 11001	100110 1001	100110 1001
D26.0	000 11010	010110 1011	010110 0100	D26.1	001 11010	010110 1001	010110 1001
D27.0	000 11011	110110 0100	001001 1011	D27.1	001 11011	110110 1001	001001 1001
D28.0	000 11100	001110 1011	001110 0100	D28.1	001 11100	001110 1001	001110 1001
D29.0	000 11101	101110 0100	010001 1011	D29.1	001 11101	101110 1001	010001 1001
D30.0	000 11110	011110 0100	100001 1011	D30.1	001 11110	011110 1001	100001 1001
D31.0	000 11111	101011 0100	010100 1011	D31.1	001 11111	101011 1001	010100 1001

Table 25. Valid Data Characters (TXCTx[0] = 0, RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.2	010 00000	100111 0101	011000 0101	D0.3	011 00000	100111 0011	011000 1100
D1.2	010 00001	011101 0101	100010 0101	D1.3	011 00001	011101 0011	100010 1100
D2.2	010 00010	101101 0101	010010 0101	D2.3	011 00010	101101 0011	010010 1100
D3.2	010 00011	110001 0101	110001 0101	D3.3	011 00011	110001 1100	110001 0011
D4.2	010 00100	110101 0101	001010 0101	D4.3	011 00100	110101 0011	001010 1100
D5.2	010 00101	101001 0101	101001 0101	D5.3	011 00101	101001 1100	101001 0011
D6.2	010 00110	011001 0101	011001 0101	D6.3	011 00110	011001 1100	011001 0011
D7.2	010 00111	111000 0101	000111 0101	D7.3	011 00111	111000 1100	000111 0011
D8.2	010 01000	111001 0101	000110 0101	D8.3	011 01000	111001 0011	000110 1100
D9.2	010 01001	100101 0101	100101 0101	D9.3	011 01001	100101 1100	100101 0011
D10.2	010 01010	010101 0101	010101 0101	D10.3	011 01010	010101 1100	010101 0011
D11.2	010 01011	110100 0101	110100 0101	D11.3	011 01011	110100 1100	110100 0011
D12.2	010 01100	001101 0101	001101 0101	D12.3	011 01100	001101 1100	001101 0011
D13.2	010 01101	101100 0101	101100 0101	D13.3	011 01101	101100 1100	101100 0011
D14.2	010 01110	011100 0101	011100 0101	D14.3	011 01110	011100 1100	011100 0011
D15.2	010 01111	010111 0101	101000 0101	D15.3	011 01111	010111 0011	101000 1100
D16.2	010 10000	011011 0101	100100 0101	D16.3	011 10000	011011 0011	100100 1100
D17.2	010 10001	100011 0101	100011 0101	D17.3	011 10001	100011 1100	100011 0011
D18.2	010 10010	010011 0101	010011 0101	D18.3	011 10010	010011 1100	010011 0011
D19.2	010 10011	110010 0101	110010 0101	D19.3	011 10011	110010 1100	110010 0011
D20.2	010 10100	001011 0101	001011 0101	D20.3	011 10100	001011 1100	001011 0011
D21.2	010 10101	101010 0101	101010 0101	D21.3	011 10101	101010 1100	101010 0011
D22.2	010 10110	011010 0101	011010 0101	D22.3	011 10110	011010 1100	011010 0011
D23.2	010 10111	111010 0101	000101 0101	D23.3	011 10111	111010 0011	000101 1100
D24.2	010 11000	110011 0101	001100 0101	D24.3	011 11000	110011 0011	001100 1100
D25.2	010 11001	100110 0101	100110 0101	D25.3	011 11001	100110 1100	100110 0011
D26.2	010 11010	010110 0101	010110 0101	D26.3	011 11010	010110 1100	010110 0011
D27.2	010 11011	110110 0101	001001 0101	D27.3	011 11011	110110 0011	001001 1100
D28.2	010 11100	001110 0101	001110 0101	D28.3	011 11100	001110 1100	001110 0011
D29.2	010 11101	101110 0101	010001 0101	D29.3	011 11101	101110 0011	010001 1100
D30.2	010 11110	011110 0101	100001 0101	D30.3	011 11110	011110 0011	100001 1100
D31.2	010 11111	101011 0101	010100 0101	D31.3	011 11111	101011 0011	010100 1100

Table 25. Valid Data Characters (TXCTx[0] = 0, RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.4	100 00000	100111 0010	011000 1101	D0.5	101 00000	100111 1010	011000 1010
D1.4	100 00001	011101 0010	100010 1101	D1.5	101 00001	011101 1010	100010 1010
D2.4	100 00010	101101 0010	010010 1101	D2.5	101 00010	101101 1010	010010 1010
D3.4	100 00011	110001 1101	110001 0010	D3.5	101 00011	110001 1010	110001 1010
D4.4	100 00100	110101 0010	001010 1101	D4.5	101 00100	110101 1010	001010 1010
D5.4	100 00101	101001 1101	101001 0010	D5.5	101 00101	101001 1010	101001 1010
D6.4	100 00110	011001 1101	011001 0010	D6.5	101 00110	011001 1010	011001 1010
D7.4	100 00111	111000 1101	000111 0010	D7.5	101 00111	111000 1010	000111 1010
D8.4	100 01000	111001 0010	000110 1101	D8.5	101 01000	111001 1010	000110 1010
D9.4	100 01001	100101 1101	100101 0010	D9.5	101 01001	100101 1010	100101 1010
D10.4	100 01010	010101 1101	010101 0010	D10.5	101 01010	010101 1010	010101 1010
D11.4	100 01011	110100 1101	110100 0010	D11.5	101 01011	110100 1010	110100 1010
D12.4	100 01100	001101 1101	001101 0010	D12.5	101 01100	001101 1010	001101 1010
D13.4	100 01101	101100 1101	101100 0010	D13.5	101 01101	101100 1010	101100 1010
D14.4	100 01110	011100 1101	011100 0010	D14.5	101 01110	011100 1010	011100 1010
D15.4	100 01111	010111 0010	101000 1101	D15.5	101 01111	010111 1010	101000 1010
D16.4	100 10000	011011 0010	100100 1101	D16.5	101 10000	011011 1010	100100 1010
D17.4	100 10001	100011 1101	100011 0010	D17.5	101 10001	100011 1010	100011 1010
D18.4	100 10010	010011 1101	010011 0010	D18.5	101 10010	010011 1010	010011 1010
D19.4	100 10011	110010 1101	110010 0010	D19.5	101 10011	110010 1010	110010 1010
D20.4	100 10100	001011 1101	001011 0010	D20.5	101 10100	001011 1010	001011 1010
D21.4	100 10101	101010 1101	101010 0010	D21.5	101 10101	101010 1010	101010 1010
D22.4	100 10110	011010 1101	011010 0010	D22.5	101 10110	011010 1010	011010 1010
D23.4	100 10111	111010 0010	000101 1101	D23.5	101 10111	111010 1010	000101 1010
D24.4	100 11000	110011 0010	001100 1101	D24.5	101 11000	110011 1010	001100 1010
D25.4	100 11001	100110 1101	100110 0010	D25.5	101 11001	100110 1010	100110 1010
D26.4	100 11010	010110 1101	010110 0010	D26.5	101 11010	010110 1010	010110 1010
D27.4	100 11011	110110 0010	001001 1101	D27.5	101 11011	110110 1010	001001 1010
D28.4	100 11100	001110 1101	001110 0010	D28.5	101 11100	001110 1010	001110 1010
D29.4	100 11101	101110 0010	010001 1101	D29.5	101 11101	101110 1010	010001 1010
D30.4	100 11110	011110 0010	100001 1101	D30.5	101 11110	011110 1010	100001 1010
D31.4	100 11111	101011 0010	010100 1101	D31.5	101 11111	101011 1010	010100 1010

Table 25. Valid Data Characters (TXCTx[0] = 0, RXSTx[2:0] = 000) (continued)

Data Byte Name	Bits	Current RD–	Current RD+	Data Byte Name	Bits	Current RD–	Current RD+
	HGF EDCBA	abcdei fghj	abcdei fghj		HGF EDCBA	abcdei fghj	abcdei fghj
D0.6	110 00000	100111 0110	011000 0110	D0.7	111 00000	100111 0001	011000 1110
D1.6	110 00001	011101 0110	100010 0110	D1.7	111 00001	011101 0001	100010 1110
D2.6	110 00010	101101 0110	010010 0110	D2.7	111 00010	101101 0001	010010 1110
D3.6	110 00011	110001 0110	110001 0110	D3.7	111 00011	110001 1110	110001 0001
D4.6	110 00100	110101 0110	001010 0110	D4.7	111 00100	110101 0001	001010 1110
D5.6	110 00101	101001 0110	101001 0110	D5.7	111 00101	101001 1110	101001 0001
D6.6	110 00110	011001 0110	011001 0110	D6.7	111 00110	011001 1110	011001 0001
D7.6	110 00111	111000 0110	000111 0110	D7.7	111 00111	111000 1110	000111 0001
D8.6	110 01000	111001 0110	000110 0110	D8.7	111 01000	111001 0001	000110 1110
D9.6	110 01001	100101 0110	100101 0110	D9.7	111 01001	100101 1110	100101 0001
D10.6	110 01010	010101 0110	010101 0110	D10.7	111 01010	010101 1110	010101 0001
D11.6	110 01011	110100 0110	110100 0110	D11.7	111 01011	110100 1110	110100 1000
D12.6	110 01100	001101 0110	001101 0110	D12.7	111 01100	001101 1110	001101 0001
D13.6	110 01101	101100 0110	101100 0110	D13.7	111 01101	101100 1110	101100 1000
D14.6	110 01110	011100 0110	011100 0110	D14.7	111 01110	011100 1110	011100 1000
D15.6	110 01111	010111 0110	101000 0110	D15.7	111 01111	010111 0001	101000 1110
D16.6	110 10000	011011 0110	100100 0110	D16.7	111 10000	011011 0001	100100 1110
D17.6	110 10001	100011 0110	100011 0110	D17.7	111 10001	100011 0111	100011 0001
D18.6	110 10010	010011 0110	010011 0110	D18.7	111 10010	010011 0111	010011 0001
D19.6	110 10011	110010 0110	110010 0110	D19.7	111 10011	110010 1110	110010 0001
D20.6	110 10100	001011 0110	001011 0110	D20.7	111 10100	001011 0111	001011 0001
D21.6	110 10101	101010 0110	101010 0110	D21.7	111 10101	101010 1110	101010 0001
D22.6	110 10110	011010 0110	011010 0110	D22.7	111 10110	011010 1110	011010 0001
D23.6	110 10111	111010 0110	000101 0110	D23.7	111 10111	111010 0001	000101 1110
D24.6	110 11000	110011 0110	001100 0110	D24.7	111 11000	110011 0001	001100 1110
D25.6	110 11001	100110 0110	100110 0110	D25.7	111 11001	100110 1110	100110 0001
D26.6	110 11010	010110 0110	010110 0110	D26.7	111 11010	010110 1110	010110 0001
D27.6	110 11011	110110 0110	001001 0110	D27.7	111 11011	110110 0001	001001 1110
D28.6	110 11100	001110 0110	001110 0110	D28.7	111 11100	001110 1110	001110 0001
D29.6	110 11101	101110 0110	010001 0110	D29.7	111 11101	101110 0001	010001 1110
D30.6	110 11110	011110 0110	100001 0110	D30.7	111 11110	011110 0001	100001 1110
D31.6	110 11111	101011 0110	010100 0110	D31.7	111 11111	101011 0001	010100 1110

Table 26. Valid Special Character Codes and Sequences (TXCTx = special character code or RXSTx[2:0] = 001)[37, 38]

S.C. Code Name	S.C. Byte Name (Cypress)[39]		Bits HGF EDCBA (Cypress)	S.C. Byte Name (Alternate)[39]		Bits HGF EDCBA (Alternate)	Current RD– abcdei fghj	Current RD+ abcdei fghj
K28.0	C0.0	(C00)	000 00000	C28.0	(C1C)	000 11100	001111 0100	110000 1011
K28.1[40]	C1.0	(C01)	000 00001	C28.1	(C3C)	001 11100	001111 1001	110000 0110
K28.2[40]	C2.0	(C02)	000 00010	C28.2	(C5C)	010 11100	001111 0101	110000 1010
K28.3	C3.0	(C03)	000 00011	C28.3	(C7C)	011 11100	001111 0011	110000 1100
K28.4[40]	C4.0	(C04)	000 00100	C28.4	(C9C)	100 11100	001111 0010	110000 1101
K28.5[40, 41]	C5.0	(C05)	000 00101	C28.5	(CBC)	101 11100	001111 1010	110000 0101
K28.6[40]	C6.0	(C06)	000 00110	C28.6	(CDC)	110 11100	001111 0110	110000 1001
K28.7[40, 42]	C7.0	(C07)	000 00111	C28.7	(CFC)	111 11100	001111 1000	110000 0111
K23.7	C8.0	(C08)	000 01000	C23.7	(CF7)	111 10111	111010 1000	000101 0111
K27.7	C9.0	(C09)	000 01001	C27.7	(CFB)	111 11011	110110 1000	001001 0111
K29.7	C10.0	(C0A)	000 01010	C29.7	(CFD)	111 11101	101110 1000	010001 0111
K30.7	C11.0	(C0B)	000 01011	C30.7	(CFE)	111 11110	011110 1000	100001 0111
End of Frame Sequence								
EOFxx [43]	C2.1	(C22)	001 00010	C2.1	(C22)	001 00010	–K28.5, Dn.xxx0	+K28.5, Dn.xxx1
Code Rule Violation and SVS Tx Pattern								
Exception[42, 44]	C0.7	(CE0)	111 00000	C0.7	(CE0)	111 00000 [48]	100111 1000	011000 0111
–K28.5[45]	C1.7	(CE1)	111 00001	C1.7	(CE1)	111 00001 [48]	001111 1010	001111 1010
+K28.5[46]	C2.7	(CE2)	111 00010	C2.7	(CE2)	111 00010 [48]	110000 0101	110000 0101
Running Disparity Violation Pattern								
Exception[47]	C4.7	(CE4)	111 00100	C4.7	(CE4)	111 00100 [48]	110111 0101	001000 1010

Notes:

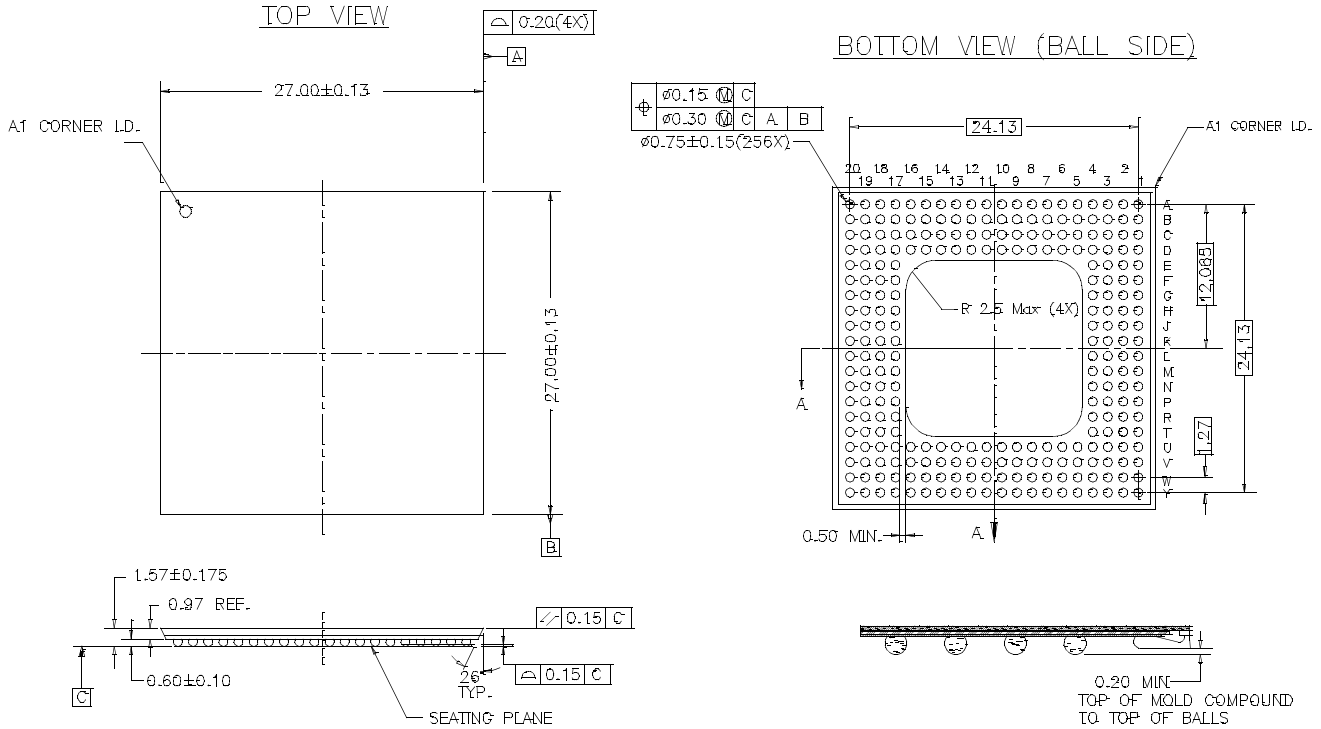
37. All codes not shown are reserved.
38. Notation for Special Character Code Name is consistent with Fibre Channel and ESCON naming conventions. Special Character Code Name is intended to describe binary information present on I/O pins. Common usage for the name can either be in the form used for describing Data patterns (i.e., C0.0 through C31.7), or in hex notation (i.e., Cnn where nn = the specified value between 00 and FF).
39. Both the Cypress and alternate encodings may be used for data transmission to generate specific Special Character Codes. The decoding process for received characters generates Cypress codes or Alternate codes as selected by the DECMODE configuration input.
40. These characters are used for control of ESCON interfaces. They can be sent as embedded commands or other markers when not operating using ESCON protocols.
41. The K28.5 character is used for framing operations by the receiver. It is also the pad or fill character transmitted to maintain the serial link when no user data is available.
42. Care must be taken when using this Special Character code. When a C7.0 is followed by a D11.x or D20.x, or when an SVS (C0.7) is followed by a D11.x, an alias K28.5 sync character is created. These sequences can cause erroneous framing and should be avoided while RFEN = HIGH.
43. C2.1 = Transmit either –K28.5+ or +K28.5– as determined by Current RD and modify the Transmission Character that follows, by setting its least significant bit to 1 or 0. If Current RD at the start of the following character is plus (+) the LSB is set to 0, and if Current RD is minus (–) the LSB becomes 1. This modification allows construction of X3.230 “EOF” frame delimiters wherein the second data byte is determined by the Current RD.
    For example, to send “EOFdt” the controller could issue the sequence C2.1–D21.4– D21.4–D21.4, and the HOTLink IITransmitter will send either K28.5–D21.4–D21.4–D21.4 or K28.5–D21.5– D21.4–D21.4 based on Current RD. Likewise to send “EOFdti” the controller could issue the sequence C2.1–D10.4–D21.4–D21.4, and the HOTLink II Transmitter will send either K28.5–D10.4–D21.4– D21.4 or K28.5–D10.5–D21.4– D21.4 based on Current RD.
    The receiver will never output this Special Character, since K28.5 is decoded as C5.0, C1.7, or C2.7, and the subsequent bytes are decoded as data.
44. C0.7 = Transmit a deliberate code rule violation. The code chosen for this function follows the normal Running Disparity rules. The receiver will only output this Special Character if the Transmission Character being decoded is not found in the tables.
45. C1.7 = Transmit Negative K28.5 (–K28.5+) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C1.7 if –K28.5 is received with RD+, otherwise K28.5 is decoded as C5.0 or C2.7.
46. C2.7 = Transmit Positive K28.5 (+K28.5–) disregarding Current RD. The receiver will only output this Special Character if K28.5 is received with the wrong running disparity. The receiver will output C2.7 if +K28.5 is received with RD–, otherwise K28.5 is decoded as C5.0 or C1.7.
47. C4.7 = Transmit a deliberate code rule violation to indicate a Running Disparity violation. The receiver will only output this Special Character if the Transmission Character being decoded is found in the tables, but Running Disparity does not match. This might indicate that an error occurred in a prior byte.
48. Supported only for data transmission. The receive status for these conditions will be reported by specific combinations of receive status bits.

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
Standard	CYP15G0401DXA-BGC	BL256	256-Ball Thermally Enhanced Ball Grid Array	Commercial
Standard	CYP15G0401DXA-BGI	BL256	256-Ball Thermally Enhanced Ball Grid Array	Industrial

Package Diagram

256-Lead L2 Ball Grid Array (27 x 27 x 1.57 mm) BL256



51-85123-*E

Revision History

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REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	117225	08/21/02	AMV	New Data Sheet