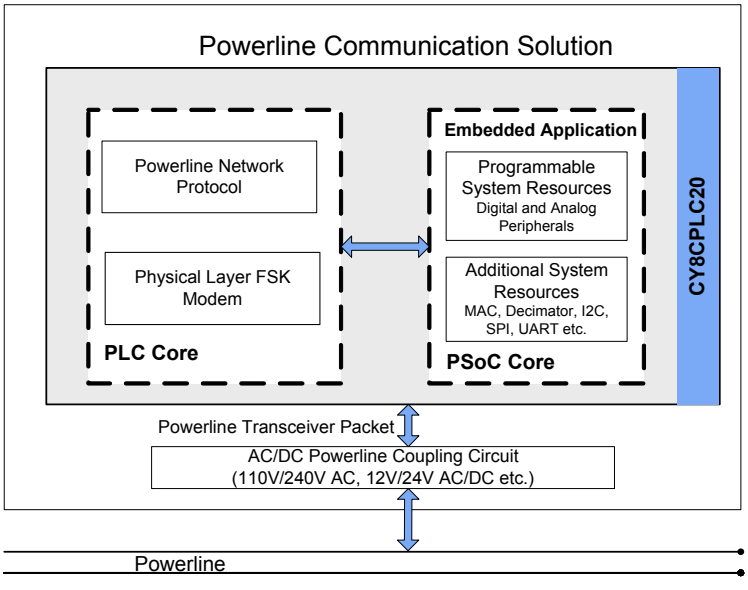
CY8CPLC20

Powerline Communication Solution

Features

- Powerline Communication Solution
  - Integrated Powerline Modem PHY
  - Frequency Shift Keying Modulation
  - Configurable baud rates up to 2400 bps
  - Powerline Optimized Network Protocol
  - Integrates Data Link, Transport, and Network Layers
  - Supports Bidirectional Half Duplex Communication
  - 8-bit CRC Error Detection to Minimize Data Loss
  - I^2C enabled Powerline Application Layer
  - Supports I^2C Frequencies of 50, 100, and 400 kHz
  - Reference Designs for 110V/240V AC and 12V/24V AC/DC Powerlines
  - Reference Designs comply with CENELEC EN 50065-1:2001 and FCC Part 15
- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - Two 8x8 Multiply, 32-Bit Accumulate
- Programmable System Resources (PSoC® Blocks)
  - 12 Rail-to-Rail Analog PSoC Blocks provide:
    - Up to 14-Bit ADCs
    - Up to 9-Bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
  - 16 Digital PSoC Blocks provide:
    - 8 to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Up to Four Full Duplex UARTs
    - Multiple SPI™ Masters or Slaves
    - Connectable to all GPIO Pins
  - Complex Peripherals by Combining Blocks
- Flexible On-Chip Memory
  - 32 KB Flash Program Storage 50,000 Erase or Write Cycles
  - 2 KB SRAM Data Storage
  - EEPROM Emulation in Flash
- Programmable Pin Configurations
  - 25 mA Sink, 10 mA Source on all GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - Up to 12 Analog Inputs on GPIO
  - Configurable Interrupt on all GPIO
- Additional System Resources
  - I^2C Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - Full Featured In-Circuit Emulator (ICE) and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128 KB Trace Memory
  - Complex Events
  - C Compilers, Assembler, and Linker

Logic Block Diagram



1. PLC Functional Overview

The CY8CPLC20 is an integrated Powerline Communication (PLC) chip with the Powerline Modem PHY and Network Protocol Stack running on the same device. Apart from the PLC core, the CY8CPLC20 also offers Cypress's revolutionary PSoC technology that enables system designers to integrate multiple functions on the same chip.

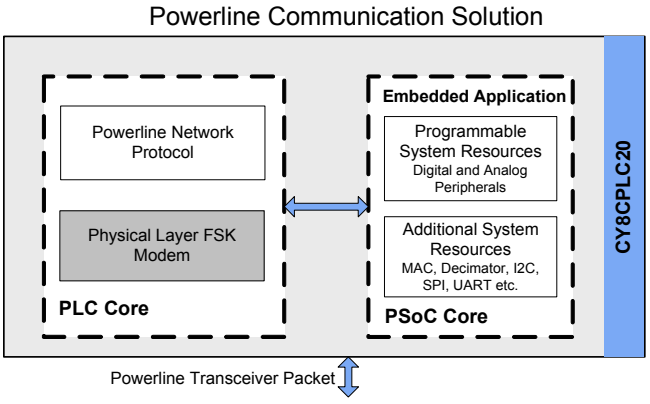
1.1 Robust Communication using Cypress's PLC Solution

Powerlines are available everywhere in the world and are a widely available communication medium for PLC technology. The pervasiveness of powerlines also makes it difficult to predict the characteristics and operation of PLC products. Because of the variable quality of powerlines around the world, implementing robust communication has been an engineering challenge for years. The Cypress PLC solution enables secure and reliable communications. Cypress PLC features that enable robust communication over powerlines include:

- Integrated Powerline PHY modem with optimized filters and amplifiers to work with lossy high voltage and low voltage powerlines.
- Powerline optimized network protocol that supports bidirectional communication with acknowledgement-based signaling. In case of data packet loss due to bursty noise on the powerline, the transmitter has the capability to retransmit data.
- The Powerline Network Protocol also supports an 8-bit CRC for error detection and data packet retransmission.
- A Carrier Sense Multiple Access (CSMA) scheme is built into the network protocol that minimizes collisions between packet transmissions on the powerline and supports multiple masters and reliable communication on a bigger network.

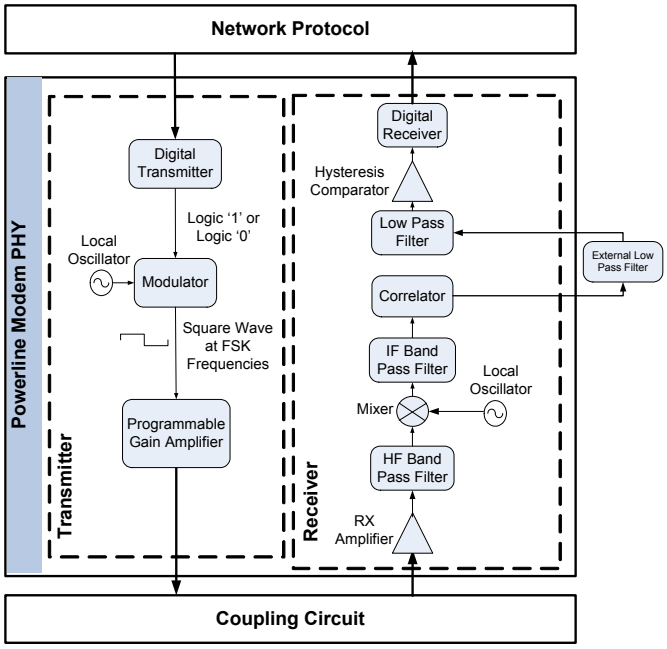
1.2 Powerline Modem PHY

Figure 1-1. Physical Layer FSK Modem



The physical layer of the Cypress PLC solution is implemented using an FSK modem that enables half duplex communication on any high voltage and low voltage powerline. This modem supports raw data rates up to 2400 bps. A block diagram is shown in Figure 1-2.

Figure 1-2. Physical Layer FSK Modem Block Diagram



1.2.1 Transmitter Section

Digital data from the network layer is serialized by the digital transmitter and fed as input to the modulator. The modulator divides the local oscillator frequency by a definite factor depending on whether the input data is high level logic '1' or low level logic '0'. It then generates a square wave at 133.3 kHz (logic '0') or 131.8 kHz (logic '1'), which is fed to the Programmable Gain Amplifier to generate FSK modulated signals. This enables tunable amplification of the signal depending on the noise in the channel. The logic '1' frequency can also be configured as 130.4 kHz for wider FSK deviation.

1.2.2 Receiver Section

The incoming FSK signal from the powerline is input to a high frequency (HF) band pass filter that filters out-of-band frequency components and outputs a filtered signal within the desired spectrum of 125 kHz to 140 kHz for further demodulation. The mixer block multiplies the filtered FSK signals with a locally generated signal to produce heterodyned frequencies.

The intermediate frequency (IF) band pass filters further remove out-of-band noise as required for further demodulation. This signal is fed to the correlator, which produces a DC component (consisting of logic '1' and '0') and a higher frequency component.

The output of the correlator is fed to a low pass filter (LPF) that outputs only the demodulated digital data at 2400 baud and suppresses all other higher frequency components generated in the correlation process. The output of the LPF is digitized by the hysteresis comparator. This eliminates the effects of correlator delay and false logic triggers due to noise. The digital receiver deserializes this data and outputs to the network layer for interpretation.

1.2.3 Coupling Circuit Reference Design

The coupling circuit couples low voltage signals from the CY8CPLC20 to the powerline. The topology of this circuit is determined by the voltage on the powerline and design constraints mandated by powerline usage regulations.

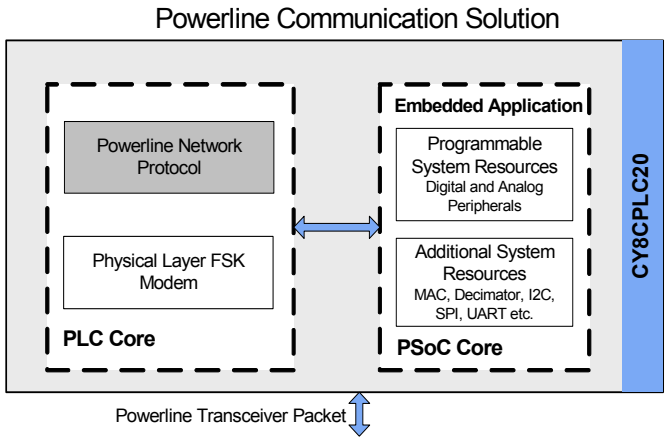
Cypress provides reference designs for a range of powerline voltages including 110V/240V AC and 12V/24V AC/DC. The CY8CPLC20 is capable of data communication over other AC/DC Powerlines as well with the appropriate external coupling circuit. The 110V AC and 240V AC designs are compliant to the following powerline usage regulations:

- FCC Part 15 for North America
- EN 50065-1:2001 for Europe

1.3 Network Protocol

Cypress's powerline optimized network protocol performs the functions of the data link and network layers in an ISO/OSI-equivalent model.

Figure 1-3. Powerline Network Protocol



The network protocol implemented on the CY8CPLC20 supports the following features:

- Bidirectional half-duplex communication
- Master-slave or peer-to-peer network topologies
- Multiple masters on powerline network
- 8-bit logical addressing supports up to 256 powerline nodes
- 16-bit extended logical addressing supports up to 65536 powerline nodes
- 64-bit physical addressing supports up to 2^{64} powerline nodes
- Individual, broadcast or group mode addressing
- Carrier Sense Multiple Access (CSMA)
- Full control over transmission parameters
  - Acknowledged
  - Unacknowledged
  - Repeated Transmit

1.3.1 CSMA and Timing Parameters

- CSMA – The protocol provides the random selection of a period between 85 and 115 ms (out of seven possible values in this range) in which the Band-In-Use (BIU) detector must indicate that the line is not in use, before attempting a transmission.
- BIU – A Band-In-Use detector, as defined under CENELEC EN 50065-1, is active whenever a signal that exceeds 86 dBmVrms anywhere in the range 131.5 kHz to 133.5 kHz is present for at least 4 ms. This threshold can be configured for different end-system applications not requiring CENELEC compliance.The modem tries to retransmit after every 85 to 115 ms when the band is in use. The transmitter times out after 1.1 seconds to 3 seconds (depending on the noise on the Powerline) and generates an interrupt to indicate that the transmitter was unable to acquire the powerline.

1.3.2 Powerline Transceiver Packet

The powerline network protocol defines a Powerline Transceiver (PLT) packet structure, which is used for data transfer between nodes across the powerline. Packet formation and data transmission across the powerline network are implemented internally in CY8CPLC20.

A PLT packet is divided into a variable length header (minimum 6 bytes to maximum 20 bytes, depending on address type), a variable length payload (minimum 0 bytes to maximum 31 bytes), and a packet CRC byte.

This packet (preceded by a one byte preamble "0xAB") is then transmitted by the powerline modem PHY and the external coupling circuit across the powerline.

The format of the PLT packet is shown in Table 1-1 on page 4.

Table 1-1. Powerline Transceiver (PLT) Packet Structure

Byte Offset	Bit Offset							
	7	6	5	4	3	2	1	0
0x00	SA Type	DA Type		Service Type	RSVD	RSVD	Response	RSVD
0x01	Destination Address (8-Bit Logical, 16-Bit Extended Logical or 64-Bit Physical)							
0x02	Source Address (8-Bit Logical, 16-Bit Extended Logical or 64-Bit Physical)							
0x03	Command							
0x04	RSVD			Payload Length				
0x05	Seq Num				Powerline Packet Header CRC			
0x06	Payload (0 to 31 Bytes)							
	Powerline Transceiver Packet CRC							

1.3.3 Packet Header

The packet header contains the first 6 bytes of the packet when 1-byte logical addressing is used. When 8-byte physical addressing is used, the source and destination addresses each contain 8 bytes. In this case, the header can consist of a maximum of 20 bytes. Unused fields marked RSVD are for future expansion and are transmitted as bit 0. Table 1-2 describes the PLT packet header fields in detail.

Table 1-2. Powerline Transceiver (PLT) Packet Header

Field Name	No. of Bits	Tag	Description
SA Type	1	Source Address Type	0 – Logical Addressing 1 – Physical Addressing
DA Type	2	Destination Address Type	00 – Logical Addressing 01 – Group Addressing 10 – Physical Addressing 11 – Invalid
Service Type	1		0 – Unacknowledged Messaging 1 – Acknowledged Messaging
Response	1	Response	0 - Not an acknowledgement or response packet 1 - Acknowledgement or response packet
Seq Num	4	Sequence Number	4-bit unique identifier for each packet between source and destination.
Header CRC	4		4-bit CRC value. This enables the receiver to suspend receiving the rest of the packet if its header is corrupted

1.3.4 Payload

The packet payload has a length of 0 to 31 bytes. Payload content is user defined and can be read or written through I^2C.

1.3.5 Packet CRC

The last byte of the packet is an 8-bit CRC value used to check packet data integrity. This CRC calculation includes the header and payload portions of the packet and is in addition to the powerline packet header CRC.

1.3.6 Sequence Numbering

The sequence number is increased for every new unique packet transmitted. If in acknowledged mode and an acknowledgment is not received for a given packet, that packet is re-transmitted (if TX_Retry > 0) with the same sequence number. If in unacknowledged mode, the packet is transmitted (TX_Retry + 1) times with the same sequence number.

If the receiver receives consecutive packets from the same source address with the same sequence number and packet CRC, it does not notify the host of the reception of the duplicate packet. If in acknowledged mode, it still sends an acknowledgment so that the transmitter knows that the packet was received.

1.3.7 Addressing

The CY8CPLC20 has three modes of addressing:

- Logical addressing: Every CY8CPLC20 node can have either a 8-bit logical address or a 16-bit logical address. The logical address of the PLC Node is set by the local application or by a remote node on the Powerline.
- Physical addressing: Every CY8CPLC20 has a unique 64-bit physical address.
- Group addressing: This is explained in the next section.

1.3.8 Group Membership

Group membership enables the user to multicast messages to select groups. The CY8CPLC20 supports two types of group addressing:

- Single Group Membership – The network protocol supports up to 256 different groups on the network in this mode. In this mode, each PLC node can only be part of a single group. For example, multiple PLC nodes can be part of Group 131.
- Multiple Group Membership – The network protocol supports eight different groups in this mode and each PLC node can be a part of multiple groups. For example, a single PLC node can be a part of Group 3, Group 4, and Group 7 at the same time.

Both these membership modes can also be used together for group membership. For example, a single PLC node can be a part of Group 131 and also multiple groups such as Group 3, Group 4, and Group 7.

The group membership ID for broadcasting messages to all nodes in the network is 0x00.

The service type is always set to Unacknowledgment Mode in Group Addressing Mode. This is to avoid acknowledgment flooding on the powerline during multicast.

1.3.9 Remote Commands

In addition to sending normal data over the Powerline, the CY8CPLC10 can also send (and request) control information to (and from) another node on the network. The type of remote command to transmit is set by the TX_CommandID register and when received, is stored in the RX_CommandID register.

When a control command (Command ID = 0x01-0x08 and 0x0C-0x0F) is received, the protocol automatically processes the packet (if Lock_Configuration is '0'), responds to the initiator, and notifies the host of the successful transmission and reception.

When the send data command (ID 0x09) or request for data command (ID 0x0A) is received, the protocol replies with an acknowledgment packet (if TX_Service_Type = '1'), and notify the host of the new received data. If the initiator doesn't receive the acknowledgment packet within 500ms, it notifies the host of the no acknowledgment received condition.

When a response command (ID 0x0B) is received by the initiator within 1.5s of sending the request for data command, the protocol notifies the host of the successful transmission and reception. If the response command is not received by the initiator within 1.5s, it notifies the host of the no response received condition.

The host is notified by updating the appropriate values in the INT_Status register (including Status_Value_Change).

The command IDs 0x30-0xff can be used for custom commands that would be processed by the external host (e.g. set an LED color, get a temperature/voltage reading).

The available remote commands are described in Table 1-3 with the respective Command IDs.

Table 1-3. Remote Commands

Cmd ID	Command Name	Description	Payload (TX Data)	Response (RX Data)
0x01	SetRemote_TXEnable	Sets the TX Enable bit in the PLC Mode Register. Rest of the PLC Mode register is unaffected	0 - Disable Remote TX 1 - Enable Remote TX	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x03	SetRemote_ExtendedAddr	Set the Addressing to Extended Addressing Mode	0 - Disable Extended Addressing 1 - Enable Extended Addressing	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x04	SetRemote_LogicalAddr	Assigns the specified logical address to the remote PLC node	If Ext Address = 0, Payload = 8-bit Logical Address If Ext Address = 1, Payload = 16-bit Logical Address	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x05	GetRemote_LogicalAddr	Get the Logical Address of the remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, {If Ext Address = 0, Response = 8-bit Logical Address If Ext Address = 1, Response = 16-bit Logical Address}
0x06	GetRemote_PhysicalAddr	Get the Physical Address of the remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = 64-bit Physical Address
0x07	GetRemote_State	Request PLC_Mode Register content from a Remote PLC node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = Remote PLC Mode register
0x08	GetRemote_Version	Get the Version Number of the Remote Node	None	If TX Enable = 0, Response = None If TX Enable = 1, Response = Remote Version register
0x09	SendRemote_Data	Transmit data to a Remote Node.	Payload = Local TX Data	If Local Service Type = 0, Response = None If Local Service Type = 1, Response = Ack

Table 1-3. Remote Commands (continued)

Cmd ID	Command Name	Description	Payload (TX Data)	Response (RX Data)
0x0A	RequestRemote_Data	Request data from a Remote Node	Payload = Local TX Data	If Local Service Type = 1, Response = Ack Then, the remote node host must send a ResponseRemote_Data command. The response must be completely transmitted within 1.5s of receiving the request. Otherwise, the requesting node will time out.
0x0B	ResponseRemote_Data	Transmit response data to a Remote Node.	Payload = Local TX Data	None
0x0C	SetRemote_BIU	Enables/Disables BIU functionality at the remote node	0 - Enable Remote BIU 1 - Disable Remote BIU	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0D	SetRemote_ThresholdValue	Sets the Threshold Value at the Remote node	3-bit Remote Threshold Value	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0E	SetRemote_GroupMembership	Sets the Group Membership of the Remote node	Byte0 - Remote SIngle Group Membership Address Byte1- Remote Multiple Group Membership Address	If Remote Lock Config = 0, Response = 00 (Success) If Remote Lock Config = 1, Response = 01 (Denied)
0x0F	GetRemote_GroupMembership	Gets the Group Membership of the Remote node	None	If Remote TX Enable = 0, Response = None If Remote TX Enable = 1, Response = Byte0 - Remote SIngle Group Membership Address Byte1- Remote Multiple Group Membership Address
0x10 - 0x2F	Reserved			
0x30 - 0xFF	User Defined Command Set			

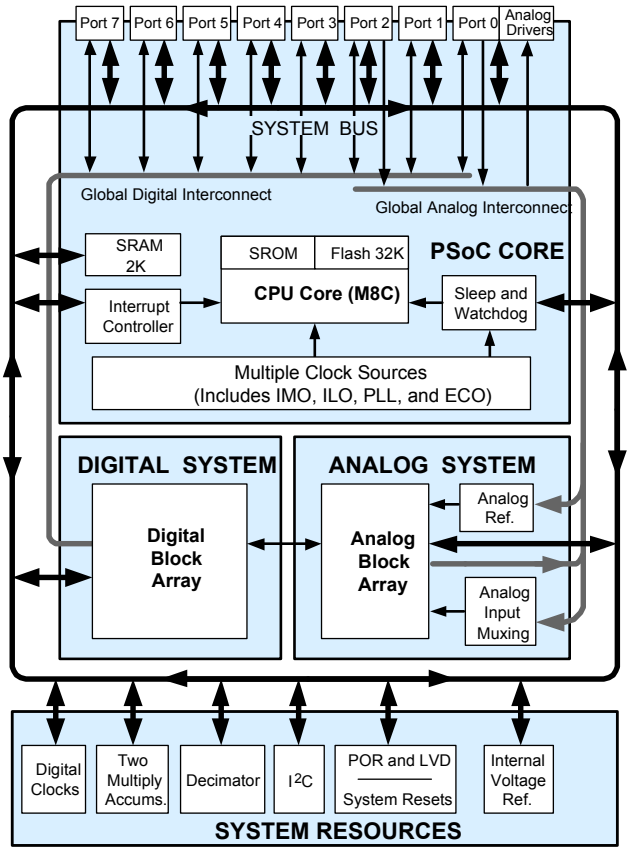
2. PSoC Core

The CY8CPLC20 is based on the Cypress PSoC® 1 architecture. The PSoC platform consists of many *Programmable System-on-chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/Os are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in Figure 2-1., consists of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing enables all the device resources to be combined into a complete custom system. The CY8CPLC20 family can have up to five I/O ports that connect to the global digital and analog interconnects, providing access to 16 digital blocks and 12 analog blocks.

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose I/O).

Figure 2-1. PSoC Core



The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a 4 MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with 25 vectors, to simplify programming of realtime embedded events. Program execution is timed and protected using the included Sleep and Watchdog timers (WDT).

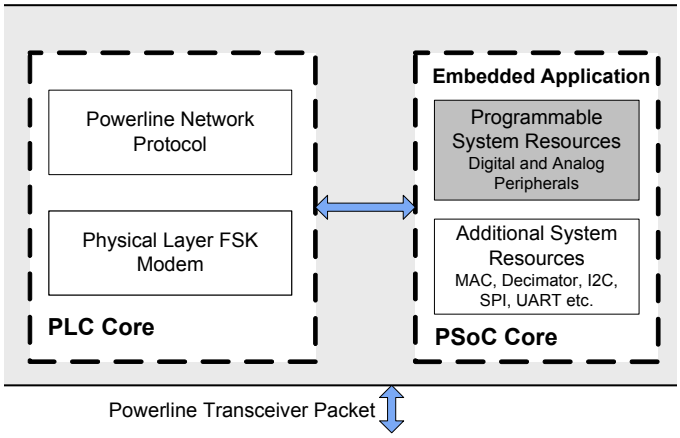
Memory encompasses 32 KB of Flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using Flash. Program Flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for the digital system use. A low power 32 kHz ILO (internal low speed oscillator) is provided for the sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. When operating the Powerline Transceiver (PLT) user module, the ECO must be selected to ensure accurate protocol timing. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

2.1 Programmable System Resources

Figure 2-2. Programmable System Resources



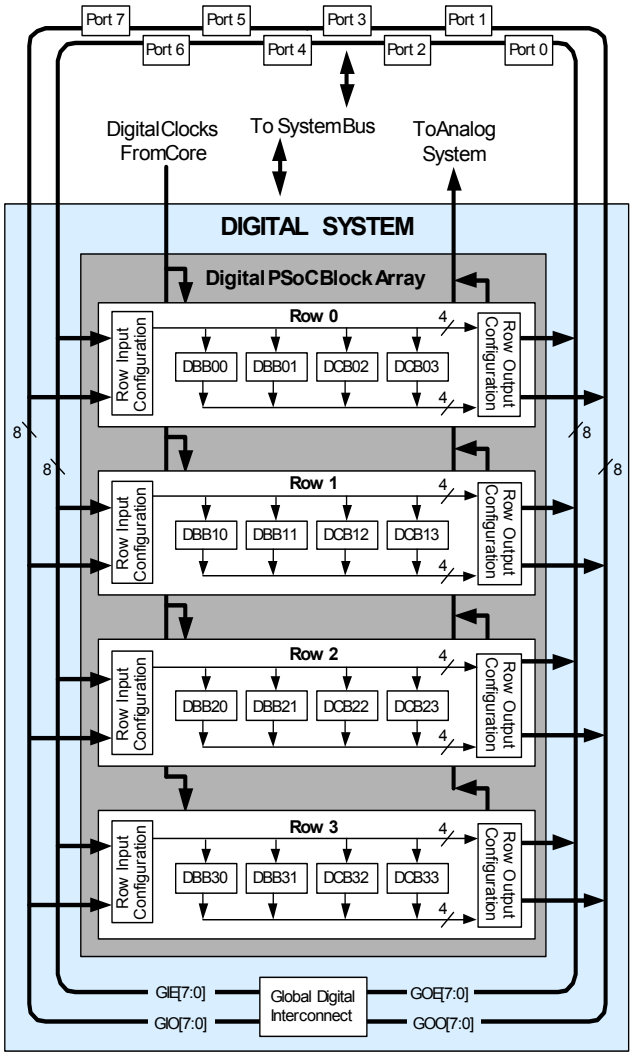
2.1.1 The Digital System

The digital system contains 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone, or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals called user module references. Digital peripheral configurations include:

- PWMs (8 to 32 bit)
- PWMs with Dead Band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to four)
- SPI master and slave (up to four each)
- I^2C slave and multi-master (one available as a System Resource)
- Cyclical Redundancy Checker and Generator (8 to 32 bit)
- IrDA (up to four)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and perform logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Figure 2-3. Digital System Block Diagram



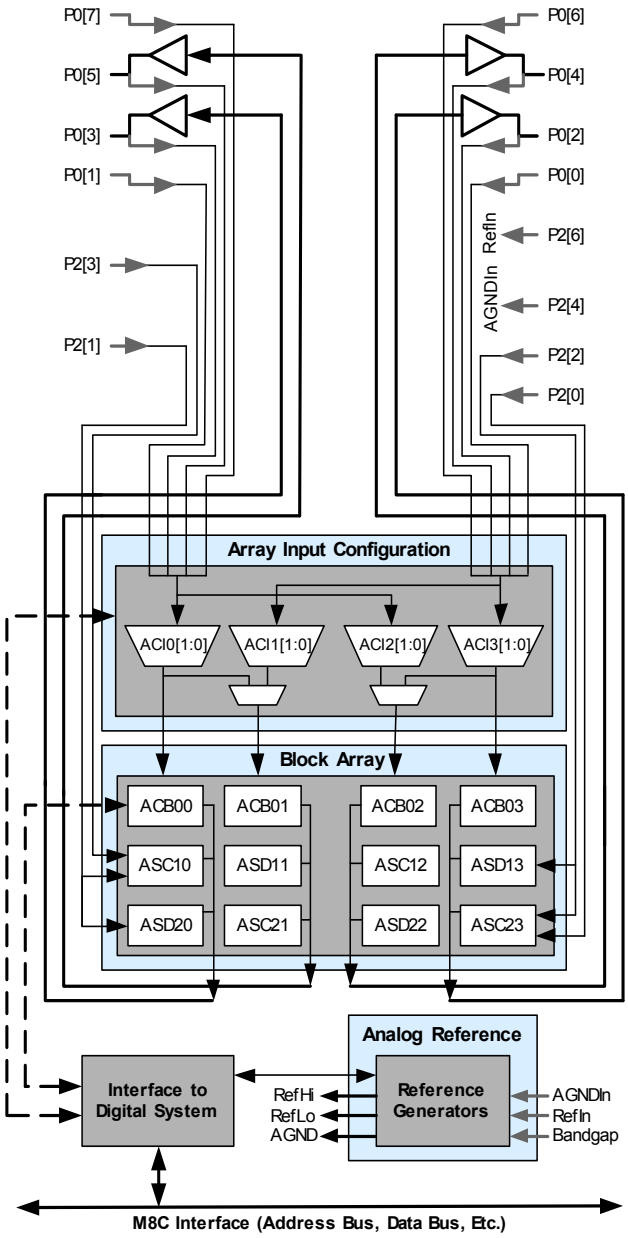
2.1.2 The Analog System

The analog system contains 12 configurable blocks, each containing an opamp circuit, enabling the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to four, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band pass, low pass, and notch)
- Amplifiers (up to four, with selectable gain to 48x)
- Instrumentation amplifiers (up to two, with selectable gain to 93x)
- Comparators (up to four, with 16 selectable thresholds)
- DACs (up to four, with 6- to 9-bit resolution)
- Multiplying DACs (up to four, with 6- to 9-bit resolution)
- High current output drivers (4 with 40 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

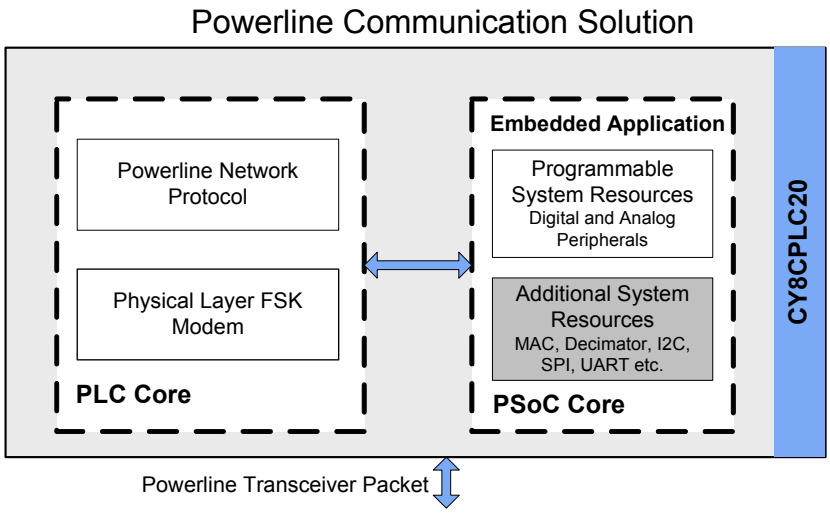
Analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks, as shown in the Figure 2-4..

Figure 2-4. Analog System Block Diagram



2.2 Additional System Resources

Figure 2-5. CY8CPLC20: Additional System Resources



System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Resources include a multiplier, decimator, low voltage detection, and power on reset. The following statements describe the merits of each system resource.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are supported.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.

3. Getting Started

The quickest way to understand Cypress's Powerline Communication offering is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). The latest version of PSoC Designer can be downloaded from www.cypress.com/psocdesigner. PSoC Designer 5.0 SP5 or later provides support for CY8CPLC20 devices. This data sheet is an overview of the CY8CPLC20 integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PLC Technical Reference Manual.

For up to date ordering, packaging, and electrical specification information, see the latest PLC device data sheets on the web at www.cypress.com/go/plc.

3.1 Application Notes

Application notes are an excellent introduction to the wide variety of possible PLC designs. They are located here: www.cypress.com/go/plc. Select Application Notes under the Support tab.

3.2 Development Kits

PLC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

3.3 Training

Free PLC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

3.4 CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

3.5 Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

3.6 Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

4. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built in support for third party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

4.1 PSoC Designer Software Subsystems

4.1.1 System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Programmable System-on-Chip Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

4.1.2 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

4.1.3 Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

4.1.4 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

4.1.5 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

4.1.6 Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

4.2 In-Circuit Emulator (ICE)

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

5. Designing with User Modules

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify, and Debug

5.1 Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and programmable system-on-chip varieties.

5.2 Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

5.3 Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

5.4 Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed. The system-level design also generates a C `main()` program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

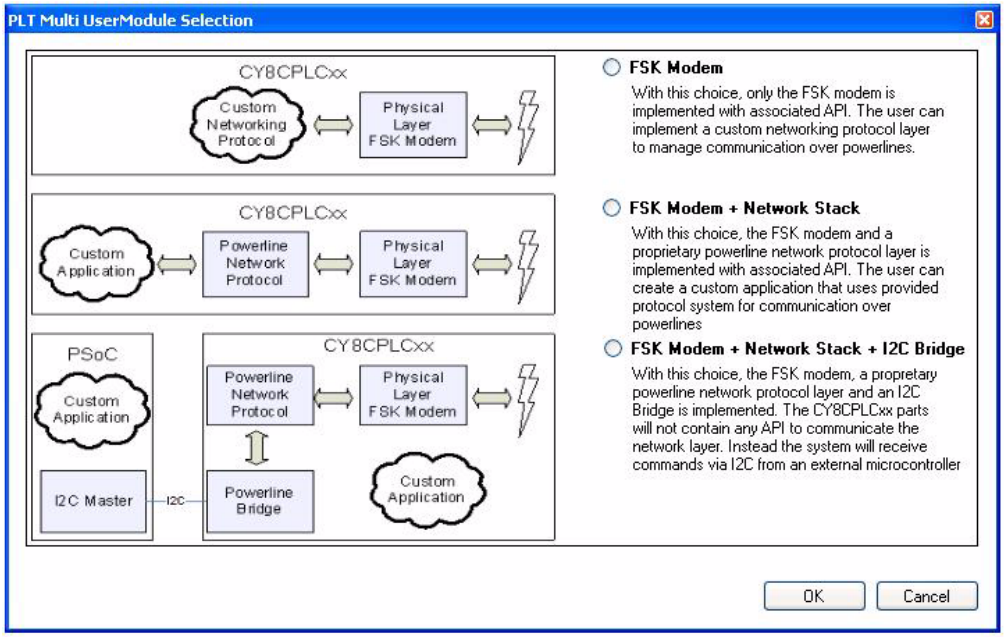
5.5 PLC User Modules

The CY8CPLC20 has the Powerline Transceiver (PLT) User Module in PSoC Designer 5.0 SP5 or later. The PLT User Module (UM) enables data communication over powerlines up to baud rates of 2400 bps. This UM also exposes all the APIs from the network protocol for ease of application development. The UM, when instantiated, provides the user with three implementation modes:

- **FSK Modem Only** – This mode enables the user to use the raw FSK modem and build any network protocol or application with the help of the APIs generated by the modem PHY.
- **FSK Modem + Network Stack** – This mode enables the user to use the Cypress network protocol for PLC and build any application with the APIs provided by the network protocol.
- **FSK Modem + Network Stack + I2C** – This mode enables the user to interface the CY8CPLC20 with any other microcontroller or PSoC device. Users can also split the application between the PLC device and the external microcontroller. If the external microcontroller is a PSoC device, then the I2C UMs can be used to interface it with the PLC device.

Figure 5-1. on page 13 shows the starting window for the PLT UM with the three implementation modes from which the user can choose.

Figure 5-1. PLT User Module



The power consumption estimate of the CY8CPLC20 chip with the PLT User Module loaded along with the other User Modules can be determined using the application note AN55403 titled "Estimating CY8CPLC20/CY8CLED16P01 Power Consumption".

6. Document Conventions

6.1 Acronyms Used

This table lists the acronyms used in this data sheet.

Table 6-1. Acronyms

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose I/O
ICE	in-circuit emulator
IDE	integrated development environment
I/O	input/output
ISSP	in-system serial programming
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PGA	programmable gain amplifier
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip
PWM	pulse width modulator
ROM	read only memory
SC	switched capacitor
SRAM	static random access memory

6.2 Units of Measure

A units of measure table is located in the section Electrical Specifications on page 22.

6.3 Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or 0x are decimal.

7. Pin Information

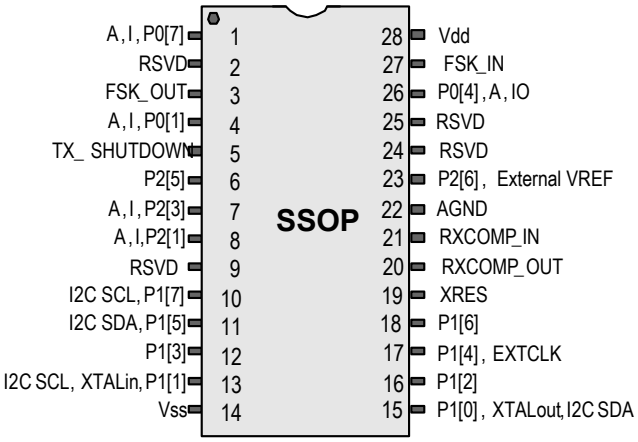
The CY8CPLC20 PLC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd and XRES are not capable of Digital I/O.

7.1 28-Pin Part Pinout

Table 7-1. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog Column Mux Input
2	Reserved		RSVD	Reserved
3		O	FSK_OUT	Analog FSK Output
4	I/O	I	P0[1]	Analog Column Mux Input
5	O		TX_SHUTDOWN	Output to disable PLC transmit circuitry in receive mode Logic ‘0’ - When the Modem is transmitting Logic ‘1’ - When the Modem is not transmitting
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Reserved		RSVD	Reserved
10	I/O		P1[7]	I2C Serial Clock (SCL)
11	I/O		P1[5]	I2C Serial Data (SDA)
12	I/O		P1[3]	XTAL_STABILITY. Connect a 0.1 µF capacitor between the pin and Vss.
13	I/O		P1[1]	Crystal (XTALin[2]), ISSP-SCLK[1], I2C SCL
14	Power		Vss	Ground connection.
15	I/O		P1[0]	Crystal (XTALout[2]), ISSP-SDATA[1], I2C SDA
16	I/O		P1[2]	
17	I/O		P1[4]	Optional External Clock Input (EXTCLK[2])
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
21		I	RXCOMP_IN	Analog Input from the external Low Pass Filter Circuitry
22	Analog Ground		AGND	Analog Ground
23	I/O		P2[6]	External Voltage Reference (VREF)
24	Reserved		RSVD	Reserved
25	Reserved		RSVD	Reserved
26	I/O	I/O	P0[4]	Analog column mux input and column output
27		I	FSK_IN	Analog FSK Input
28	Power		Vdd	Supply Voltage

Figure 7-1. CY8CPLC20 28-Pin PLC Device



LEGEND: A = Analog, I = Input, O = Output., RSVD = Reserved (Should be left unconnected)

Notes
1. These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.
2. When using the PLT user module, the external crystal is always required for protocol timing. For the FSK modem, either enable the PLL Mode or select the external 24 MHz on P1[4]. Do not use the IMO.

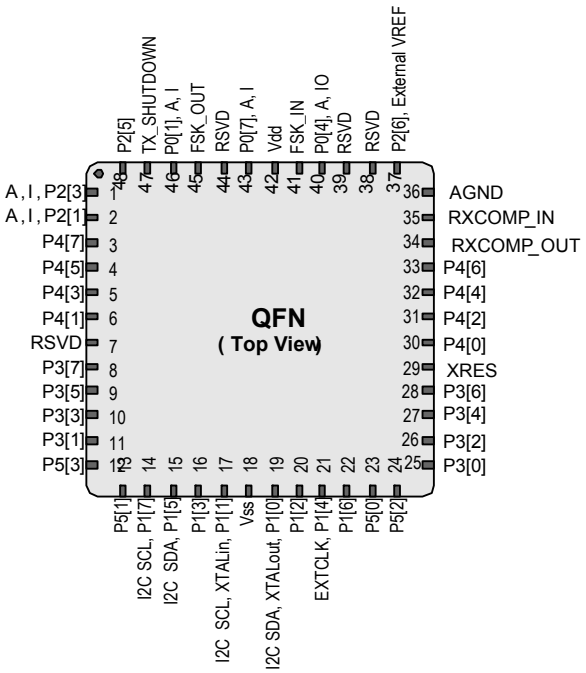
7.2 48-Pin Part Pinout

Table 7-2. 48-Pin Part Pinout (QFN)[3]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P2[3]	Direct switched capacitor block input
2	I/O	I	P2[1]	Direct switched capacitor block input
3	I/O		P4[7]	
4	I/O		P4[5]	
5	I/O		P4[3]	
6	I/O		P4[1]	
7	Reserved		RSVD	Reserved
8	I/O		P3[7]	
9	I/O		P3[5]	
10	I/O		P3[3]	
11	I/O		P3[1]	
12	I/O		P5[3]	
13	I/O		P5[1]	
14	I/O		P1[7]	I2C Serial Clock (SCL)
15	I/O		P1[5]	I2C Serial Data (SDA)
16	I/O		P1[3]	XTAL_STABILITY. Connect a 0.1 µF capacitor between the pin and Vss.
17	I/O		P1[1]	Crystal (XTALin[2]), I2C Serial Clock (SCL), ISSP-SCLK[1]
18	Power		Vss	Ground connection.
19	I/O		P1[0]	Crystal (XTALout[2]), I2C Serial Data (SDA), ISSP-SDATA[1]
20	I/O		P1[2]	
21	I/O		P1[4]	Optional External Clock Input (EXTCLK[2])
22	I/O		P1[6]	
23	I/O		P5[0]	
24	I/O		P5[2]	
25	I/O		P3[0]	
26	I/O		P3[2]	
27	I/O		P3[4]	
28	I/O		P3[6]	
29	Input		XRES	Active high external reset with internal pull down
30	I/O		P4[0]	
31	I/O		P4[2]	
32	I/O		P4[4]	
33	I/O		P4[6]	
34		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
35		I	RXCOMP_IN	Analog Input from external Low Pass Filter Circuitry
36	Analog Ground		AGND	Analog Ground
37	I/O		P2[6]	External Voltage Reference (VREF)
38	Reserved		RSVD	Reserved
39	Reserved		RSVD	Reserved
40	I/O	I/O	P0[4]	Analog column mux input and column output
41		I	FSK_IN	Analog FSK Input
42	Power		Vdd	Supply Voltage
43	I/O	I	P0[7]	Analog column mux input
44	Reserved		RSVD	Reserved
45		O	FSK_OUT]	Analog FSK Output
46	I/O	I	P0[1]	Analog column mux input
47	O		TX_SHUTDOWN	Output to disable transmit circuitry in receive mode Logic '0' - When the Modem is transmitting Logic '1' - When the Modem is not transmitting
48	I/O		P2[5]	

LEGEND: A = Analog, I = Input, O = Output, RSVD = Reserved (should be left unconnected).

Figure 7-2. CY8CPLC20 48-Pin PLC Device



Note
3. The QFN package has a center pad that must be connected to ground (Vss).

7.3 100-Pin Part Pinout (On-Chip Debug)

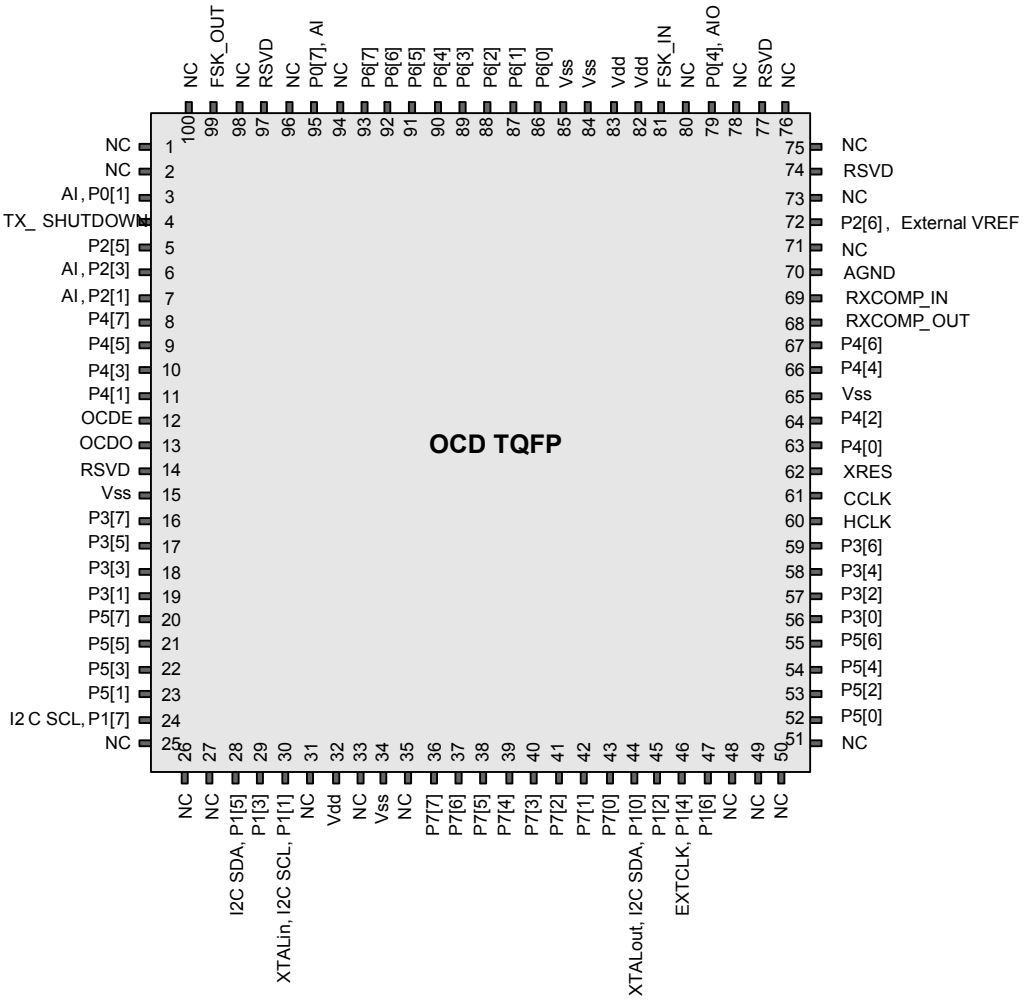
The 100-pin TQFP part is for the CY8CPLC20-OCD On-Chip Debug PLC device. Note that the OCD parts are only used for in-circuit debugging. OCD parts are NOT available for production.

Table 7-3. 100-Pin OCD Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No Connection	51			NC	No Connection
2			NC	No Connection	52	I/O		P5[0]	
3	I/O	I	P0[1]	Analog Column Mux Input	53	I/O		P5[2]	
4	O		TX_SHUTDOWN	Output to disable transmit circuitry in receive mode Logic '0' - When the Modem is transmitting Logic '1' - When the Modem is not transmitting	54	I/O		P5[4]	
5	I/O		P2[5]		55	I/O		P5[6]	
6	I/O	I	P2[3]	Direct switched capacitor block input	56	I/O		P3[0]	
7	I/O	I	P2[1]	Direct switched capacitor block input	57	I/O		P3[2]	
8	I/O		P4[7]		58	I/O		P3[4]	
9	I/O		P4[5]		59	I/O		P3[6]	
10	I/O		P4[3]		60			HCLK	OCD high speed clock output
11	I/O		P4[1]		61			CCLK	OCD CPU clock output
12			OCDE	OCD even data I/O	62	Input		XRES	Active high pin reset with internal pull down
13			OCDO	OCD odd data output	63	I/O		P4[0]	
14	Reserved		RSVD	Reserved	64	I/O		P4[2]	
15	Power		Vss	Ground Connection	65	Power		Vss	Ground Connection
16	I/O		P3[7]		66	I/O		P4[4]	
17	I/O		P3[5]		67	I/O		P4[6]	
18	I/O		P3[3]		68		O	RXCOMP_OUT	Analog Output to external Low Pass Filter Circuitry
19	I/O		P3[1]		69		I	RXCOMP_IN	Analog Input from external Low Pass Filter Circuitry
20	I/O		P5[7]		70	Ground		AGND	Analog Ground
21	I/O		P5[5]		71			NC	No Connection
22	I/O		P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF) input
23	I/O		P5[1]		73			NC	No Connection
24	I/O		P1[7]	I2C Serial Clock (SCL)	74	Reserved		RSVD	Reserved
25			NC	No Connection	75			NC	No Connection
26			NC	No Connection	76			NC	No Connection
27			NC	No Connection	77	Reserved		RSVD	Reserved
28	I/O		P1[5]	I2C Serial Data (SDA)	78			NC	No Connection
29	I/O		P1[3]	I_{FMTEST}, XTAL_STABILITY. Connect a 0.1 µF capacitor between the pin and Vss.	79	I/O	I/O	P0[4]	Analog column mux input and column output, VREF
30	I/O		P1[1]*	Crystal (XTALin[2]), I2C Serial Clock (SCL), TC SCLK	80			NC	No Connection
31			NC	No Connection	81		I	FSK_IN	Analog FSK Input
32	Power		Vdd	Supply Voltage	82	Power		Vdd	Supply Voltage
33			NC	No Connection	83	Power		Vdd	Supply Voltage
34	Power		Vss	Ground Connection	84	Power		Vss	Ground Connection
35			NC	No Connection	85	Power		Vss	Ground Connection
36	I/O		P7[7]		86	I/O		P6[0]	
37	I/O		P7[6]		87	I/O		P6[1]	
38	I/O		P7[5]		88	I/O		P6[2]	
39	I/O		P7[4]		89	I/O		P6[3]	
40	I/O		P7[3]		90	I/O		P6[4]	
41	I/O		P7[2]		91	I/O		P6[5]	
42	I/O		P7[1]		92	I/O		P6[6]	
43	I/O		P7[0]		93	I/O		P6[7]	
44	I/O		P1[0]*	Crystal (XTALout[2]), I2C Serial Data (SDA), TC SDATA	94			NC	No Connection
45	I/O		P1[2]	V_{FMTEST}	95	I/O	I	P0[7]	Analog Column Mux Input
46	I/O		P1[4]	Optional External Clock Input (EXTCLK[2])	96			NC	No Connection
47	I/O		P1[6]		97	Reserved		RSVD	Reserved
48			NC	No Connection	98			NC	No Connection
49			NC	No Connection	99		O	FSK_OUT	Analog FSK Output
50			NC	No Connection	100			NC	No Connection

LEGEND A = Analog, I = Input, O = Output, NC = No Connection, TC/TM: Test, RSVD = Reserved (should be left unconnected).

Figure 7-3. CY8CPLC20-OCD



Not for Production

8. Register Reference

This section lists the registers of the CY8CPLC20 PLC device. For detailed register information, reference the *PLC Technical Reference Manual*.

8.1 Register Conventions

8.1.1 Abbreviations Used

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

8.2 Register Mapping Tables

The CY8CPLC20 device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 8-1. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	DBB20DR0	40	#	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0IE	01	RW	DBB20DR1	41	W	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0GS	02	RW	DBB20DR2	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0DM2	03	RW	DBB20CR0	43	#	ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DR	04	RW	DBB21DR0	44	#	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1IE	05	RW	DBB21DR1	45	W	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1GS	06	RW	DBB21DR2	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1DM2	07	RW	DBB21CR0	47	#	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	DCB22DR0	48	#	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2IE	09	RW	DCB22DR1	49	W	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2GS	0A	RW	DCB22DR2	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2DM2	0B	RW	DCB22CR0	4B	#	ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DR	0C	RW	DCB23DR0	4C	#	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3IE	0D	RW	DCB23DR1	4D	W	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3GS	0E	RW	DCB23DR2	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3DM2	0F	RW	DCB23CR0	4F	#	ASD13CR3	8F	RW		CF	
PRT4DR	10	RW	DBB30DR0	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	DBB30DR1	51	W	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	DBB30DR2	52	RW	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	DBB30CR0	53	#	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	DBB31DR0	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	DBB31DR1	55	W	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	DBB31DR2	56	RW	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	DBB31CR0	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
PRT6DR	18	RW	DCB32DR0	58	#	ASD22CR0	98	RW	I2C_DR	D8	RW
PRT6IE	19	RW	DCB32DR1	59	W	ASD22CR1	99	RW	I2C_MSCR	D9	#
PRT6GS	1A	RW	DCB32DR2	5A	RW	ASD22CR2	9A	RW	INT_CLR0	DA	RW
PRT6DM2	1B	RW	DCB32CR0	5B	#	ASD22CR3	9B	RW	INT_CLR1	DB	RW
PRT7DR	1C	RW	DCB33DR0	5C	#	ASC23CR0	9C	RW	INT_CLR2	DC	RW
PRT7IE	1D	RW	DCB33DR1	5D	W	ASC23CR1	9D	RW	INT_CLR3	DD	RW
PRT7GS	1E	RW	DCB33DR2	5E	RW	ASC23CR2	9E	RW	INT_MSK3	DE	RW
PRT7DM2	1F	RW	DCB33CR0	5F	#	ASC23CR3	9F	RW	INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 8-1. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 8-2. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
PRT6DM0	18	RW	DCB32FN	58	RW	ASD22CR0	98	RW		D8	
PRT6DM1	19	RW	DCB32IN	59	RW	ASD22CR1	99	RW		D9	
PRT6IC0	1A	RW	DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
PRT6IC1	1B	RW		5B		ASD22CR3	9B	RW		DB	
PRT7DM0	1C	RW	DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
PRT7DM1	1D	RW	DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
PRT7IC0	1E	RW	DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
PRT7IC1	1F	RW		5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 8-2. Register Map Bank 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7		DEC_CR2	E7	RW
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

9. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CPLC20 device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

The following table lists the units of measure that are used in this chapter.

Table 9-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	µW	microwatts
dB	decibels	mA	milliamperes
fF	femtofarads	ms	millisecond
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoamperes
Kbit	1024 bits	ns	nanoseconds
kHz	kilohertz	nV	nanovolts
kΩ	kilohms	Ω	ohms
MHz	megahertz	pA	picoamperes
MΩ	megaohms	pF	picofarads
µA	microamperes	pp	peak-to-peak
µF	microfarads	ppm	parts per million
µH	microhenrys	ps	picoseconds
µs	microseconds	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

9.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 9-2. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

9.2 Operating Temperature

Table 9-3. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 39. The user must limit the power consumption to comply with this requirement.

9.3 DC Electrical Characteristics

9.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-4. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	4.75	–	5.25	V	
I_{DD}	Supply Current	–	8	14	mA	Conditions are 5.0V, T_A = 25°C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz
V_{REF}	Reference Voltage (Bandgap)	1.28	1.3	1.32	V	Trimmed for appropriate Vdd

9.3.2 DC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature range: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-5. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined IOL budget.
I_{OH}	High Level Source Current	10	–	–	mA	VOH = Vdd-1.0V, see the limitations of the total current in the note for VOH
I_{OL}	Low Level Source Current	25	–	–	mA	VOL = 0.75V, see the limitations of the total current in the note for VOL
V_{IL}	Input Low Level	–	–	0.8	V	
V_{IH}	Input High Level	2.1	–		V	
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

9.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-6. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (Absolute Value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range. All cases, except highest. Power = High, Opamp Bias = High	0.0 0.5	– –	Vdd Vdd - 0.5	V V	
$CMRR_{OA}$	Common Mode Rejection Ratio	60	–	–	dB	
G_{OLOA}	Open Loop Gain	80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (Internal Signals)	Vdd - 0.01	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (Internal Signals)	–	–	0.1	V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	67	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

9.3.4 DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-7. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low Power Comparator (LPC) Reference Voltage Range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC Supply Current	–	10	40	µA	
V_{OSLPC}	LPC Voltage Offset	–	2.5	30	mV	

9.3.5 DC Analog Output Buffer Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-8. DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 – –	 1 1	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.3 0.5 x Vdd + 1.3	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 2 5	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	40	64	–	dB	

9.3.6 DC Analog Reference Specifications

Table 9-9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 9-9. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
V_{BG5}	Bandgap Voltage Reference 5V	1.28	1.30	1.32	V
–	AGND = Vdd/2[4]	Vdd/2 - 0.02	Vdd/2	Vdd/2 + 0.02	V
–	AGND = 2 x Bandgap[4]	2.52	2.60	2.72	V
–	AGND = P2[4] (P2[4] = Vdd/2)[4]	P2[4] - 0.013	P2[4]	P2[4] + 0.013	V
–	AGND = Bandgap[3]	1.27	1.3	1.34	V
–	AGND = 1.6 x Bandgap[4]	2.03	2.08	2.13	V
–	AGND Block to Block Variation (AGND = Vdd/2)[4]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + Bandgap	Vdd/2 + 1.21	Vdd/2 + 1.3	Vdd/2 + 1.382	V
–	RefHi = 3 x Bandgap	3.75	3.9	4.05	V
–	RefHi = 2 x Bandgap + P2[6] (P2[6] = 1.3V)	P2[6] + 2.478	P2[6] + 2.6	P2[6] + 2.722	V
–	RefHi = P2[4] + Bandgap (P2[4] = Vdd/2)	P2[4] + 1.218	P2[4] + 1.3	P2[4] + 1.382	V

Note
4. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V

Table 9-9. 5V DC Analog Reference Specifications (continued)

Symbol	Description	Min	Typ	Max	Units
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.058	P2[4] + P2[6]	P2[4] + P2[6] + 0.058	V
–	RefHi = 2 x Bandgap	2.50	2.60	2.70	V
–	RefHi = 3.2 x Bandgap	4.02	4.16	4.29	V
–	RefLo = Bandgap	BG - 0.082	BG + 0.023	BG + 0.129	V
–	RefLo = 2 x Bandgap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – Bandgap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

9.3.7 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-10. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

9.3.8 POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-11. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PPOR2R}	Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 10b	–	4.55	–	V	
V_{PPOR2}	Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 10b	–	4.55	–	V	
V_{PH2}	PPOR Hysteresis PORLEV[1:0] = 10b	–	0	–	mV	
V_{LVD6} V_{LVD7}	Vdd value for LVD Trip VM[2:0] = 110b VM[2:0] = 111b	4.63 4.72	4.73 4.81	4.82 4.91	V V	

9.3.9 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-12. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	10	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash Endurance (total)[5]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note

5. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles). For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

9.4 AC Electrical Characteristics

9.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Note See the individual user module data sheets for information on maximum frequencies for user modules.

Table 9-13. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6	MHz	Trimmed for 5V operation using factory trim values. SLIMO Mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.5	6	6.5[6]	MHz	Trimmed for 5V operation using factory trim values. SLIMO Mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[6]	MHz	
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[6, 7]	MHz	Refer to the AC Digital Block Specifications below.
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{32K_U}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	–	–	kHz	After a reset and before the m8c starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on timing this.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	250	500	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	300	600	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 µW maximum drive level 32.768 kHz crystal. -40°C ≤ T_A ≤ 85°C.
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC_{ILO}	Internal Low Speed Oscillator Duty Cycle	20	50	80	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2	MHz	Trimmed. Utilizing factory trim values.

Notes
6. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
7. See the individual user module data sheets for information on maximum frequencies for user modules.

Table 9-13. AC Chip-Level Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0V. See the System Resets section of the PSoC Technical Reference Manual.

Figure 9-1. PLL Lock Timing Diagram

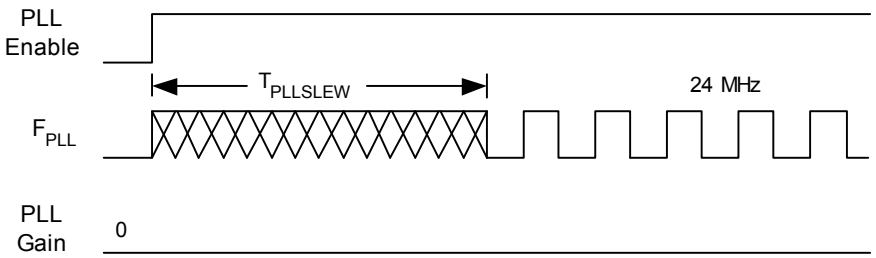


Figure 9-2. PLL Lock for Low Gain Setting Timing Diagram

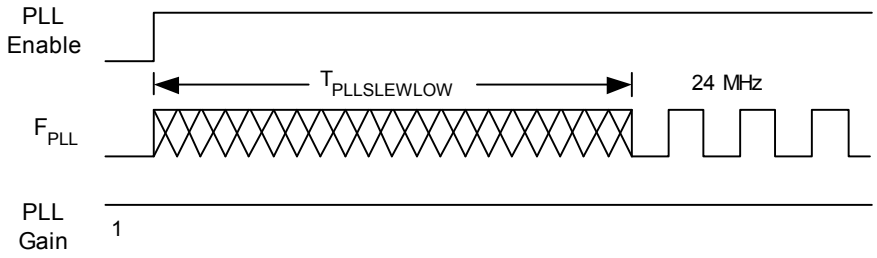


Figure 9-3. External Crystal Oscillator Startup Timing Diagram

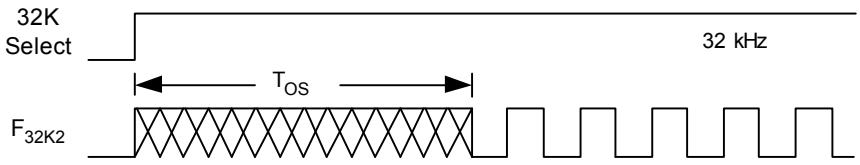


Figure 9-4. 24 MHz Period Jitter (IMO) Timing Diagram

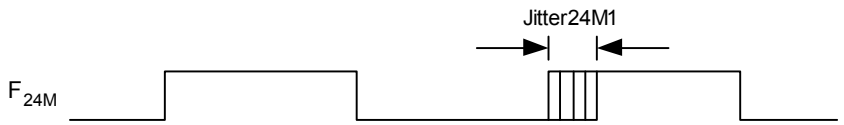


Figure 9-5. 32 kHz Period Jitter (ECO) Timing Diagram

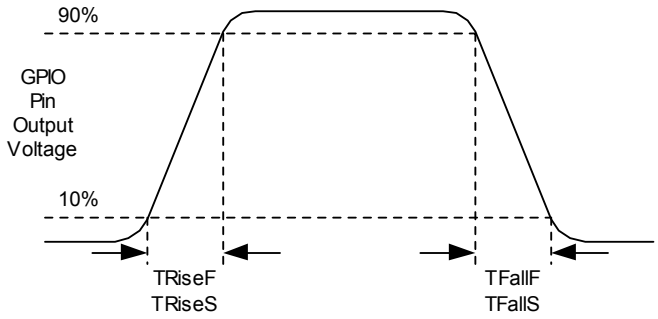
9.4.2 AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-14. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	10% - 90%

Figure 9-6. GPIO Timing Diagram



9.4.3 AC Operational Amplifier Specifications

Table 9-15 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

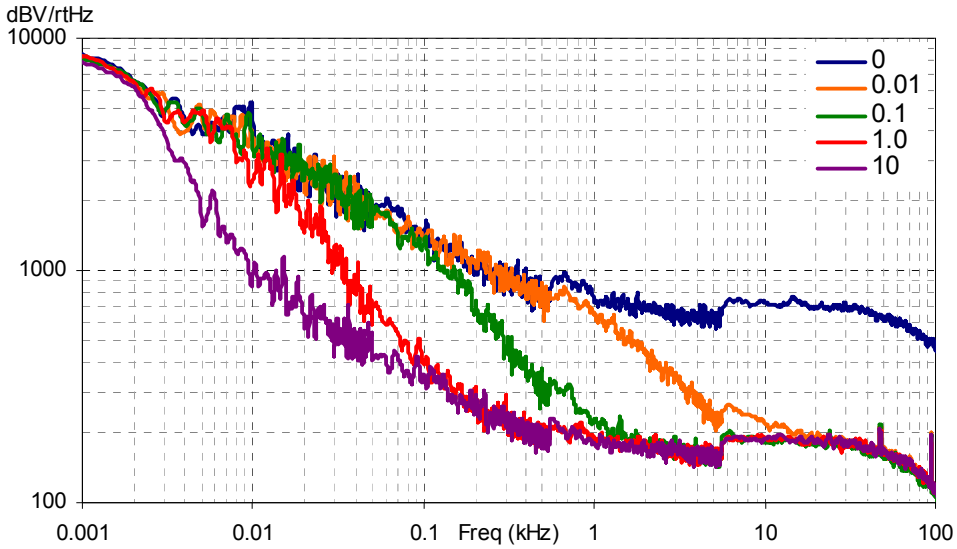
Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 9-15. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs	
T_{SOA}	Falling Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs	
SR_{ROA}	Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs	
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	

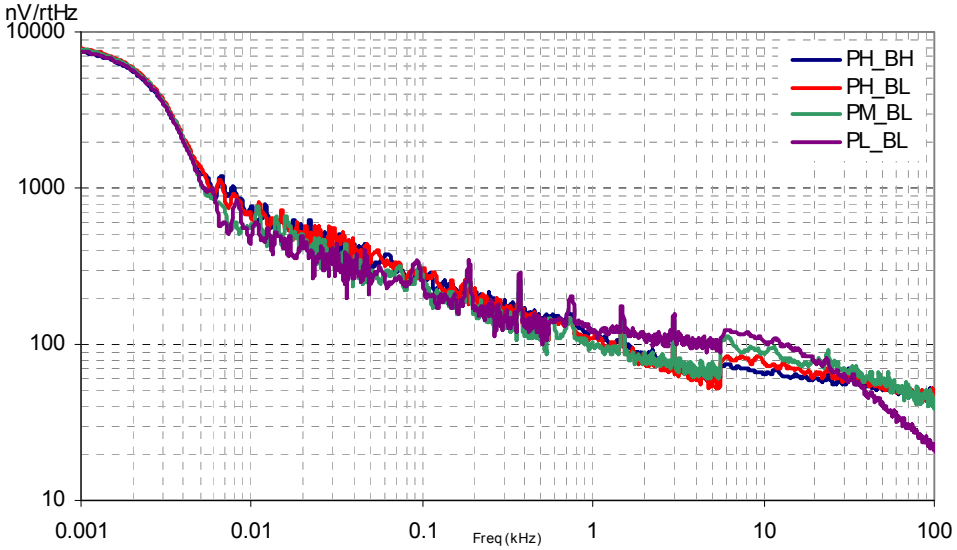
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 9-7. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 9-8. Typical Opamp Noise



9.4.3 AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-16. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC Response Time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

9.4.4 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-17. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			49.2	MHz	
Timer	Capture Pulse Width	50[8]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50[8]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[8]	–	–	ns	
	Disable Mode	50[8]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	

Table 9-17. AC Digital Block Specifications (continued)

Function	Description	Min	Typ	Max	Units	Notes
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50[8]	–	–	ns	
Transmitter	Maximum Input Clock Frequency Vdd ≥ 4.75V, 2 Stop Bits	– –	– –	24.6 49.2	MHz MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking. Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency Vdd ≥ 4.75V, 2 Stop Bits	– –	– –	24.6 49.2	MHz MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking. Maximum data rate at 6.15 MHz due to 8 x over clocking.

9.4.5 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-18. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	– –	– –	4 4	µs µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	– –	– –	3.4 3.4	µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	0.5 0.5	– –	– –	V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	0.55 0.55	– –	– –	V/µs V/µs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100 pF Load Power = Low Power = High	0.8 0.8	– –	– –	MHz MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100 pF Load Power = Low Power = High	300 300	– –	– –	kHz kHz	

Note
8. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period)

9.4.6 AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-19. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

9.4.7 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-20. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	40	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	
$T_{ERASEALL}$	Flash Erase Time (Bulk)	–	80	–	ms	Erase all Blocks and protection fields at once
$T_{PROGRAM\_HOT}$	Flash Block Erase + Flash Block Write Time	–	–	100[9]	ms	0°C <= Tj <= 100°C
$T_{PROGRAM\_COLD}$	Flash Block Erase + Flash Block Write Time	–	–	200[9]	ms	-40°C <= Tj <= 0°C

9.4.8 AC I^2C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°CC ≤ T_A ≤ 85°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

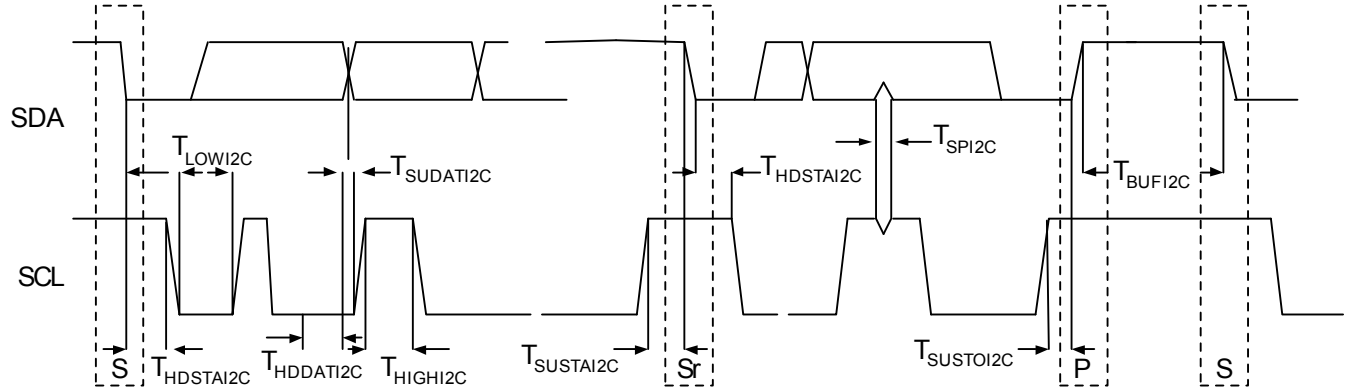
Table 9-21. AC Characteristics of the I^2C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[10]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Notes

9. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com for more information.
10. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 9-9. Definition for Timing for Fast/Standard Mode on the I²C Bus Packaging Dimensions



10. Packaging Information

This chapter illustrates the packaging specifications for the CY8CPLC20 PLC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

10.1 Packaging Dimensions

Figure 10-1. 28-Pin (210-Mil) SSOP

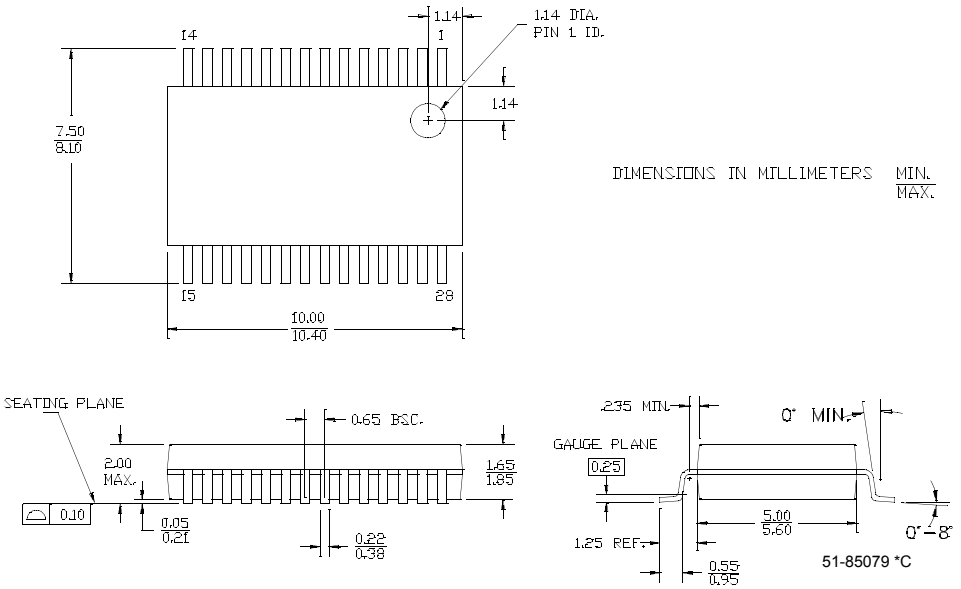
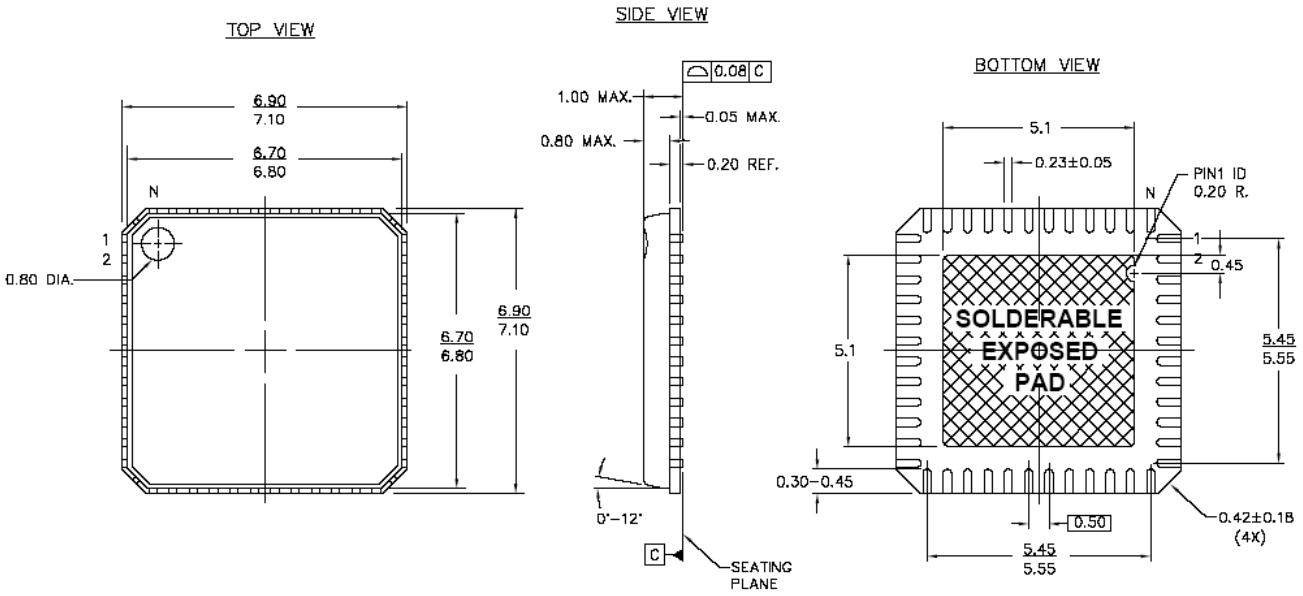


Figure 10-2. 48-Pin (7x7 mm) QFN



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *A

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Important Note Pinned vias for thermal conduction are not required for the low-power PSoC devices.

Figure 10-3. 48-Pin QFN 7x7x 0.90 MM (Sawn Type)

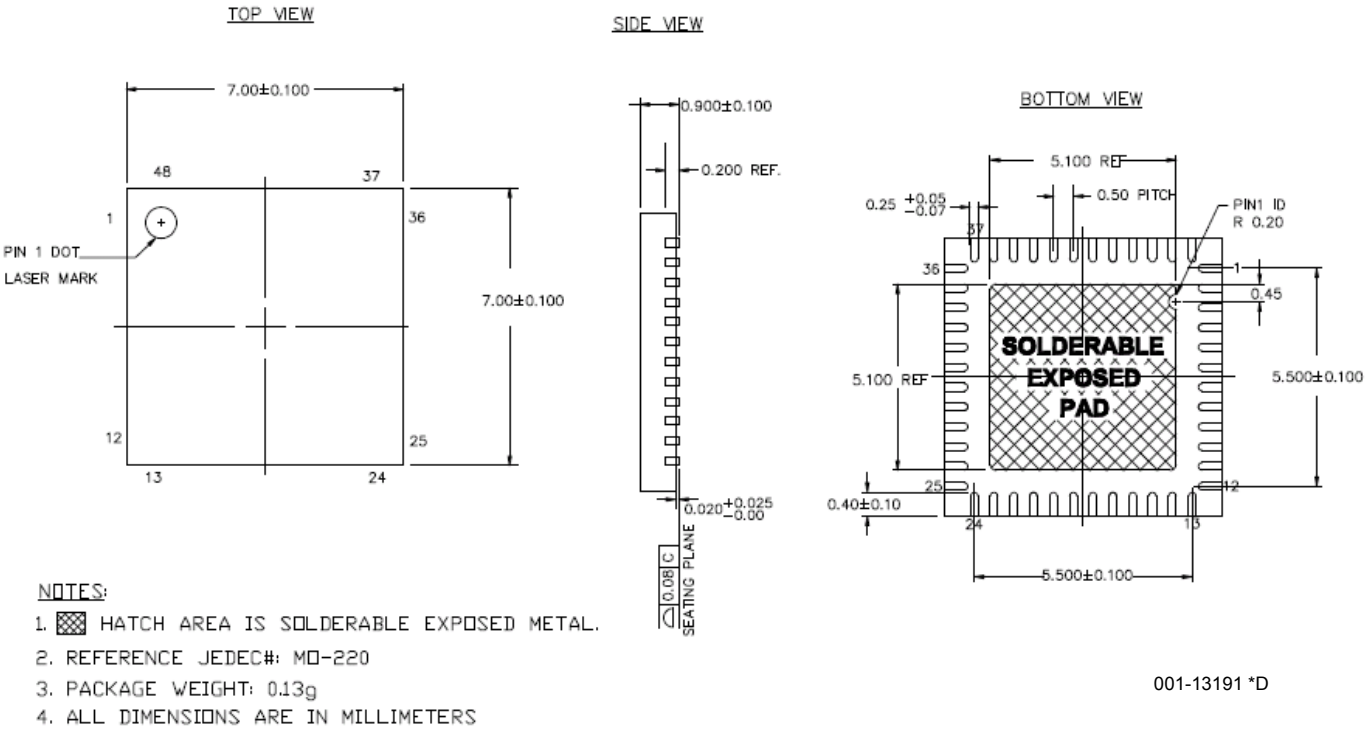
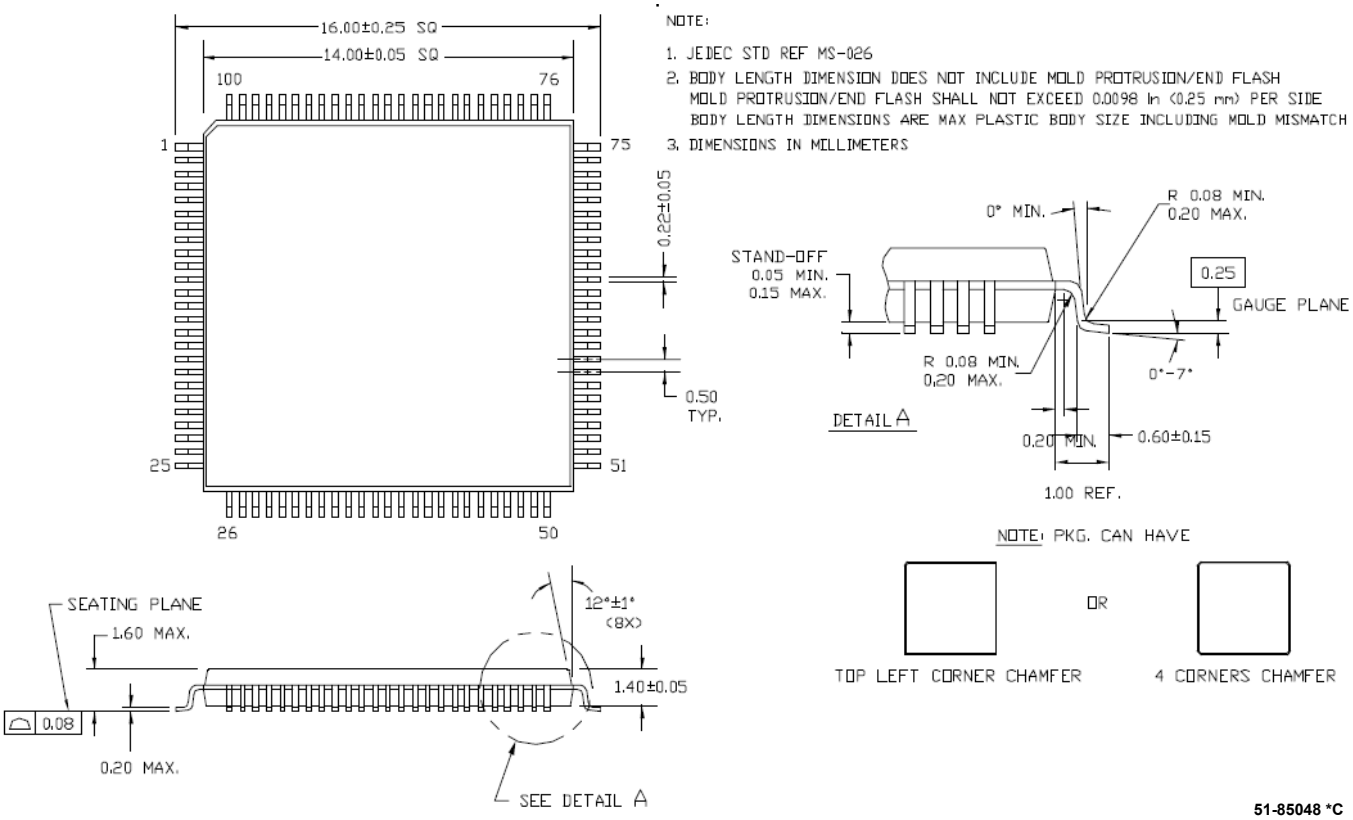


Figure 10-4. 100-Pin TQFP



10.1 Thermal Impedances

Table 10-1. Thermal Impedances per Package

Package	Typical θ_{JA}[11]
28 SSOP	94°C/W
48 QFN[12]	28°CC/W
100 TQFP	50°C/W

10.2 Capacitance on Crystal Pins

Table 10-2. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
28 SSOP	2.8 pF
48 QFN	1.8 pF
100 TQFP	3.1 pF

10.3 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 10-3. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[13]	Maximum Peak Temperature
28 SSOP	240°C	260°C
48 QFN	220°C	260°C
100 TQFP	220°C	260°C

Notes
11. $T_J = T_A + POWER \times \theta_{JA}$
12. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
13. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

11. Development Tool Selection

11.1 Software

11.1.1 PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

11.1.2 PSoC Programmer

PSoC Programmer is a very flexible programming application. It is used on the bench in development and is also suitable for factory programming. PSoC Programmer works either in a standalone configuration or operates directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

11.2 Development Kits

All development kits are sold at the Cypress Online Store.

11.2.1 CY3274 HV Development Kit

The CY3274 is for prototyping and development on the CY8CPLC20 with PSoC Designer. This kit supports in-circuit emulation. The software interface enables users to run, halt, and single-step the processor and view the content of specific memory locations. PSoC Designer also supports the advanced emulation features. The hardware comprises of the high voltage coupling circuit for 110VAC-240VAC powerline, which is compliant with the CENELEC/FCC standards. This board also has an onboard switch mode power supply. The kit comprises:

- One High Voltage (110-230VAC) PLC Board. Cypress recommends that a user purchases two CY3274 kits to setup a two-node PLC subsystem for evaluation and development.
- CY8CPLC20-OCD (100 TQFP)
- Software CD
- Supporting Literature
- MiniProg1

11.2.2 CY3275 LV Development Kit

The CY3275-PLC is for prototyping and development on the CY8CPLC20 with PSoC Designer. This kit supports in-circuit emulation. The software interface enables users to run, halt, and single-step the processor and view the content of specific memory locations. PSoC Designer also supports advanced emulation features. The hardware comprises of the low voltage coupling circuit for 12-24V AC/DC powerline. This board also has an onboard switch mode power supply. The kit comprises:

- One Low Voltage (12-24V AC/DC) PLC Board. Cypress recommends that a user purchases two CY3275 kits to setup a two-node PLC subsystem for evaluation and development.
- CY8CPLC20-OCD (100TQFP)
- Software CD
- Supporting Literature
- MiniProg1

11.2.3 CY3250-PLC Pod Kits

The CY3250-PLC Pod Kits are essential for development purposes as they provide the users a medium to emulate and debug their designs. The pod kits are available for all the available footprints. The details are:

- CY3250-PLC20NQ – One SSOP Pod (CY8CPLC20-OCD), Two 28-SSOP Feet, One 3250-Flex Cable, One 28-SSOP foot Mask
- CY3250-PLC20QFN – One QFN Pod (CY8CPLC20-OCD), Two 48-QFN Feet, One 3250-Flex Cable
- CY3250-PLC20NQ-POD – Two SSOP Pods (CY8CPLC20-OCD)
- CY3250-PLC20QFN-POD – Two QFN Pods (CY8CPLC20-OCD)

11.2.4 CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit can be used in conjunction with the PLC kits to support in-circuit emulation. The software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer also supports the advanced emulation features. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

11.3 Evaluation Kits

The evaluation kits do not have onboard Powerline capability, but can be used with a PLC kit for evaluation purposes. All evaluation tools are sold at the Cypress Online Store.

11.3.1 CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.3.2 CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.3.3 CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator, and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

11.4 Device Programmers

All device programmers are purchased from the Cypress Online Store.

11.4.1 CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.4.2 CY3207 ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.

Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

11.4.3 Third Party Tools

Several tools are specially designed by the following third party vendors to accompany PSoC devices during development and production. Specific details of each of these tools are found at http://www.cypress.com under Support.

11.4.4 Build a PSoC Emulator into Your Board

For details on emulating the circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/design/AN2323.

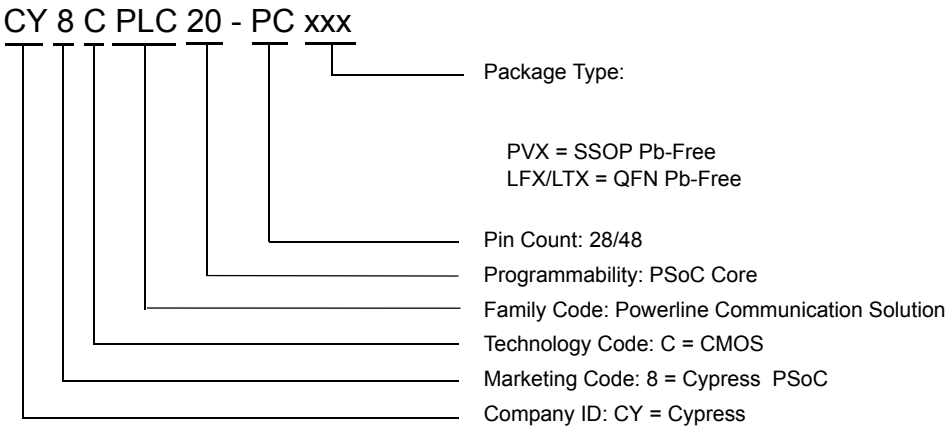
12. Ordering Information

The following table lists the CY8CPLC20 PLC devices' key package features and ordering codes.

Table 1. CY8CPLC20 PLC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Temperature Range	Digital PSoC Blocks	Analog PSoC Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
28-Pin (210 Mil) SSOP	CY8CPLC20-28PVXI	32K	2K	-40C to +85C	16	12	24	12	4	Yes
28-Pin (210 Mil) SSOP (Tape and Reel)	CY8CPLC20-28PVXIT	32K	2K	-40C to +85C	16	12	24	12	4	Yes
48-Pin QFN	CY8CPLC20-48LFXI	32K	2K	-40C to +85C	16	12	44	12	4	Yes
48-Pin QFN (Sawn)	CY8CPLC20-48LTXI	32K	2K	-40°C to +85°C	16	12	44	12	4	Yes
48-Pin QFN (Sawn) (Tape and Reel)	CY8CPLC20-48LTXIT	32K	2K	-40°C to +85°C	16	12	44	12	4	Yes
100-Pin OCD TQFP[14]	CY8CPLC20-OCD	32K	2K	-40C to +85C	16	12	64	12	4	Yes

13. Ordering Code Definitions



Note
14. This part may be used for in-circuit debugging. It is NOT available for production.

14. Document History Page

Document Title: CY8CPLC20 Powerline Communication Solution Document Number: 001-48325				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2571957	GHH/PYRS	09/24/08	New Datasheet
*A	2731927	GHH/HMT/ DSG	07/06/09	Added - Configurable baud rates and FSK frequencies - PLC Pod Kits for development purposes Modified - Pin information for all packages
*B	2748537	GHH	See ECN	Added Sections on 'Getting Started' and 'Document Conventions' Modified the following Electrical Parameters - FIMO6 Min: Changed from 5.75 MHz to 5.5 MHz - FIMO6 Max: Changed from 6.35 MHz to 6.5 MHz - SPIS (Maximum input clock frequency): Changed from 4.1 ns to 4.1 MHz - TWRITE (Flash Block Write Time): Changed from 40 ms to 10 ms
*C	2752799	GHH	08/17/09	Posting to external web.
*D	2759000	GHH	09/02/2009	Fixed typos in the data sheet
*E	2778970	FRE	10/05/2009	Added a table for DC POR and LVD Specifications Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: - Modified FIMO6, TWRITE, and Power Up IMO to Switch specifications - Added IOH, IOL, DCILO, F32K_U, TPOWERUP, TERASEALL, and SRPOWER_UP specifications Added 48-Pin QFN (Sawn) package diagram and CY8CPLC20-48LTXI and CY8CPLC20-48LTXIT part details in the Ordering Information table Updated section 4 and Tables 9-1, 9-2, and 9-3 to state the requirement to use the external crystal for PLC protocol timing Table 9-1 and Figure 9-1: Changed pins 9 and 25 from NC to RSVD Table 9-2 and Figure 9-2: Changed pins 7 and 39 from NC to RSVD Table 9-3 and Figure 9-3: Changed pins 14 and 77 from NC to RSVD Tables 9-1, 9-2, 9-3: Added explanation to Connect a 0.1 uF capacitor between XTAL_Stability and VSS. Fixed minor typos.

15. Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at www.cypress.com/go/home/order/sales.

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