BlueCore®4-PC-ROM WLCSP

Single Chip Bluetooth® v2.1 + EDR System

Production Information

BC0401PC08

Issue 1

Features

- Fully Qualified Bluetooth® v2.1 + EDR specification Including both 2Mbps and 3Mbps Modulation Modes
- Full-speed Bluetooth Operation with Piconet and Scatternet Support
- 6dBm Transmit Power and -86dBm Receive Sensitivity
- 1.8V core, 1.7 to 3.6V I/O Split Rails
- Ultra Low Power Consumption
- Minimum External Components Required
- Integrated 1.8V Regulator
- USB Interface
- 4Mbit Internal ROM
- Support for 802.11 Coexistence
- 3.8 x 4.0 x 0.7mm, 0.5mm pitch 47-Ball WLCSP
- Green (RoHS and no Antimony or Halogenated Flame Retardants)

General Description

BlueCore®4-PC-ROM WLCSP is a single-chip radio and baseband IC for Bluetooth 2.4GHz systems including EDR to 3Mbits/s.

With the on-chip CSR Bluetooth software stack, BlueCore4-PC-ROM WLCSP provides a fully compliant Bluetooth v2.1 + EDR specification system for data and voice communications.

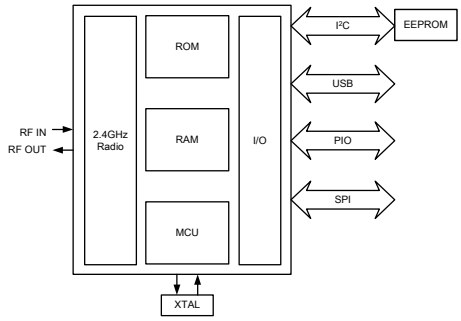

Figure: System Architecture

Applications

- USB Dongles
- PC Bluetooth Modules

BlueCore4-PC-ROM WLCSP has been designed to reduce the number of external components required which ensures production costs are minimised.

The device incorporates auto-calibration and BIST routines to simplify development, type approval and production test.

All hardware and device firmware is fully compliant with the Bluetooth v2.1 + EDR specification (all mandatory features).

Document History

Revision	Date	Change Reason
Issue 1	07 NOV 08	Original publication of this document If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.

Status Information

The status of this Product Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

ESD Precautions

BlueCore4-PC-ROM WLCSP is classified as a JESD22-A114 class 2 product. Apply ESD static handling precautions during manufacturing.

Life Support Policy and Use in Safety-critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

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BlueCore4-PC-ROM WLCSP devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

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1 Device Details

Radio

- Common TX/RX terminals simplify external matching; eliminates external antenna switch
- BIST minimises production test time
- Bluetooth v2.1 + EDR specification compliant
- Full RF example designs are available

Transmitter

- 6dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >35dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch
- Class1 support using external power amplifier with RF power controlled by an internal 8-bit DAC
- Supports DQPSK (2Mbps) and 8DPSK modulation (3Mbps) modulation

Receiver

- Receiver sensitivity of -86dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range
- Channel classification
- Supports DQPSK and 8DPSK modulation

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 8MHz to 40MHz or an external clock 8MHz to 40MHz
- Accepts 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Physical Interfaces

- Synchronous serial interface up to 4Mbits/s for system debugging
- Full-speed USB v2.0 interface supports OHCI and UHCI host interfaces
- I^2C compatible interface
- 802.11 coexistence interface

Auxiliary Features

- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown, and wake up commands with an integrated low power oscillator for ultra low power Park/Sniff/Hold mode
- Clock request output to control external clock
- Device can run in low power modes from an external 32768Hz clock signal
- On-chip regulator, producing 1.8V output from 2.2V to 5.6V input
- Power-on-reset cell detects low supply voltage

Baseband and Software

- 4Mbit internal ROM
- 48Kbyte internal RAM, allows full speed data transfer, mixed voice and data, and full piconet operation, including all EDR packet types
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping. Supports all mandatory Bluetooth v2.1 + EDR specification features including eSCO and AFH
- Transcoders for A-law, µ-law and linear voice from host and A-law, µ-law and CVSD voice over air
- Standard HCI over USB

Package Option

- 47-Ball 3.8 x 4.0 x 0.7mm 0.5mm pitch WLCSP

2 Device Diagram

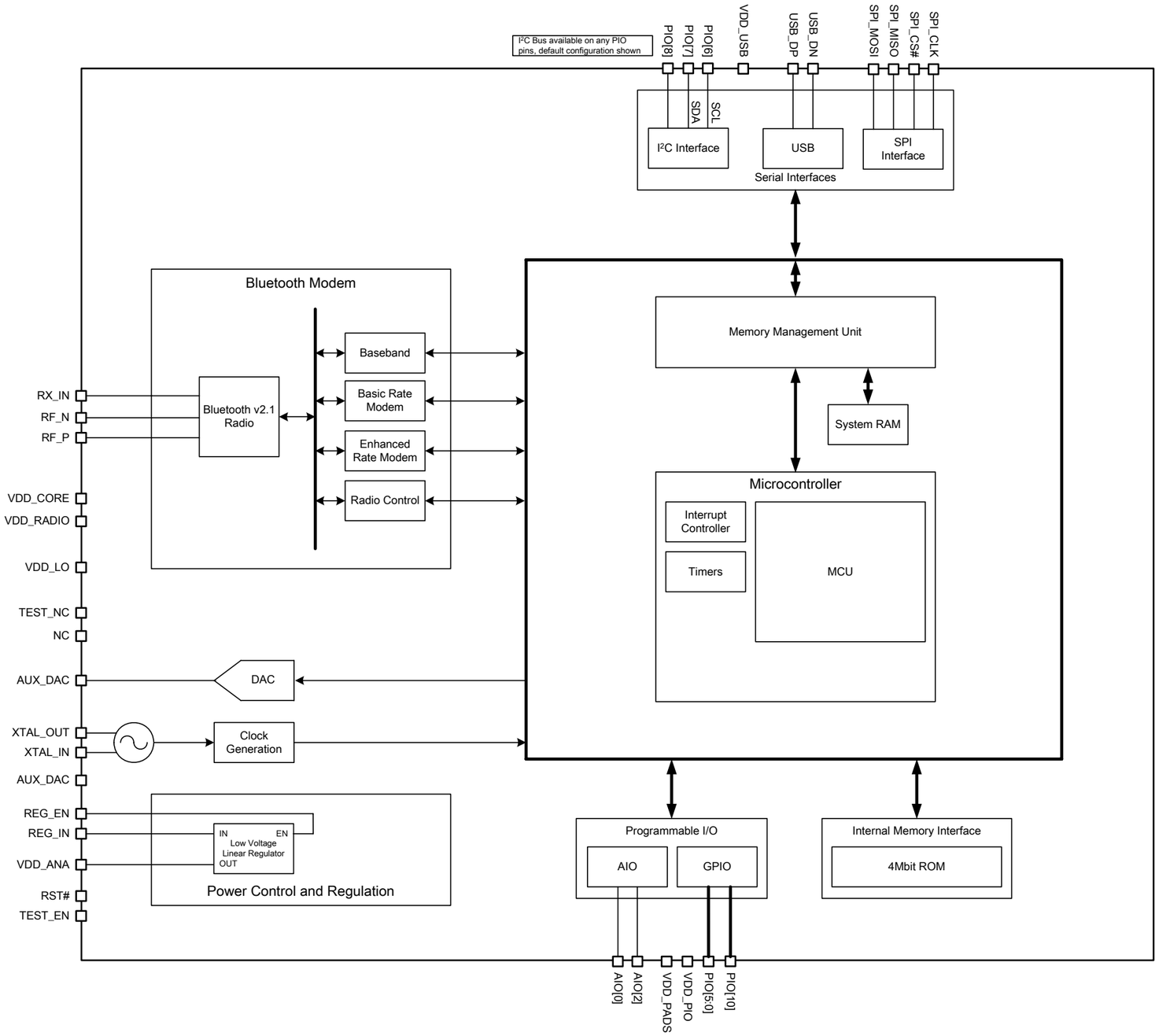


Figure 2.1: BlueCore4-PC-ROM WLCSP Device Diagram

3 Package Information

3.1 47-Ball 3.8 x 4.0 x 0.7mm, 0.5mm pitch WLCSP Pinout Diagram

Orientation from top of device

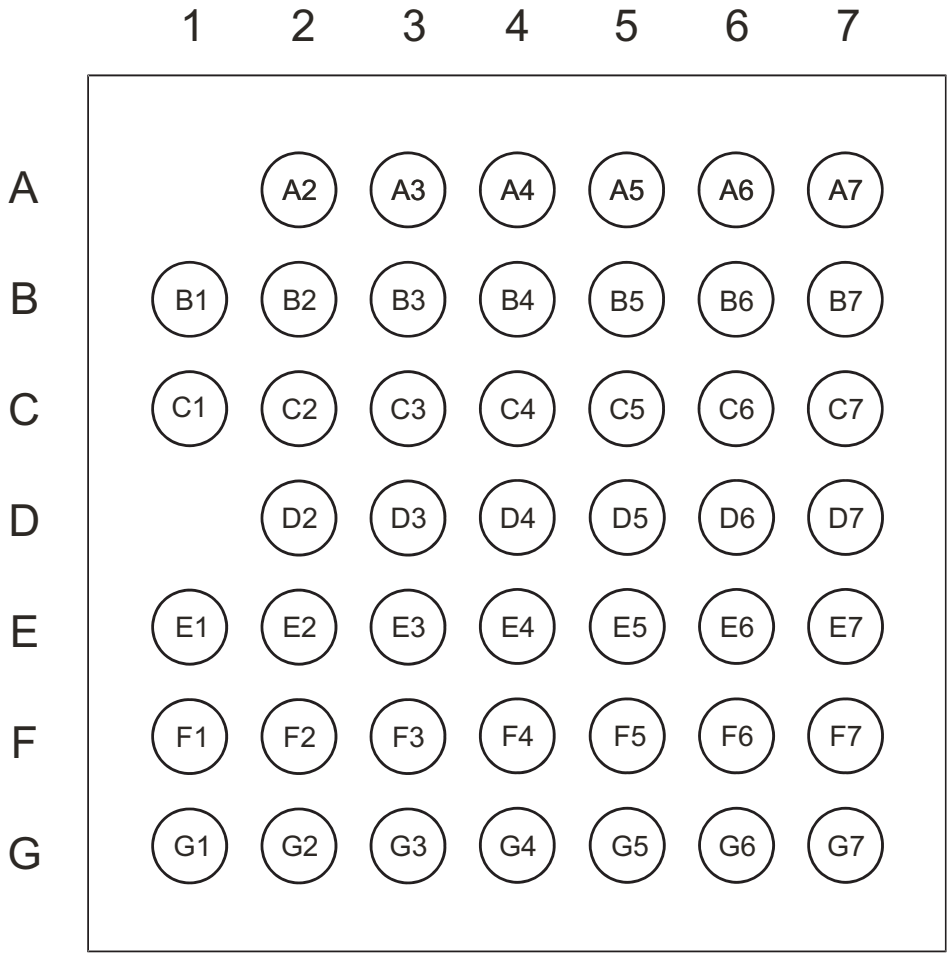


Figure 3.1: 47-Ball 3.8 x 4.0 x 0.7mm, 0.5mm pitch WLCSP Pinout Diagram

3.2 Device Terminal Functions

Bluetooth Radio	Ball	Pad Type	Description
RF_A	E2	Analogue	Transmitter output/switched receiver input
RF_B	E1	Analogue	Complement of RF_A
AUX_DAC	D2	Analogue	Voltage DAC

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	A3	Analogue	For crystal or external clock input
XTAL_OUT	B3	Analogue	Drive for crystal

USB	Ball	Pad Type	Description
USB_DP	B5	Bi-directional	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	A6	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESETB	E7	CMOS input with weak internal pull-up	Reset if low. Input debounced so must be low for >5ms to cause a reset
SPI_CSB	G6	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface, active low
SPI_CLK	G5	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	F6	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	F7	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	G7	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port	Ball	Pad Type	Description/Function
PIO[0]	F3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Reserved for RX monitoring.
PIO[1]	F4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Reserved for TX monitoring.
PIO[2]	G1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Serial EEPROM clock or data.

PIO Port	Ball	Pad Type	Description/Function
PIO[3]	G2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Serial EEPROM clock or data.
PIO[4]	E6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Intel wireless co-existence, BT_Priority.
PIO[5]	F5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Flashing LED.
PIO[6]	D7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Intel wireless co-existence, WLAN.
PIO[7]	E5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Intel wireless co-existence, internally reserved.
PIO[8]	E3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Serial EEPROM write protect.
PIO[9]	F1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Intel USB Sideband Deferring.
PIO[10]	F2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line. Serial EEPROM PIO selection, tied high.
AIO[1]	D3	Bi-directional	Programmable input/output line. Unused.
AIO[2][(a)]	C3	Bi-directional	Programmable input/output line. PIO[12]VM application interpreted Bluetooth TX enable.[(b)]

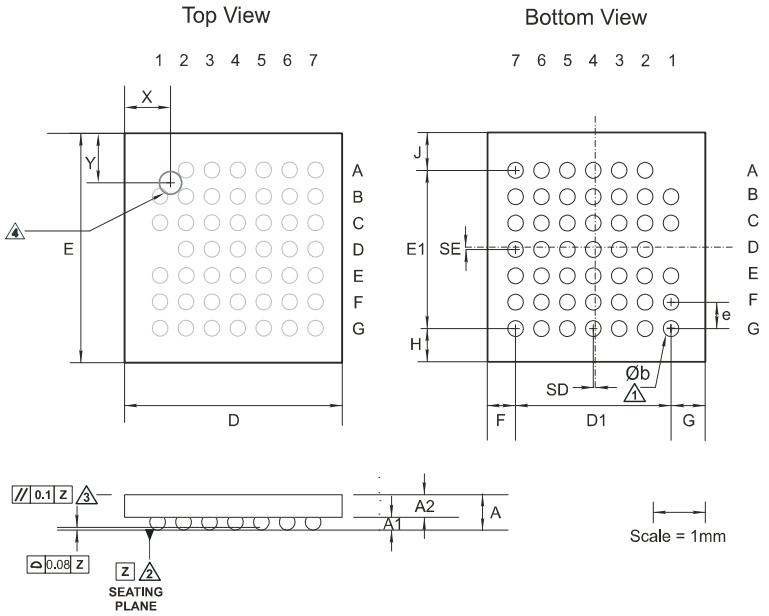
[(a)] AIOs set up to function as PIOs, PIO[12] for example, are a bad choice as it is possible for it to be connected to logic values in the chip at boot time.

[(b)] CSR do not recommend using PIO[12]. It causes some CSR tests to fail as it is internally tied to ground at boot time, but will not be used for tests in future ROMs.

Power Supplies Control	Ball	Pad Type	Description
VREG_IN	A2	Regulator input	Regulator input
VDD_USB	A5	VDD	Positive supply USB port and AIOs
VDD_PIO	G4	VDD	Positive supply for PIO [3:0] and [10:8]
VDD_PADS	D6	VDD	Positive supply for all digital Input/ Output ports and PIO[7:4]
VDD_CORE	C6	VDD	Positive supply for internal digital circuitry
VDD_LO	B2	VDD	Positive supply for VCO and synthesiser circuitry
VDD_RADIO	C2	VDD	Positive supply for RF circuitry
VDD_ANA	A4	VDD/Regulator output	Positive supply for analogue circuitry and 1.8V regulated output
VSS_DIG	C7	VSS	Ground connection for internal digital circuitry and digital ports
VSS_PADS	G3	VSS	Ground connection for digital ports
VSS_RADIO	C1	VSS	Ground connections for RF circuitry
VSS_ANA	B4	VSS	Ground connections for analogue circuitry
VSS_LO	B1	VSS	Ground connection for VCO and synthesiser circuitry

Unconnected Terminals	Ball	Description
NC	A7, B6, B7, C4, C5, D4, D5, E4	Leave Unconnected

3.3 Package Dimensions



Description	47-Ball Chip Scale Package (CSP)			
Size	3.8 x 4.0 x 0.7mm			
Pitch	0.5mm			
Package Ball Land	Non solder mask defined. Land aperture 300µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A	0.61	0.67	0.70	1 Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.21	0.24	0.27	
A2		0.43		
b	0.25	0.30	0.35	2 Datum Z is defined by the spherical crowns of the solder balls
D	3.65	3.75	3.85	
E	3.85	3.95	4.05	
e		0.50		3 Parallelism measurement shall exclude any effect of mark on top surface of package
D1		3.00		
E1		3.00		
F	0.285	0.335	0.385	4 Polarity mark. The dimension of the polarity mark is 0.3mm diameter
G	0.365	0.415	0.465	
H	0.375	0.425	0.475	
J	0.475	0.525	0.575	
SD		0.04		
SE		0.05		
X		1		
Y		1		
JEDEC	MO-211			
Unit	mm			

Figure 3.2: 47-Ball 3.8 x 4.0 x 0.7mm, 0.5mm pitch WLCSP Package

3.4 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

4 Bluetooth Modem

4.1 RF Ports

4.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair and are available for both transmit and receive. On transmit their outputs are combined using an external balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally.

Both terminals present similar complex impedances that may require matching networks between them and the balun. Viewed from the chip, the outputs can each be modelled as an ideal current source in parallel with a lossy capacitor. An equivalent series inductance can represent the package parasitics.

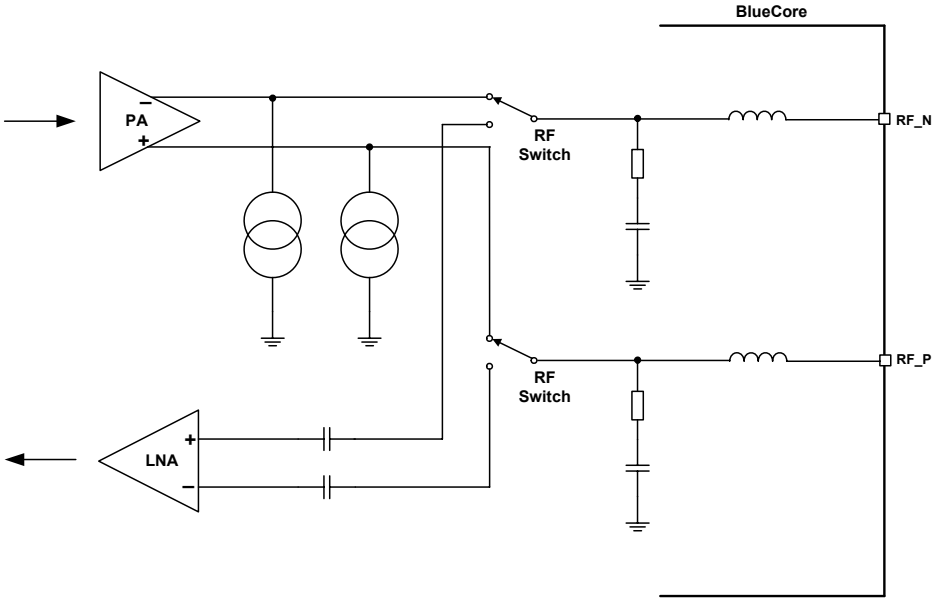


Figure 4.1: Simplified Circuit RF_N and RF_P

The DC level must be set at VDD_RADIO.

4.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore4-PC-ROM WLCSP to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

4.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

4.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

4.3 RF Transmitter

4.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise the frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

4.3.2 Power Amplifier

The internal PA has a maximum output power that allows BlueCore4-PC-ROM WLCSP to be used in Class 2 and Class 3 radios without an external RF PA.

4.3.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

An 8-bit voltage DAC (AUX_DAC) controls the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on-chip band gap and is virtually independent of temperature and supply voltage. Equation 4.1 and Equation 4.2 show the the output voltage:

$$V_{DAC} = \mathrm{MIN}\left(\left(3.7V \times \frac{EXT\_PA\_GAIN}{255} - 0.008 \times I\right),\ PIOSupply - 0.008 \times I\right)$$

Equation 4.1: Output Voltage with Load Current I

or

$$V_{DAC} = \mathrm{MIN}\left(\left(3.7V \times \frac{EXT\_PA\_GAIN}{255}\right),\ PIO\ Supply\right)$$

Equation 4.2: Output Voltage with No Load Current

Note:

PIOSupply = VDD_PIO

BlueCore4-PC-ROM WLCSP enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.

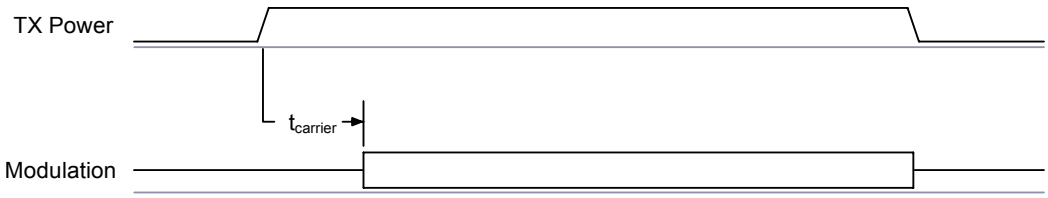


Figure 4.2: Internal Power Ramping

The PS Key PSKEY_TX_GAINRAMP (`0x1d`), is used to control the delay (in units of µs) between the end of the transmit power ramp and the start of modulation.

PS Key TXRX_PIO_CONTROL (0x209) controls external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose, as Table 4.1 shows.

TXRX_PIO_CONTROL Value	PIO and AUX_DAC Use
0	PIO[0], PIO[1], and AUX_DAC not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal.

Table 4.1: TXRX_PIO_CONTROL Values

4.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

4.5 Baseband

4.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

4.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/μ-law/linear voice data (from host)
- A-law/μ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR specification including AFH and eSCO.

4.6 Basic Rate Modem

The basic rate modem satisfies the basic data rate requirements of the Bluetooth v2.1 + EDR specification. The basic rate was the standard data rate available on the Bluetooth v1.2 specification and below, it is based on GFSK modulation scheme.

The inclusion of the basic rate modem allows BlueCore4-PC-ROM WLCSP compatibility with earlier Bluetooth products.

The basic rate modem uses the RF ports, receiver, transmitter and synthesiser, alongside the baseband components described in Section 4.5.

4.7 Enhanced Data Rate Modem

The EDR modem satisfies the requirements of the Bluetooth v2.1 + EDR specification. EDR has been introduced to provide 2x and 3x data rates with minimal disruption to higher layers of the Bluetooth stack. BlueCore4-PC-ROM WLCSP supports both the basic and enhanced data rates and is compliant with the Bluetooth v2.1 + EDR specification.

At the baseband level, EDR utilises both the same 1.6kHz slot rate and the 1MHz symbol rate as defined for the basic data rate. EDR differs in that each symbol in the payload portion of a packet represents 2 or 3-bits. This is achieved using two new distinct modulation schemes. Table 4.2 and Figure 4.3 summarise these. Link Establishment and management are unchanged and still use GFSK for both the header and payload portions of these packets.

The enhanced data rate modem uses the RF Ports, Receiver, Transmitter and Synthesiser, with the baseband components described in Section 4.5.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Data Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 4.2: Data Rate Schemes

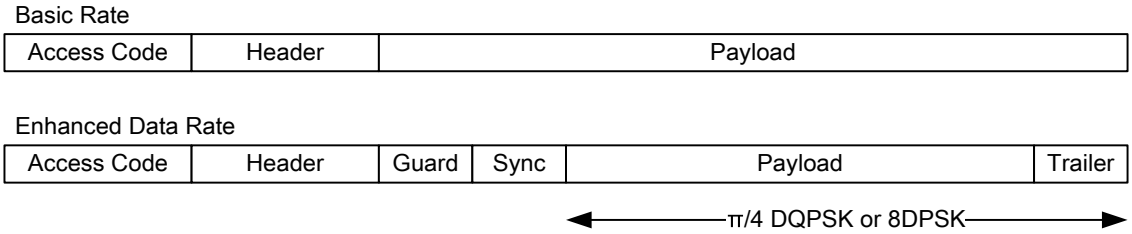


Figure 4.3: Basic Rate and Enhanced Data Rate Packet Structure

4.7.1 Enhanced Data Rate π/4 DQPSK

The 2x data rate for EDR uses a π/4-DQPSK. Each symbol represents 2-bits of information. Figure 4.4 shows the constellation. It has two planes, each having four points. Although it seems there are eight possible phase states, the encoding ensures that the trajectory of the modulation between symbols is restricted to the four states in the other plane.

For a given starting point, each phase change between symbols is restricted to 3π/4, π/4, -π/4 or -3π/4 radians (135°, 45°, -45° or -135°). For example, the arrows shown in Figure 4.4 represent trajectory to the four possible states in the other plane. Table 4.3 shows the phase shift encoding of symbols.

There are two main advantages in using π/4 DQPSK modulation:

- The scheme avoids the crossing of the origin (a π or -π phase shift) and therefore minimises amplitude variations in the envelope of the transmitted signal. This in turn allows the RF power amplifiers of the transmitter to be operated closer to their compression point without introducing spectral distortions. Consequently, the DC to RF efficiency is maximised.
- The differential encoding also allows for the demodulation without the knowledge of an absolute value for the phase of the RF carrier.

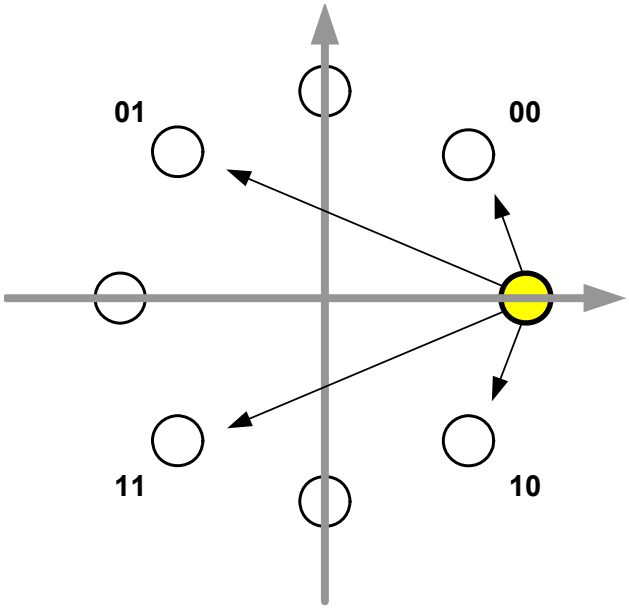


Figure 4.4: π/4 DQPSK Constellation Pattern

Bit Pattern	Phase Shift
00	π/4
01	3π/4
11	-3π/4
10	-π/4

Table 4.3: 2-Bits Determine Phase Shift Between Consecutive Symbols

4.7.2 Enhanced Data Rate 8DPSK

The 3x data rate modulation uses 8DPSK. Each symbol in the payload portion of the packet represents 3 baseband bits. Although it seems the 8DPSK is similar to π/4 DQPSK, the differential phase shifts between symbols are now permissible between any of the eight possible phase states. This reduces the separation between adjacent symbols on the constellation to π/4 (45°) and thereby reduces the noise and interference immunity of the modulation scheme. Nevertheless, because each symbol now represents 3 baseband bits, the actual throughput of the data is 3x when compared with the basic rate packet.

Figure 4.5 shows the 8DPSK constellation and Table 4.4 shows the phase encoding.

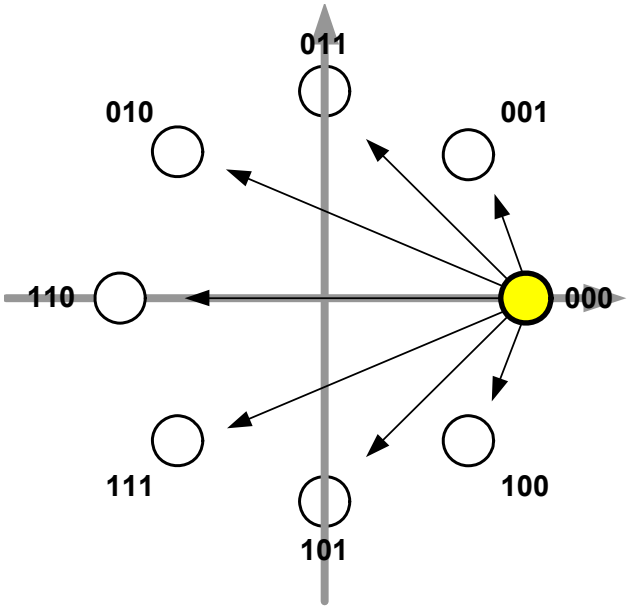


Figure 4.5: 8DPSK Constellation Pattern

Bit Pattern	Phase Shift
000	0
001	π/4
011	π/2
010	3π/4
110	π
111	-3π/4
101	-π/2
100	-π/4

Table 4.4: 3-Bits Determine Phase Shift Between Consecutive Symbols

5 Clock Generation

BlueCore4-PC-ROM WLCSP requires a Bluetooth reference clock frequency of 8MHz to 40MHz from either an externally connected crystal or from an external TCXO source.

All BlueCore4-PC-ROM WLCSP internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external 8MHz to 40MHz reference clock source or an internally generated watchdog clock frequency of 1kHz.

The Bluetooth operation determines the use of the watchdog clock in low-power modes.

5.1 Clock Architecture

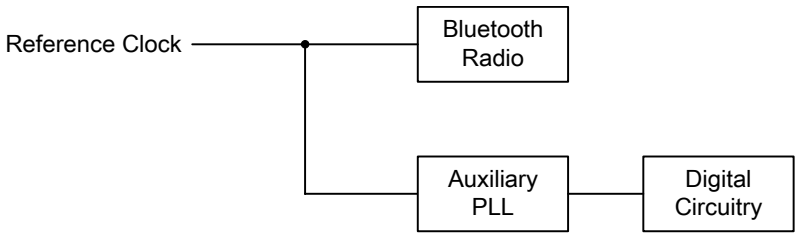


Figure 5.1: Clock Architecture

5.2 Input Frequencies and PS Key Settings

BlueCore4-PC-ROM WLCSP should be configured to operate with the chosen reference frequency. Do this by setting the PS Key PSKEY_ANA_FREQ (`0x01FE`) for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore4-PC-ROM WLCSP is 16MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

The following CDMA/3G phone TCXO frequencies are also catered for: 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. The value of the PS Key is a multiple of 1kHz, so 38.4MHz is selected by using a PS Key value of 38400.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (`0x1fe`) (kHz)
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 0.25	n x 250
26.00 (default)	26000

Table 5.1: PS Key Values for CDMA/3G Phone TCXO

5.3 External Reference Clock

5.3.1 Input (XTAL_IN)

The external reference clock is applied to the BlueCore4-PC-ROM WLCSP XTAL_IN input.

BlueCore4-PC-ROM WLCSP is configured to accept the external reference clock at XTAL_IN by connecting XTAL_OUT to ground. The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion. If peaks of the reference clock are either below VSS or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN.

The external reference clock signal should meet the specifications outlined in Table 5.2.

			Min	Typ	Max	Unit
Frequency[a]			8	16	40	MHz
Duty cycle			20:80	50:50	80:20	
Edge jitter (at zero crossing)			-	-	15	ps rms
Signal level	AC coupled sinusoid		400	-	VDD_ANA[b]	mV pk-pk
	DC coupled digital	V_{IL}	-	VSS[c]	-	V
		V_{IH}	-	VDD_ANA[b] [c]	-	V

Table 5.2: External Clock Specifications

[a] The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

[b] VDD_ANA is 1.8V nominal

[c] If driven via a DC blocking capacitor max amplitude is reduced to 750mV pk-pk for non 50:50 duty cycle

5.3.2 XTAL_IN Impedance in External Mode

The impedance of XTAL_IN does not change significantly between operating modes, typically 10fF. When transitioning from Deep Sleep to an active state a spike of up to 1pC may be measured. For this reason CSR recommends that a buffered clock input is used.

5.3.3 Clock Start-up Delay

BlueCore4-PC-ROM WLCSP hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore4-PC-ROM WLCSP firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1-31ms. Zero is the default entry for 5ms delay.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore4-PC-ROM WLCSP as low as possible. BlueCore4-PC-ROM WLCSP consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

5.3.4 Clock Timing Accuracy

As Figure 5.2 shows, the 250ppm timing accuracy on the external clock is required 2ms after the firmware begins to run. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.1 + EDR specification. Radio activity may occur after 6ms after the firmware starts. Therefore, at this point the timing accuracy of the external clock source must be within ±20ppm.

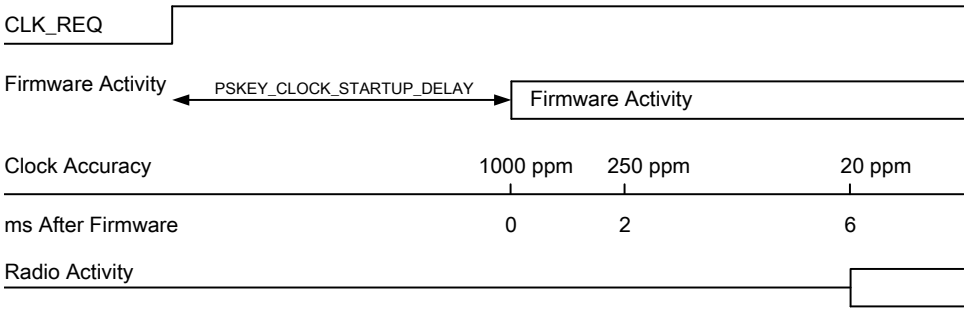


Figure 5.2: TCXO Clock Accuracy

5.3.5 External 32kHz Clock

A 32kHz clock can be applied to AIO[0] by setting PS Key `DEEP_SLEEP_EXTERNAL_CLOCK_SOURCE`.

If the external clock is applied to the analogue pad AIO[0], the digital signal should be driven with a maximum 1.8V.

Note:

If the 32kHz clock is accurate and stable to within 200ppm, then further power saving features can be enabled. See the relevant software release note for more information.

5.4 Crystal Oscillator (XTAL_IN, XTAL_OUT)

BlueCore4-PC-ROM WLCSP contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. The external crystal is connected to pins XTAL_IN, XTAL_OUT.

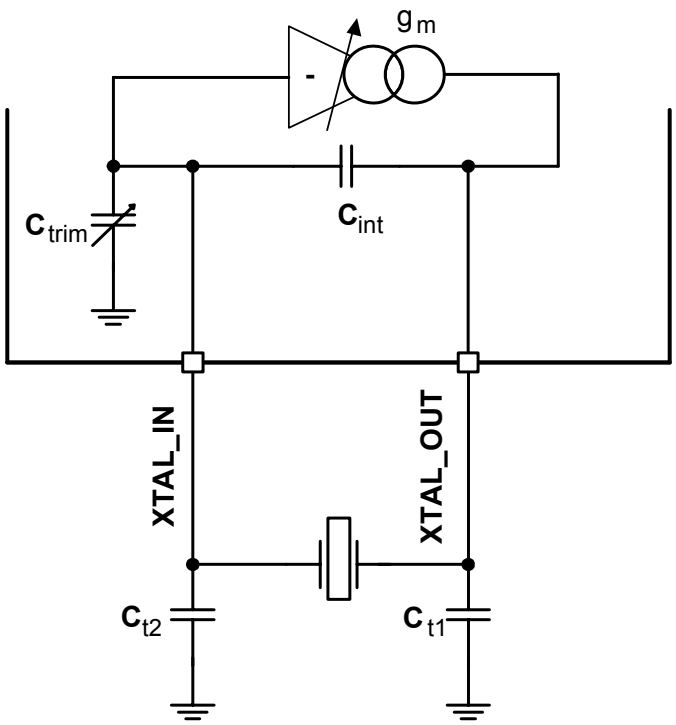


Figure 5.3: Crystal Driver Circuit

Figure 5.4 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

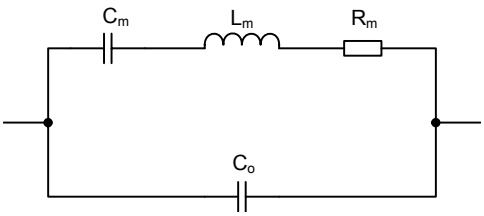


Figure 5.4: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore4-PC-ROM WLCSP contains variable internal capacitors to provide a fine trim.

Parameter	Min	Typ	Max	Unit
Frequency	8	16	40	MHz
Initial Tolerance	-	±25	-	ppm
Pullability	-	±20	-	ppm/pF
Transconductance	2.0	-	-	mS

Table 5.3: Crystal Specification

The BlueCore4-PC-ROM WLCSP driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

5.4.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore4-PC-ROM WLCSP provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing, hence slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated with Equation 5.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 5.1: Load Capacitance

Note:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

5.4.2 Frequency Trim

BlueCore4-PC-ROM WLCSP enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, C_{trim}. The value of C_{trim} is set by a 6-bit word in the PS Key PSKEY_ANA_FTRIM (`0x1f6`). Its value is calculated as follows:

$$C_{trim} = 125fF \times PSKEY\_ANA\_FTRIM$$

Equation 5.2: Trim Capacitance

The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of PSKEY_ANA_FTRIM.

Equation 5.3 describes the frequency trim.

$$\frac{\Delta (F_x)}{F_x} = \text{pullability} \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}} \right) \text{(ppm / LSB)}$$

Equation 5.3: Frequency Trim

Note:

F_x = crystal frequency

Pullability is a crystal parameter with units of ppm/pF.

Total trim range is 0 to 63.

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 5.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \bullet \frac{C_m}{2(C_l + C_0)^2}$$

Equation 5.4: Pullability

Note:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model). See Figure 5.4.

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

5.4.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore4-PC-ROM WLCSP uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit will oscillate if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 5.5.

$$g_m > 3 \frac{(2 \pi F_x)^2 R_m \left((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1} (C_{t2} + C_{trim}) \right)}{C_{t1} (C_{t2} + C_{trim})}$$

Equation 5.5: Transconductance Required for Oscillation

BlueCore4-PC-ROM WLCSP guarantees a transconductance value of at least 2mA/V at maximum drive level.

Note:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading.

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

5.4.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore4-PC-ROM WLCSP crystal driver circuit is based on a transimpedance amplifier, an equivalent negative resistance can be calculated for it using Equation 5.6.

$$R_{neg} > \frac{C_{t1} (C_{t2} + C_{trim})}{g_m (2 \pi F_x)^2 (C_0 + C_{int}) \left((C_{t1} + C_{t2} + C_{trim}) + C_{t1} (C_{t2} + C_{trim}) \right)^2}$$

Equation 5.6: Equivalent Negative Resistance

This formula shows the negative resistance of the BlueCore4-PC-ROM WLCSP driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

5.4.5 Crystal PS Key Settings

The BlueCore4-PC-ROM WLCSP firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. The PS Key PSKEY_XTAL_TARGET_AMPLITUDE (`0x24b`) is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

BlueCore4-PC-ROM WLCSP should be configured to operate with the chosen reference frequency.

6 Bluetooth Stack Microcontroller

A 16-bit RISC MCU is used for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

6.1 Programmable I/O (PIO) Parallel Ports

10 lines of programmable bi-directional I/O are provided.

Note:

PIO[0:3, 8, 10] are powered from VDD_PIO. AIO[0] and AIO[2] is powered from VDD_ANA.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. Using PS Key PSKEY_CLOCK_REQUEST_ENABLE (`0x246`), this terminal can be configured to be low when BlueCore4-PC-ROM WLCSP is in Deep Sleep and high when a clock is required.

Note:

CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

BlueCore4-PC-ROM WLCSP has 3 general-purpose analogue interface pins, AIO[0] and AIO[2], used to access internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 10-bit ADC. Signals selectable on this interface include the band gap reference voltage and a variety of clock signals: 64, 48, 32, 24, 16, 12, 8, 6 and 2MHz (output from AIO[0] only) and the XTAL and XTAL/2 clock frequency (output from AIO[0] and AIO[2]). When used with analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_ANA.

6.2 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore4-PC-ROM WLCSP where either device can turn on the clock without having to wake up the other device, see Figure 6.1. PIO[3] can be used as the host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore4-PC-ROM WLCSP.

Note:

To turn on the clock, the clock enable signal on PIO[3] must be high.

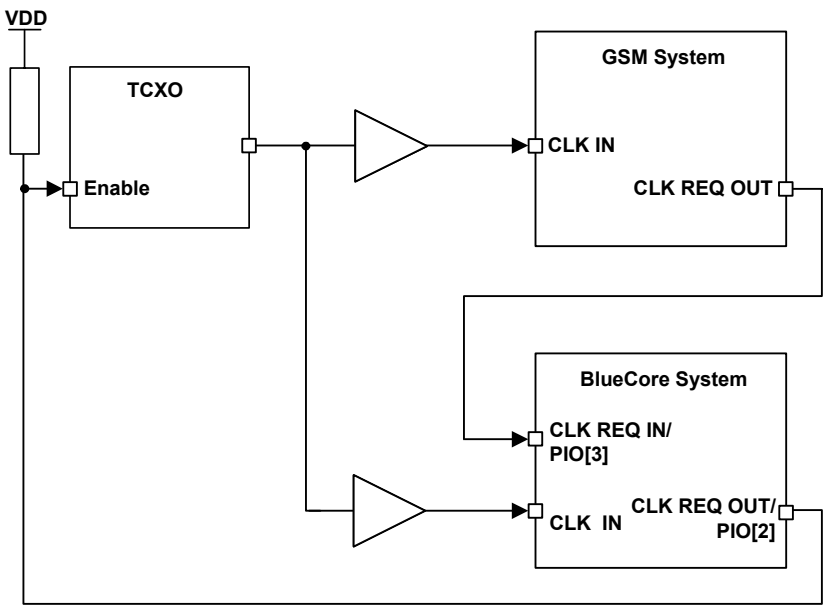


Figure 6.1: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] is tri-state. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

6.3 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware.

For more information see *Bluetooth and IEEE 802.11 b/g Coexistence Solutions Overview*.

7 Memory Interface and Management

7.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is transferred between BlueCore4-PC-ROM WLCSP and the air, or the host. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

7.2 System RAM

48Kbyte of on-chip RAM supports the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

7.3 Internal ROM

4Mbit of internal ROM is provided on the BlueCore4-PC-ROM WLCSP. This memory is provided for system firmware implimentation.

8 Serial Interfaces

8.1 USB Interface

BlueCore4-PC-ROM WLCSP has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on the BlueCore4-PC-ROM WLCSP acts as a USB peripheral, responding to requests from a master host controller.

BlueCore4-PC-ROM WLCSP supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)*, available from http://www.usb.org. For more information on how to integrate the USB interface on BlueCore4-PC-ROM WLCSP see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

8.2 Serial Peripheral Interface

The primary function of the SPI is for debug. BlueCore4-PC-ROM WLCSP uses a 16-bit data and 16-bit address SPI, where transactions may occur when the internal processor is running or is stopped. This section details the interface considerations for connection to BlueCore4-PC-ROM WLCSP.

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

8.2.1 Instruction Cycle

The BlueCore4-PC-ROM WLCSP is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 8.1 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 8.1: Instruction Cycle for an SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore4-PC-ROM WLCSP on the rising edge of the clock line SPI_CLK. When reading, BlueCore4-PC-ROM WLCSP replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore4-PC-ROM WLCSP offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

8.2.2 Writing to the Device

To write to BlueCore4-PC-ROM WLCSP, the 8-bit write command (00000010) is sent first (C[7:0]) followed by a 16-bit address (A[15:0]). The next 16-bits (D[15:0]) clocked in on SPI_MOSI are written to the location set by the address (A). Thereafter for each subsequent 16-bits clocked in, the address (A) is incremented and the data written to consecutive locations until the transaction terminates when SPI_CS# is taken high.

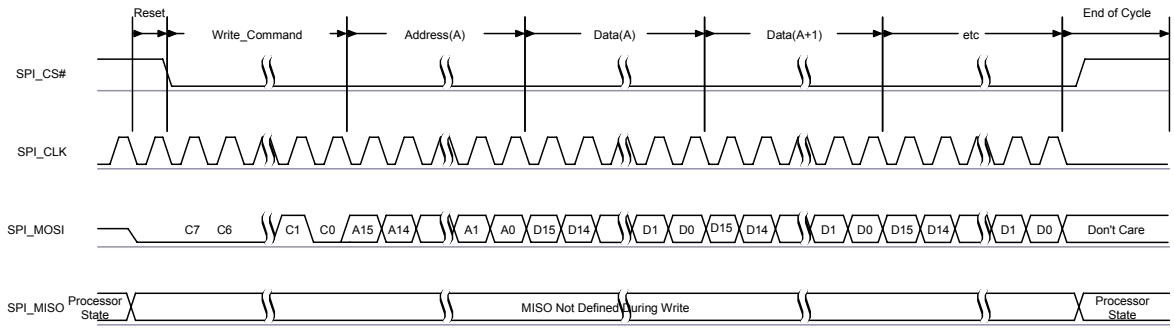


Figure 8.1: SPI Write Operation

8.2.3 Reading from the Device

Reading from BlueCore4-PC-ROM WLCSP is similar to writing to it. An 8-bit read command (00000011) is sent first (C[7:0]), followed by the address of the location to be read (A[15:0]). BlueCore4-PC-ROM WLCSP then outputs on SPI_MISO a check word during T[15:0] followed by the 16-bit contents of the addressed location during bits D[15:0].

The check word is composed of {command, address [15:8]}. The check word may be used to confirm a read operation to a memory location. This overcomes the problems encountered with typical serial peripheral interface slaves, whereby it is impossible to determine whether the data returned by a read operation is valid data or the result of the slave device not responding.

If SPI_CS# is kept low, data from consecutive locations is read out on SPI_MISO for each subsequent 16 clocks, until the transaction terminates when SPI_CS# is taken high.

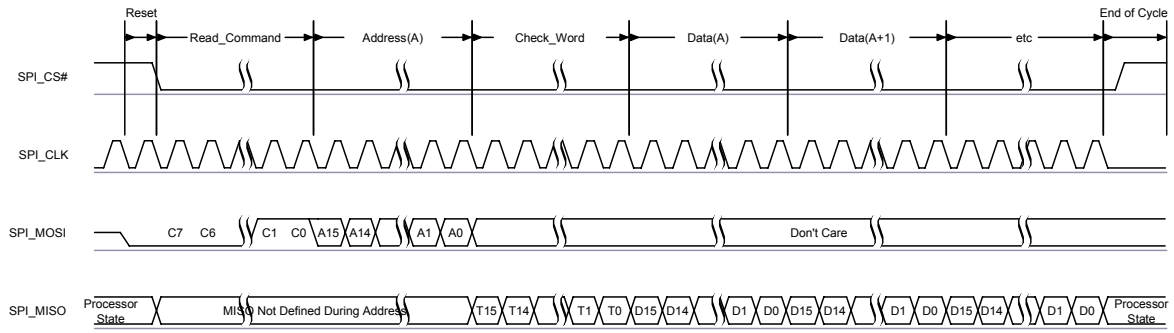


Figure 8.2: SPI Read Operation

8.2.4 Multi-slave Operation

BlueCore4-PC-ROM WLCSP should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore4-PC-ROM WLCSP is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BlueCore4-PC-ROM WLCSP outputs 0 if the processor is running or 1 if it is stopped.

8.3 I^{2}C Interface

PIO[8:6] is available to form a master I^{2}C interface. The interface is formed using software to drive these lines.

Note:

The program memory for the BlueCore4-PC-ROM WLCSP is internal ROM so the I^2C interface can only connect to a serial EEPROM, an example is shown in Figure 8.3. The EEPROM stores PS Keys and configuration information.

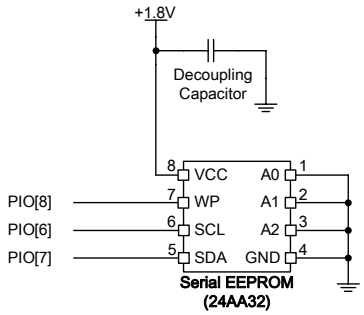


Figure 8.3: Example EEPROM Connection

9 Power Control and Regulation

9.1 Low-voltage Linear Regulator

The low-voltage linear regulator is available to power a 1.8V supply rail. Its output is connected internally to VDD_ANA, and can be connected externally to the other 1.8V power inputs.

If the low-voltage linear regulator is used a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground, should be connected to the output of the low-voltage linear regulator, VDD_ANA. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The low-voltage linear regulator is enabled by either:

- REG_EN pin
- BlueCore4-PC-ROM WLCSP device firmware

The low-voltage linear regulator is switched into a low power mode when the device is in deep-sleep mode, or in reset.

When the low-voltage linear regulator is not used the terminal REG_IN must be left unconnected, or tied to VDD_ANA.

9.2 Power Sequencing

The 1.8V supply rails are VDD_ANA, VDD_CORE, VDD_LO and VDD_RADIO. CSR recommends that these supply rails are all powered at the same time.

The digital I/O supply rails are VDD_PIO, VDD_PADS and VDD_USB.

The sequence of powering the 1.8V supply rails relative to the digital I/O supply rails is not important. If the digital I/O supply rails are powered before the 1.8V supply rails, all digital I/Os will have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_LO and VDD_RADIO can connect directly to a 1.8V supply.

A simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The digital I/O supply rails are connected together or independently to an appropriate voltage rail. Decoupling of the digital I/O supply rails is recommended.

9.3 External Voltage Source

If any of the supply rails for BlueCore4-PC-ROM WLCSP are supplied from an external voltage source, rather than one of the internal voltage regulators, then it is recommended that VDD_LO and VDD_RADIO should have less than 10mV rms noise levels between 0 to 10MHz. Also avoid single tone frequencies.

The transient response of any external regulator used should match or be better than the internal regulator available on BlueCore4-PC-ROM WLCSP, refer to regulator characteristics in Section 11. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels.

9.4 Voltage Regulator Enable Pins

The regulator enable pin, REG_EN, enables the BlueCore4-PC-ROM WLCSP device if the on-chip regulator, Low-voltage Linear Regulator, is used.

REG_EN pin is active high, with a logic threshold of around 1V, and a weak pull-down. It can tolerate voltages up to 4.9V, so can be connected directly to a battery to enable the device.

When the voltage regulator enable pin is pulled high the Low-voltage Linear Regulator is enabled, allowing the BlueCore4-PC-ROM WLCSP to boot-up. The firmware can then latch the regulator on and the regulator enable pin may be released.

9.5 Reset (RST#)

BlueCore4-PC-ROM WLCSP can be reset from several sources:

- RST# pin
- Power-on reset
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RST# being active. CSR recommends that RST# be applied for a period greater than 5ms.

The power-on reset typically occurs when the VDD_CORE supply falls below 1.26V and is released when VDD_CORE rises above typically 1.31V. At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. Following a reset, BlueCore4-PC-ROM WLCSP assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore4-PC-ROM WLCSP is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore4-PC-ROM WLCSP free runs, again at a safe frequency.

9.5.1 Digital Pin States on Reset

Table 9.1 shows the pin states of BlueCore4-PC-ROM WLCSP on reset. Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
USB_DP	Digital bi-directional	N/a	N/a
USB_DN	Digital bi-directional	N/a	N/a
SPI_MOSI	Digital input with PD	PD	PD
SPI_CLK	Digital input with PD	PD	PD
SPI_CS#	Digital bi-directional with PD	PD	PD
SPI_MISO	Digital tri-state output with PD	PD	PD
RST#	Digital input with PU	PU	PU
TEST_EN	Digital input with PD	PD	PD
PIO[0:3, 8, 10] PIO[4:7]	Digital bi-directional with PU/ PD	PD	PD

Table 9.1: Pin States on Reset

9.5.2 Status after Reset

The chip status after a reset is as follows:

- Warm reset: data rate and RAM data remain available
- Cold reset: data rate and RAM data not available

9.6 Bluetooth Advanced Power Management

Increase's in system power consumption can be contributed to polling activities of USB subsystems. Limiting USB polling to only those times that actual data is ready on the Bluetooth module would reduce the impact Bluetooth has on overall system power consumption. But USB is by design a polled bus. Enter CSR's Bluetooth Advanced Power Management.

CSR's Bluetooth APM feature reduce's the USB polling of internally connected Bluetooth modules to only those instances where the module has data ready. The main component of CSR's Bluetooth APM feature is a WDF filter driver, `CsrAPM.sys`. `CsrAPM.sys` sits between the Microsoft Bluetooth stack and the USB subsystem and modifies the polling behaviour of Bluetooth by deferring USB polling until Bluetooth data is available, thereby increasing the opportunity for the CPU to enter the low power C3 state.

Bluetooth protocol stacks issue USB polling IRPs whenever it sees connected Bluetooth devices, even if the devices are currently idle. `CsrAPM.sys` allows the CPU to be in its low power C3 state by suspending specific USB polling IRPs issued by the Bluetooth stack to the USB subsystem when it determines Bluetooth is idle. The Bluetooth module uses a hardware PIO line connected to an ACPI chipset as a 'sideband' signal to the ACPI subsystem telling it that Bluetooth data is available. The ACPI subsystem passes this indication on to `CsrAPM.sys` via call-back functionality in the CSR filter driver. Figure 9.1 provides an overview of the Bluetooth APM feature.

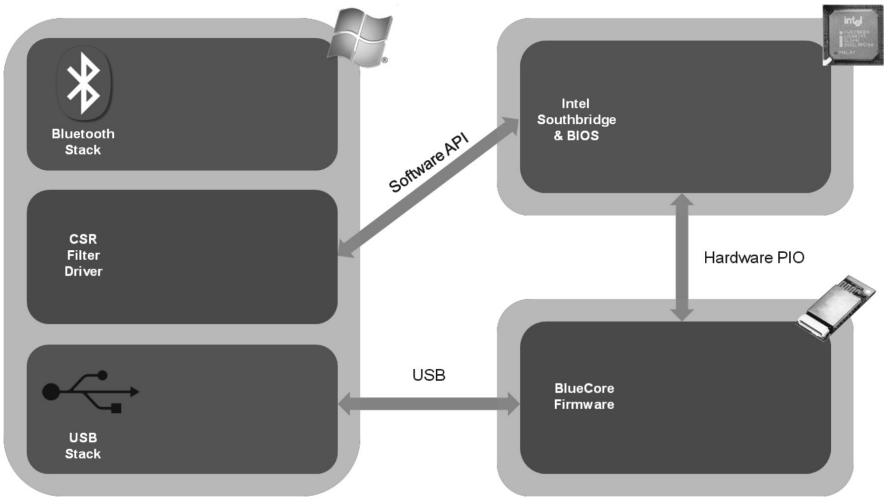


Figure 9.1: Bluetooth APM Feature Architecture

`CsrAPM.sys` is able to buffer IRPs from the Vista Bluetooth stack and suspend USB polling and not cause a loss of Bluetooth functionality due to sideband 'interrupt-like' feature provided by the CSR Bluetooth APM feature. Normally, if these IRPs are buffered the USB connected Bluetooth module will no longer be polled and USB data will be lost. However, with CSR's Bluetooth APM feature, the Bluetooth radio can send a signal to `CsrAPM.sys` that data is available and the data needs to be serviced. `CsrAPM.sys` issues the buffered IRP's and the USB subsystem retrieves the available data.

Figure 9.2 shows how the CPU C3 power state residency percentage increases to nearly 80% from 0% when the Bluetooth APM feature is enabled even though there are several Bluetooth devices connected to the system (stereo headset, keyboard and mouse). Without the Bluetooth APM feature, the CPU would be unable to enter the C3 power state and the C3 residency percentage would remain at 0%, having a dramatic impact on overall system power consumption.

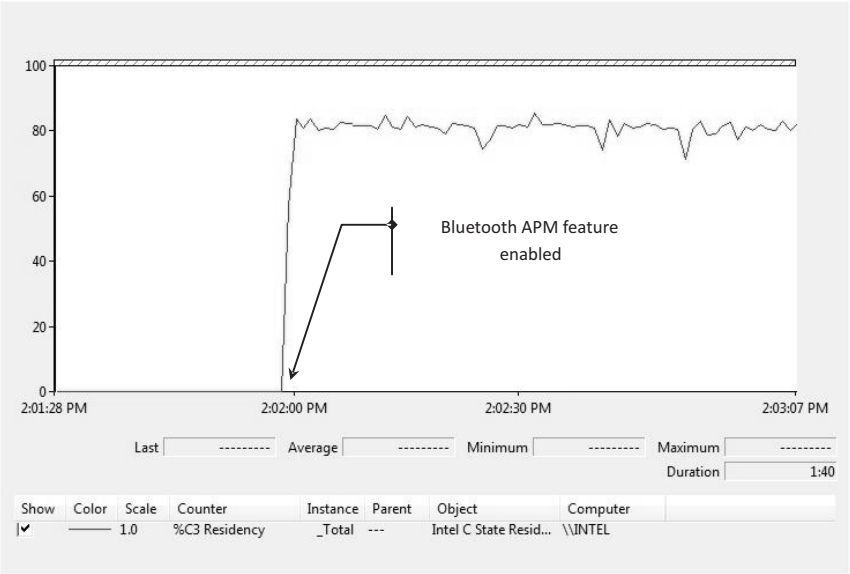


Figure 9.2: Bluetooth Impact on C3 Power State Residency %

10 Example Application Schematic

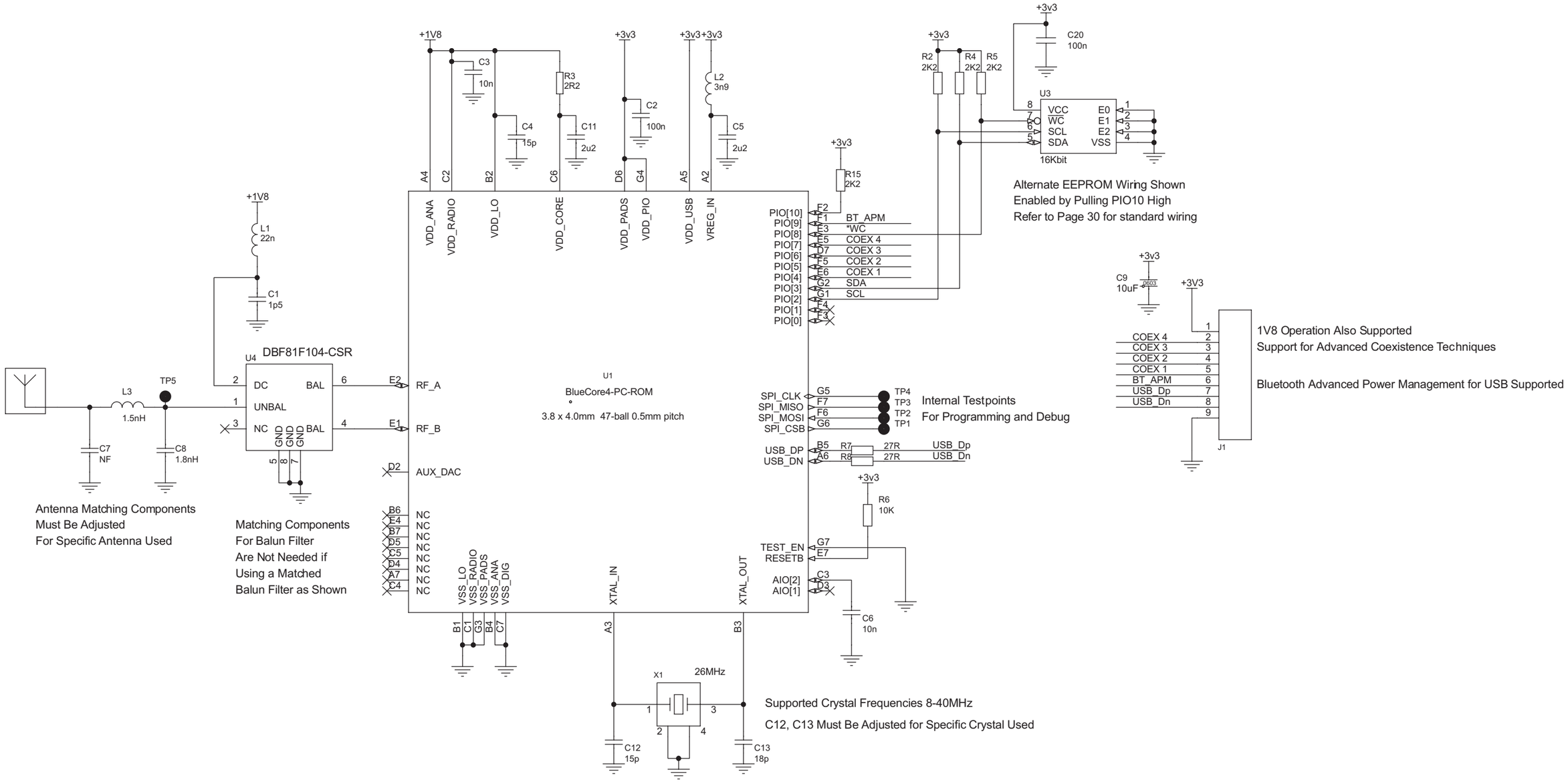


Figure 10.1: Example Application Schematic for BlueCore4-PC-ROM WLCSP

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature		-40	150	°C
Core Supply Voltage	VDD_ANA, VDD_CORE, VDD_LO and VDD_RADIO	-0.4	2.2	V
I/O Supply Voltage	VDD_PIO, VDD_PADS and VDD_USB	-0.4	3.7	V
Supply Voltage	REG_IN	-0.4	5.6	V
Other Terminal Voltages		VSS - 0.4	VDD + 0.4	V

11.2 Recommended Operating Conditions

Operating Condition		Min	Typ	Max	Unit
Operating Temperature Range[(a)]		-40	-	105	°C
Core Supply Voltage	VDD_ANA, VDD_CORE, VDD_LO and VDD_RADIO	1.7	1.8	1.9	V
I/O Supply Voltage	VDD_PIO, VDD_PADS and VDD_USB	1.7	3.3	3.6	V
Supply Voltage	REG_IN	2.2	-	4.2[(b)]	V

[(a)] For radio performance over temperature refer to BlueCore4-PC-ROM (WLCSP) Performance Specification.

[(b)] BlueCore4-PC-ROM operates up to the maximum supply voltage given in the Absolute Maximum Ratings, but RF performance is not guaranteed above 4.2V.

11.3 Input/Output Terminal Characteristics

Note:

For all I/O Terminal Characteristics:

- VDD_ANA, VDD_CORE, VDD_LO and VDD_RADIO at 1.8V unless shown otherwise.
- VDD_PIO, VDD_PADS and VDD_USB at 3.3V unless shown otherwise.
- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

11.3.1 Low-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.2	-	4.2	V
Output voltage (I_{load} = 70mA / REG_IN = 3.0V)	1.70	1.78	1.85	V
Temperature coefficient	-250	0	250	ppm/°C
Output noise[(a) (b)]	-	-	1	mV rms
Load regulation (I_{load} < 70mA)	-	-	50	mV/A
Settling time[(a) (c)]	-	-	50	µs
Maximum output current	70	-	-	mA
Minimum load current	5	-	-	µA
Drop-out voltage (I_{load} = 70mA)	-	-	350	mV
Quiescent current (excluding load, I_{load} < 1mA)	25	35	50	µA
Low Power Mode [(d)]				
Quiescent current (excluding load, I_{load} < 100µA)	4	7	10	µA
Disabled Mode [(e)]				
Quiescent current	TBD	TBD	TBD	nA

[(a)] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[(b)] Frequency range 100Hz to 100kHz

[(c)] 1mA to 115mA pulsed load

[(d)] The regulator is in low power mode when the chip is in deep sleep mode, or in reset

[(e)] Regulator is disabled when REG_IN is either open circuit or driven to the same voltage as VDD_ANA

11.3.2 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.40	1.50	1.60	V
VDD_CORE rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

11.3.3 Clocks

Clock Source	Min	Typ	Max	Unit
Crystal Oscillator				
Crystal frequency[(a)]	8	16	40	MHz
Digital trim range[(b)]	5.0	6.2	8.0	pF
Trim step size[(b)]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[(c)]	870	1500	2400	Ω
External Clock				
Input frequency[(d)]	8	16	40	MHz
Clock input level[(e)]	0.4	-	VDD_ANA	V pk-pk
Edge jitter (allowable jitter), at zero crossing	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

[(a)] Integer multiple of 250kHz

[(b)] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[(c)] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF.

[(d)] Clock input can be any frequency between 8MHz to 40MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

[(e)] Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN.

11.3.4 Digital Terminals

Supply Voltage Levels		Min	Typ	Max	Unit
Input Voltage Levels					
V_{IL} input logic level low	2.7V ≤ VDD ≤ 3.0V	-0.4	-	0.8	V
	1.7V ≤ VDD ≤ 1.9V	-0.4	-	0.4	V
V_{IH} input logic level high		0.7VDD	-	VDD+0.4	V
Output Voltage Levels					
V_{OL} output logic level low, I_{OL} = 4.0mA	2.7V ≤ VDD ≤ 3.0V	-	-	0.2	V
	1.7V ≤ VDD ≤ 1.9V	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	2.7V ≤ VDD ≤ 3.0V	VDD - 0.2	-	-	V
	1.7V ≤ VDD ≤ 1.9V	VDD - 0.4	-	-	V
Input and Tri-state Currents					
I_i input leakage current at V_{in} = VDD or 0V		-100	0	100	nA
I_{oz} tri-state output leakage current at V_o = VDD or 0V		-100	0	100	nA
With strong pull-up		-100	-40	-10	µA
With strong pull-down		10	40	100	µA
With weak pull-up		-5	-1.0	-0.2	µA
With weak pull-down		-0.2	+1.0	5.0	µA
C_I Input Capacitance		1.0	-	5.0	pF
Resistive Strength					
R_{puw} weak pull-up strength at VDD-0.2V		500k	-	2M	Ω
R_{pdw} weak pull-down strength at 0.2V		500k	-	2M	Ω
R_{pus} strong pull-up strength at VDD-0.2V		10k	-	50k	Ω
R_{pds} strong pull-down strength at 0.2V		10k	-	50k	Ω

11.3.5 USB

	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1	-	3.6	V
Input Threshold				
V_{IL} input logic level low	-	-	0.3 x VDD_USB	V
V_{IH} input logic level high	0.7 x VDD_USB	-	-	V
Input Leakage Current				
VSS < V_{IN} < VDD_USB[(a)]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

[(a)] Internal USB pull-up disabled

11.3.6 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	8	Bits
Input voltage range[(a)]		0	-	VDD_ANA	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain Error		-0.8	-	0.8	%
Input Bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[(b)]		-	-	700	Samples/s

[(a)] LSB size = VDD_ANA/255

[(b)] The auxilliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

11.3.7 Auxiliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Average output step size[(a)]	12.5	14.5	17.0	mV
Output Voltage		monotonic[(a)]		
Voltage range (I_O=0mA)	VSS	-	VDD_PIO	V
Current range	-10.0	-	0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO - 0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	1	µA
Offset	-220	-	120	mV
Integral non-linearity[(a)]	-2	-	2	LSB
Settling time (50pF load)	-	-	10	µs

[(a)] Specified for an output voltage between 0.2V and VDD_PIO - 0.2V. Output is high impedance when chip is in Deep Sleep mode.

12 HCI Power Consumption

Operation Mode	Connection Type	Average	Unit
Page scan, time interval 1.28s	-	0.43	mA
Inquiry and page scan	-	0.75	mA
ACL no traffic	Master	3.71	mA
ACL with file transfer	Master	8.44	mA
ACL no traffic	Slave	15.1	mA
ACL with file transfer	Slave	17.7	mA
ACL 40ms sniff	Master	1.58	mA
ACL 1.28s sniff	Master	0.14	mA
eSCO EV3 - Setting S1	Master	24.0	mA
SCO HV1	Master	36.3	mA
SCO HV3	Master	17.8	mA
SCO HV3 30ms sniff	Master	17.5	mA
ACL 40ms sniff	Slave	1.39	mA
ACL 1.28s sniff	Slave	0.26	mA
eSCO EV3 - Setting S1	Slave	22.7	mA
SCO HV1	Slave	35.7	mA
SCO HV3	Slave	22.7	mA
SCO HV3 30ms sniff	Slave	16.8	mA
Parked 1.28s beacon	Slave	0.19	mA
Standby Host connection[(a)]	-	36	µA
Reset (RST# low)[(a)]	-	49	µA

[(a)] Low-power mode on the linear regulator is entered and exited automatically when the chip enters/leaves Deep Sleep mode. For more information about the electrical characteristics of the linear regulator, see Section 11.3.1.

Note:

Conditions: 20°C, 1.8V supply

13 CSR Green Semiconductor Products and RoHS Compliance

13.1 RoHS Statement

BlueCore4-PC-ROM WLCSP where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the *Restriction of Hazardous Substance* (RoHS).

13.1.1 List of Restricted Materials

BlueCore4-PC-ROM WLCSP is compliant with RoHS in relation to the following substances:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- Polybrominated Biphenyl
- Polybrominated Diphenyl Ether

In addition, the following substances are not intentionally added to BlueCore4-PC-ROM WLCSP devices:

- Halogenated flame retardant
- Antinomy (Sb) and Compounds, including Antimony Trioxide flame retardant
- Polybrominated Diphenyl and Biphenyl Oxides
- Tetrabromobisphenol-A bis (2,3-dibromopropylether)
- Asbestos or Asbestos compounds
- Azo compounds
- Organic tin compounds
- Mirex
- Polychlorinated napthelenes
- Polychlorinated terphenyls
- Polychlorinated biphenyls
- Polychlorinated/Short chain chlorinated paraffins
- Polyvinyl Chloride (PVC) and PVC blends
- Formaldehyde
- Arsenic and compounds (except as a semiconductor dopant)
- Beryllium and its compounds
- Ethylene Glycol Monomethyl Ether or its acetate
- Ethylene Glycol Monoethyl Ether or its acetate
- Halogenated dioxins and furans
- Persistent Organic Pollutants (POP), including Perfluorooctane sulphonates
- Red phosphorous
- Ozone Depleting Chemicals (Class I and II): Chlorofluorocarbons (CFC) and Halons
- Radioactive substances

For further information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products.*

14 CSR Bluetooth Software Stack

BlueCore4-PC-ROM WLCSP is supplied with Bluetooth v2.1 + EDR specification compliant stack firmware, which runs on the internal RISC MCU.

The BlueCore4-PC-ROM WLCSP software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC MCU and an external host processor (if any). The upper layers of the Bluetooth stack, above the HCI, can be run either on-chip or on the host processor.

14.1 BlueCore HCI Stack

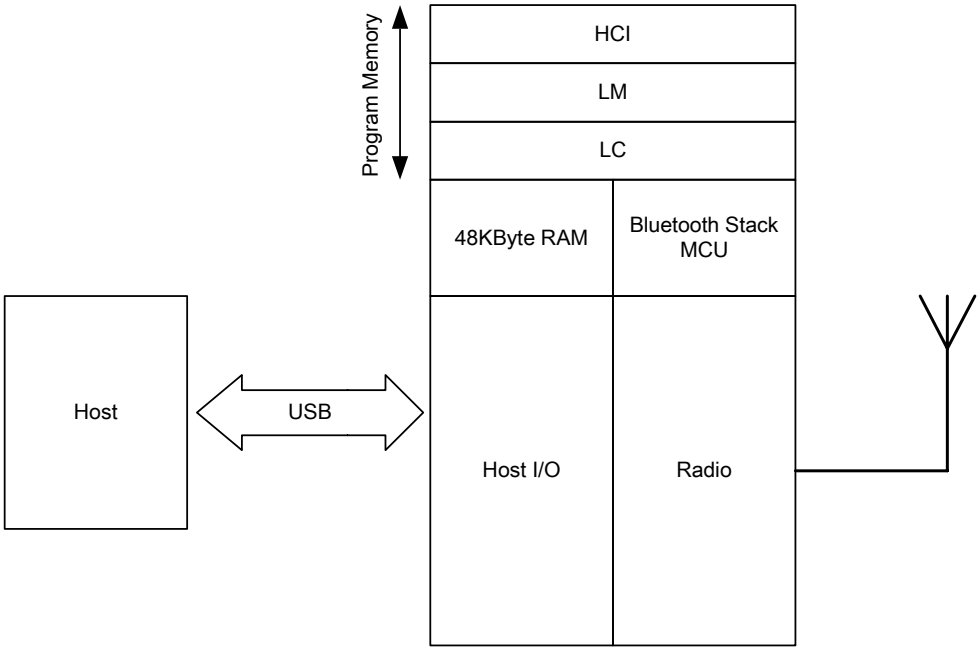


Figure 14.1: BlueCore HCI Stack

Note:

Program Memory in Figure 14.1 is internal ROM.

In the implementation shown in Section 14.1 the internal processor runs the Bluetooth stack up to the HCI. The Host processor must provide all upper layers including the application.

14.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v2.1 + EDR specification functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

As well as the following mandatory functions of Bluetooth v2.0 + EDR specification:

- *Adaptive frequency hopping* (AFH), including classifier
- Faster connection - enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

And optional Bluetooth v2.0 + EDR specification functionality:

- AFH as Master and Automatic Channel Classification
- Fast Connect - Interlaced Inquiry and Page Scan plus RSSI during Inquiry
- *Extended SCO* (eSCO), eV3 +CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.1 + EDR specification:

- Bluetooth components:
  - Baseband (including LC)
  - LM
  - HCI
- Standard HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps
- Operation with up to seven active slaves[1]
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7
- Maximum number of simultaneous active SCO connections: 3[2]
- Operation with up to three SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/Slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

14.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called *BlueCore Command* (BCCMD), provides:
  - Access to BlueCore4-PC-ROM WLCSP general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of BlueCore4-PC-ROM WLCSP external pins. This is normally used to build a battery monitor
- A block of BCCMD commands provides access to the BlueCore4-PC-ROM WLCSP *Persistent Store* (PS) configuration database . The database sets the BlueCore4-PC-ROM WLCSP Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, *link manager* (LM), etc.
- A block of Bluetooth radio test or BIST commands allows direct control of the BlueCore4-PC-ROM WLCSP radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: Shallow Sleep and Deep Sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI.

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

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[1] This is the maximum allowed by Bluetooth v2.1 + EDR specification.

[2] BlueCore4-PC-ROM WLCSP supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.1 + EDR specification.

15 Ordering Information

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
USB	WLCSP 47-Ball (Pb free)	3.8 x 4.0 x 0.7mm, 0.5mm pitch	Tape and reel	BC0401PC08-IXB-R[(a)] [(b)]

[(a)] Until BC0401PC08-1x13 reaches **Production** status, engineering samples order number applies. This is BC0401PC08-ES-IXB-E, with no minimum order quantity.

[(b)] BlueCore4-PC-ROM WLCSP is a ROM-based device where the product code has the form BC0401PCxx. xx is the specific ROM-variant, 08 is the ROM-variant for BC0401PC08-IXB-R.

Note:

At **Production** status **Minimum Order Quantity** is 2kpcs taped and reeled.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts

15.1 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

16 Document References

Document	Reference, Date
BlueCore4-PC-ROM WLCSP Performance Specification	CS-123972-SP
Bluetooth and IEEE 802.11 b/g Coexistence Solutions Overview	bcore-an-066P
Bluetooth and USB Design Considerations	CS-101412-AN
Core Specification of the Bluetooth System	v2.1 + EDR, 26 July 2007
Environmental Compliance Statement for CSR Green Semiconductor Products	CB-001036-ST
IC Packing and Labelling Specification	CS-112584-SPP
Selection of I^2C EEPROMS for Use with BlueCore	bcore-an-008P
Test Suite Structure (TSS) and Test Purposes (TP) System Specification 1.2/2.0/2.0 + EDR/ 2.1/2.1 + EDR	RF.TS/2.1.E.0, 27 December 2006
Typical Solder Reflow Profile for Lead-free Devices Information Note	CS-116434-AN
Universal Serial Bus Specification	v2.0, 27 April 2000

Terms and Definitions

Term	Definition
8DPSK	8 phase Differential Phase Shift Keying
π/4 DQPSK	π/4 rotated Differential Quaternary Phase Shift Keying
ADC	Analogue to Digital Converter
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIO	Asynchronous Input/Output
BCCMD	BlueCore Command
BIST	Built-In Self Test
BlueCore®	Group term for CSR's range of Bluetooth wireless technology ICs
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
BT	Bluetooth
CDMA	Code Division Multiple Access
CRC	Cyclic Redundancy Check
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DC	Direct Current
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory
eSCO	Extended SCO
ESR	Equivalent Series Resistance
FHS	Frequency Hop Synchronisation
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GSM	Global System for Mobile communications
HCI	Host Controller Interface
IQ	In-Phase and Quadrature
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
IF	Intermediate Frequency
IRPs	I/O request packets
LC	An inductor (L) and capacitor (C) network
LED	Light-Emitting Diode
LM	Link Manager
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
MCU	Micro Controller Unit
MMU	Memory Management Unit
PA	Power Amplifier
PIO	Programmable Input Output

Term	Definition
PS	Persistent Store
PS Key	Persistent Store Key
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RX	Receive or Receiver
SCO	Synchronous Connection-Oriented
TBD	To Be Defined
TCXO	Temperature Compensated crystal Oscillator
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
W-CDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WLCSP	Wafer Level Chip Scale Package