PCI32 4000 Master & Slave Interfaces Version 2.0

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Introduction

With Xilinx LogiCORE PCI32 4000 Master and Slave interfaces Version 2.0, a designer can build a customized, 32 bit, 33 MHz fully PCI compliant system with the highest possible sustained performance, 132 Mbytes/s, and up to 124,000 system gates in a XC4000XLT FPGA.

Features

- Fully 2.1 PCI compliant 32 bit, 33 MHz PCI Interface
  - Master (Initiator/Target)
  - Slave (Target-only)
- Programmable single-chip solution with customizable back-end functionality
- Pre-defined implementation for predictable timing in Xilinx XC4000XLT FPGAs or HardWire™ FpgASICs (see *LogiCORE Facts* for listing of supported devices)
- Incorporates Xilinx Smart-IP Technology
- 3.3 V Operation with XC4000XLT devices
- Zero wait-state burst operation
- Fully verified design
  - Tested with the Xilinx internal testbench
  - Tested in hardware (proven in FPGAs and HardWire devices)
- Configurable on-chip dual-port FIFOs can be added for maximum burst speed (see *Xilinx Documents* section)
- Design Once™ - automatic conversion to a HardWire FpgASIC for cost reduction
- Supported Initiator functions (PCI Master only)
  - Initiate Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL) commands
  - Initiate I/O Read, I/O Write commands
  - Initiate Configuration Read, Configuration Write commands
  - Bus Parking
  - Basic Host Bridging

LogiCORE™ Facts

Core Specifics	
Device Family	XC4000XLT
CLBs Used	178 - 308
IOBs Used[1]	53/51
System Clock f_{max}	0 - 33MHz
Device Features Used	Bi-directional data buses SelectRAM™ (optional user FIFO) Boundary scan (optional)

Supported Devices/Resources Remaining		
	I/O[1,2]	**CLB**[3]
XC4013XLT PQ208	99/101	268 - 398
XC4013XLT PQ240	133/135	268 - 398
XC4028XLT HQ240	133/135	716 - 846
XC4062XLT HQ240	133/135	1996 - 2126
XC4062XLT BG432	293/295	1996 - 2126

Provided with Core	
Documentation	*PCI32 User's Guide* *PCI Data Book*
Design File Formats	VIEW*logic* schematics VHDL, Verilog Simulation Model NGO Netlist[4]
Constraint Files	M1 User Constraint File (UCF) M1 Guide files
Verification Tools	VIEW*logic* command files VHDL Testbench Verilog Testbench
Core Symbols	VIEW*logic*, VHDL, Verilog
Reference designs & application notes	Example design: Ping Reference Design[5] Synthesizable PCI Bridge
Additional Items	Reference book: *PCI System Architecture*

Design Tool Requirements	
Xilinx Core Tools	M1.4
Entry/Verification Tools[6]	For CORE instantiation: VHDL, Verilog, Schematic For changing source files: Workview Office V7.1.2 or V7.2

Notes: See next page.

LogiCORE™ Facts (cont.)

Support
Xilinx provides technical support for this LogiCORE™ product when used as described in the User's Guide or supporting Application Notes. Xilinx cannot guarantee timing, functionality, or support of the product if implemented in devices not listed above, or customized beyond that referenced in the product documentation, or if any changes are done in sections of the design marked as "DO NOT MODIFY".

Notes:
1. Master/Slave.
2. The XLT devices use 8 I/O locations for Vtt pins; see XC4000XLT Data Sheet.
3. The exact number of CLBs depends on user configuration of the core and level of resource sharing with adjacent logic. Factors that can affect the size of the design are number and size of the BARs, zero vs. one wait-state, and medium vs. slow decode. These numbers include a 16 x 32 FIFO.
4. Available on Xilinx Home Page, in the LogiCORE PCI Lounge: www.xilinx.com/products/logicore/pci/pci_sol.htm
5. Slave only.
6. See Xilinx Home Page for supported EDA tools.

Features (cont.)

- Supported Target functions (PCI Master and Slave)
  - Type 0 Configuration Space Header
  - Up to 3 Base Address Registers (memory or I/O with adjustable block size from 16 bytes to 2 GBytes, slow or medium decode speed)
  - Parity Generation (PAR), Parity Error Detection (PERR# and SERR#)
  - Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Real Line (MRL), Memory Write, Invalidate (MWI) commands
  - I/O Read, I/O Write commands
  - Configuration Read, Configuration Write commands
  - 32-bit data transfers, burst transfers with linear address ordering
  - Target Abort, Target Retry, Target Disconnect
  - Full Command/Status Register
- Available for configuration and download on the Web
  - Web-based configuration with intuitive GUI
  - Generation of proven design files

Applications

- PCI add-in boards such as graphic cards, video adapters, LAN adapters and data acquisition boards
- Embedded applications within telecommunication and industrial systems
- CompactPCI boards
- Other applications that need PCI

General Description

The LogiCORE™ PCI32 4000 Master and Slave Interfaces V2.0 are pre-implemented and fully tested modules for Xilinx XC4000XLT FPGAs (see *LogiCORE Facts* for listing of supported devices). The pin-out and the relative placement of the internal Configurable Logic Blocks (CLBs) are predefined. Critical paths are controlled by TimeSpecs and guide files to ensure that timing is always met. This significantly reduces engineering time required to implement the PCI portion of your design. Resources can instead be

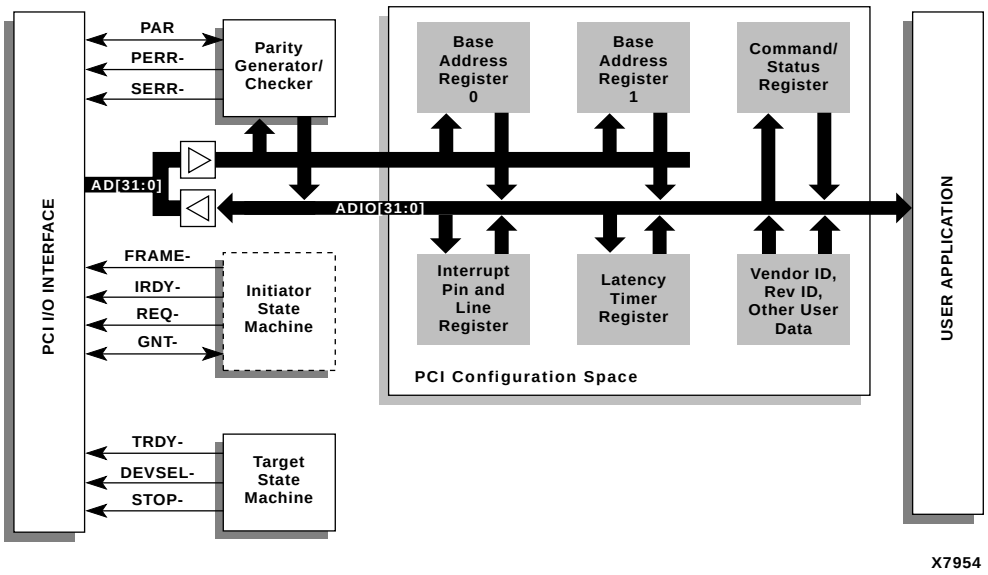


Figure 1: LogiCORE™ PCI32 4000 Interface Block Diagram (BAR 2 not shown)

focused on the unique back-end logic in the FPGA and the system level design. As a result, the LogiCORE™ PCI products can cut your development time by several months.

Xilinx XC4000XLT Series FPGAs enable designs of fully PCI-compliant systems. The devices meet all required electrical and timing parameters including AC output drive characteristics, input capacitance specifications (10pF), 7 ns setup and 0 ns hold to system clock, and 11 ns system clock to output. These devices meet all specifications for 3.3 V PCI. Although the XLT devices have a 3V driver they can be used in a 5V PCI system and meet timing for up to 8 loads.

The XC4000XLT devices differ from regular XL devices by the addition of clamp diodes, required by the PCI 3.3 V electrical specification. For more details about this see the *XC4000XLT FPGA Data Sheet*.

The PCI Compliance Checklist (later in this databook) has additional details about electrical compliance. Other features that enable efficient implementation of a complete PCI system in the XC4000XLT includes:

- Select-RAM™ memory: on-chip ultra-fast RAM with synchronous write option and dual-port RAM option. Used in the PCI Interfaces to implement the FIFO.
- Individual output enable for each I/O
- Internal 3-state bus capability
- 8 global low-skew clock or signal distribution networks
- IEEE 1149.1-compatible boundary scan logic support

The module is carefully optimized for best possible performance and utilization in the XC4000XLT FPGA architecture. When implemented in the XC4013, more than 50% of the FPGA's resources remain for integrating a unique back-end interface and other system functions into a fully programmable one-chip solution. When implemented in a XC4062, 90% of the FPGA's resources remain.

Xilinx DesignOnce™ service allows an automatic conversion to a low cost HardWire™ device for high-volume production.

Smart-IP Technology

Drawing on the architectural advantages of Xilinx FPGAs, new Xilinx Smart-IP technology ensures highest performance, predictability, repeatability, and flexibility in PCI designs. The Smart-IP technology is incorporated in every LogiCORE PCI Core.

Xilinx Smart-IP technology leverages the Xilinx architectural advantages, such as look-up tables (LUTs), distributed RAM, and segmented routing, and floorplanning information, such as logic mapping and relative location constraints. This technology provides the best physical layout, predictability, and performance. Additionally, these predetermined features allow for significantly reduced compile times over competing architectures.

The PCI32 Spartan Interface can parameterized, allowing for design flexibility in which users can create the exact PCI interface needed. PCI Cores made with Smart-IP technology are unique by maintaining their performance and predictability regardless of the device size.

Functional Description

The LogiCORE PCI32 4000 Interfaces are partitioned into five major blocks, plus the user application, shown in Figure 1. Each block is described below.

PCI I/O Interface Block

The I/O interface block handles the physical connection to the PCI bus including all signaling, input and output synchronization, output three-state controls, and all request-grant handshaking for bus mastering.

Parity Generator/Checker

Generates/checks even parity across the AD bus, the CBE lines, and the PAR signal. Reports data parity errors via PERR- and address parity errors via SERR-.

Target State Machine

This block manages control over the PCI interface for Target functions. The states implemented are a subset of equations defined in "Appendix B" of the *PCI Local Bus Specification*. The controller is a high-performance state machine using state-per-bit (one-hot) encoding for maximum performance. State-per-bit encoding has narrower and shallower next-state logic functions that closely match the Xilinx FPGA architecture.

Initiator State Machine (PCI Master only)

This block manages control over the PCI interface for Initiator functions. The states implemented are a subset of equations defined in "Appendix B" of the *PCI Local Bus Specification*. The Initiator Control Logic also uses state-per-bit encoding for maximum performance.

PCI Configuration Space

This block provides the first 64 bytes of Type 0, version 2.1, Configuration Space Header (CSH) (see Table 1) to support software-driven "Plug-and Play" initialization and configuration. This includes Command, Status, and three Base Address Registers (BARs). BAR 2 is not shown in figure 1. These BARs illustrate how to implement memory- or I/O-mapped address spaces. Each BAR sets the base address for the interface and allows the system software to determine the addressable range required by the interface. Using a combination of Configurable Logic Block (CLB) flip-flops for the read/write registers and CLB look-up tables for the read-only registers results in optimized packing density and layout.

With this release, the hooks for extending configuration space has been built into the backend interface. These hooks, including the ability to implement a CapPtr in configuration space, allows the user to implement functions such as Advanced Configuration and Power Interface (ACPI) in the backend design.

Table 1: PCI Configuration Space Header

31 16	15 0	
Device ID	Vendor ID	00h
Status	Command	04h
Class Code	Rev ID	08h
BIST / Header Type	Latency Timer / *Cache Line Size*	0Ch
Base Address Register 0 (BAR0)		10h
Base Address Register 1 (BAR1)		14h
Base Address Register 2 (BAR2)		18h
Base Address Register 3 (BAR3)		1Ch
Base Address Register 4 (BAR5)		20h
Base Address Register 5 (BAR5)		24h
Cardbus CIS Pointer		28h
Subsystem ID	Subsystem Vendor ID	2Ch
Expansion ROM Base Address		30h
Reserved	CapPtr	34h
Reserved		38h
Max_Lat / Min_Gnt / Interrupt Pin / Interrupt Line		3Ch
Reserved		40h-FFh

Note:
Italicized address areas are not implemented in the LogiCORE PCI32 4000 Interface default configuration. These locations return zero during configuration read accesses.

User Application with Optional Burst FIFOs

The LogiCORE PCI32 4000 Interfaces provide a simple, general-purpose interface with a 32-bit data path and latched address for de-multiplexing the PCI address/data bus. The general-purpose user interface allows the rest of the device to be used in a wide range of applications.

Typically, the user application contains burst FIFOs to increase PCI system performance (An Application Note is available, please see the *Xilinx Documents* section). An on-chip read/write FIFO, built from the on-chip synchronous dual-port RAM (SelectRAM™) available in XC4000XLT devices, supports data transfers in excess of 33 MHz.

Interface Configuration

The LogiCORE PCI32 4000 Interfaces can easily be configured to fit unique system requirements using Xilinx web-based graphical configuration tool or changing the VHDL, Verilog, or VIEW*logic* configuration file. The following customization is supported by the LogiCORE product and described in accompanying documentation.

- Initiator or target functionality (PCI Master only)
- Base Address Register configuration (1 - 3 Registers, size and mode)
- Configuration Space Header ROM
- Initiator and target state machine (e.g., termination conditions, transaction types and request/transaction arbitration)
- Burst functionality
- User Application including FIFO (back-end design)

Table 2: PCI Bus Commands

CBE [3:0]	Command	PCI Master	PCI Slave
0000	Interrupt Acknowledge	No[1]	Ignore
0001	Special Cycle	No[1]	Ignore
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	Ignore	Ignore
1001	Reserved	Ignore	Ignore
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	No[1]	Ignore
1110	Memory Read Line	Yes	Yes
1111	Memory Write Invalidate	No[1]	Yes

Note:
1. The Initiator can present these commands, however, they either require additional user-application logic to support them or have not been thoroughly tested.

Supported PCI Commands

Table 2 illustrates the PCI bus commands supported by the LogiCORE™ PCI32 4000 Interfaces. The PCI Compliance Checklist, found later in this data book, has more details on supported and unsupported commands.

Burst Transfer

The PCI bus derives its performance from its ability to support burst transfers. The performance of any PCI

application depends largely on the size of the burst transfer. A FIFO to support PCI burst transfer can efficiently be implemented using the XC4000XLT on-chip RAM feature, SelectRAM™. Each XC4000XLT CLB supports two 16x1 RAM blocks. This corresponds to 32 bits of single-ported RAM or 16 bits of dual-ported RAM, with simultaneous read/write capability.

Bandwidth

The Xilinx PCI32 4000 Interfaces support a sustained bandwidth of up to 132 MBytes/sec. The design can be configured to take advantage of the ability of the LogiCORE PCI32 Interface to do very long bursts. Since the FIFO isn't a fixed size, burst can go on as long as the chipset arbiter will allow. Furthermore, since the FIFOs and DMA are decoupled from the proven core, a designer can modify these functions without effecting the critical PCI timing.

The flexible Xilinx backend, combined with support for many different PCI features, gives users a solution that lends itself to being used in many high-performance applications. Xilinx is able to support different depths of FIFOs as well as dual port FIFOs, synchronous or asynchronous FIFOs and multiple FIFOs. The user is not locked into one DMA engine, hence, a DMA that fits a specific application can be designed.

The theoretical maximum bandwidth of a 32 bit, 33 MHz PCI bus is 132 MB/s. How close you get to this maximum will depend on several factors, including the PCI design used, PCI chipset, the processor's ability to keep up with your data stream, the maximum capability of your PCI design and other traffic on the PCI bus. Older chipsets and processors will tend to allow less bandwidth than newer ones.

This version of the Interface, supports a selectable wait-state for burst operation. The XC4013XLT-1, XC4028XLT-09 and XC4062XLT-09 support zero wait-state burst, equal to a sustained bandwidth of up to 132 MBytes/sec. The XC4028XLT-1 and the XC4062XLT-1 support zero wait-states while sinking data, but require one wait-state while sourcing data. See Table 3 for a list of required speed grades.

Table 3: Required Speed Grade for Desired Number of wait-states.

Device	Required Speed Grade	
	One Wait-State	Zero Wait-State
XC4013XLT	-1	-1
XC4028XLT	-1	-09
XC4062XLT PQ240	-1	TBD
XC4062XLT BG432	-1	-09

In the Zero wait-state mode, no wait-states are inserted either while sourcing data or receiving data. This allows a 100% burst transfer rate in both directions with full PCI compliance. No additional wait-states are inserted in response to a wait-state from another agent on the bus. Either IRDY or TRDY is kept asserted until the current data phase ends, as required by the V2.1 PCI Specification.

In one wait-state mode, the LogiCORE PCI32 4000 Interface automatically inserts a wait-state when sourcing data (Initiator Write, Target Read) during a burst transfer. In this mode, the LogiCORE PCI32 4000 Interface can accept data at 100% burst transfer rate and supply data at 50%.

See Table 4 for a PCI bus transfer rates for various operations in either zero or one wait-state mode.

Table 4: LogiCORE PCI32 4000 Transfer Rates

Zero Wait-State Mode	
Operation	**Transfer Rate**
Initiator Write (PCI ← LogiCORE)	3-1-1-2
Initiator Read (PCI → LogiCORE)	4-1-1-2
Target Write (PCI→ LogiCORE)	5-1-1-1
Target Read (PCI ← LogiCORE)	6-1-1-1
One Wait-State Mode	
Operation	**Transfer Rate**
Initiator Write (PCI ← LogiCORE)	3-2-2-2
Initiator Read (PCI → LogiCORE)	4-1-1-2
Target Write (PCI→ LogiCORE)	5-1-1-1
Target Read (PCI ← LogiCORE)	6-2-2-2

Note: Initiator Read and Target Write operations have effectively the same bandwidth for burst transfer.

Timing Specification

The XC4000XLT family, together with the LogiCORE PCI32 products enables design of fully compliant PCI systems. Backend design can affect the maximum speed your design is capable of. Factors in your back-end designs that can affect timing include loading of hot signals coming directly from the PCI bus, and gate count. Table 5 shows the key timing parameters for the LogiCORE PCI32 Interfaces that must be met for full PCI compliance.

Table 5: Timing Parameters [ns]

Parameter	Ref.	PCI Spec.		LogiCORE PCI32 4000, XC4000XLT-1	
		Min	Max	Min	Max
CLK Cycle Time		30	∞	30[1]	∞
CLK High Time		11		11	
CLK Low Time		11		11	
CLK to Bus Signals Valid[3]	T_{ICKOF}	2	11	2[2]	8.5
CLK to REQ# and GNT# Valid[3]	T_{ICKOF}	2	12	2[2]	11
Tri-state to Active		2		2[2]	
CLK to Tri-state			28		28[1]

Parameter	Ref.	PCI Spec.		LogiCORE PCI32 4000, XC4000XLT-1	
		Min	Max	Min	Max
Bus Signal Setup to CLK (IOB)	T_{PSD}		7		7
Bus Signal Setup to CLK (CLB)			7		7[1]
GNT# Setup to CLK	T_{PSD}		10		7
GNT# Setup to CLK (CLB)	T_{PSD}		10		10
Input Hold Time After CLK (IOB)	T_{PHD}		0		0
Input Hold Time After CLK (CLB)			0		0[2]
RST# to Tri-state			40		40[2]

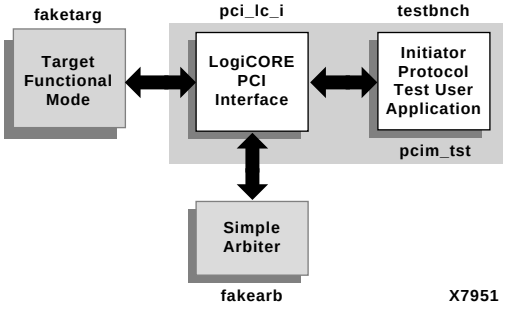
Notes:
1. Controlled by TIMESPECS, included in product
2. Verified by analysis and bench-testing
3. IOB configured for Fast slew rate

Verification Methods

Xilinx has developed a testbench with numerous vectors to test the Xilinx PCI design; this is included with the LogiCORE PCI32 4000 Master and Slave Interfaces A version of this testbench is also used internally by the Xilinx PCI team to verify the PCI32 Interfaces. Additionally, the PCI32 Interfaces have been tested in hardware for electrical, functional and timing compliance.

The testbench shipped with the interface verifies the PCI interface functions according to the test scenarios specified in the *PCI Local Bus Specification, V2.1*; see Figure 2. This testbench consists of 28 test scenarios, each designed to test a specific PCI bus operation. Refer to the checklists chapter in this databook for a complete list of scenarios.

Figure 2: PCI Protocol Testbench



Ping Reference Design

The Xilinx LogiCORE PCI “PING” Application Example, delivered in VHDL and Verilog, has been developed to provide an easy-to-understand example which demonstrates many of the principles and techniques required to successfully use a LogiCORE PCI32 4000 Interface in a System On A Chip solution.

Synthesizable PCI Bridge Design Example

Synthesizable PCI bridge design examples, delivered in Verilog and VHDL, are available to demonstrate how to interface to the LogiCORE PCI32 4000 V2.0 Interfaces and provides a modular foundation upon which to base other designs. See separate data sheet for details.

Device Utilization

The Target-Only and Target/Initiator options require a variable amount of CLB resources for the PCI32 4000 Interfaces. Choosing between one and zero wait-states device (e.g. XC4062-1 vs. -09) will change the amount of logic used. The core now includes a switch to force the entire deletion of unused Base Address Registers.

Utilization can vary widely, depending on the configuration choices made by the designer. Options that can affect the size of the core are:

- Initiator vs. Target-Only. The Initiator requires about 12 CLBs more than the target (not set in the cfg file; set at the time the core is generated).
- Number of Base Address Registers Used. Turning off any unused BARs will save on resources.
- Size of the BARs. Setting the BAR to a smaller size requires more flip-flops. A smaller address space requires more flip-flops to decode.
- Decode Speed. Medium decode requires slightly more logic than slow decode.
- Number of wait-states. Zero wait-states requires more logic than one wait-state.
- Latency timer. Disabling the latency timer will save a few resources. It must be enabled for bursting.

Recommended Design Experience

The LogiCORE PCI32 4000 Interfaces are pre-implemented allowing engineering focus at the unique back-end functions of a PCI design. Regardless, PCI is a high-performance system that is challenging to implement in any technology, ASIC or FPGA. Therefore, we recommend previous experience with building high-performance, pipelined FPGA designs using Xilinx implementation software, TIMESPECs, and guide files. The challenge to implement a complete PCI design including back-end functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation for your specific requirements.