

TOSHIBA Original CMOS 8-bit Microcontroller

TLCS-870/C Series

TMP86C820 , TMP86C420

Databook

6th Edition

TOSHIBA CORPORATION

CMOS 8-Bit Microcontroller

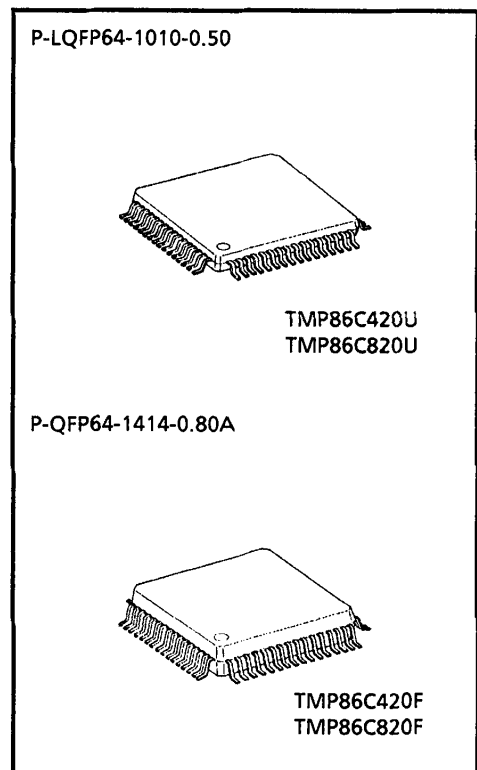
TMP86C420U/F, TMP86C820U/F

The TMP86C420/820 are the high-speed, high-performance and low power consumption 8-bit microcomputer, including ROM, RAM, LCD driver, multi-function timer/counter, serial interface (SIO), a 8-bit AD converter and two clock generators on chip.

Product No.	ROM	RAM	PACKAGE	OTP MCU
TMP86C420U/F	4 K × 8 bits	256 × 8 bits	P-LQFP64-1010-0.50	TMP86PM29AU/AF
TMP86C820U/F	8 K × 8 bits		P-QFP64-1414-0.80A	

Features

- ◆ 8-bit single chip microcomputer TLCS-870/C series
- ◆ Instruction execution time: 0.25 μ s (at 16 MHz)
122 μ s (at 32.768 kHz)
- ◆ 132 types and 731 basic instructions
- ◆ 15 interrupt sources (External: 5, Internal: 10)
- ◆ Input/Output ports (39 pins)
(Out of which 24 pins are also used as SEG pins)
- ◆ 18-bit timer counter: 1 ch
 - Timer, Event counter, Pulse width measurement, Frequency measurement modes
- ◆ 8-bit timer counter: 2 ch
 - Timer, Event counter, PWM output, Programmable Divider Output PPG modes
- ◆ Time Base Timer
- ◆ Divider output function



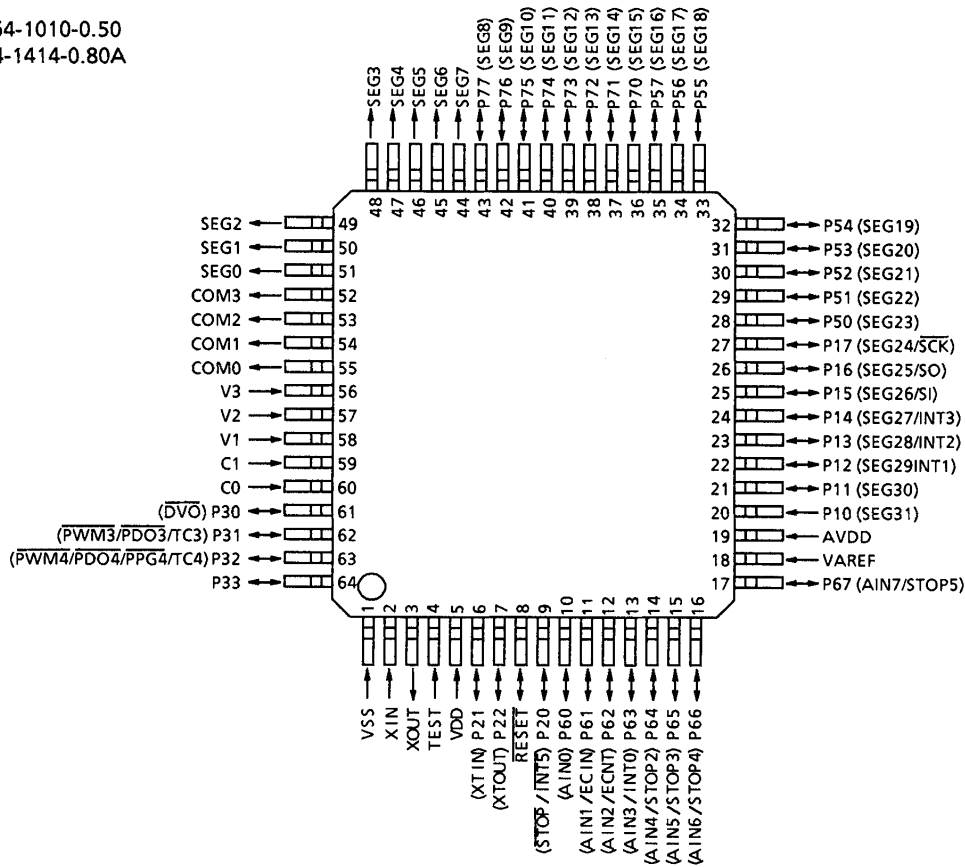
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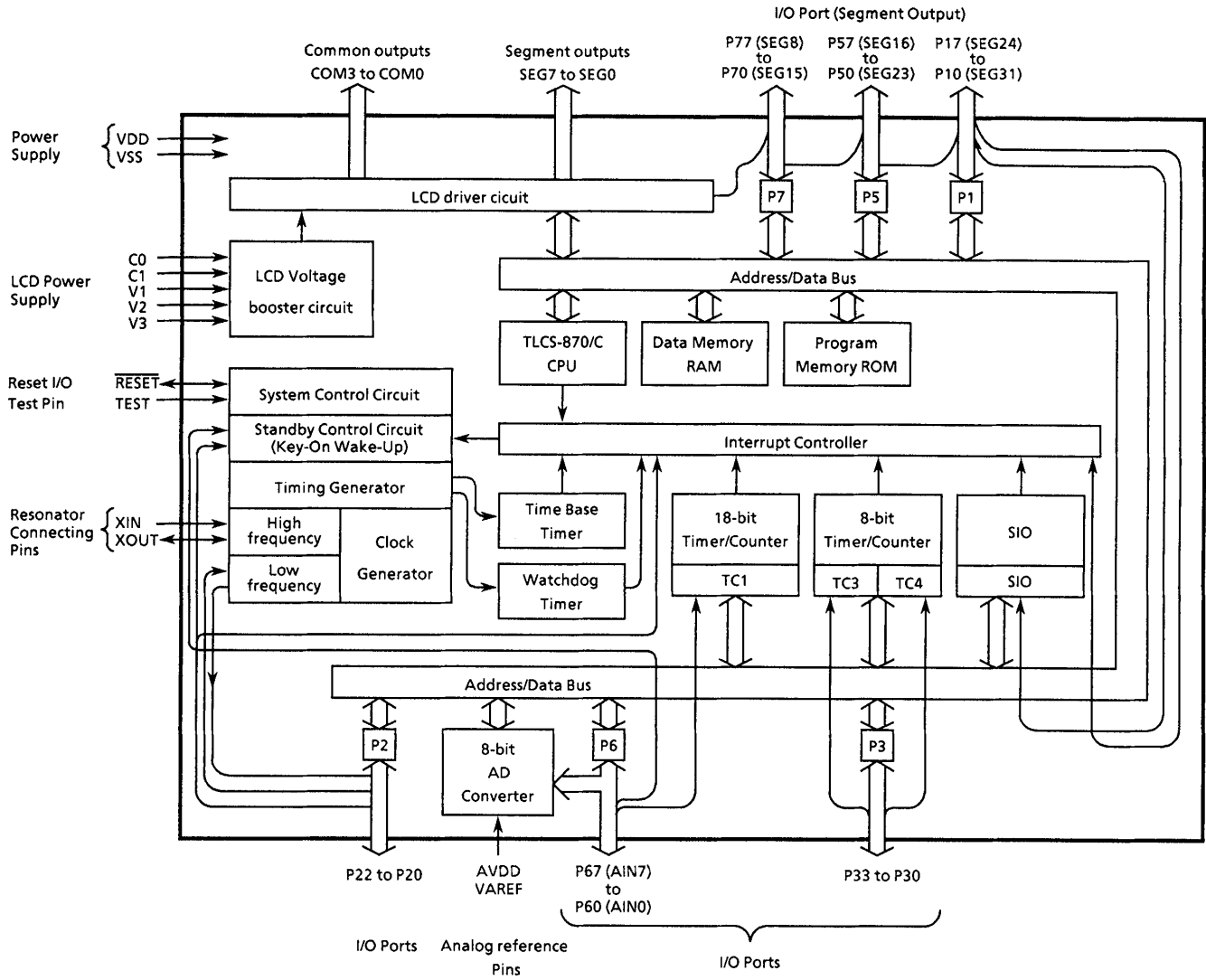
- ◆ Watchdog Timer
 - Interrupt source/reset output (programmable)
- ◆ Serial interface
 - 8-bit SIO: 1ch
- ◆ 8-bit successive approximation type AD converter
 - Analog input: 8 ch
- ◆ Four Key-On Wake-Up pins
- ◆ LCD driver/controller
 - Built-in voltage booster for LCD driver
 - With displaymemory
 - LCD direct drive capability (Max 32 seg × 4 com)
 - 1/4, 1/3, 1/2duties or static drive are programmably selectable
- ◆ Dual clock operation
 - Single/Dual-clock mode
- ◆ Nine power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
 - SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
 - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by falling edge of TBTCCR <TBTCK> setting.
 - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
 - IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
 - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of Time-Base-Timer. Release by falling edge of TBTCCR <TBTCK> setting.
 - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
 - SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock. Release by interrupts.
- ◆ Wide operating voltage: 1.8 to 5.5 V at 4.2 MHz / 32.768 kHz,
2.7 to 5.5 V at 8 MHz / 32.768 kHz,
4.2 to 5.5 V at 16 MHz / 32.768 kHz

Pin Assignments (Top View)

P-LQFP64-1010-0.50
 P-QFP64-1414-0.80A



Block Diagram



Pin Function

Pin Name	Input / Output	Function		
P17 (SEG24, \overline{SCK})	I/O (I/O)	8-bit input/output port with latch. When used as input port, an external interrupt input and serial interface input/output, the P1LCR must be set to "0" after setting output latch to "1". When used as a LCD segment output, the P1LCR must be set to "1".	Serial clock input/output	LCD segment outputs.
P16 (SEG25, SO)	I/O (Output)		Serial data input	
P15 (SEG26, SI)	I/O (I/O)		Serial data input	
P14 (SEG27, INT3)	I/O (I/O)		External interrupt 3 input	
P13 (SEG28, INT2)	I/O (I/O)		External interrupt 2 input	
P12 (SEG29, INT1)	I/O (I/O)		External interrupt 1 input	
P11 (SEG30)	I/O (Output)			
P10 (SEG31)	I/O (Output)			
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, the output latch must be set to "1".	Resonator connecting pins (32.768 kHz) For inputting external clock, XTIN is used and XOUT is opened.	
P21 (XTIN)	I/O (Input)		External interrupt input 5 or STOP mode release signal input	
P20 ($\overline{INT5}$, \overline{STOP})	I/O (Input)			
P33	I/O	4-bit programmable input/output port (Nch high current output). When used as a timer/counter output or divider output, the output latch must be set to "1". When used as an input port or timer/counter input, the P3OUTCR must be set to "0" after P3DR is set to "1".	Timer counter 4 input/output	
P32 (PWM4, PDO4, PPG4, TC4)	I/O (I/O)		Timer counter 3 input/output	
P31 (PWM3, PDO3, TC3)	I/O (I/O)		Divider output	
P30 (DVO)	I/O (Output)			
P57 (SEG16) to P50 (SEG23)	I/O (Output)	8-bit input/output port with latch. When used as a LCD segment output, the P5LCR must be set to "1".	LCD segment outputs	
P67 (AIN7, STOP5)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as an analog input, the P6CR must be set to "0" after setting output latch to "0". When used as an input port, a key on wake up input, an external interrupt input and timer/counter input, the P6CR must be set to "0" after setting output latch to "1".	STOP 5 input	AD converter analog inputs
P66 (AIN6, STOP4)	I/O (Input)		STOP 4 input	
P65 (AIN5, STOP3)	I/O (Input)		STOP 3 input	
P64 (AIN4, STOP2)	I/O (Input)		STOP 2 input	
P63 (AIN3, $\overline{INT0}$)	I/O (Input)		External interrupt 0 input	
P62 (AIN2, ECNT)	I/O (Input)		Timer / counter 1 input	
P61 (AIN1, ECIN)	I/O (Input)			
P60 (AIN0)	I/O (Input)			
P77 (SEG8) to P70 (SEG15)	I/O (Output)	8-bit input/output port with latch. When used as a LCD segment output, the P7LCR must be set to "1".	LCD segment outputs	
SEG7 to SEG0	Output	LCD segment outputs		
COM3 to COM0		LCD common outputs		
V3 to V1 C1 to C0	LCD voltage booster pin	LCD voltage booster pin. Capacitors are required between C0 and C1 pin and V1/V2/V3 pin and GND.		
XIN, XOUT	Input Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.		
\overline{RESET}	I/O	Reset signal input or watchdog timer output/address-trap-reset output		
TEST	Input	Test pin for out-going test. Be fixed to low.		
VDD, VSS	Power Supply	+ 5 V, 0 (GND)		
VAREF		Analog reference voltage inputs (High)		
AVDD		AD circuit power supply		

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86C420/820 memory consist of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86C420/820 memory address map. The general-purpose registers are not assigned to the RAM address space.

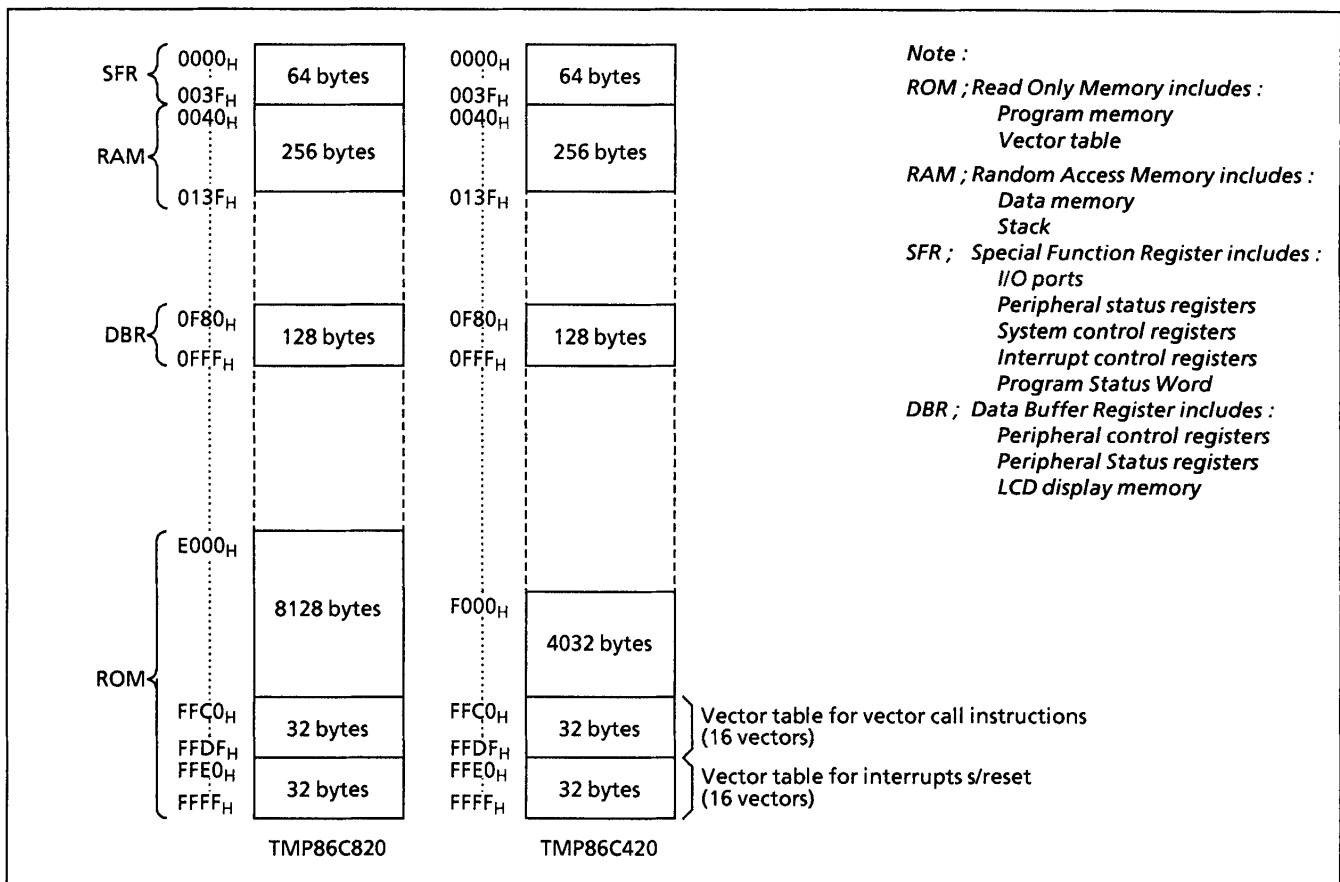


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86C420 has a 4 K×8 bits (address F000_H to FFFF_H), TMP86C820 has a 8 K×8 bits (address E000_H to FFFF_H) of program memory (mask programmed ROM). However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address trap).

1.3 Data Memory (RAM)

The TLCS-870/C is available up to 64 Kbytes of data memory area. Data memory consists of internal data memory (internal ROM or RAM). The TMP86C420/820 have 256 bytes, of internal RAM. The first 192 bytes (0040H to 00FFH) of the internal RAM are located in the direct area; instructions with shorten operations are available against such an area.

The data memory contents become unstable when the power supply is turned on; therefore, the data memory should be initialized by an initialization routine.

Example: Clears RAM to "00H".

```
LD HL, 0040H ; Set start address
LD A, H      ; Set initialization data (00H)
LD BC, 00FFH ; Set byte number (-1)

SRAMCLR: LD (HL), A ;
INC HL
DEC BC
JRS F, SRAMCLR
```


1.4 System Clock Controller

The system clock controller consists of a clock generator, a timing generator, and a stand-by controller.

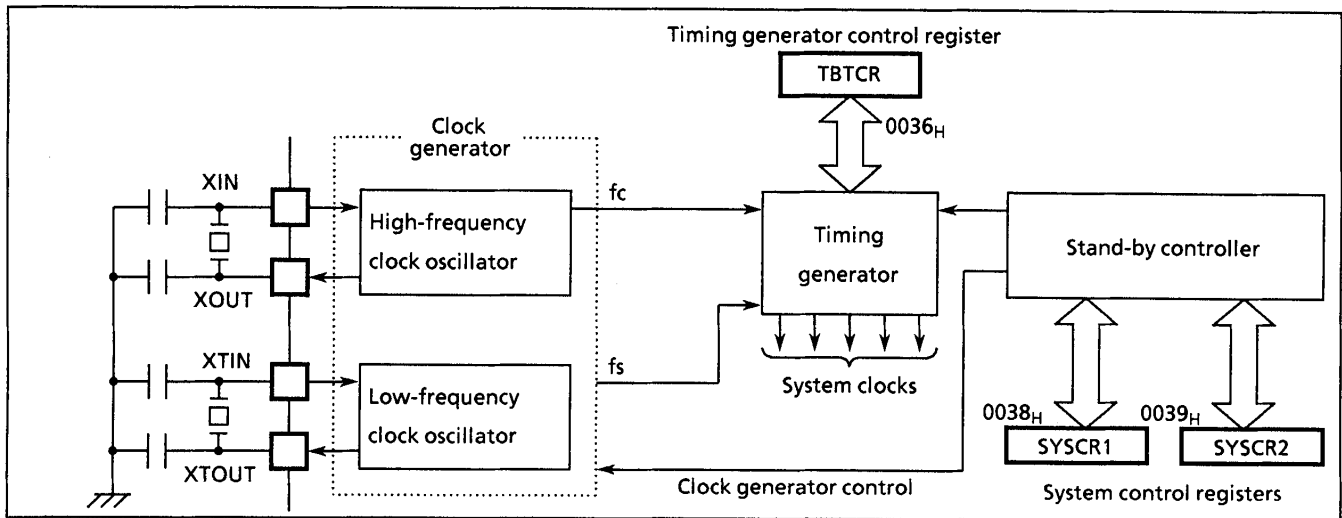


Figure 1-2. System Clock Control

1.4.1 Clock Generator

The Clock generator generates the basic clock which provides the system clocks supplied to the CPU core and peripheral hardware. It contains two oscillation circuits : one for the high-frequency clock and one for the low-frequency clock. Power consumption can be reduced by switching of the standby controller to low-power operation based on the low-frequency clock.

The high-frequency (f_c) and low-frequency (f_s) clocks can easily be obtained by connecting a resonator between the XIN/XOUT and XTIN/XTOUT pins respectively. Clock input from an external oscillator is also possible. In this case, external clock is applied to XIN/XTIN pin with XOUT/XTOUT pin not connected.

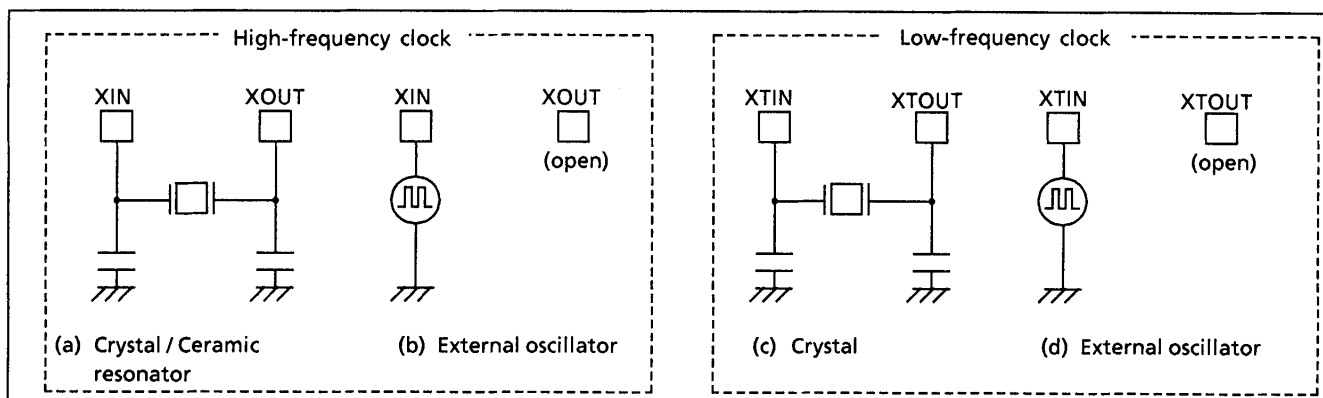


Figure 1-3. Examples of Resonator Connection

Note : The function to monitor the basic clock directly at external is not provided for hardware, however, with disabling all interrupts and watchdog timers, the oscillation frequency can be adjusted by monitoring the pulse which the fixed frequency is outputted to the port by the program. The system to require the adjustment of the oscillation frequency should create the program for the adjustment in advance.

1.4.2 Timing Generator

The timing generator generates the various system clocks supplied to the CPU core and peripheral hardware from the basic clock (fc or fs). The timing generator provides the following functions.

- ① Generation of main system clock
- ② Generation of divider output (\overline{DVO}) pulses
- ③ Generation of source clocks for time base timer
- ④ Generation of source clocks for watchdog timer
- ⑤ Generation of internal source clocks for timer/counters
- ⑥ Generation of warm-up clocks for releasing STOP mode
- ⑦ Generation of base clocks for LCD driver/controller

(1) Configuration of timing generator

The timing generator consists of a 2-stage prescaler, a 21-stage divider, a main system clock generator, and machine cycle counters.

An input clock to the 7th stage of the divider depends on the operating mode, DV7CK (bit 4 in TBTCR), that is shown in Table 1-2. As reset and STOP mode started/canceled, the prescaler and the divider are cleared to "0".

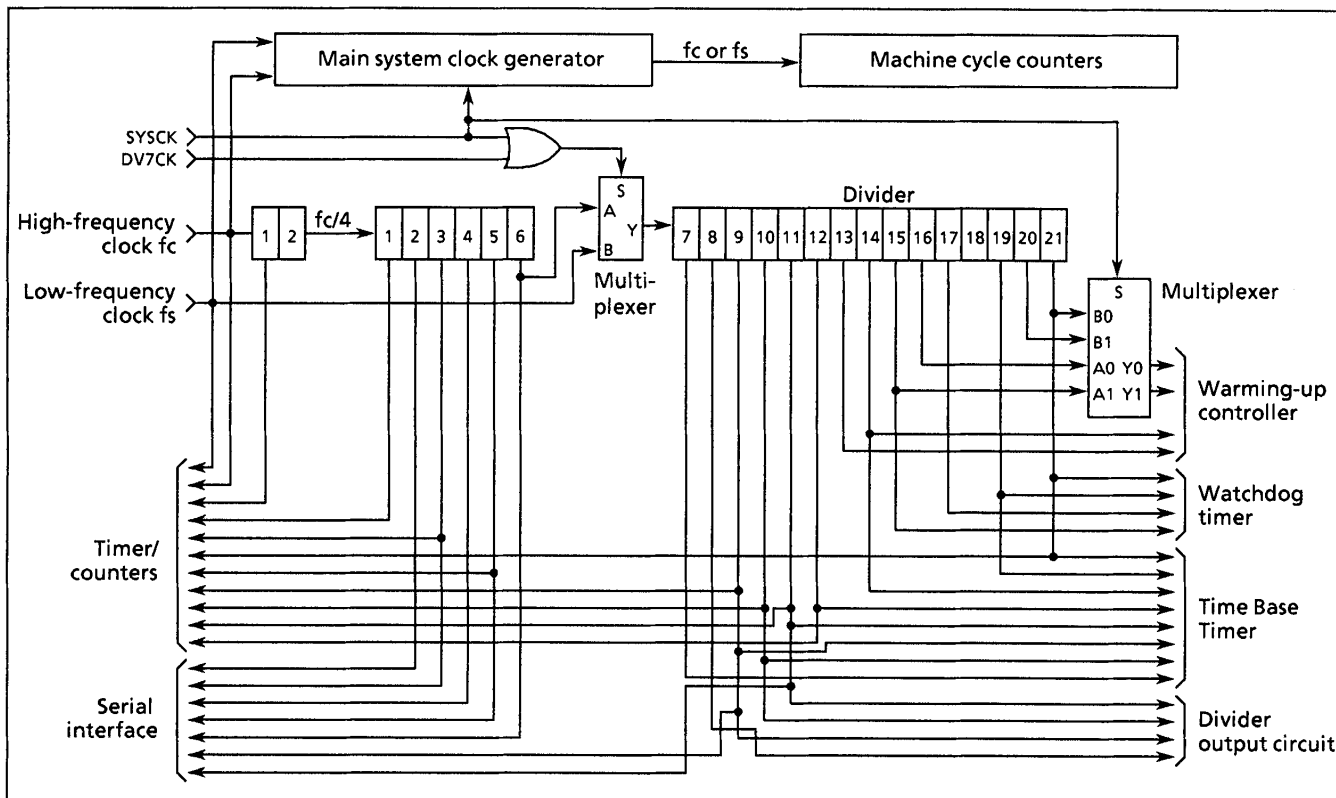


Figure 1-4. Configuration of Timing Generator

TBTCR (0036 _H)	7	6	5	4	3	2	1	0	(initial value 0**0 0***)
	(DVOEN)	(DVQCK)	DV7CK	(TBTEN)	(TB \overline{T} CK)				
	DV7CK	Selection of input to the 7th stage of the divider				0 : $fc/2^8$ [Hz] 1 : fs			R/W

Note 1: In single clock mode, do not set DV7CK to "1".
 Note 2: Do not set "1" on DV7CK while the low-frequency clock is not operated stably.
 Note 3: fc ; High-frequency clock [Hz], fs ; Low-frequency clock [Hz], * ; Don't care
 Note 4: During warming-up after STOP mode is released or in IDLE0 mode, output of the 6th stage of the divider is input to the 7th stage of the divider regardless of DV7CK.

Figure 1-5. Timing Generator Control Register

(2) Machine cycle

Instruction execution and peripheral hardware operation are synchronized with the main system clock. The minimum instruction execution unit is called a “machine cycle”. There are a total of 10 different types of instructions for the TLCS-870/C Series : ranging from 1-cycle instructions which require one machine cycle for execution to 10-cycle instructions which require 10 machine cycles for execution. A machine cycle consists of 4 states (S0 to S3), and each state consists of one main system clock.

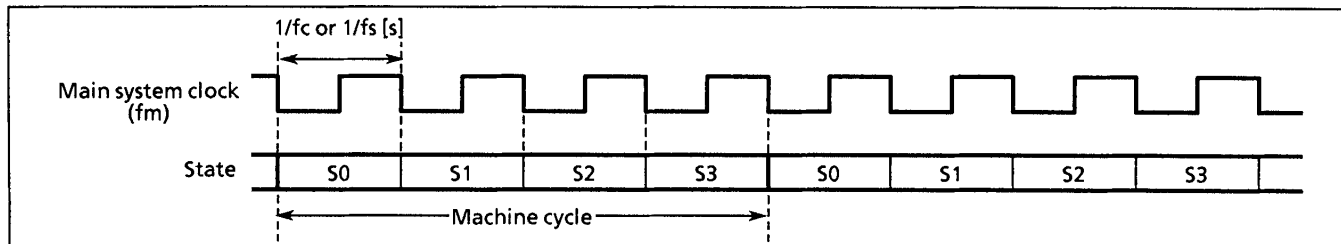


Figure 1-6. Machine Cycle

1.4.3 Operation mode control circuit

The operation mode control circuit starts and stops the oscillation circuits for the high-frequency and low-frequency clocks, and switches the main system clock. There are two operating modes: single-clock and dual-clock. These modes are controlled by the system control registers (SYSCR1 and SYSCR2). Figure 1-7 shows the operating mode transition diagram and Figure 1-8 shows the system control registers.

(1) Single-clock mode

Only the oscillation circuit for the high-frequency clock is used, and P21 (XTIN) and P22 (XTOUT) pins are used as input / output ports. The main-system clock is obtained from the high-frequency clock. In the single-clock mode, the machine cycle time is $4/f_c$ [s].

① NORMAL1 mode

In this mode, both the CPU core and on-chip peripherals operate using the high-frequency clock. The TMP86C420/820 are placed in this mode after reset.

② IDLE1 mode

In this mode, the internal oscillation circuit remains active. The CPU and the watchdog timer are halted; however on-chip peripherals remain active (operate using the high-frequency clock). IDLE1 mode is started by SYSCR2 <IDLE>, and IDLE1 mode is released to NORMAL1 mode by an interrupt request from the on-chip peripherals or external interrupt inputs. When the IMF (interrupt master enable flag) is “1” (interrupt enable), the execution will resume with the acceptance of the interrupt, and the operation will return to normal after the interrupt service is completed. When the IMF is “0” (interrupt disable), the execution will resume with the instruction which follows the IDLE1 mode start instruction.

③ IDLE0 mode

In this mode, all the circuit, except oscillator and the Timer-Base-Timer, stops operation.

This mode is enabled by setting "1" on bit TGHALT on the system control register 2 (SYSCR2).

When IDLE0 mode starts, the CPU stops and the timing generator stops feeding the clock to the peripheral circuits other than TBT. Then, upon detecting the falling edge of the source clock selected with TBTCR<TBTCK>, the timing generator starts feeding the clock to all peripheral circuits.

When returned from IDLE0 mode, the CPU restarts operating, entering NORMAL1 mode back again. IDLE0 mode is entered and returned regardless of how TBTCR<TBTEN> is set. When IMF = "1", EF₆ (TBT interrupt individual enable flag) = "1", and TBTCR<TBTEN> = "1", interrupt processing is performed. When IDLE0 mode is entered while TBTCR<TBTEN> = "1", the INTTBT interrupt latch is set after returning to NORMAL1 mode.

(2) Dual-clock mode

Both the high-frequency and low-frequency oscillation circuits are used in this mode. P21 (XTIN) and P22 (XTOUT) pins cannot be used as input/output ports. The main system clock is obtained from the high-frequency clock in NORMAL2 and IDLE2 modes, and is obtained from the low-frequency clock in SLOW and SLEEP modes. The machine cycle time is $4/f_c$ [s] in the NORMAL2 and IDLE2 modes, and $4/f_s$ [s] ($122 \mu\text{s}$ at $f_s = 32.768 \text{ kHz}$) in the SLOW and SLEEP modes.

The TLCS-870/C is placed in the signal-clock mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on at the start of a program.

① NORMAL2 mode

In this mode, the CPU core operates with the high-frequency clock. On-chip peripherals operate using the high-frequency clock and/or low-frequency clock.

② SLOW2 mode

In this mode, the CPU core operates with the low-frequency clock, while both the high-frequency clock and the low-frequency clock are operated. On-chip peripherals are triggered by the low-frequency clock. As the SYSCK on SYSCR2 becomes "0", the hardware changes into NORMAL2 mode. As the XEN on SYSCR2 becomes "0", the hardware changes into SLOW1 mode. Do not clear XTEN to "0" during SLOW2 mode.

③ SLOW1 mode

This mode can be used to reduce power-consumption by turning off oscillation of the high-frequency clock. The CPU core and on-chip peripherals operate using the low-frequency clock.

Switching back and forth between SLOW1 and SLOW2 modes are performed by XEN bit on the system control register 2 (SYSCR2). In SLOW1 and SLEEP mode, the input clock to the 1st stage of the divider is stopped; output from the 1st to 6th stages is also stopped.

④ IDLE2 mode

In this mode, the internal oscillation circuit remain active. The CPU and the watchdog timer are halted ; however, on-chip peripherals remain active (operate using the high-frequency clock and/or the low-frequency clock). Starting and releasing of IDLE2 mode are the same as for IDLE1 mode, except that operation returns to NORMAL2 mode.

⑤ SLEEP1 mode

In this mode, the internal oscillation circuit of the low-frequency clock remains active. The CPU, the watchdog timer, and the internal oscillation circuit of the high-frequency clock are halted; however, on-chip peripherals remain active (operate using the low-frequency clock). Starting and releasing of SLEEP mode are the same as for IDLE1 mode, except that operation returns to SLOW mode. In SLOW and SLEEP mode, the input clock to the 1st stage of the divider is stopped; output from the 1st to 6th stages is also stopped.

⑥ SLEEP2 mode

The SLEEP2 mode is the idle mode corresponding to the SLOW2 mode. The status under the SLEEP2 mode is same as that under the SLEEP1 mode, except for the oscillation circuit of the high-frequency clock.

⑦ SLEEP0 mode

In this mode, all the circuit, except oscillator and the Timer-Base-Timer, stops operation.

This mode is enabled by setting "1" on bit TGHALT on the system control register 2 (SYSCR2).

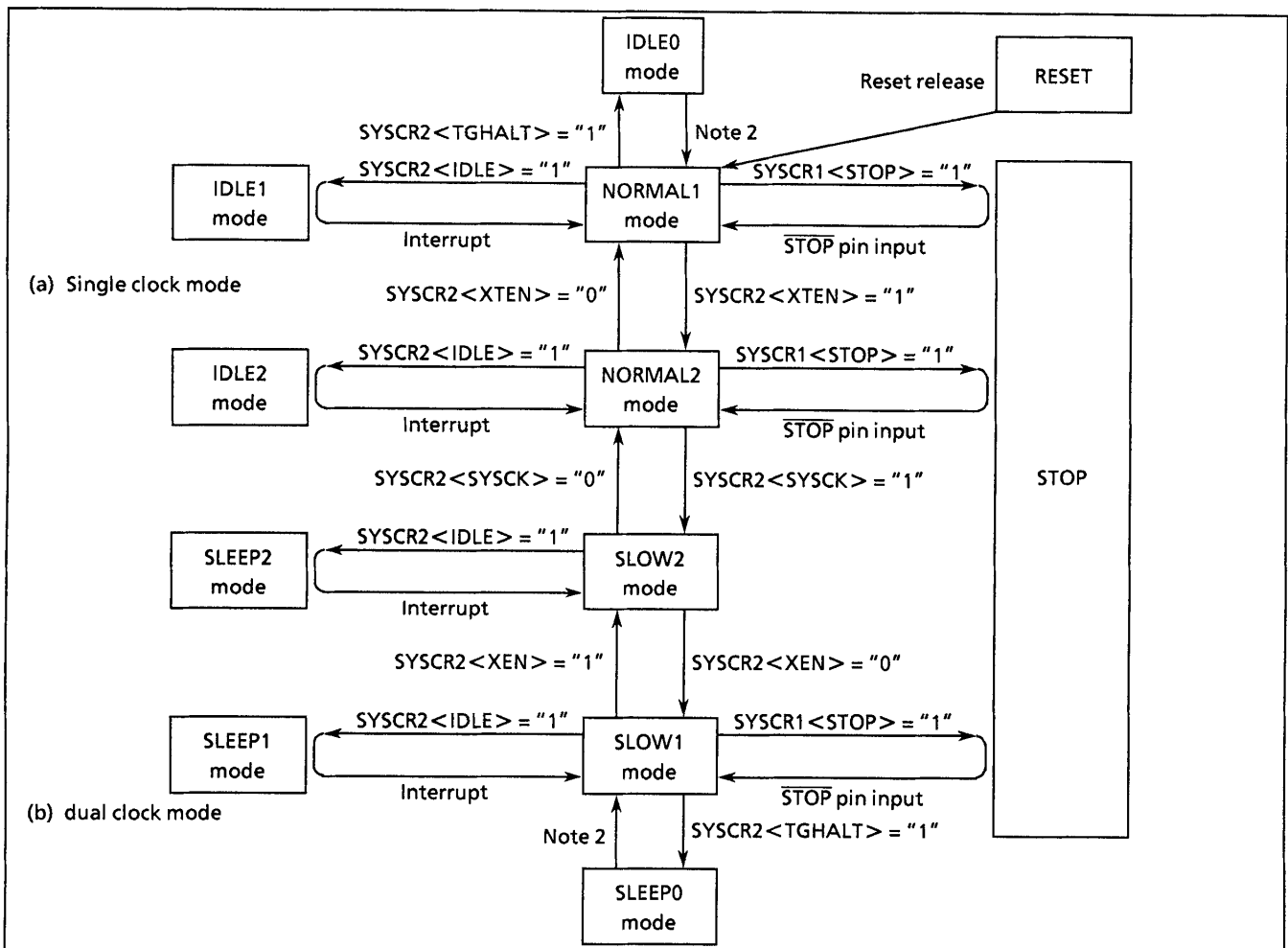
When SLEEP0 mode starts, the CPU stops and the timing generator stops feeding the clock to the peripheral circuits other than TBT. Then, upon detecting the falling edge of the source clock selected with $TBTCR < TBTCCK >$, the timing generator starts feeding the clock to all peripheral circuits.

When returned from SLEEP0 mode, the CPU restarts operating, entering SLOW1 mode back again. SLEEP0 mode is entered and returned regardless of how $TBTCR < TBTEN >$ is set. When $IMF = "1"$, EF_6 (TBT interrupt individual enable flag) = "1", and $TBTCR < TBTEN > = "1"$, interrupt processing is performed. When SLEEP0 mode is entered while $TBTCR < TBTEN > = "1"$, the INTTBT interrupt latch is set after returning to SLOW1 mode.

(3) STOP mode

In this mode, the internal oscillation circuit is turned off, causing all system operations to be halted. The internal status immediately prior to the halt is held with a lowest power consumption during STOP mode.

STOP mode is started by the system control register 1 (SYSCR1), and STOP mode is released by a inputting (either level-sensitive or edge-sensitive can be programmably selected) to the \overline{STOP} pin. After the warming-up period is completed, the execution resumes with the instruction which follows the STOP mode start instruction.



Note 1: NORMAL1 and NORMAL2 modes are generically called NORMAL ; SLOW1 and SLOW2 are called SLOW ; IDLE0, IDLE1 and IDLE2 are called IDLE; SLEEP0, SLEEP1 and SLEEP2 are called SLEEP.

Note 2: The mode is released by falling edge of TBTCR<TBTC> setting.

Operating Mode		Oscillator		CPU core	TBT	Other Peripherals	Machine Cycle Time
		High-freq.	Low-freq.				
Single Clock	RESET	Oscillation	Stop	Reset	Reset	Reset	4/fc [s]
	NORMAL1			Operate	Operate	Operate	
	IDLE1			Halt		Halt	
	IDLE0						
	STOP			Stop	Halt	Halt	—
Dual Clock	NORMAL2	Oscillation	Oscillation	Operate with High Freq.	Operate	Operate	4/fc [s]
	IDLE2			Halt			
	SLOW2			Operate with Low Freq.			
	SLEEP2			Halt			
	SLOW1	Stop	Oscillation	Operate with Low Freq.	Operate	Operate	4/fs [s]
	SLEEP1			Halt			
	SLEEP0						
	STOP			Stop			

Figure 1-7. Operating Mode Transition Diagram

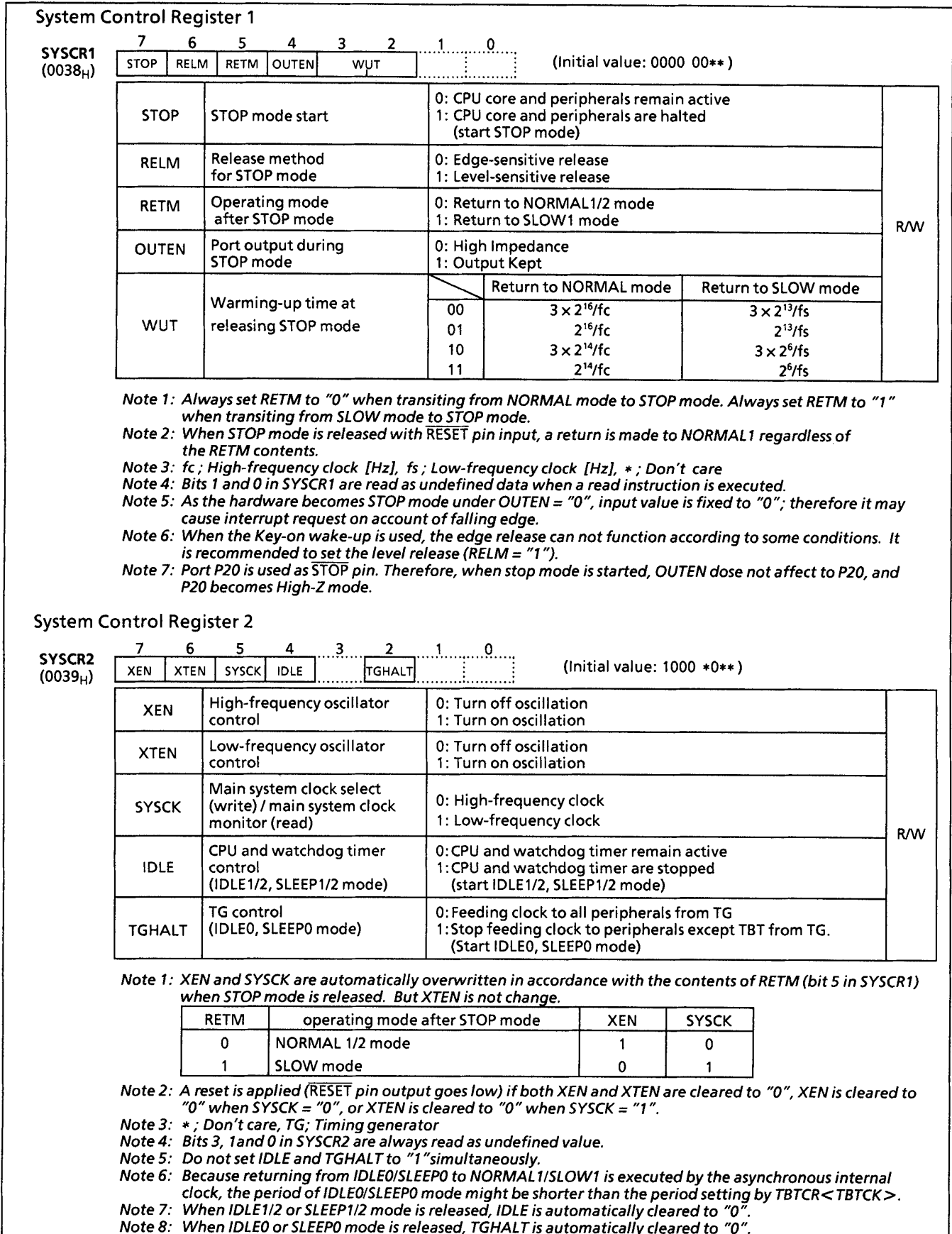


Figure 1-8. System Control Registers

1.4.4 Operating Mode Control

(1) STOP mode

STOP mode is controlled by the system control register 1, the $\overline{\text{STOP}}$ pin input and key wake-up input (STOP2 to STOP5) which is controlled by the STOP mode release control register (STOPCR).

The $\overline{\text{STOP}}$ pin is also used both as a port P20 and an $\overline{\text{INT5}}$ (external interrupt input 5) pin.

STOP mode is started by setting STOP (bit 7 in SYSCR1) to "1". During STOP mode, the following status is maintained.

- ① Oscillations are turned off, and all internal operations are halted.
- ② The data memory, registers, the program status word and port output latches are all held in the status in effect before STOP mode was entered.
- ③ The prescaler and the divider of the timing generator are cleared to "0".
- ④ The program counter holds the address 2 ahead of the instruction (e.g. [SET (SYSCR1).7]) which started STOP mode.

STOP mode includes a level-sensitive release mode and an edge-sensitive release mode, either of which can be selected with the RELM (bit 6 in SYSCR1). Do not use any STOPx (x; 2 to 5) pin input for releasing STOP mode in edge-sensitive release mode.

Note 1: $\overline{\text{STOP}}$ pin doesn't have the control register such as STOPCR, so when STOP mode is released by STOPx (x; 2 to 5), P20 pin should be used as STOP function.

Note 2: During STOP period (from start of STOP mode to end of warming-up), due to changes in the external interrupt pin signal, interrupt latches may be set to "1" and interrupts may be accepted immediately after STOP mode is released. Before starting STOP mode, therefore, disable interrupts. Also, before enabling interrupts after STOP mode is released, clear unnecessary interrupt latches.

a. Level-sensitive release mode (RELM = "1")

In this mode, STOP mode is released by setting the $\overline{\text{STOP}}$ pin high or setting the STOPx (x; 2 to 5) pin input which is enabled by STOPCR. This mode is used for capacitor back-up when the main power supply is cut off and long term battery back-up.

When the $\overline{\text{STOP}}$ pin input is high or STOPx (x; 2 to 5) pin input which is enabled by STOPCR is low, executing an instruction which starts STOP mode will not place in STOP mode but instead will immediately start the release sequence (warm-up). Thus, to start STOP mode in the level-sensitive release mode, it is necessary for the program to first confirm that the $\overline{\text{STOP}}$ pin input is low and STOPx (x; 2 to 5) pin input which is enabled by STOPCR is high. The following two methods can be used for confirmation.

- ① Testing a port P20.
- ② Using an external interrupt input $\overline{\text{INT5}}$ ($\overline{\text{INT5}}$ is a falling edge-sensitive input).

Example 1: Starting STOP mode from NORMAL mode by testing a port P20.

```
LD    (SYSCR1), 01010000B    ; Sets up the level-sensitive release mode
SSTOPH:TEST (P2PRD). 0      ; Wait until the  $\overline{\text{STOP}}$  pin input goes low level
JRS  F, SSTOPH
SET  (SYSCR1). 7            ; Starts STOP mode
```


Example 2: Starting STOP mode from NORMAL mode with an INT5 interrupt.

```

PINT5: TEST (P2PRD). 0      ; To reject noise, STOP mode does not start if
      JRS F, SINT5          ; port P20 is at high
      LD (SYSCR1), 01010000B ; Sets up the level-sensitive release mode.
      SET (SYSCR1). 7       ; Starts STOP mode
SINT5: RETI
    
```

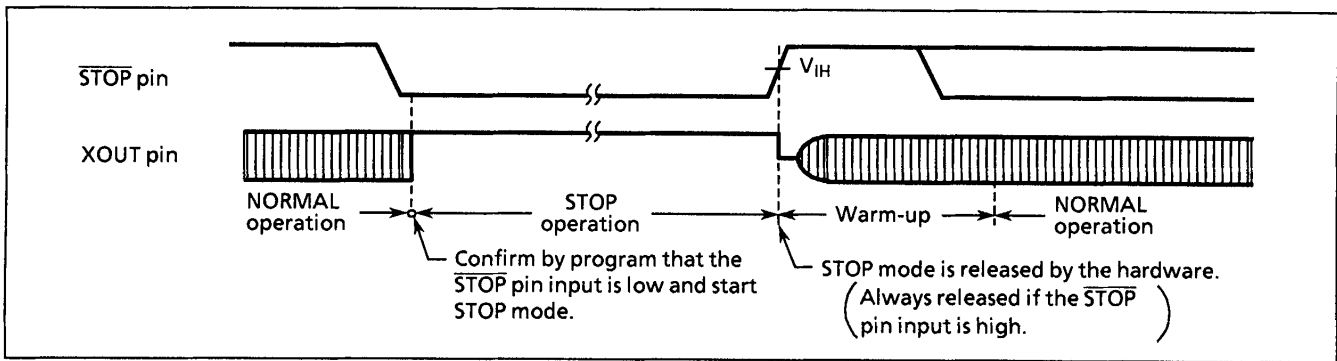


Figure 1-9. Level-sensitive Release Mode

Note 1: Even if the \overline{STOP} pin input is low or $STOPx$ (x ; 2 to 5) pin input which is enabled by $STOPCR$ is high after warming up start, the STOP mode is not restarted.

Note 2: In this case of changing to the level-sensitive release mode from the edge-sensitive release mode, the release mode is not switched until a rising edge of the \overline{STOP} pin input is detected.

b. Edge-sensitive release mode (RELM="0")

In this mode, STOP mode is released by a rising edge of the \overline{STOP} pin input. This is used in applications where a relatively short program is executed repeatedly at periodic intervals. This periodic signal (for example, a clock from a low-power consumption oscillator) is input to the \overline{STOP} pin. In the edge-sensitive release mode, STOP mode is started even when the \overline{STOP} pin input is high level. Do not use any $STOPx$ (x ; 2 to 5) pin input for releasing STOP mode in edge-sensitive release mode.

Example: Starting STOP mode from NORMAL mode

```
LD(SYSCR1), 10010000B; Starts after specified to the edge-sensitive release mode
```

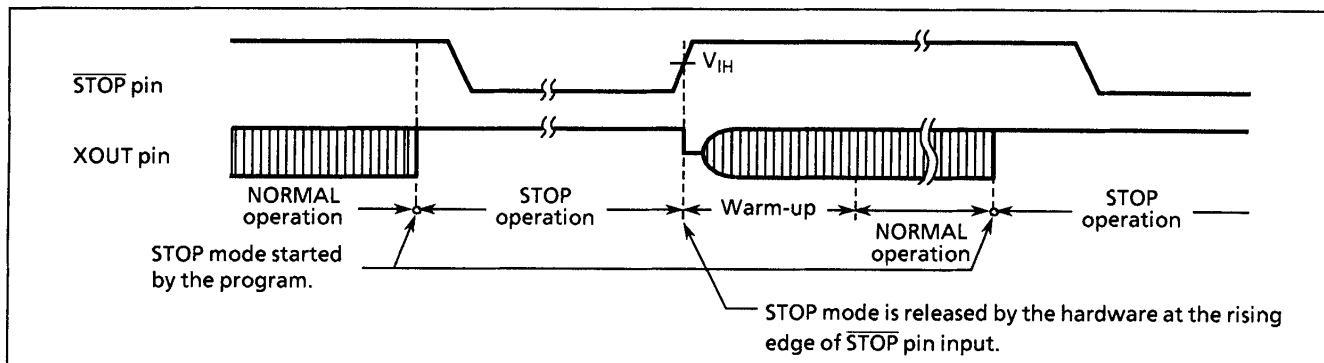


Figure 1-10. Edge-sensitive Release Mode

STOP mode is released by the following sequence.

- ① In the dual-clock mode, when returning to NORMAL2 or SLOW2, both the high-frequency and low-frequency clock oscillators are turned on ; when returning to SLOW1 mode, only the low-frequency clock oscillator is turned on. In the signal-clock mode, only the high-frequency clock oscillator is turned on.
- ② A warm-up period is inserted to allow oscillation time to stabilize. During warm-up, all internal operations remain halted. Four different warm-up times can be selected with the WUT (bits 2 and 3 in SYSCR1) in accordance with the resonator characteristics.
- ③ When the warm-up time has elapsed, normal operation resumes with the instruction following the STOP mode start instruction. The start is made after the prescaler and the divider of the timing generator are cleared to "0".

Table 1-1. Warm-up Time Example (at $f_c = 16.0$ MHz, $f_s = 32.768$ kHz)

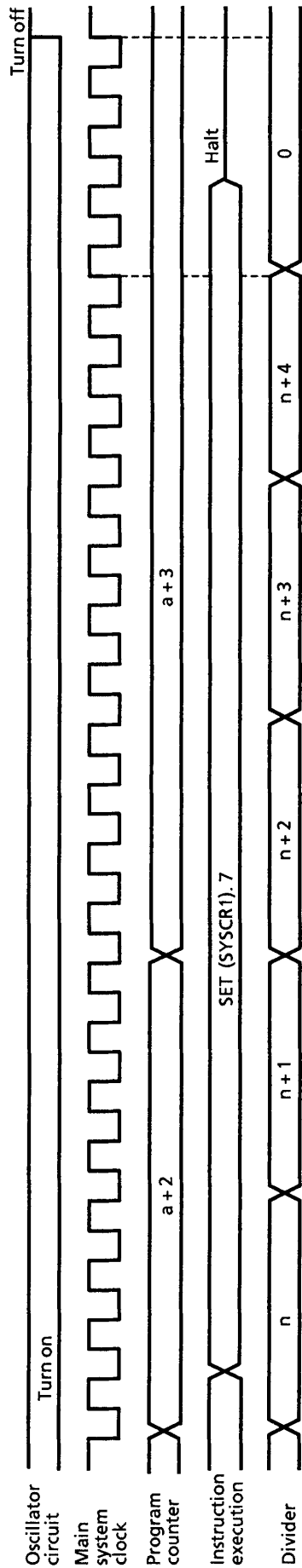
WUT	Warm-up Time [ms]	
	Return to NORMAL mode	Return to SLOW mode
00	12.288	750
01	4.096	250
10	3.072	5.85
11	1.024	1.95

Note: The warm-up time is obtained by dividing the basic clock by the divider; therefore, the warm-up time may include a certain amount of error if there is any fluctuation of the oscillation frequency when STOP mode is released. Thus, the warm-up time must be considered an approximate value.

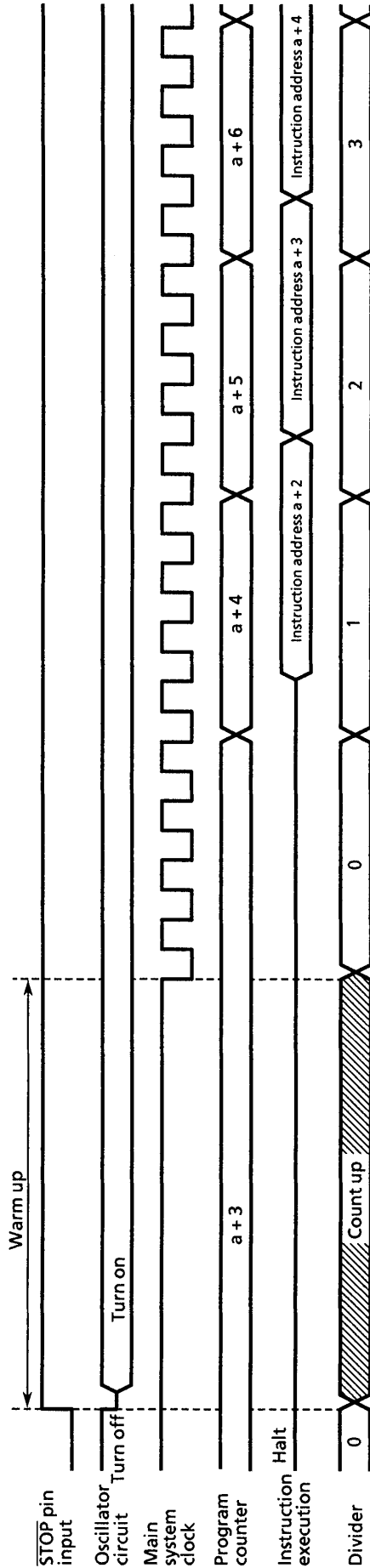
STOP mode can also be released by inputting low level on the $\overline{\text{RESET}}$ pin, which immediately performs the normal reset operation.

Note: When STOP mode is released with a low hold voltage, the following cautions must be observed.

The power supply voltage must be at the operating voltage level before releasing STOP mode. The $\overline{\text{RESET}}$ pin input must also be "H" level, rising together with the power supply voltage. In this case, if an external time constant circuit has been connected, the $\overline{\text{RESET}}$ pin input voltage will increase at a slower pace than the power supply voltage. At this time, there is a danger that a reset may occur if input voltage level of the $\overline{\text{RESET}}$ pin drops below the non-inverting high-level input voltage (hysteresis input).



(a) STOP mode start (Example : Start with SET (SYSCR1). 7 instruction located at address a)



(b) STOP mode release

Figure 1-11. STOP Mode Start / Release

(2) IDLE1/2 mode, SLEEP1/2 mode

IDLE1/2 and SLEEP1/2 modes are controlled by the system control register 2 (SYSCR2) and maskable interrupts. The following status is maintained during these modes.

- ① Operation of the CPU and watchdog timer (WDT) is halted. On-chip peripherals continue to operate.
- ② The data memory, CPU registers, program status word and port output latches are all held in the status in effect before these modes were entered.
- ③ The program counter holds the address 2 ahead of the instruction which starts these modes.

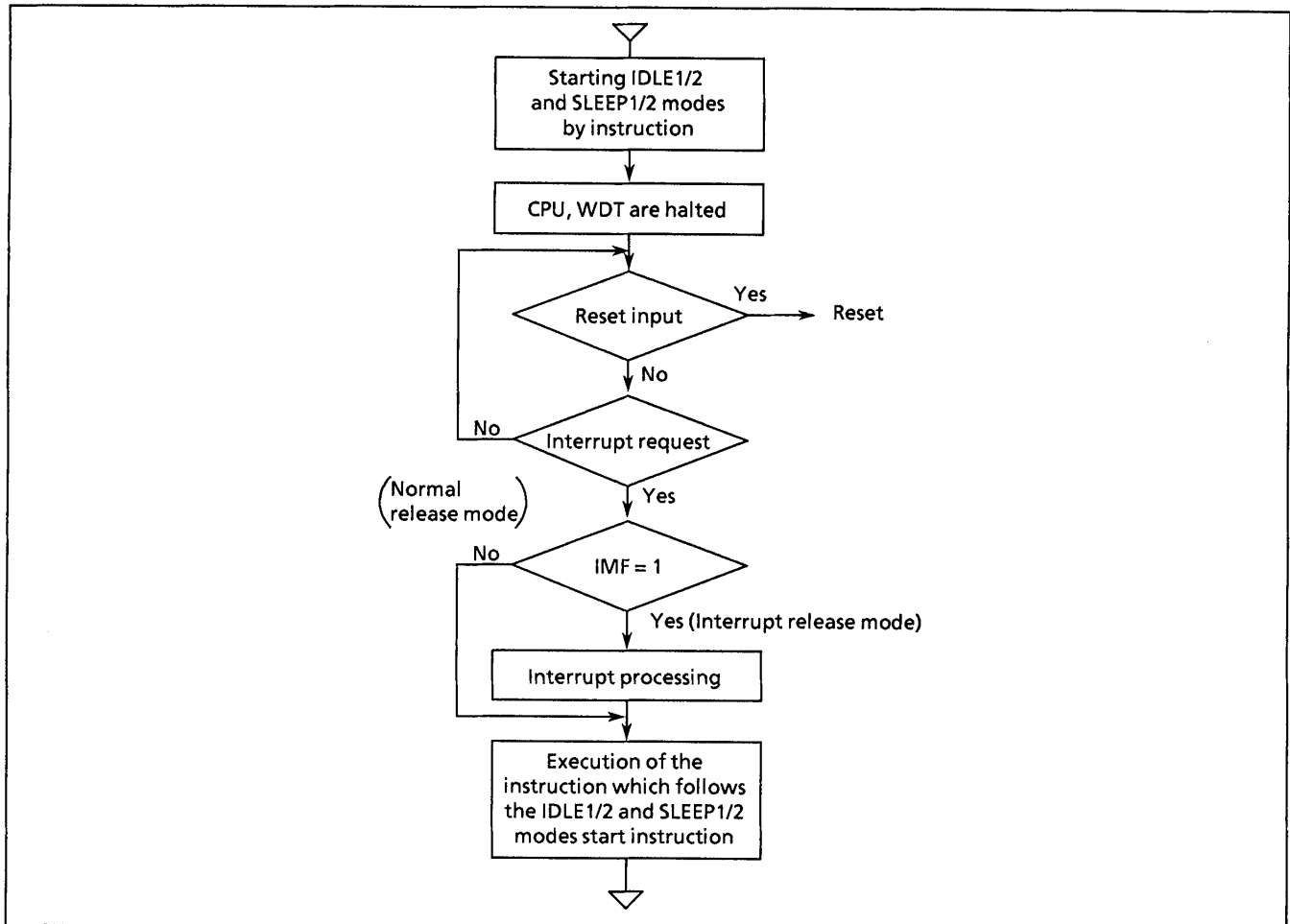


Figure 1-12. IDLE1/2, SLEEP1/2 Modes

- Start the IDLE1/2 and SLEEP1/2 modes

When IDLE1/2 and SLEEP1/2 modes start, set SYSCR2 <IDLE> to "1".

- Release the IDLE1/2 and SLEEP1/2 modes

IDLE1/2 and SLEEP1/2 modes include a normal release mode and an interrupt release mode. These modes are selected by interrupt master enable flag (IMF).

After releasing IDLE1/2 and SLEEP1/2 modes, the SYSCR2 <IDLE> is automatically cleared to "0" and the operation mode is returned to the mode preceding IDLE1/2 and SLEEP1/2 modes.

IDLE1/2 and SLEEP1/2 modes can also be released by inputting low level on the $\overline{\text{RESET}}$ pin. After releasing reset, the operation mode is started from NORMAL1 mode.

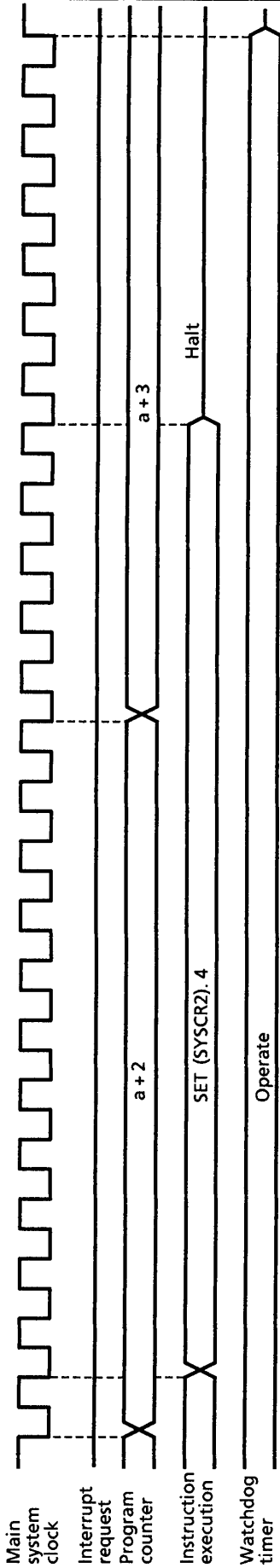
a. Normal release mode (IMF = "0")

IDLE1/2 and SLEEP1/2 modes are released by any interrupt source enabled by the individual interrupt enable flag (EF). After the interrupt is generated, the program operation is resumed from the instruction following the IDLE1/2 and SLEEP1/2 modes start instruction. Normally, the interrupt latches (IL) of the interrupt source used for releasing must be cleared to "0" by load instructions.

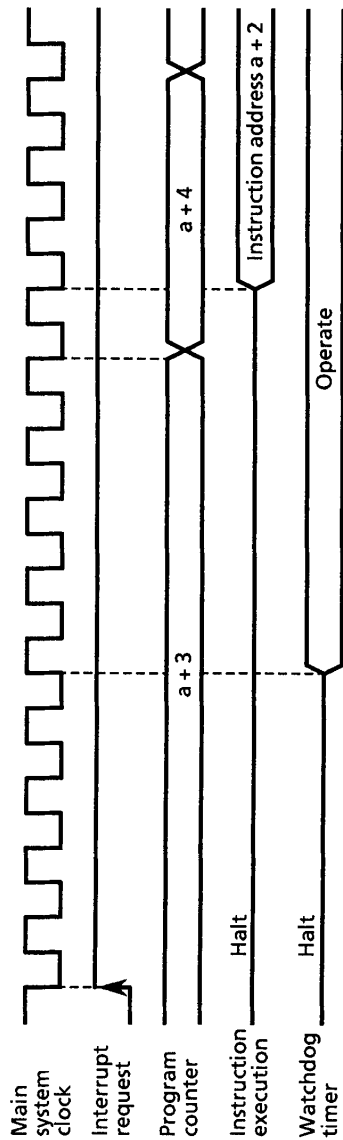
b. Interrupt release mode (IMF = "1")

IDLE1/2 and SLEEP1/2 modes are released by any interrupt source enabled with the individual interrupt enable flag (EF) and INTTBT interrupt processing is started. After the interrupt is processed, the program operation is resumed from the instruction following the instruction, which starts IDLE1/2 and SLEEP1/2 modes.

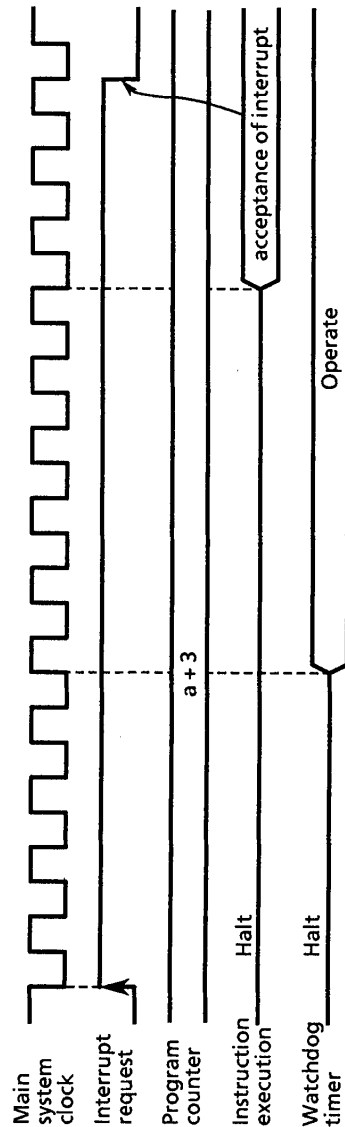
Note: When a watchdog timer interrupts is generated immediately before IDLE1/2 and SLEEP1/2 mode are started, the watchdog timer interrupt will be processed but IDLE1/2 and SLEEP1/2 mode will not be started.



(a) IDLE1/2, SLEEP1/2 mode start (Example: starting with the SET instruction located at address a)



① Normal release mode



② Interrupt release mode

(b) IDLE1/2, SLEEP1/2 mode release

Figure 1-13. IDLE1/2, SLEEP1/2 Mode Start / Release

(3) IDLE0, SLEEP0 mode (IDLE0,SLEEP0)

IDLE0 and SLEEP0 modes are controlled by the system control register 2 (SYSCR2) and the time base timer control register (TBTCR). The following status is maintained during IDLE0 and SLEEP0 modes.

- ① Timing generator stops feeding clock to peripherals except TBT.
- ② The data memory, CPU registers, program status word and port output latches are all held in the status in effect before IDLE0 and SLEEP0 modes were entered.
- ③ The program counter holds the address 2 ahead of the instruction which starts IDLE0 and SLEEP0 modes.

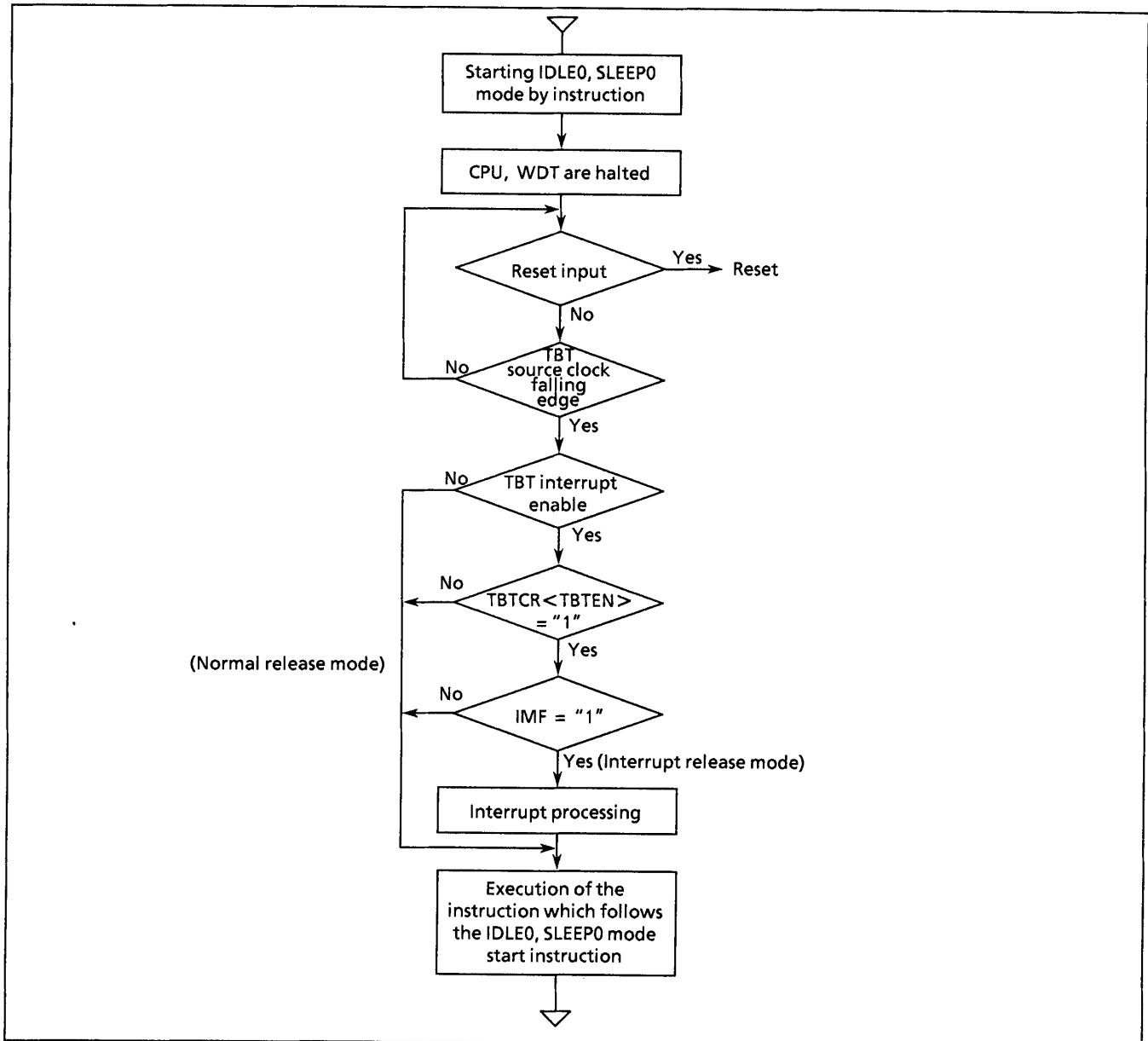


Figure 1-14. IDLE0, SLEEP0 mode

- Start the IDLE0 and SLEEP0 modes

When IDLE0 and SLEEP0 modes start, set SYSCR2<TGHALT> to "1".

- Release the IDLE0 and SLEEP modes

IDLE0 and SLEEP0 modes include a normal release mode and an interrupt release mode.

These modes are selected by interrupt master flag (IMF).

After releasing IDLE0 and SLEEP0 modes, the SYSCR2<TGHALT> is automatically cleared to "0" and the operation mode is returned to the mode preceding IDLE0 and SLEEP0 modes. Before starting the IDLE0 or SLEEP0 mode, when the TBTCR<TBTEN> is set to "1", INTTBT interrupt latch is set to "1".

IDLE0 and SLEEP0 modes can also be released by inputting low level on the $\overline{\text{RESET}}$ pin. After releasing reset, the operation mode is started from NORMAL1 mode.

Note: IDLE0 and SLEEP0 modes start/release without reference to TBTCR<TBTEN> setting.

a. Normal release mode (IMF = "0")

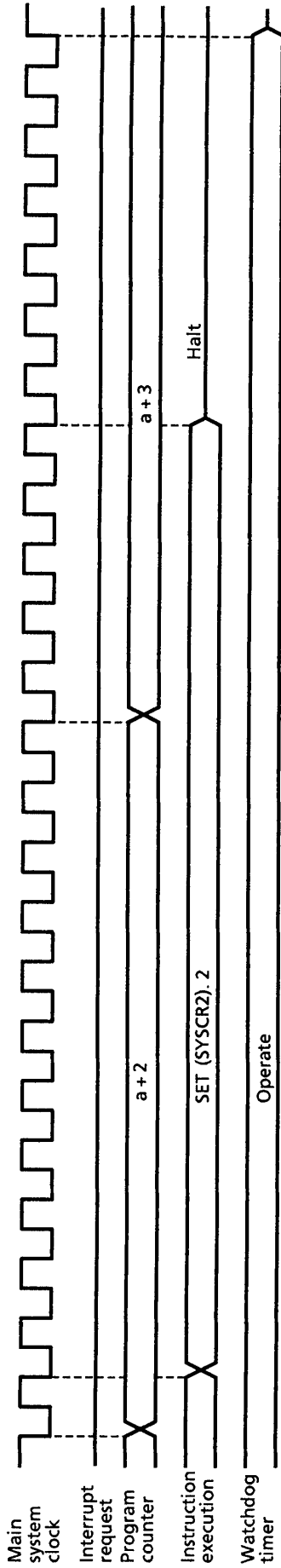
IDLE0 and SLEEP0 modes are released by the source clock falling edge, which is setting by the TBTCR<TBTK> without reference to individual interrupt enable flag (EF). After the falling edge is detected, the program operation is resumed from the instruction following the IDLE0 and SLEEP0 modes start instruction.

b. Interrupt release mode (IMF = "1", TBTCR<TBTEN> = "1")

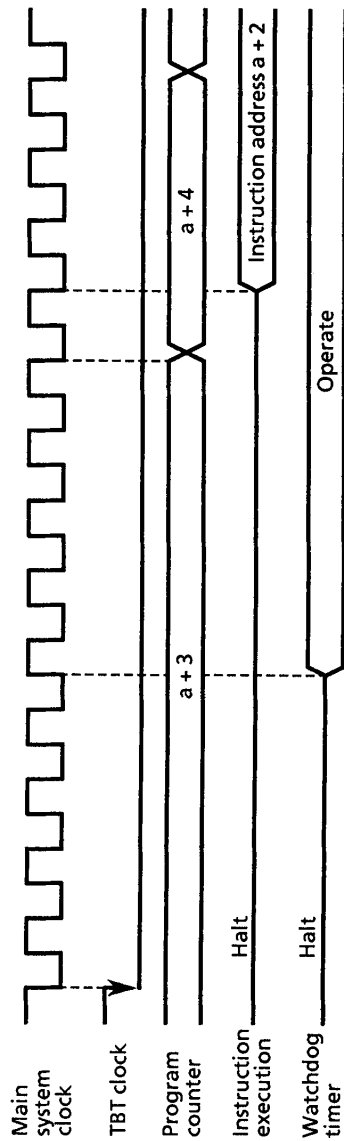
IDLE0 and SLEEP0 modes are released by the source clock falling edge, which is setting by the TBTCR<TBTK> at INTTBT interrupt source enabled with the individual interrupt enable flag (EF) and INTTBT interrupt processing is started.

Note 1: Because returning from IDLE0, SLEEP0 to NORMAL1, SLOW1 is executed by the asynchronous internal clock, the period of IDLE0, SLEEP0 mode might be the shorter than the period setting by TBTCR<TBTK>.

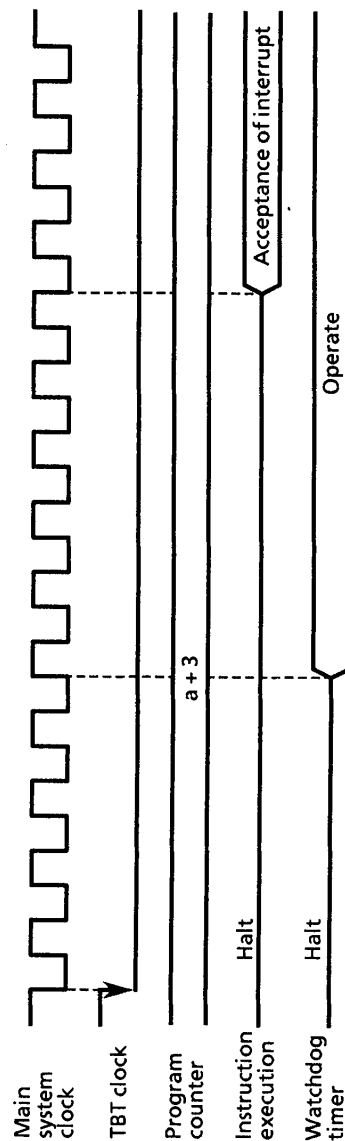
Note 2: When a watchdog timer interrupt is generated immediately before IDLE0/SLEEP0 mode is started, the watchdog timer interrupt will be processed but IDLE0/SLEEP0 mode will not be started.



(a) IDLE0, SLEEP0 mode start (Example: starting with the SET instruction located at address a)



① Normal release mode



② Interrupt release mode

(b) IDLE0, SLEEP0 mode release

Figure 1-15. IDLE0, SLEEP0 Mode Start / Release

(4) SLOW mode

SLOW mode is controlled by the system control register 2 (SYSCR2).

The following is the methods to switch the mode with the warming-up counter (TC4, 3).

a. Switching from NORMAL2 mode to SLOW1 mode

First, set SYSCK (bit 5 in SYSCR2) to switch the main system clock to the low-frequency clock for SLOW2 mode.

Next, clear XEN (bit 7 in SYSCR2) to turn off high-frequency oscillation.

Note: The high-frequency clock oscillation can be continued to return quickly to NORMAL2 mode.

When the low-frequency clock oscillation is unstable, wait until oscillation stabilizes before performing the above operations. The timer / counter 4, 3 (TC4, TC3) can conveniently be used to confirm that low-frequency clock oscillation has stabilized.

Example1: Switching from NORMAL2 mode to SLOW1 mode.

```

SET (SYSCR2). 5      ; SYSCR2<SYSCK> ← 1
                      ; (switches the main system clock to the low-frequency
                      ; clock for SLOW2)
CLR (SYSCR2). 7      ; SYSCR2<XEN> ← 0
                      ; (turns off high-frequency oscillation)

```

Example2: Switching to the SLOW1 mode after low-frequency clock has stabilized.

```

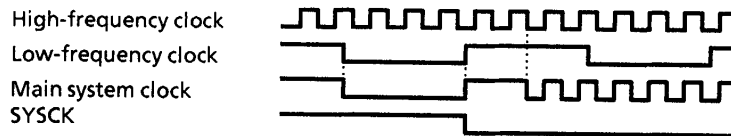
SET (SYSCR2).6      ; SYSCR2<XTEN> ← 1
LD (TC3CR), 43H     ; Sets mode for TC4, TC3 (16-bit TC, fs for source)
LD (TC4CR), 05H
LDW (TTREG3), 8000H ; Sets warming-up time
                    ; (depend on oscillator accompanied)
DI                  ; IMF ← 0
SET (EIRH). 3      ; Enables INTTC4
EI                  ; IMF ← 1
SET (TC4CR). 3     ; Starts TC4, 3
:
PINTTC4: CLR (TC4CR). 3 ; Stops TC4, 3
SET (SYSCR2). 5     ; SYSCR2<SYSCK> ← 1 (Switches the main system clock
                    ; to the low-frequency clock)
CLR (SYSCR2). 7     ; SYSCR2<XEN> ← 0
                    ; (Turns off high-frequency oscillation)
RETI
:
VINTTC4: DW PINTTC4 ; INTTC4 vector table

```

b. Switching from SLOW1 mode to NORMAL2 mode

First, set XEN (bit 7 in SYSCR2) to turn on the high-frequency oscillation. When time for stabilization (warm-up) has been taken by the timer / counter 4, 3 (TC4, 3), clear SYSCK (bit 5 in SYSCR2) to switch the main system clock to the high-frequency clock.

Note 1: After SYSCK is cleared to "0", executing the instructions is continued by the low-frequency clock for the period synchronized with low-frequency and high-frequency clocks.



Note 2: SLOW mode can also be released by inputting low level on the RESET pin, which immediately performs the reset operation. After reset, the TMP86C420/820 are placed in NORMAL1 mode.

Example: Switching from the SLOW1 mode to the NORMAL2 mode

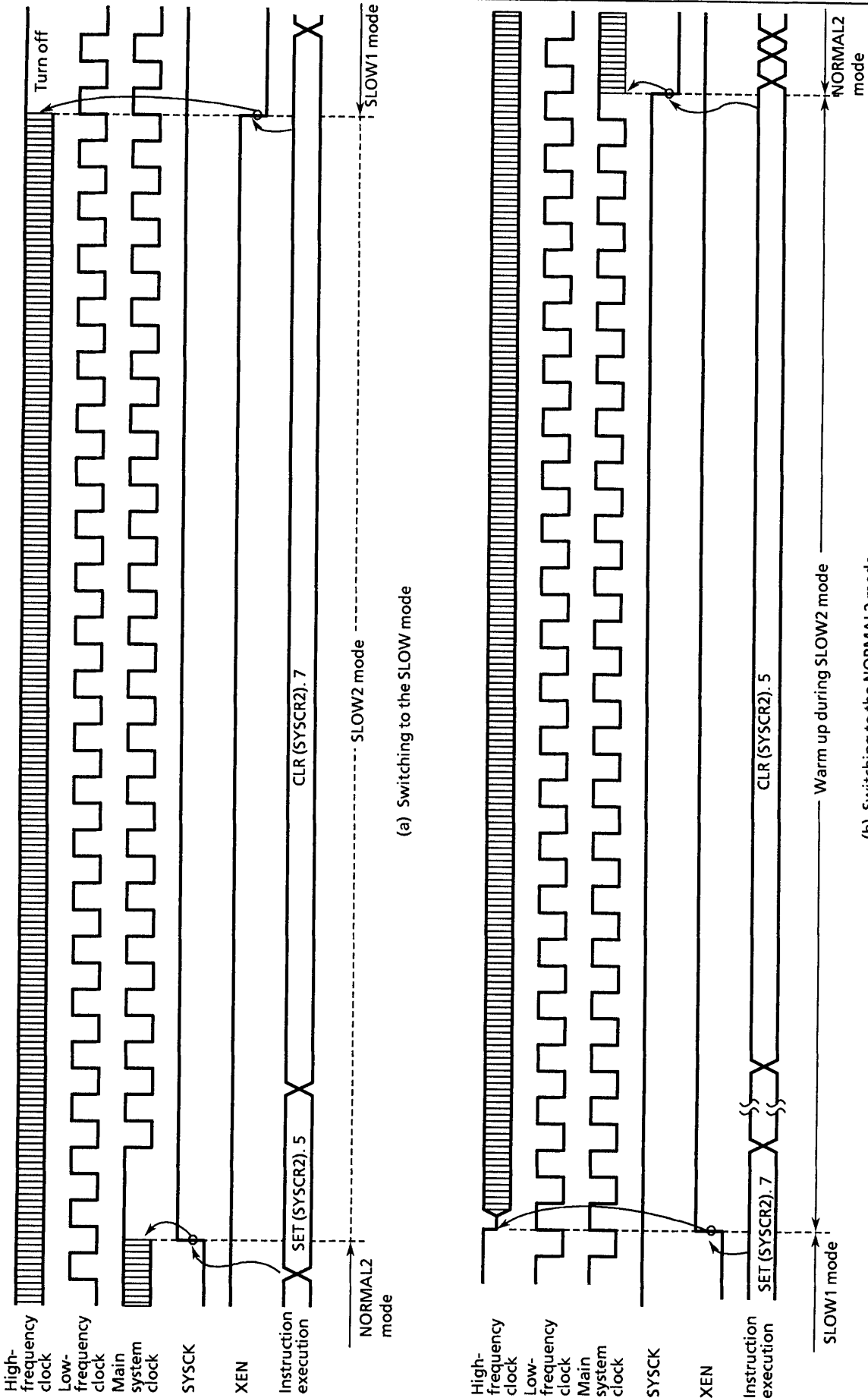
(fc = 16 MHz, warm-up time is 4.0 ms).

```

SET  (SYSCR2). 7      ; SYSCR2<XEN> ← 1 (Starts high-frequency oscillation)
LD   (TC3CR), 63H    ; Sets mode for TC4, TC3 (16-bit TC, fc for source)
LD   (TC4CR), 05H

LD   (TTREG4), 0F8H  ; Sets warming-up time
DI                                       ; IMF ← 0
SET  (EIRH). 3      ; Enables INTTC4
EI                                       ; IMF ← 1
SET  (TC4CR). 3     ; Starts TC4, 3
:
PINTTC4: CLR (TC4CR). 3 ; Stops TC4, 3
      CLR (SYSCR2). 5 ; SYSCR2<SYSCK> ← 0
                          (Switches the main system clock to the high-frequency
                          clock)

      RETI
:
VINTTC4: DW  PINTTC4 ; INTTC4 vector table
    
```



(a) Switching to the SLOW mode

(b) Switching to the NORMAL2 mode

Figure 1-16. Switching between the NORMAL2 and SLOW Modes

1.5 Interrupt Control Circuit

The TMP86C420/820 are a total (Reset is excluded) of 15 interrupt sources for 17 interrupt factors; 1 of the sources are multiplexed. Multiple interrupt with priorities is available. 5 of the internal factors are non-maskable interrupts, and the rest of them are maskable interrupts.

Interrupt sources are provided with interrupt latches (IL), which hold interrupt requests, and independent vectors. The interrupt latch is set to "1" by the generation of its interrupt request which requests the CPU to accept its interrupts. Interrupts are enabled or disabled by software using the interrupt master enable flag (IMF) and interrupt enable flag (EF). If more than one interrupts are generated simultaneously, interrupts are accepted in order which is dominated by hardware. However, there are no prioritized interrupt factors among non-maskable interrupts.

Table 1-2. Interrupt Sources

Interrupt Factors		Enable Condition	Interrupt Latch	Vector Address	Priority
Internal / External	(Reset)	non-maskable	—	FFFE _H	High 1
Internal	INTSWI (Software interrupt)	non-maskable	—	FFFC _H	2
Internal	INTUNDEF (Executed the Undefined Instruction interrupt)	non-maskable	—	FFFC _H	2
Internal	INTATRAP (Address Trap interrupt)	non-maskable	IL ₂	FFFA _H	2
Internal	INTWDT (Watchdog Timer interrupt)	non-maskable	IL ₃	FFF8 _H	2
External	$\overline{\text{INT}}_0$ (External interrupt 0)	IMF = 1, EF ₄ = 1	IL ₄	FFF6 _H	5
External	INT1 (External interrupt 1)	IMF = 1, EF ₅ = 1	IL ₅	FFF4 _H	6
Internal	INTTBT (Time Base Timer interrupt)	IMF = 1, EF ₆ = 1	IL ₆	FFF2 _H	7
External	INT2 (External interrupt2)	IMF = 1, EF ₇ = 1	IL ₇	FFF0 _H	8
Internal	INTTC1 (18-bit TC1 interrupt)	IMF = 1, EF ₈ = 1	IL ₈	FFEE _H	9
Internal	INTSIO (SIO interrupt)	IMF = 1, EF ₉ = 1	IL ₉	FFEC _H	10
reserved		IMF = 1, EF ₁₀ = 1	IL ₁₀	FFEA _H	11
Internal	INTTC4 (TC4 interrupt)	IMF = 1, EF ₁₁ = 1	IL ₁₁	FFE8 _H	12
reserved		IMF = 1, EF ₁₂ = 1	IL ₁₂	FFE6 _H	13
Internal	INTADC (AD converter interrupt)	IMF = 1, EF ₁₃ = 1	IL ₁₃	FFE4 _H	14
External	INT3 (External interrupt 3)	IMF = 1, EF ₁₄ = 1	IL ₁₄	FFE2 _H	15
Internal	INTTC3 (TC3 interrupt)				
External	$\overline{\text{INT}}_5$ (External interrupt 5)	IMF = 1, EF ₁₅ = 1	IL ₁₅	FFE0 _H	Low 16

Note 1: The following interrupt factors share their interrupt source; the factor is selected on the register INTSEL.

- 1) INT3 and INTTC3 share the source whose priority is 15.

Note 2: 2 alternatives are to be chosen in case INTATRAP (address trap interrupt) is executed: interrupt or reset.

(for detail, see 2.4.5 address trap interrupt (INTATRAP))

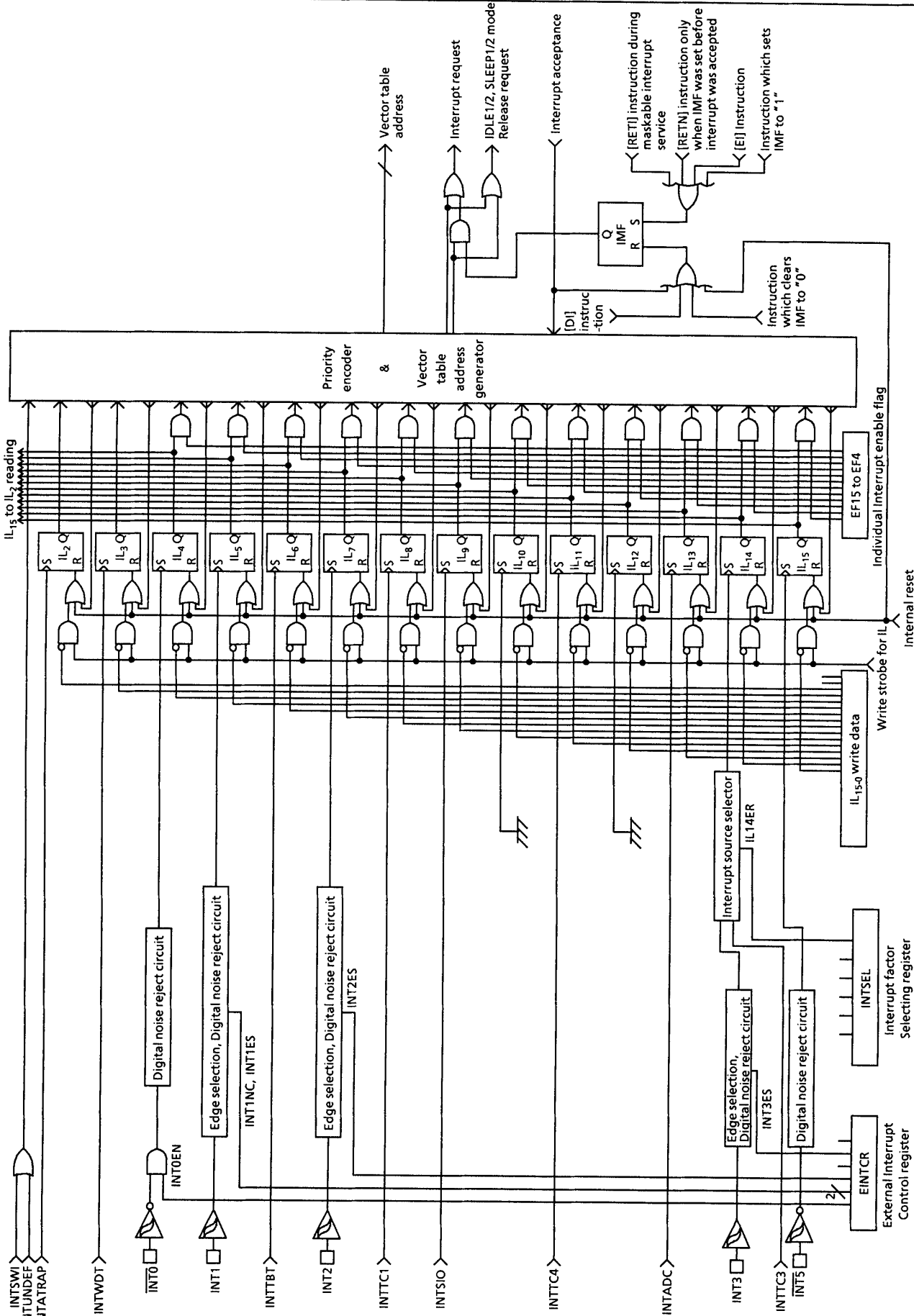


Figure 1-17. Interrupt Controller Block Diagram

(1) Interrupt Latches (IL₁₅ to IL₂)

An interrupt latch is provided for each interrupt source, except for a software interrupt. When interrupt request is generated, the latch is set to "1", and the CPU is requested to accept the interrupt if its interrupt is enabled. All interrupt latches are initialized to "0" during reset.

The interrupt latches are located on address 003C_H and 003D_H in SFR area. Except for IL₃ and IL₂, each latch can be cleared to "0" individually by instruction (However, the read-modify-write instructions such as bit manipulation or operation instructions cannot be used. Interrupt request would be cleared inadequately if interrupt is requested while such instructions are executed.). Thus interrupt request can be canceled /initialized by software.

Interrupt latches are not set to "1" by an instruction. Since interrupt latches can be read, the status for interrupt requests can be monitored by software.

Note: When manipulating IL, clear IMF (to disable interrupts) beforehand.

Example 1: Clears interrupt latches

```
DI                                ; IMF←0
LDW  (ILL), 1110100000111111B    ; IL12, IL10 to IL6←0
EI                                ; IMF←1
```

Example 2: Reads interrupt latches

```
LD      WA, (ILL)                ; W←ILH, A←ILL
```

Example 3: Tests an interrupt latches

```
TEST  (ILL). 7                   ; if IL7 = 1 then jump
JR    F, SSET
```

(2) Interrupt Enable Register (EIR)

The interrupt enable register (EIR) enables and disables the acceptance of interrupts, except for the non-maskable interrupts (software interrupt, undefined instruction interrupt, address trap interrupt and watchdog interrupt). Non-maskable interrupt is accepted regardless of the contents of the EIR.

The EIR consists of an interrupt master enable flag (IMF) and the individual interrupt enable flags (EF). These registers are located on address 003A_H and 003B_H in SFR area, and they can be read and written by an instructions (including read-modify-write instructions such as bit manipulation or operation instructions).

a) Interrupt master enable flag (IMF)

The interrupt enable register (IMF) enables and disables the acceptance of the whole maskable-interrupt. While IMF="0", all maskable interrupts are not accepted regardless of the status on each individual interrupt enable flag (EF). By setting IMF to "1", the interrupt becomes acceptable if the individuals are enabled. When an interrupt is accepted, IMF is cleared to "0" after the latest status on IMF is stacked. Thus the maskable interrupts which follow are disabled. By executing return interrupt instruction [RETI/RETN], the stacked data, which was the status before interrupt acceptance, is loaded on IMF again.

The IMF is located on bit0 in EIRL (address: 003A_H in SFR), and can be read and written by an instruction. The IMF is normally set and cleared by [EI] and [DI] instruction respectively. During reset, the IMF is initialized to "0", and maskable interrupts are not accepted until it is set to "1".

b) Individual interrupt enable flags (EF₁₅ to EF₄)

Each of these flags enables and disables the acceptance of its maskable interrupt. Setting the corresponding bit of an individual interrupt enable flag to “1” enables acceptance of its interrupt, and setting the bit to “0” disables acceptance. The individual interrupt enable flags (EF₁₅ to EF₄) are located on EIRL to EIRH (address: 003A_H to 003B_H in SFR), and can be read and written by an instruction. During reset, all the individual interrupt enable flags (EF₁₅ to EF₄) are initialized to “0” and all maskable interrupts are not accepted until they are set to “1”.

Note: Before manipulating EF, be sure to clear IMF (interrupt disabled). Then set IMF newly again after operating on the interrupt enables flag (EF). Normally, IMF is clear to “0” automatically on service routine. When IMF is set to “1” for using a multiple interrupt on service routine, be sure to process as is the case with EF.

Example 1: Enables interrupts individually and sets IMF

```

DI                               ; IMF ← 0
LDW (EIRL), 1110100010100000B   ; EF15 to EF13, EF11, EF7, EF5 ← 1
      :                               Note: IMF is not set.
      :
EI                               ; IMF ← 1
    
```

Example 2: C compiler description example

```

unsigned int __io (3AH) EIRL;      ; /* 3AH shows EIRL address */
__DI ();
EIRL = 10100000B;
      :
__EI ();
    
```

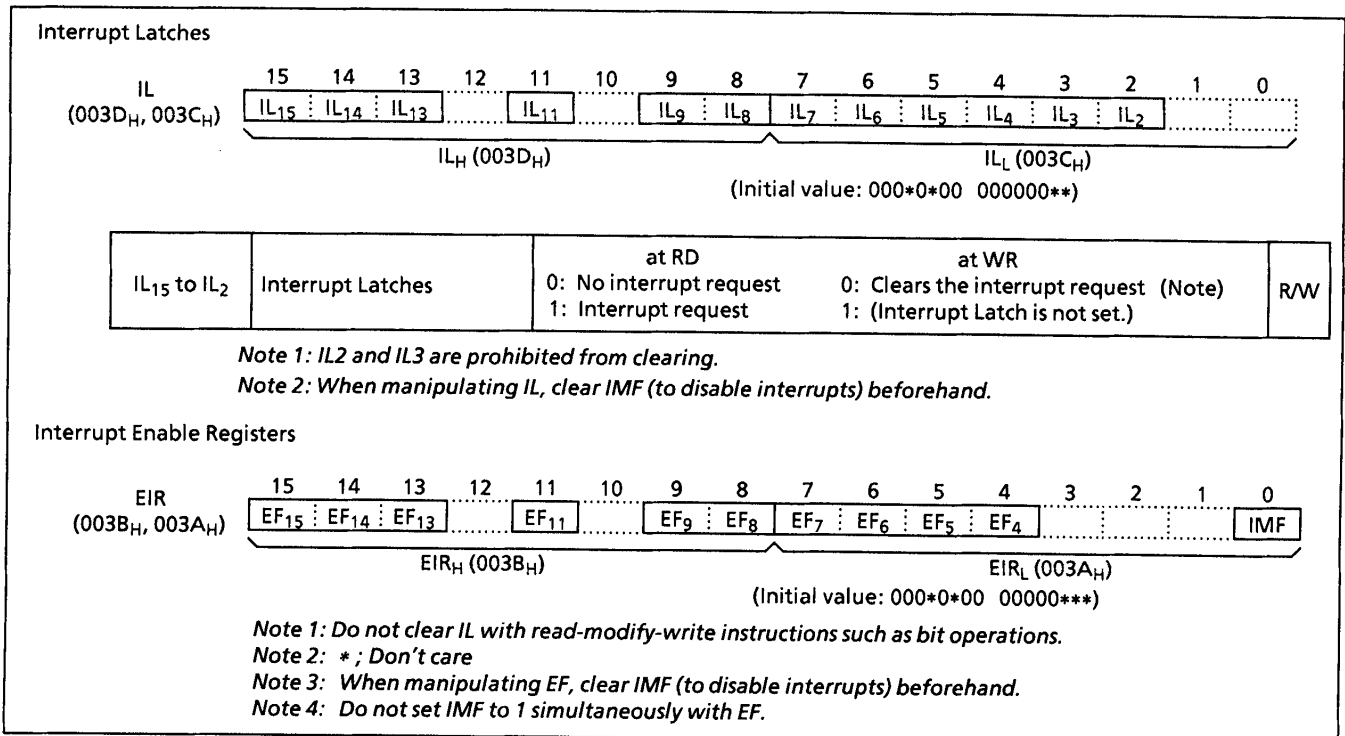


Figure 1-18. Interrupt Latch (IL) , Interrupt Enable Registers (EIR)

(3) Selecting interrupt factor (INTSEL)

Each interrupt factor, that shares its interrupt source with other factors, enables its interrupt latch (IL) only if it is selected on INTSEL. The interrupt controller does not hold the interrupt request, while the factor generates the interrupt request is not selected on INTSEL. Therefore, set INTSEL appropriately before interrupt factors arises.

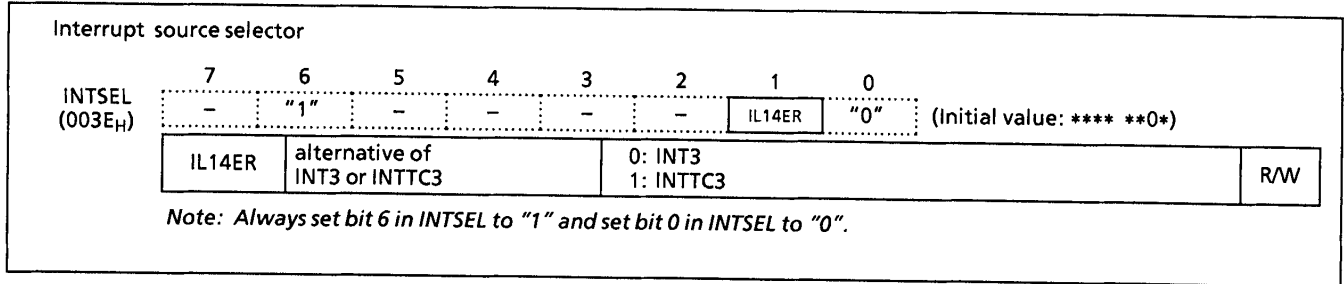


Figure 1-19. Interrupt Source Selector

1.5.1 Interrupt Sequence

An interrupt request, which raised interrupt latch, is held, until interrupt is accepted or interrupt latch is cleared to "0" by resetting or an instruction. Interrupt acceptance sequence requires 8 machine cycles (4 μs at 8.0 MHz) after the completion of the current instruction. The interrupt service task terminates upon execution of an interrupt return instruction [RETI] (for maskable interrupts) or [RETN] (for non-maskable interrupts). Figure 1-18 shows the timing chart of interrupt acceptance processing.

- (1) Interrupt acceptance processing is packaged as follows.
 - a) The interrupt latch (IL) for the interrupt source accepted is cleared to "0".
 - b) The contents of the program counter (PC) and the program status word, including the interrupt master enable flag (IMF), are saved (pushed) on the stack in sequence of PSW + IMF, PCH, PCL. Meanwhile, the stack pointer (SP) is decremented by 3.
 - c) The interrupt master enable flag (IMF) is cleared to "0" in order to disable the acceptance of any following interrupt.
 - d) The entry address (interrupt vector) of the corresponding interrupt service program, loaded on the vector table, is transferred to the program counter.
 - e) The instruction stored at the entry address of the interrupt service program is executed.

Note: When the contents of the PSW are saved on the stack, the IMF status is also saved simultaneously.

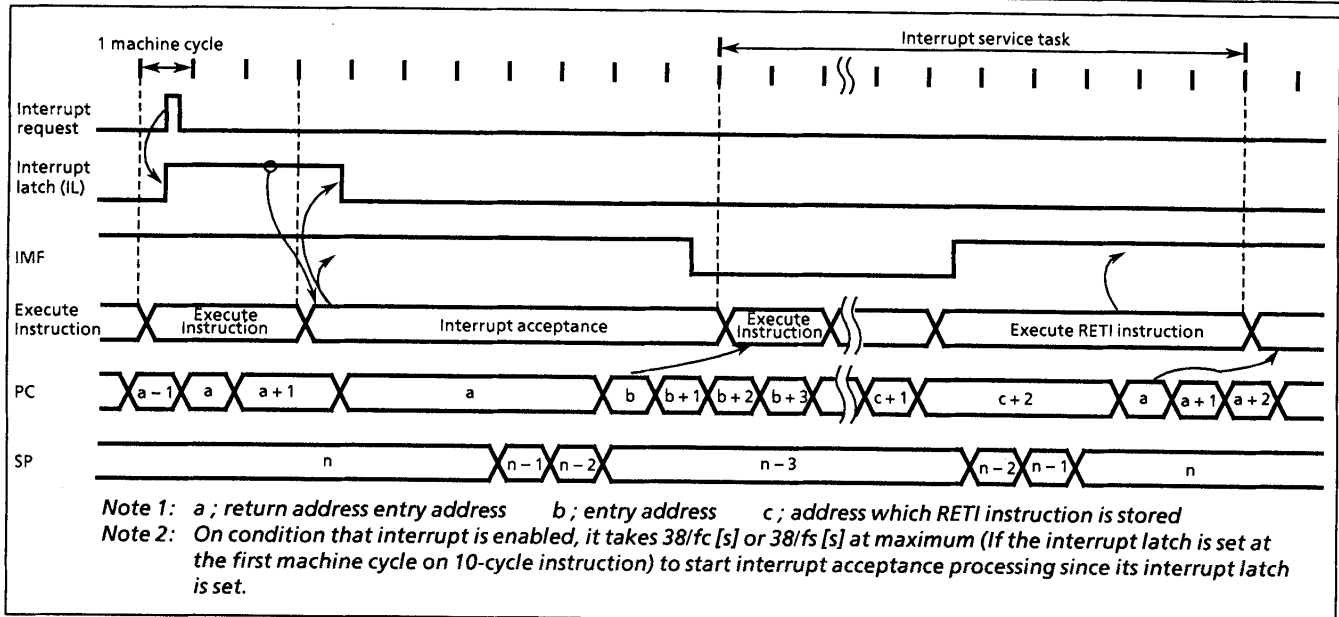
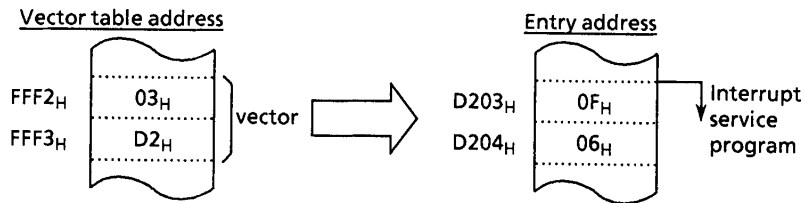


Figure 1-20. Timing chart of Interrupt Acceptance/Return Interrupt instruction

Example: Correspondence between vector table address for INTTBT and the entry address of the interrupt service program



A maskable interrupt is not accepted until the IMF is set to "1" even if the maskable interrupt higher than the level of current servicing interrupt is requested.

In order to utilize nested interrupt service, the IMF is set to "1" in the interrupt service program. In this case, acceptable interrupt sources are selectively enabled by the individual interrupt enable flags. To avoid overloaded nesting, clear the individual interrupt enable flag whose interrupt is currently serviced, before setting IMF to "1". As for non-maskable interrupt, keep interrupt service shorter compared with length between interrupt requests; otherwise the status cannot be recovered as non-maskable interrupt would simply nested.

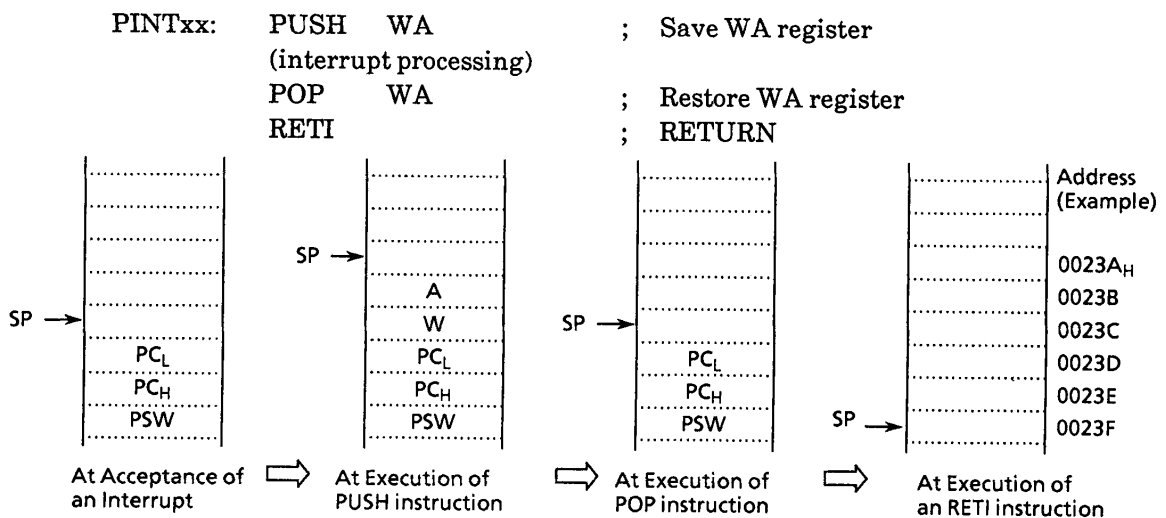
(2) Saving/Restoring general -purpose registers

During interrupt acceptance processing, the program counter (PC) and the program status word (PSW, includes IMF) are automatically saved on the stack, but the accumulator and others are not. These registers are saved by software if necessary. When multiple interrupt services are nested, it is also necessary to avoid using the same data memory area for saving registers. The following methods are used to save/restore the general-purpose registers.

a) using PUSH and POP instructions

To save only a specific register, PUSH and POP instructions are available.

Example: save/store register using PUSH and POP instructions



b) using data transfer instructions

To save only a specific register without nested interrupts, data transfer instructions are available.

Example: save/store register using data transfer instructions

```

PINTxx: LD    (GSAVA), A      ; Save A register
          (interrupt processing)
          LD    A, (GSAVA)    ; Restore A register
          RETI                 ; RETURN
    
```

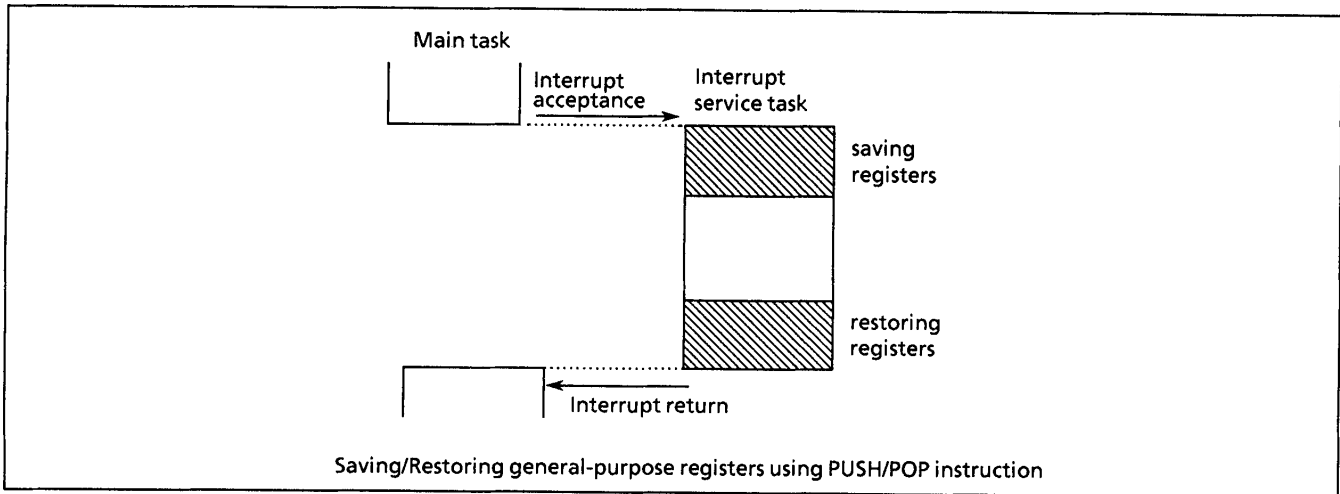


Figure 1-21. Saving/Restoring general-purpose registers under interrupt processing

(3) Interrupt return

Interrupt return instructions [RETI] / [RETN] perform as follows.

[RETI] / [RETN] Interrupt Return
① Program Counter (PC) and program status word (PSW, includes IMF) are restored from the stack.
② Stack pointer (SP) is incremented by 3.

As for Address Trap interrupt (INTARTAP), it is required to alter stacked data for program counter (PC) to restarting address, during interrupt service program. Otherwise returning interrupt causes INTATRAP again. When interrupt acceptance processing has completed, stacked data for PC_L and PC_H are located on address (SP + 1) and (SP + 2) respectively.

Note: If the return instruction [RETN] is executed without rewriting the above data, the program returns to the address trap area and an address trap interrupt occurs again. After interrupt acceptance processing has completed, the PC_L and PC_H values after returning from the interrupt are stored in addresses (SP + 1) and (SP + 2), respectively.

Example 1: returning from address trap interrupt (INTATRAP) service program

```
PINTxx : POP    WA                ; Recover SP by 2
         LD     WA, Return Address ;
         PUSH  WA                ; Alter stacked data
         (interrupt processing)
         RETN                    ; RETURN
```

Example 2: restarting without returning interrupt

(In this case, PSW (includes IMF) before interrupt acceptance is discarded.)

```
PINTxx : INC     SP                ; Recover SP by 3
         INC     SP                ;
         INC     SP                ;
         (interrupt processing)
         LD     EIRL, data         ; Set IMF to "1" or clear it to "0"
         JP     Restart Address   ; Jump into restarting address
```

Note: It is recommended that stack pointer be return to rate before INTATRAP (increment 3 times), if return interrupt instruction [RETN] is not utilized during interrupt service program under INTATRAP (such as Example 2).

Interrupt requests are sampled during the final cycle of the instruction being executed. Thus, the next interrupt can be accepted immediately after the interrupt return instruction is executed.

Note: When the interrupt processing time is longer than the interrupt request generation time, the interrupt service task is performed but not the main task.

1.5.2 Software Interrupt (INTSW)

Executing the [SWI] instruction generates a software interrupt and immediately starts interrupt processing (INTSW is highest prioritized interrupt).

Use the [SWI] instruction only for detection of the address error or for debugging.

① Address error detection

FF_H is read if for some cause such as noise the CPU attempts to fetch an instruction from a non-existent memory address during single chip mode. Code FF_H is the SWI instruction, so a software interrupt is generated and an address error is detected. The address error detection range can be further expanded by writing FF_H to unused areas of the program memory. Address-trap reset is generated in case that an instruction is fetched from RAM or SFR areas.

② Debugging

Debugging efficiency can be increased by placing the SWI instruction at the software break point setting address.

1.5.3 Undefined instruction interrupt (INTUNDEF)

Taking code which is not defined as authorized instruction for instruction causes INTUNDEF. INTUNDEF is generated when the CPU fetches such a code and tries to execute it. INTUNDEF is accepted even if non-maskable interrupt is in process. Contemporary process is broken and INTUNDEF interrupt process starts, soon after it is requested.

Note: The undefined instruction interrupt (INTUNDEF) forces CPU to jump into vector address, as software interrupt (SWI) does.

1.5.4 Address trap interrupt (INTATRAP)

Fetching instruction from unauthorized area for instructions (address trapped area) causes reset-output or address trap interrupt (INTATRAP). INTATRAP is accepted even if non-maskable interrupt is in process. Contemporary process is broken and INTATRAP interrupt process starts, soon after it is requested.

Note: The operating mode under address trapped, whether to be reset-output or interrupt processing, is selected on watchdog timer control register (WDTCR).

1.5.5 External interrupts

The TMP86C420/820 have five external interrupt inputs. These inputs are equipped with digital noise reject circuits (pulse inputs of less than a certain time are eliminated as noise).

Edge selection is also possible with INT1 to INT3. The $\overline{INT0}$ /P63 pin can be configured as either an external interrupt input pin or an input/output port, and is configured as an input port during reset.

Edge selection, noise reject control and $\overline{INT0}$ /P63 pin function selection are performed by the external interrupt control register (EINTCR).

Table 1-3. External Interrupts

Source	Pin	Secondary function pin	Enable conditions	Edge	Digital noise reject
INT0	$\overline{INT0}$	P63/AIN3	IMF = 1, EF ₄ = 1, INTOEN = 1	falling edge	Pulses of less than 2/fc [s] are eliminated as noise. Pulses of 6/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3/fs [s] or more are considered to be signals.
INT1	INT1	P12/SEG29	IMF · EF ₅ = 1	falling edge or rising edge	Pulses of less than 15/fc or 63/fc [s] are eliminated as noise. Pulses of 48/fc or 192/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3/fs [s] or more are considered to be signals. Pulses of less than 7/fc [s] are eliminated as noise. Pulses of 24/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3/fs [s] or more are considered to be signals.
INT2	INT2	P13/SEG28	IMF · EF ₇ = 1		
INT3	INT3	P14/SEG27	IMF · EF ₁₄ = 1 IL14ER = 0		
INT5	$\overline{INT5}$	P20/ \overline{STOP}	IMF · EF ₁₅ = 1 IL15ER = 0	falling edge	Pulses of less than 2/fc [s] are eliminated as noise. Pulses of 6/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3/fs [s] or more are considered to be signals.

Note1: If a noiseless signal is input to the external interrupt pin in the NORMAL 1/2 or IDLE 1/2 mode, the maximum time from the edge of input signal until the IL is set is as follows :

- ① INT1 pin 49/fc [s] (INT1NC = 1), 193/fc [s] (INT1NC = 0)
- ② INT2, INT3 pin 25/fc [s]

Note2: Even if the falling edge of $\overline{INT0}$ pin input is detected at INTOEN = 0, the interrupt latch IL₄ is not set.

Note3: When data changed and did a change of I/O when used external interrupt ports as a normal ports, interrupt request signal occurs incorrectly. Handling of prohibition of interrupt enable register (EIR) is necessary.

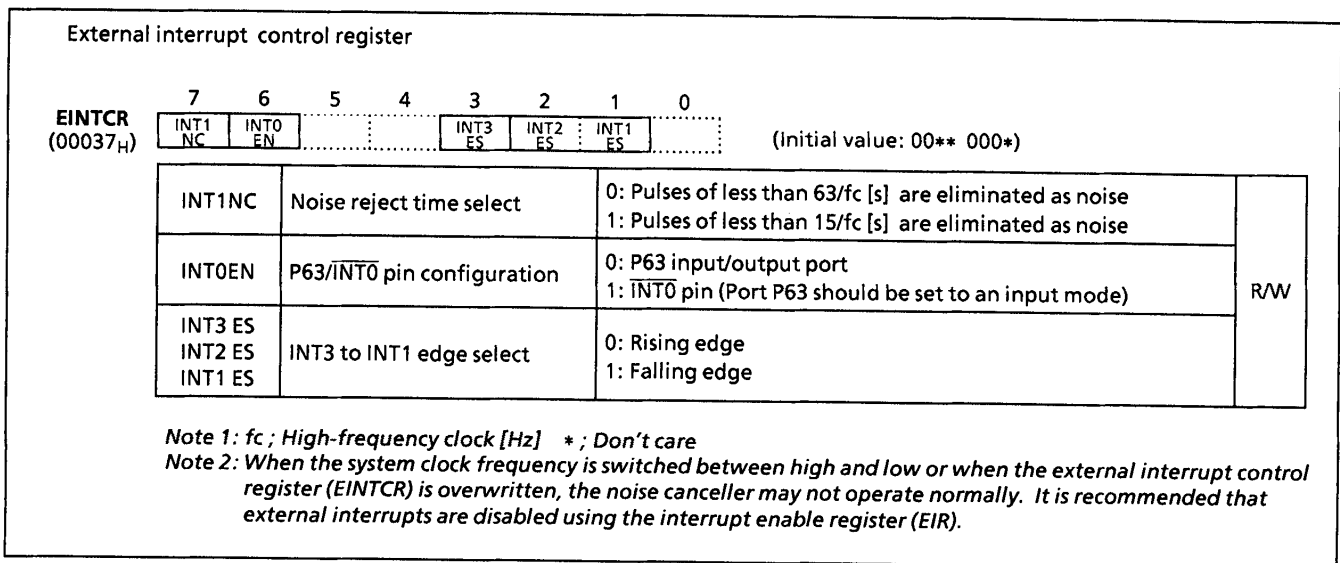


Figure 1-22. External Interrupt Control Register

1.6 Reset Circuit

The TMP86C420/820 have four types of reset generation procedures : an external reset input, an address trap reset output, a watchdog timer reset output and a system clock reset output. Table 1-4 shows on-chip hardware initialization by reset action.

The malfunction reset output circuit such as watchdog timer reset, address trap reset and system clock reset is not initialized when power is turned on. The $\overline{\text{RESET}}$ pin can output level "L" at the maximum $24/f_c[s]$ ($1.5 \mu s$ at 16.0 MHz) when power is turned on.

Table 1-4. Initializing Internal Status by Reset Action

On-chip hardware	Initial value	On-chip hardware	Initial value
Program counter (PC)	(FFFE _H)	Prescaler and Divider of timing generator	0
Stack pointer (SP)	not initialized		
General-purpose registers (W, A, B, C, D, E, H, L, IX, IY)	not initialized		
Jump status flag (JF)	not initialized	Watchdog timer	Enable
Zero flag (ZF)	not initialized	Output latches of I/O ports	Refer to I/O port circuitry
Carry flag (CF)	not initialized		
Half carry flag (HF)	not initialized		
Sign flag (SF)	not initialized		
Overflow flag (VF)	not initialized		
Interrupt master enable flag (IMF)	0	Control registers	Refer to each of control register
Interrupt individual enable flags (EF)	0		
Interrupt latches (IL)	0		
		RAM	not initialized

1.6.1 External Reset Input

The $\overline{\text{RESET}}$ pin contains a Schmitt trigger (hysteresis) with an internal pull-up resistor.

When the $\overline{\text{RESET}}$ pin is held at "L" level for at least 3 machine cycles ($12/f_c [s]$) with the power supply voltage within the operating voltage range and oscillation stable, a reset is applied and the internal state is initialized.

When the $\overline{\text{RESET}}$ pin input goes high, the reset operation is released and the program execution starts at the vector address stored at addresses FFFE to FFFF_H.

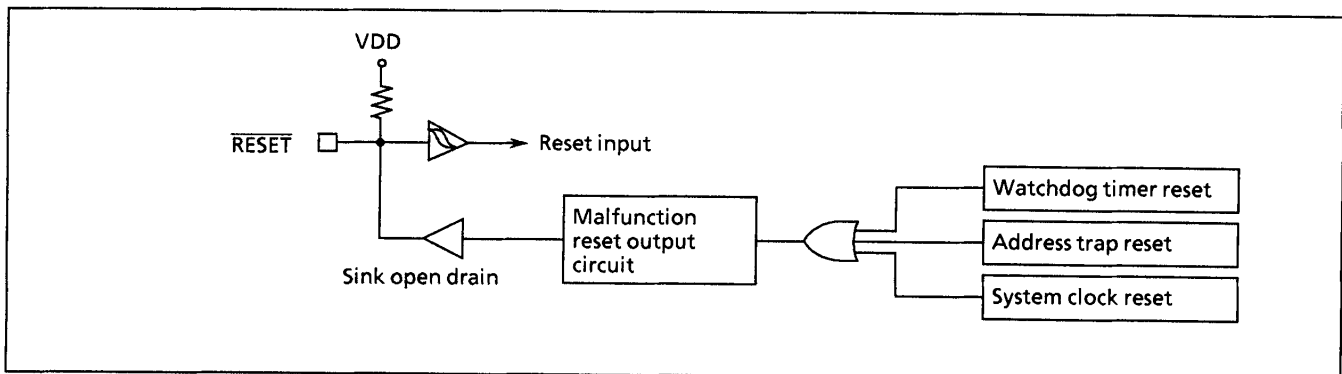


Figure 1-23. Reset Circuit

1.6.2 Address-Trap-Reset

If the CPU should start looping for some cause such as noise and an attempt be made to fetch an instruction from the on-chip RAM (when $WDTCR1 \langle ATAS \rangle$ is set to "1") or the SFR area, address-trap-reset will be generated. Then, the \overline{RESET} pin output will go low. The reset time is about $8/f_c$ to $24/f_c$ [s] (0.5 to 1.5 μ s at 16.0 MHz).

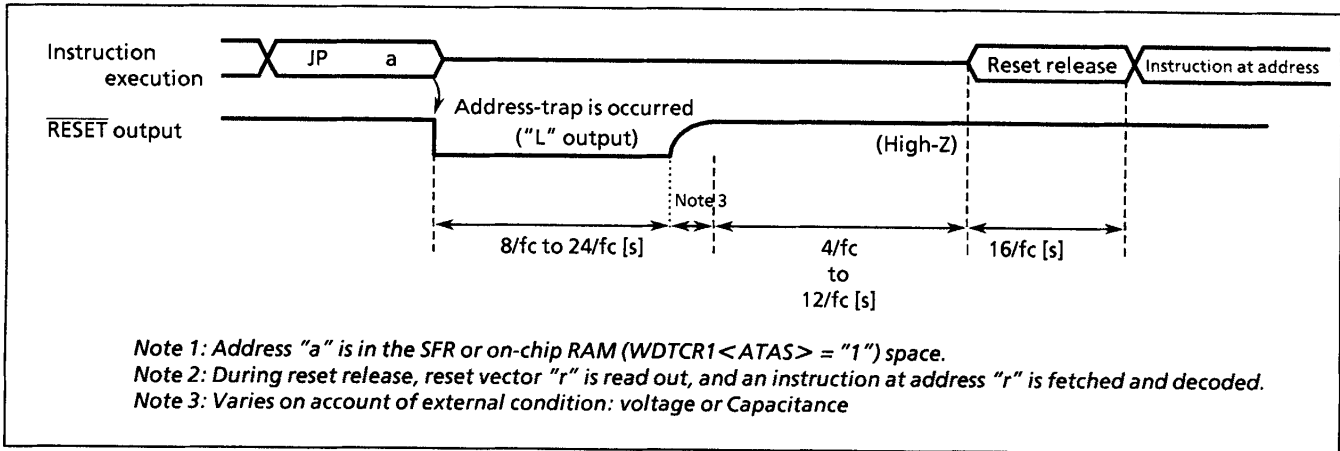


Figure 1-24. Address-Trap-Reset

Note: The operating mode under address trapped is alternative of reset or interrupt. The address trap area is alternative.

1.6.3 Watchdog Timer Reset

Refer to Section "2.4 Watchdog Timer".

1.6.4 System-Clock-Reset

Clearing both XEN and XTEN (bits 7 and 6 in SYSCR2) to "0", clearing XEN to "0" when $SYSCK = "0"$, or clearing XTEN to "0" when $SYSCK = "1"$ stops system clock, and causes the microcomputer to deadlock. This can be prevented by automatically generating a reset signal whenever $XEN = XTEN = "0"$, $XEN = SYSCK = "0"$, or $XTEN = "0"/SYSCK = "1"$ is detected to continue the oscillation. The, the \overline{RESET} pin output goes low from high-impedance. The reset time is about $8/f_c$ to $24/f_c$ [s] (0.5 to 1.5 μ s at 16.0 MHz).

2. On-Chip Peripherals Functions

2.1 Special Function Register (SFR)

The TMP86C420/820 adopt the memory mapped I/O system, and all peripheral control and data transfers are performed through the special function register (SFR). The SFR is mapped on address 0000H to 003FH, DBR is mapped on address 0F80H to 0FFFH.

Figure 2-1 (a) to 2-1 (b) indicate the special function register (SFR) and data buffer register (DBR) for TMP86C420/820.

Address	Read	Write	Address	Read	Write
0000H	reserved		0020H	ADCDR1 (AD converter register 1)	-
01	P1DR (P1 Port output latch)		21	ADCDR2 (AD converter register 2)	-
02	P2DR (P2 Port output latch)		22	reserved	-
03	P3DR (P3 Port output latch)		23	reserved	-
04	P3OUTCR (P3 Port output circuit control)		24	reserved	-
05	P5DR (P5 Port output latch)		25	reserved	-
06	P6DR (P6 Port output latch)		26	reserved	-
07	P7DR (P7 Port output latch)		27	reserved	-
08	P1PRD (P1 Terminal input)	-	28	LCDCR (LCD Control register)	
09	P2PRD (P2 Terminal input)	-	29	P1LCR (P1 segment output control)	
0A	P3PRD (P3 Terminal input)	-	2A	P5LCR (P5 segment output control)	
0B	P5PRD (P5 Terminal input)	-	2B	P7LCR (P7 segment output control)	
0C	P6CR (P6 Port input/output control)		2C	PWREG3 (Timer register 3)	
0D	P7PRD (P7 Terminal input)	-	2D	PWREG4 (Timer register 4)	
0E	ADCCR1 (AD control register 1)		2E	reserved	
0F	ADCCR2 (AD control register 2)		2F	reserved	
10	TREG1A _L		30	reserved	
11	TREG1A _M (Timer register 1 A)		31	reserved	
12	TREG1A _H		32	reserved	
13	TREG1B (Timer register 1B)		33	reserved	
14	TC1CR1 (Timer Counter 1 control 1)		34	-	WDTCR1 (watch dog timer control)
15	TC1CR2 (Timer Counter 1 control 2)		35	-	WDTCR2 (watch dog timer control)
16	TC1SR (TC1 Status)	-	36	TBTCT (TBT/TG/DVO control)	
17	reserved		37	EINTCR (External interrupt control)	
18	TC3CR (Timer Counter 3 control)		38	SYSCR1 (System control 1)	
19	TC4CR (Timer Counter 4 control)		39	SYSCR2 (System control 2)	
1A	reserved		3A	EIR _L (Interrupt enable register)	
1B	reserved		3B	EIR _H (Interrupt enable register)	
1C	TTREG3 (Timer register 3)		3C	IL _L (Interrupt latch)	
1D	TTREG4 (Timer register 4)		3D	IL _H (Interrupt latch)	
1E	reserved		3E	INTSEL (Interrupt source selector)	
1F	reserved		3F	PSW (Program Status word)	

Note 1: Do not access the reserved addresses in the program.
Note 2: -; Cannot be accessed.
Note 3: Read-modify-write instructions (bit manipulation instructions such as SET and CLR and arithmetic instructions such as AND and OR) cannot be used for the write-only registers and interrupt latches.

Figure 2-1 (a). The Special Function Register (SFR) for TMP86C420/820

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Address	Read	Write
0F80 _H		SEG1				SEG0			0F90 _H		SIOBR0 (SIO Buffer 0)
81		SEG3				SEG2			91		SIOBR1 (SIO Buffer 1)
82		SEG5				SEG4			92		SIOBR2 (SIO Buffer 2)
83		SEG7				SEG6			93		SIOBR3 (SIO Buffer 3)
84		SEG9				SEG8			94		SIOBR4 (SIO Buffer 4)
85		SEG11				SEG10			95		SIOBR5 (SIO Buffer 5)
86		SEG13				SEG12			96		SIOBR6 (SIO Buffer 6)
87		SEG15				SEG14			97		SIOBR7 (SIO Buffer 7)
88		SEG17				SEG16			98	-	SIOCR1 (SIO Control register 1)
89		SEG19				SEG18			99	SIOSR (SIO Status register)	SIOCR2 (SIO Control register 2)
8A		SEG21				SEG20			9A	-	STOPCR (Key On Wake Up Control register)
8B		SEG23				SEG22			9B		reserved
8C		SEG25				SEG24			9C		reserved
8D		SEG27				SEG26			9D		reserved
8E		SEG29				SEG18			9E		reserved
8F		SEG31				SEG30			0FFF		reserved

Note 1: Do not access the reserved addresses in the program.
Note 2: - ; Cannot be accessed.
Note 3: Read-modify-write instructions (bit manipulation instructions such as SET and CLR and arithmetic instructions such as AND and OR) cannot be used for the write-only registers and interrupt latches.

Figure 2-1 (b). The Data Buffer Register (DBR) for TMP86C420/820

2.2 I/O Ports

The TMP86C420/820 have 6 parallel input/output ports (39 pins) as follows.

	Primary Function	Secondary Functions
Port P1	8-bit I/O port	External interrupt input, serial interface input/output, and segment output.
Port P2	3-bit I/O port	Low-frequency resonator connections, external interrupt input, STOP mode release signal input.
Port P3	4-bit I/O port	Timer/counter input/output and divider output.
Port P5	8-bit I/O port	Segment output.
Port P6	8-bit I/O port	Analog input, external interrupt input, timer/counter input and STOP mode release signal input.
Port P7	8-bit I/O port	Segment output.

Each output port contains a latch, which holds the output data. All input ports do not have latches, so the external input data should be externally held until the input data is read from outside or reading should be performed several timer before processing. Figure 2-2 shows input/output timing examples. External data is read from an I/O port in the S1 state of the read cycle during execution of the read instruction. This timing cannot be recognized from outside, so that transient input such as chattering must be processed by the program.

Output data changes in the S2 state of the write cycle during execution of the instruction which writes to an I/O port.

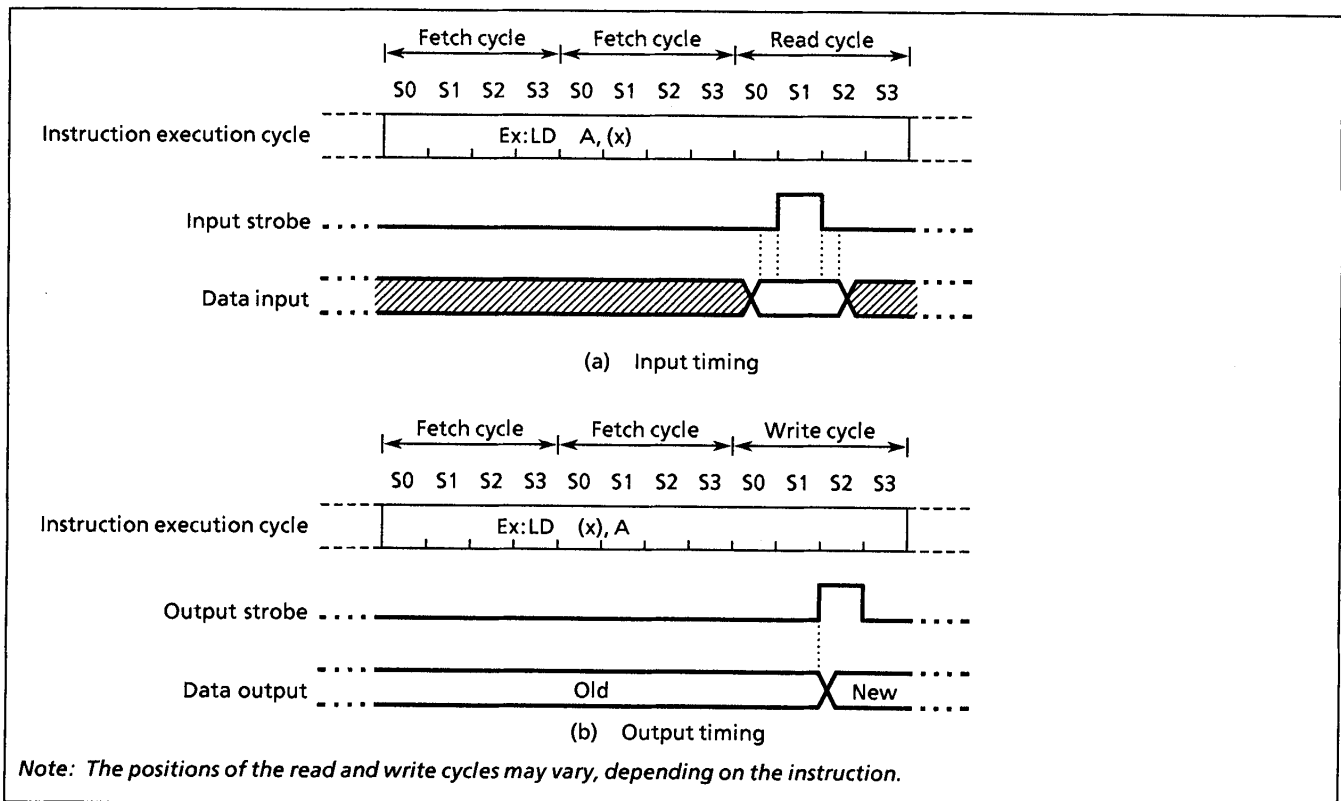


Figure 2-2. Input / Output Timing (Example)

2.2.1 Port P1 (P17 to P10)

Port P1 is an 8-bit input/output port which is also used as an external interrupt input, serial interface input/output, and segment output of LCD. When used as a segment pins of LCD, the respective bit of P1LCR should be set to "1".

When used as an input port or a secondary function (except for segment) pins, the respective output latch (P1DR) should be set to "1" and its corresponding P1LCR bit should be set to "0". When used as an output port, the respective P1LCR bit should be set to "0". During reset, the output latch is initialized to "1".

P1 port output latch (P1DR) and P1 port terminal input (P1PRD) are located on their respective address.

When read the output latch data, the P1DR register should be read and when read the terminal input data, the P1PRD register should be read.

If the terminal input data which is configured as LCD segment output is read, unstable data is read.

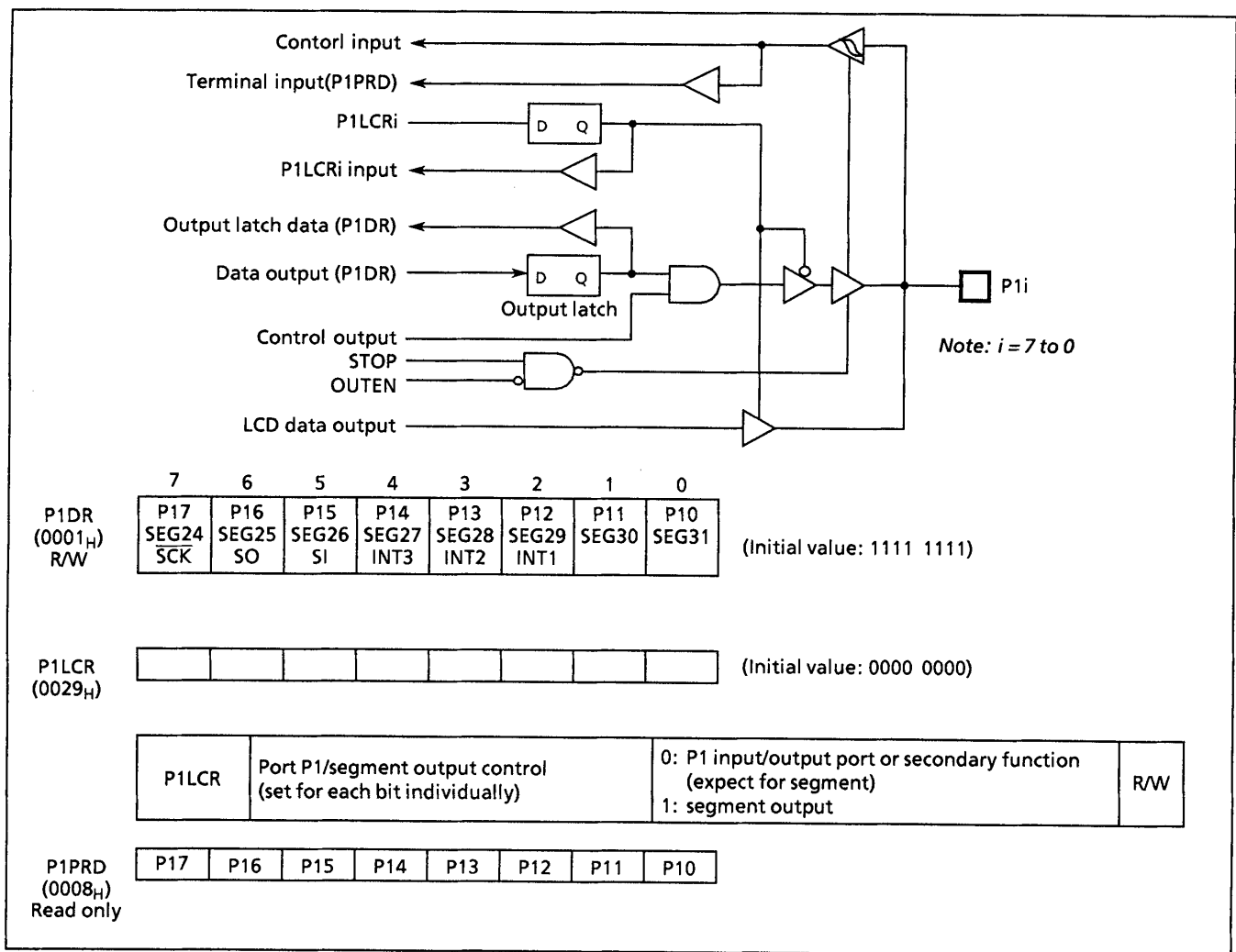


Figure 2-3. Port 1

2.2.2 Port P2 (P22 to P20)

Port P2 is a 3-bit input/output port.

It is also used as an external interrupt, a STOP mode release signal input, and low-frequency crystal oscillator connection pins. When used as an input port or a secondary function pins, respective output latch (P2DR) should be set to "1".

During reset, the output latch is initialized to "1".

A low-frequency crystal oscillator (32.768 kHz) is connected to pins P21 (XTIN) and P22 (XTOUT) in the dual-clock mode. In the single-clock mode, pins P21 and P22 can be used as normal input/output ports.

It is recommended that pin P20 should be used as an external interrupt input, a STOP mode release signal input, or an input port. If it is used as an output port, the interrupt latch is set on the falling edge of the output pulse.

P2 port output latch (P2DR) and P2 port terminal input (P2PRD) are located on their respective address.

When read the output latch data, the P2DR register should be read and when read the terminal input data, the P2PRD register should be read. If a read instruction is executed for port P2, read data of bits 7 to 3 are unstable.

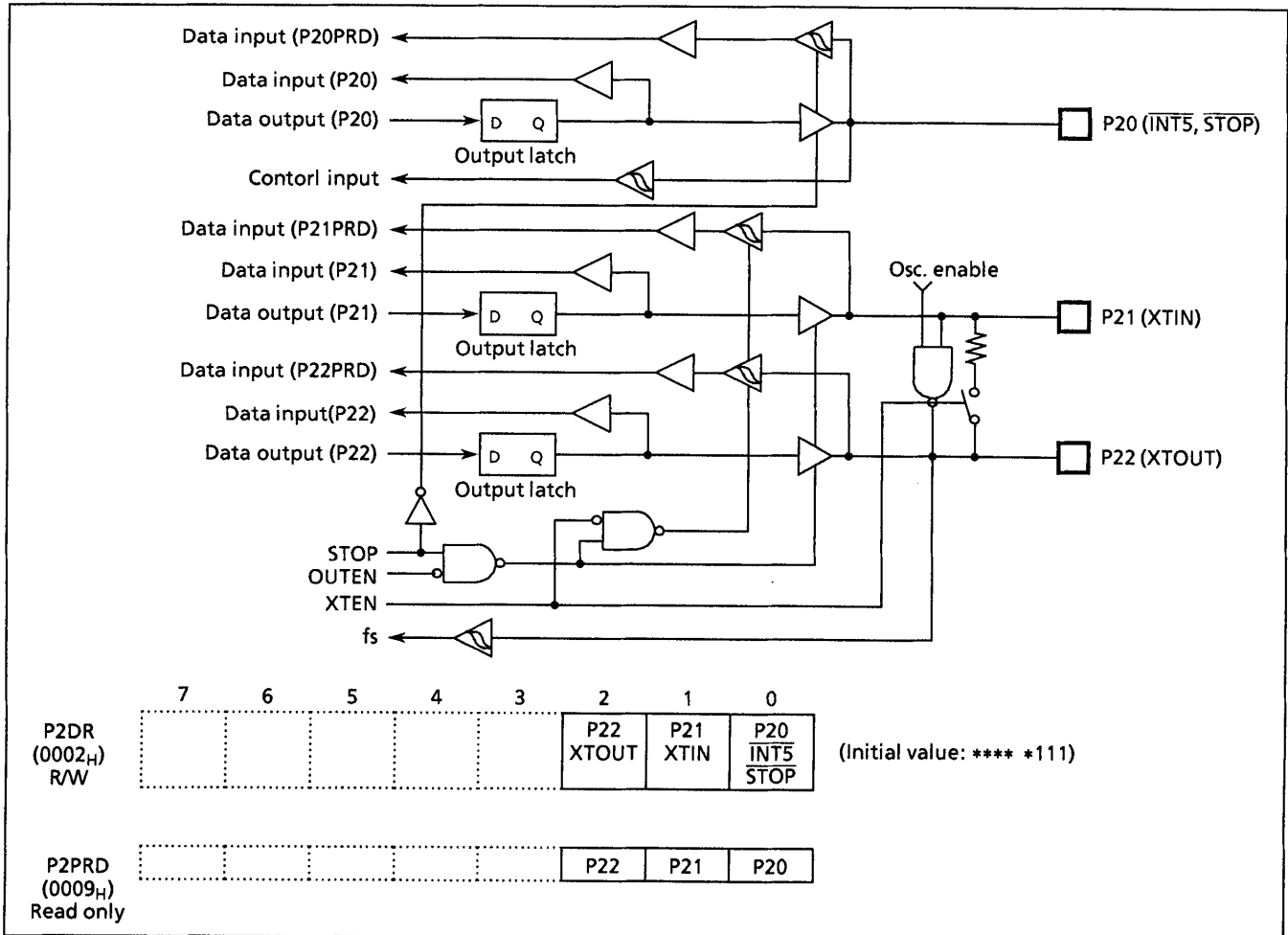


Figure 2-4. Port 2

Note: Port P20 is used as \overline{STOP} pin. Therefore, when stop mode is started, \overline{OUTEN} does not affect to P20, and P20 becomes High-Z mode.

2.2.3 Port P3 (P33 to P30)

Port P3 is a 4-bit input/output port.

It is also used as a timer/counter input/output, divider output.

When used as a timer/counter output or divider output, respective output latch (P3DR) should be set to "1".

It can be selected whether output circuit of P3 port is C-MOS output or a sink open drain individually, by setting P3OUTCR. When a corresponding bit of P3OUTCR is "0", the output circuit is selected to a sink open drain and when a corresponding bit of P3OUTCR is "1", the output circuit is selected to a C-MOS output. When used as an input port or timer/counter input, respective output control (P3OUTCR) should be set to "0" after P3DR is set to "1". During reset, the P3DR is initialized to "1", and the P3OUTCR is initialized to "0".

P3 port output latch (P3DR) and P3 port terminal input (P3PRD) are located on their respective address.

When read the output latch data, the P3DR should be read and when read the terminal input data, the P3PRD register should be read. If a read instruction is executed for port P3, read data of bits 7 to 4 are unstable.

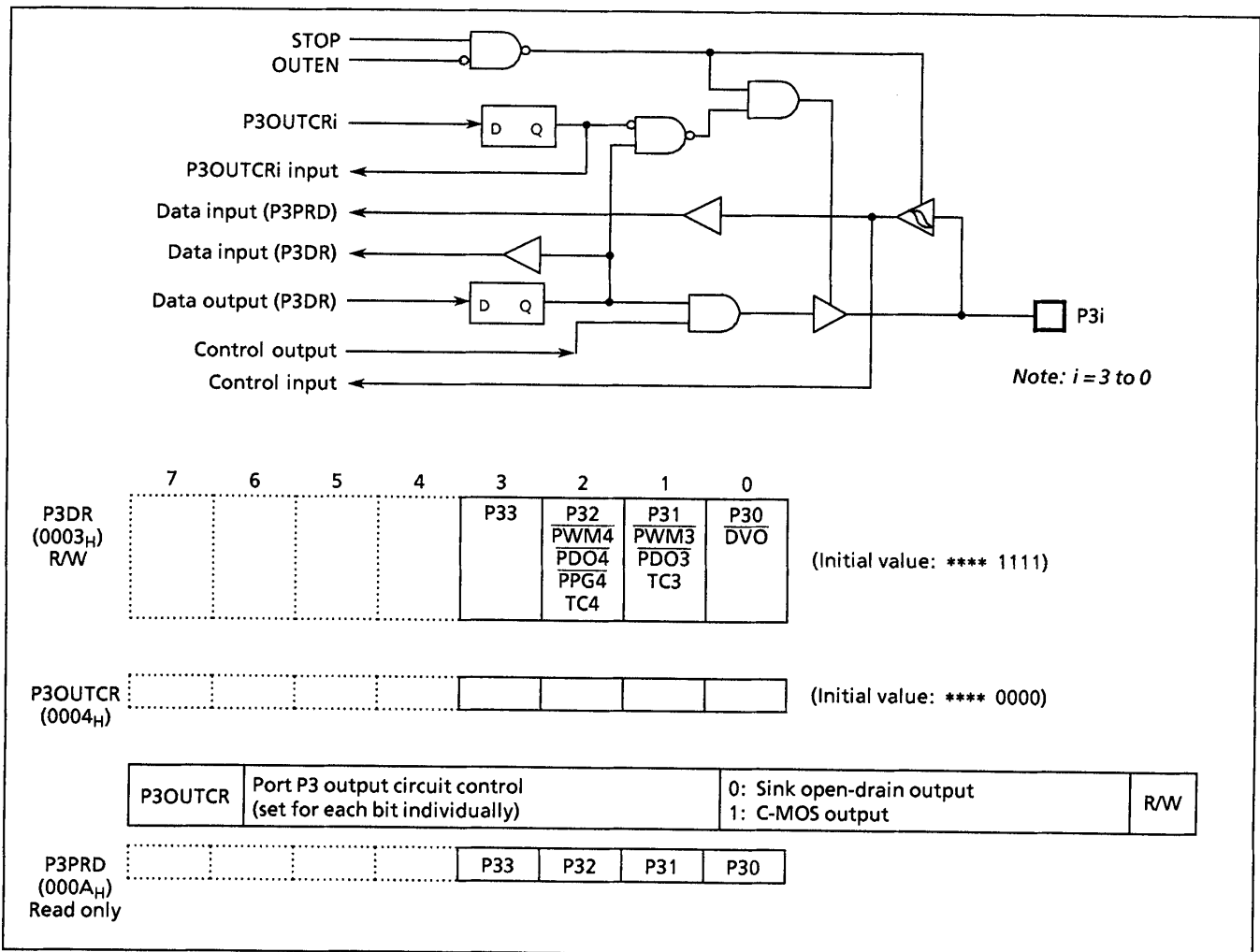


Figure 2-5. Port 3

2.2.4 Port P5 (P57 to P50)

Port P5 is an 8-bit input/output port which is also used as a segment pins of LCD.

When used as input port, the respective output latch (P5DR) should be set to "1".

During reset, the output latch is initialized to "1".

When used as a segment pins of LCD, the respective bit of P5LCR should be set to "1". When used as an output port, the respective P5LCR bit should be set to "0".

P5 port output latch (P5DR) and P5 port terminal input (P5PRD) are located on their respective address.

When read the output latch data, the P5DR register should be read and when read the terminal input data, the P5PRD register should be read. If the terminal input data which is configured as LCD segment output is read, unstable data is read.

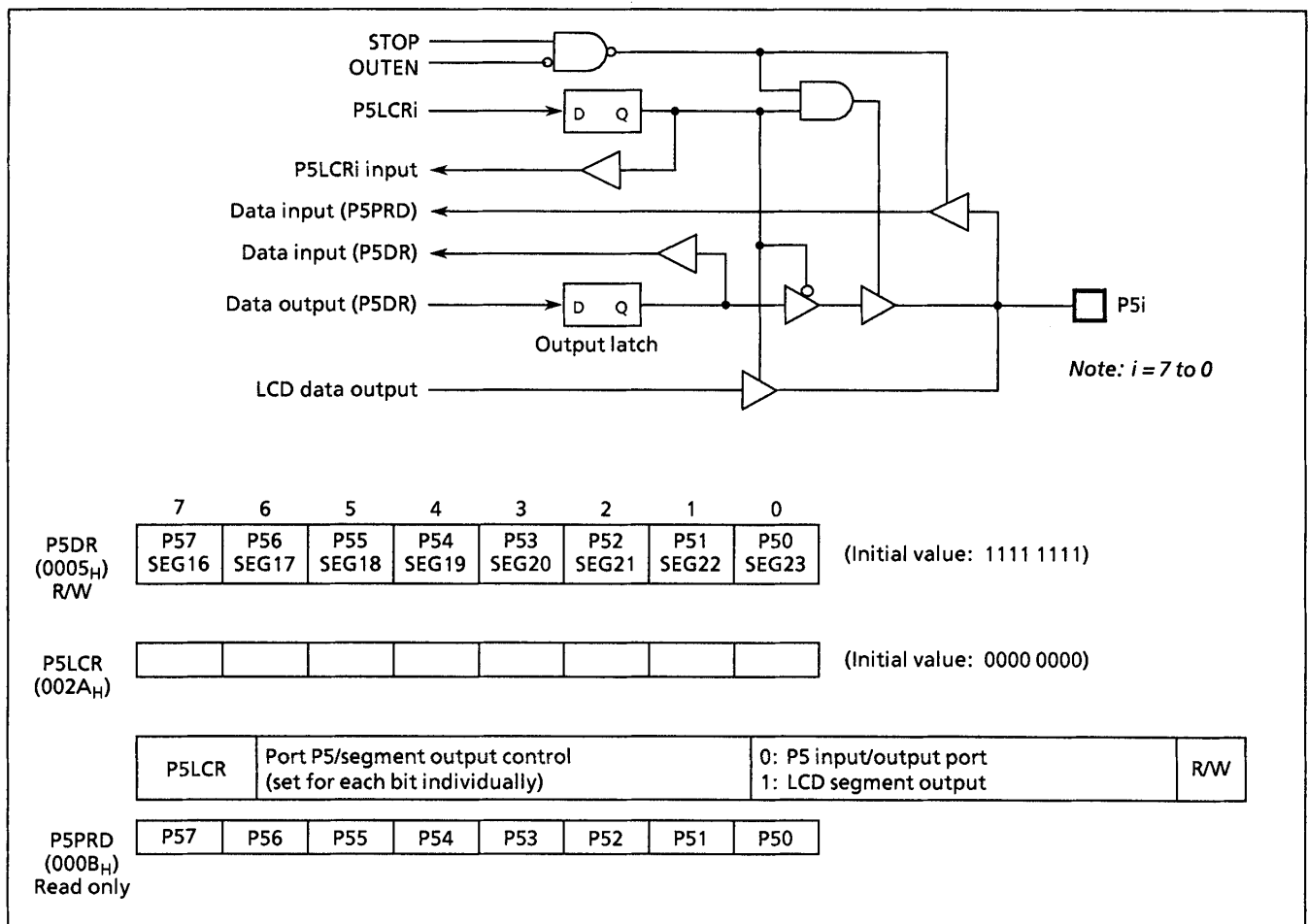


Figure 2-6. Port 5

2.2.5 Port P6 (P67 to P60)

Port P6 is an 8-bit input/output port which can be configured as an input or an output in one-bit unit. Port P6 is also used as an analog input, Key-on Wake-up input, timer/counter input and external interrupt input. Input/output mode is specified by the P6 control register (P6CR), the P6 output latch (P6DR), and AINDS (bit 4 in ADCCR1). During reset, P6CR and P6DR are initialized to "0" and AINDS is set to "1". At the same time, the input data of pins P67 to P60 are fixed to "0". To use port P6 as an input port, external interrupt input, timer/counter input or key on wake up input, set data of P6DR to "1" and P6CR to "0". To use it as an output port, set data of P6CR to "1". To use it as an analog input, set data of P6DR to "0" and P6CR to "0", and start the AD. It is the penetration electric current measures by the analog voltage.

Pins not used for analog input can be used as I/O ports. During AD conversion, output instructions should not be executed to keep a precision. In addition, a variable signal should not be input to a port adjacent to the analog input during AD conversion.

When the AD converter is in use (P6DR=0), bits mentioned above are read as "0" by executing input instructions.

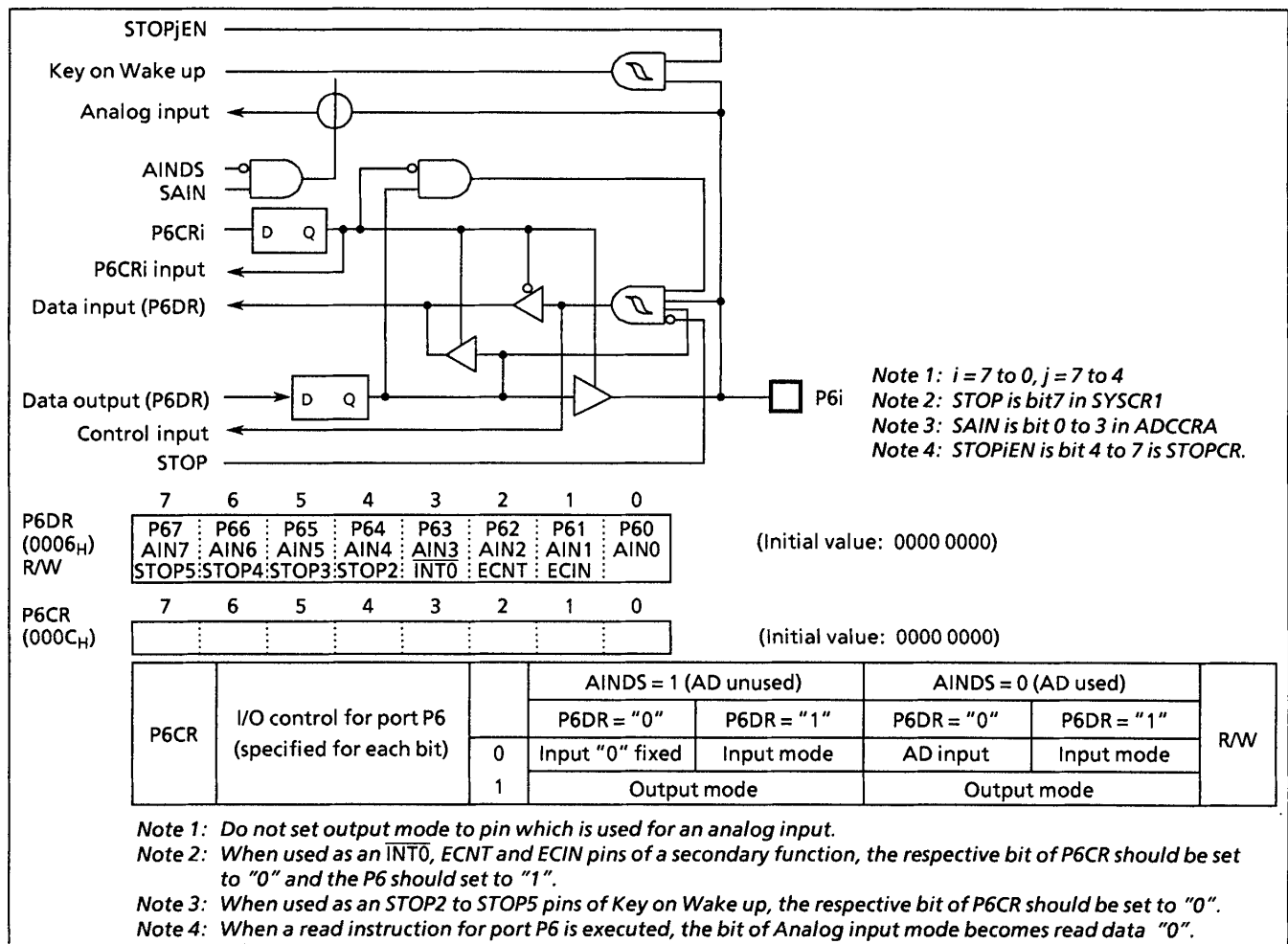


Figure 2-7. Port 6 and P6CR

Note: Although P6DR is a read / writer register, because it is also used as an input mode control function, read-modify-write instructions such as bit manipulate instructions cannot be used. Read-modify-write instruction writes the all data of 8-bit after data is read and modified. Because a bit setting Input mode read data of terminal, the output latch is changed by these instruction. So P6 port can not input data.

2.2.6 Port P7 (P77 to P70)

Port P7 is an 8-bit input/output port which is also used as a segment pins of LCD.

When used as input port, the respective output latch (P7DR) should be set to "1".

During reset, the output latch is initialized to "1".

When used as a segment pins of LCD, the respective bit of P7LCR should be set to "1" and its corresponding P7LCR bit should be set to "0". When used as an output port, the respective P7LCR bit should be set to "0".

P7 port output latch (P7DR) and P7 port terminal input (P7PRD) are located on their respective address.

When read the output latch data, the P7DR register should be read and when read the terminal input data, the P7PRD register should be read. If the terminal input data which is configured as LCD segment output is read, unstable data is read.

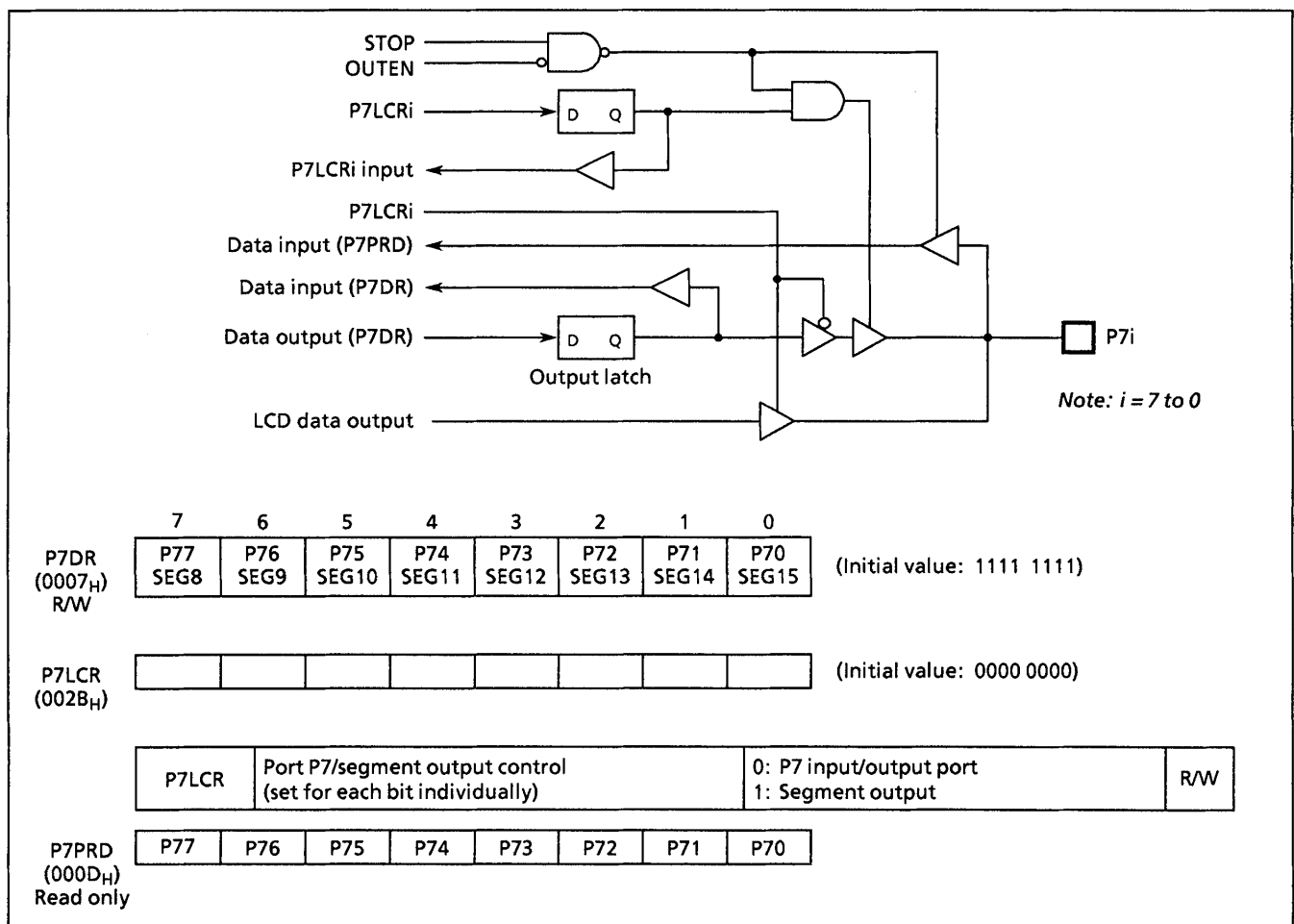


Figure 2-8. Port 7

2.3 Time Base timer (TBT)

The time base timer generates time base for key scanning, dynamic displaying, etc. It also provides a time base timer interrupt (INTTBT).

An INTTBT is generated on the first falling edge of source clock (the divider output of the timing generator) after the time base timer has been enabled. The divider is not cleared by the program ; therefore, only the first interrupt may be generated ahead of the set interrupt period (Figure 2-9.(b)).

The interrupt frequency (TBTCK) must be selected with the time base timer disabled (the interrupt frequency must not be changed with the disable from the enable state). Both frequency selection and enabling can be performed simultaneously.

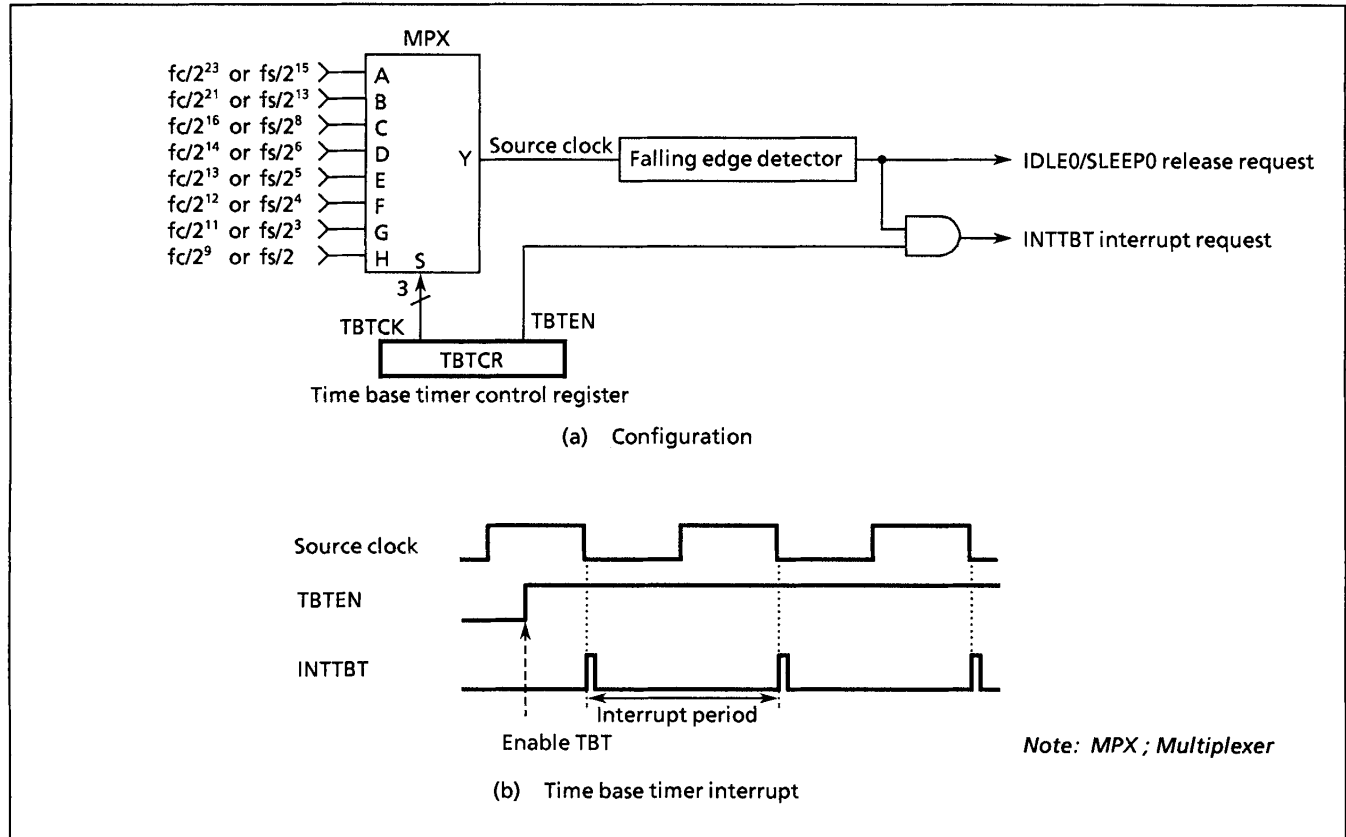


Figure 2-9. Time Base Timer

Example: Sets the time base timer frequency to $fc/2^{16}$ [Hz] and enables an INTTBT interrupt.

```
LD (TBTCK), 00000010B ; TBTEN ← 1
LD (TBTEN), 00001010B ; TBTCK ← 010
SET (EIRL), 6
```

TBTCR (0036 _H)	7	6	5	4	3	2	1	0	
	(DVOEN)	(DV0CK)	(DV7CK)	TBTEN	TBTKK				(Initial value: 0000 0000)

TBTEN	Time base timer enable / disable	0: Disable 1: Enable				
TBTKK	Time base timer interrupt frequency select [Hz]	NORMAL1/2, IDLE1/2 mode		SLOW, SLEEP mode	R/W	
		DV7CK = 0	DV7CK = 1			
		000	$fc/2^{23}$	$fs/2^{15}$		$fs/2^{15}$
		001	$fc/2^{21}$	$fs/2^{13}$		$fs/2^{13}$
		010	$fc/2^{16}$	$fs/2^8$		-
		011	$fc/2^{14}$	$fs/2^5$		-
		100	$fc/2^{13}$	$fs/2^5$		-
		101	$fc/2^{12}$	$fs/2^4$		-
110	$fc/2^{11}$	$fs/2^3$	-			
111	$fc/2^9$	$fs/2$	-			

*Note; fc; High-frequency clock [Hz], fs; Low-frequency clock [Hz], *; Don't care*

Figure 2-10. Time Base Timer Control Register

Table 2-1. Time Base Timer Interrupt Frequency (Example; $fc = 16.0$ MHz, $fs = 32.768$ kHz)

TBTKK	Time base timer interrupt frequency [Hz]			SLOW, SLEEP mode
	NORMAL1/2, IDLE1/2 mode			
	DV7CK = 0	DV7CK = 1		
000	1.91	1	1	
001	7.63	4	4	
010	244.14	128	-	
011	976.56	512	-	
100	1953.13	1024	-	
101	3906.25	2048	-	
110	7812.5	4096	-	
111	31205	16384	-	

2.4 Watchdog Timer (WDT)

The watchdog timer is a fail-safe system to rapidly detect the CPU malfunctions such as endless looping caused by noise or the like, or deadlock and resume the CPU to the normal state.

The watchdog timer signal for detecting malfunction can be selected either a reset output or a non-maskable interrupt request. However, selection is possible only once after reset. At first the reset output is selected.

When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals.

Note: Care must be given in system design so as to protect the watchdog timer from disturbing noise. Otherwise the watchdog timer may not fully exhibit its functionality.

2.4.1 Watchdog Timer Configuration

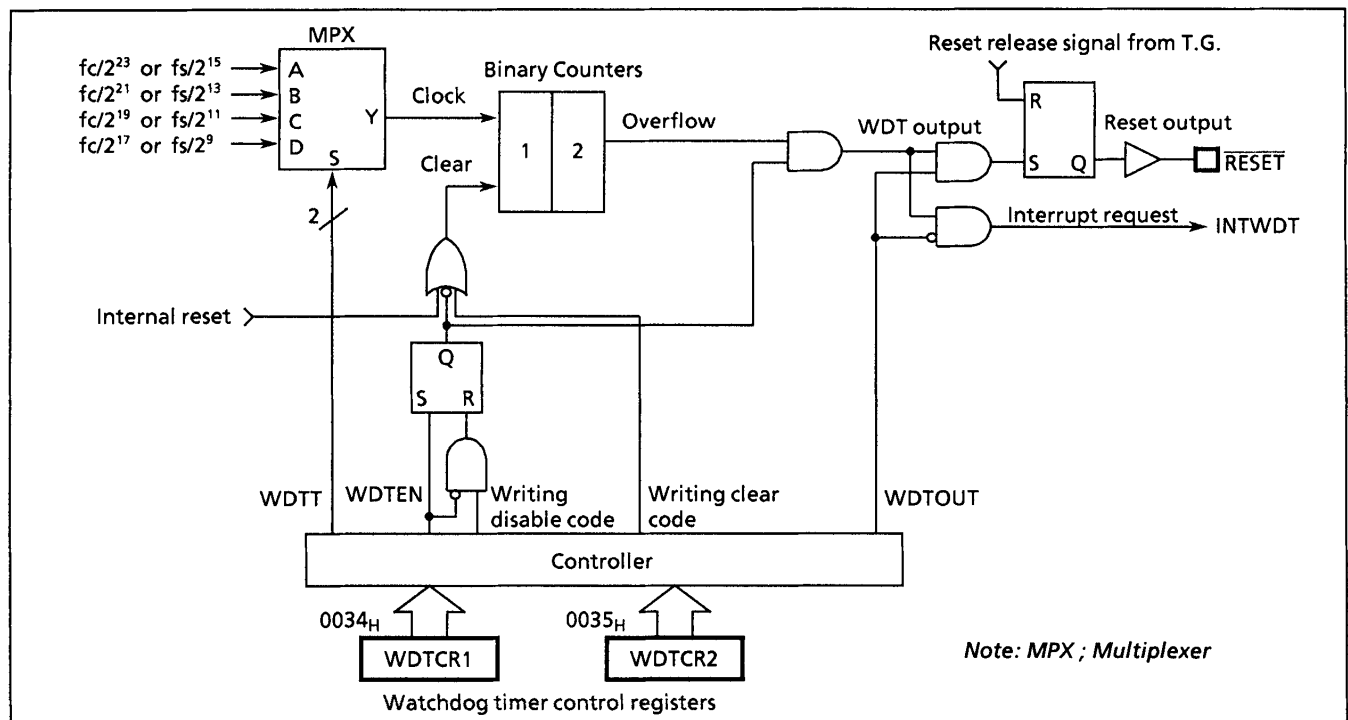


Figure 2-11. Watchdog Timer Configuration

2.4.2 Watchdog Timer Control

Figure 2-12 shows the watchdog timer control registers (WDTCR1, WDTCR2). The watchdog timer is automatically enabled after reset.

(1) Malfunction detection methods using the watchdog timer

The CPU malfunction is detected as follows.

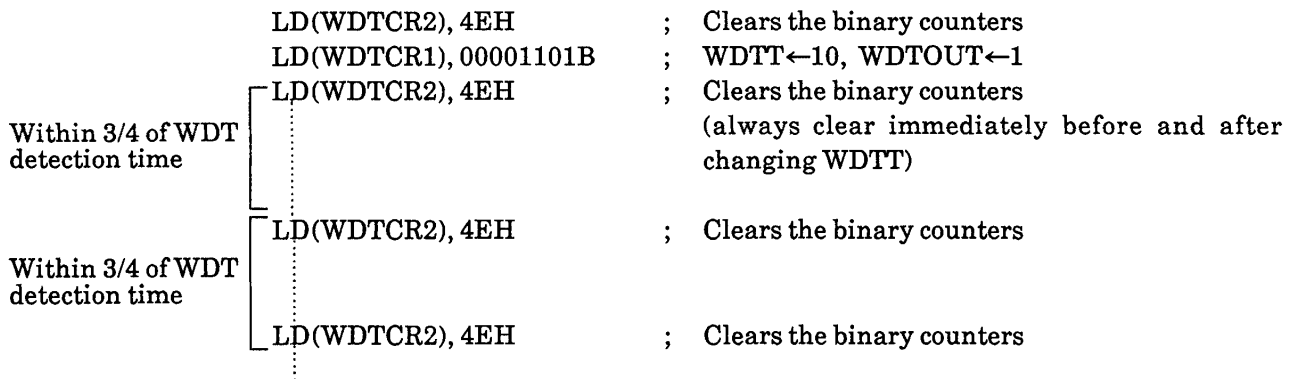
- ① Setting the detection time, selecting output, and clearing the binary counter.
- ② Repeatedly clearing the binary counter within the setting detection time

If the CPU malfunctions such as endless looping or deadlock occur for any cause, the watchdog timer output will become active at the rising of an overflow from the binary counters unless the binary counters are cleared. At this time, when WDTOUT=1 a reset is generated, which drivers the RESET pin low to reset the internal hardware and the external circuit. When WDTOUT=0, a watchdog timer interrupt (INTWDT) is generated.

The watchdog timer temporarily stops counting in STOP mode including warm-up or IDLE mode, and automatically restarts (continues counting) when the STOP/IDLE mode is released.

Note: The watchdog timer consists of an internal divider and a two-stage binary counter. When clear code 4EH is written, only the binary counter is cleared, not the internal divider. Depending on the timing at which clear code 4EH is written on the WDTCR2 register, the overflow time of the binary counter may be at minimum 3/4 of the time set in WDTCR1 <WDTT>. Thus, write the clear code using a shorter cycle than 3/4 of the time set in WDTCR1 <WDTT>.

Example: Sets the watchdog timer detection time to $2^{21}/fc$ [s] and resets the CPU malfunction.



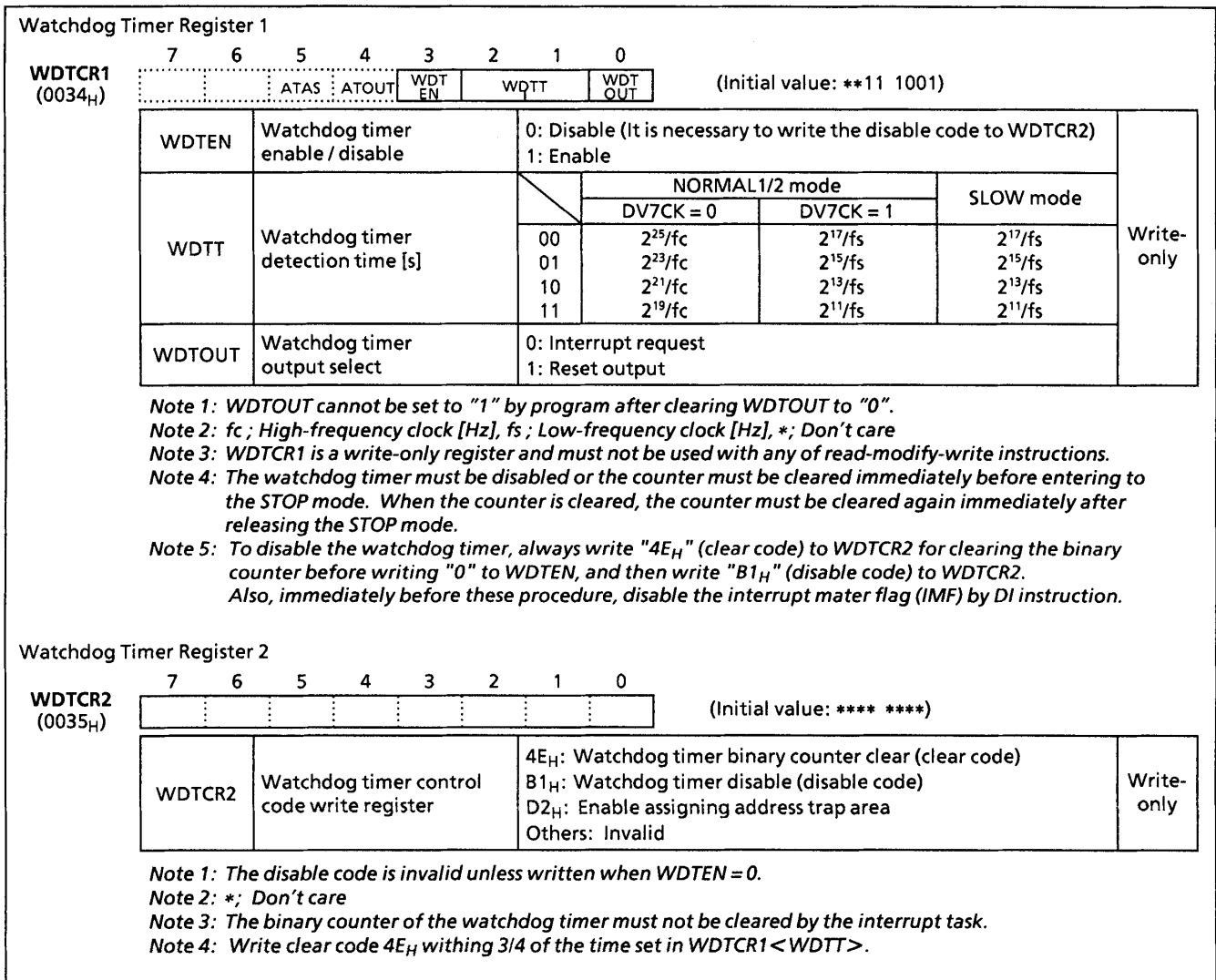


Figure 2-12. Watchdog Timer Control Registers

(2) Watchdog timer enable

The watchdog timer is enabled by setting WDTEN (bit 3 in WDTCR1) to "1". WDTEN is initialized to "1" during reset, so the watchdog timer operates immediately after reset is released.

(3) Watchdog timer disable

To disable the watchdog time, write "4EH" (clear code) to WDTCR2 for clearing the binary counter before writing "0" to WDTEN, and then write "B1H" (disable code) to WDTCR2. The watchdog timer is not disabled if this procedure is reversed and the disable code is written to WDTCR2 before WDTEN is cleared to "0". Also, immediately before these procedure, disable the interrupt master flag (IMF) by DI instruction. During disabling the watchdog timer, the binary counters are cleared to "0".

Example: Disables watchdog timer

```
DI          ; IMF ← 0
LD  (WDTCR2), 04EH ; Clear the binary counter
LDW (WDTCR1), 0B101H ; WDTEN ← 0, WDTCR2 ← Disable code
```

Table 2-2. Watchdog Timer Detection Time (Example: $f_c = 16.0$ MHz, $f_s = 32.768$ kHz)

WDTT	Watchdog timer detection time [s]		
	NORMAL1/2 mode		SLOW mode
	DV7CK = 0	DV7CK = 1	
00	2.097	4	4
01	254.288 m	1	1
10	131.072 m	250 m	250 m
11	32.768 m	62.5 m	62.5 m

2.4.3 Watchdog Timer Interrupt (INTWDT)

This is a pseudo non-maskable interrupt which can be accepted regardless of the contents of the EIR. If a watchdog timer interrupt or a software interrupt is already accepted, however, the new watchdog timer interrupt waits until the previous interrupt processing is completed (the end of the [RETN] instruction execution).

The stack pointer (SP) should be initialized before using the watchdog timer output as an interrupt source with WDTOUT.

Example: Watchdog timer interrupt setting up

```
LD  SP, 023FH ; Sets the stack pointer
LD  (WDTCR1), 00001000B ; WDTOUT ← 0
```


2.4.4 Watchdog Timer Reset

If the watchdog timer output becomes active, a reset is generated, which drives the $\overline{\text{RESET}}$ pin (sink open drain input/output with pull-up) low to reset the internal hardware. The reset output time is about $8/f_c$ to $24/f_c$ [s] (0.5 to $1.5 \mu\text{s}$ at $f_c = 16.0 \text{ MHz}$).

Note: The high-frequency clock oscillator also turns on when a watchdog timer reset is generated in SLOW mode. The reset output time is $8/f_c$ to $24/f_c$ [s]. Therefore, the reset time may include a certain amount of error if there is any fluctuation of the oscillation frequency at starting the high-frequency clock oscillation. Thus, the reset time must be considered an approximated value.

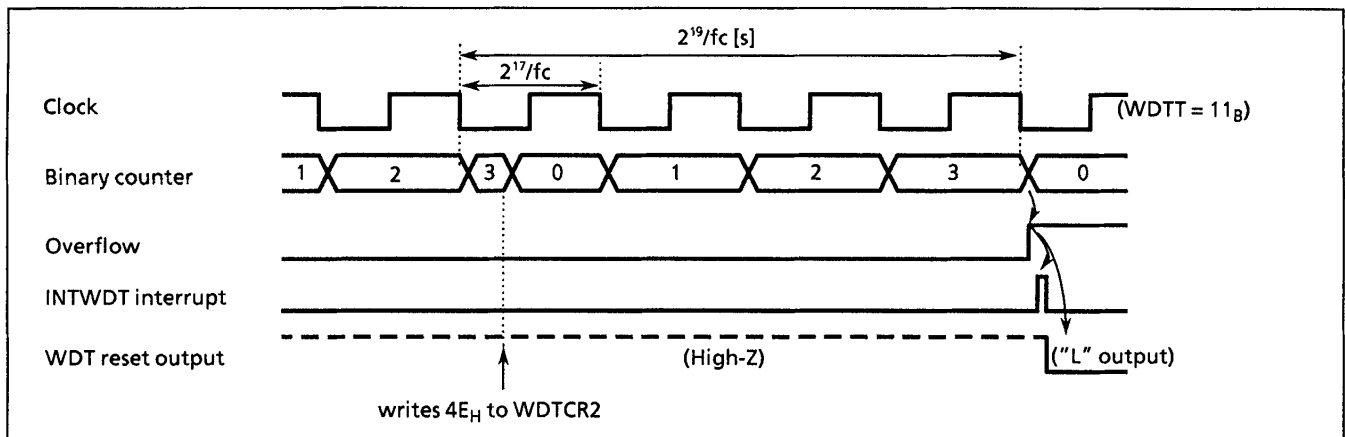


Figure 2-13. Watchdog Timer Interrupt / Reset

2.4.5 Address trap

The Watchdog Timer Control Register 1, 2 shares its addresses with the control registers in case of address trap. These control registers for address trap are shown on Figure 2-14.

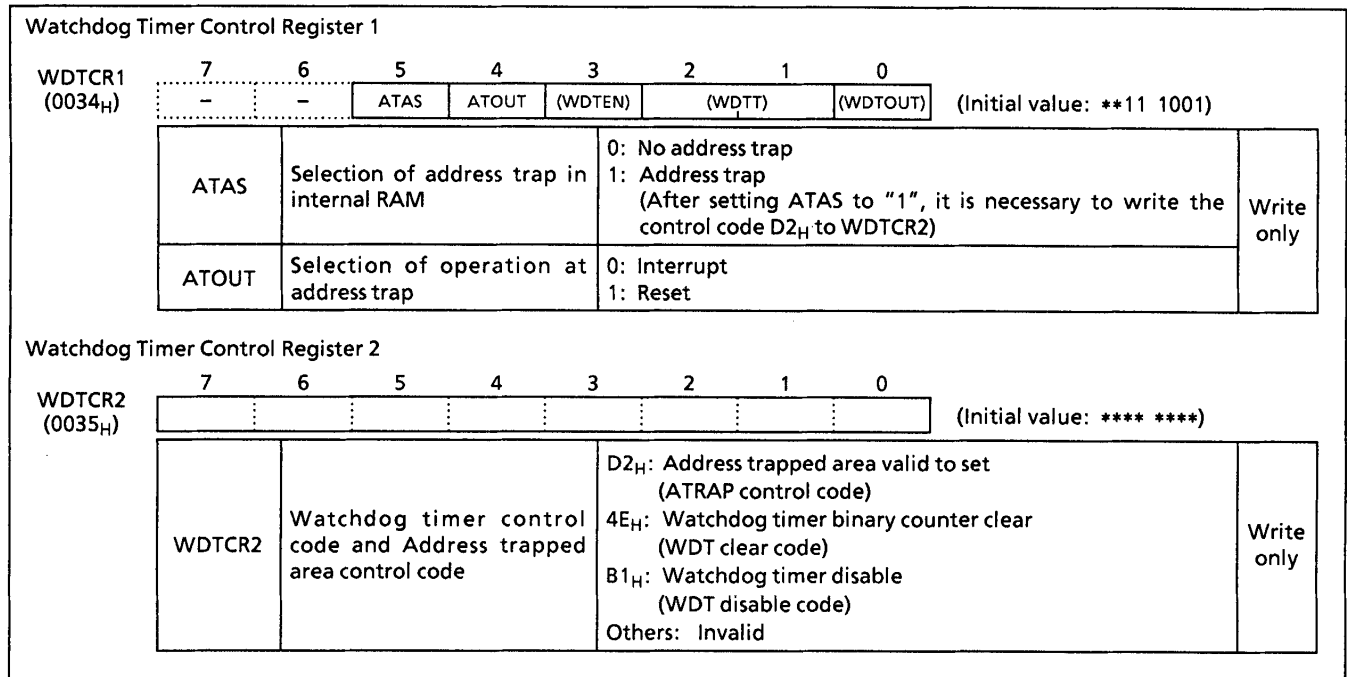


Figure 2-14. Watchdog Timer Control Registers

(1) Selection of address trap in internal RAM (ATAS)

Using WDTCR1<ATAS>, address trap or no address trap can be selected for the internal RAM area. To execute an instruction in the internal RAM area, set "0" in WDTCR1<ATAS>. Setting in WDTCR1<ATAS> becomes valid after control code D2_H is written in WDTCR2. Executing an instruction in the SFR/DBR area generates an address trap unconditionally regardless of the setting in WDTCR1<ATAS>.

(2) Selection of operation at address trap (ATOUT)

As the operation at address trap either interrupt generation or reset output can be selected by WDTCR1<ATOUT>.

2.5 Divider Output (DVO)

Approximately 50% duty pulse can be output using the divider output circuit, which is useful for piezoelectric buzzer drive. Divider output is from pin P30 (\overline{DVO}). The P30 output latch should be set to "1".

Note: Selection of divider output frequency must be made while divider output is disabled. Also, in other words, when changing the state of the divider output frequency from enabled to disable, do not change the setting of the divider output frequency.

TBTCR (0036 _H)	7	6	5	4	3	2	1	0	
	DVOEN	DVQCK	(DV7CK)	(TBTEN)	, (TBTK) ,				(Initial value: 0000 0000)
	DVOEN	Divider output enable/disable		0: Disable (It is necessary to write the disable code to WDTCSR2) 1: Enable				R/W	
	DVQCK	Divider output (\overline{DVO}) frequency selection [Hz]		NORMAL 1/2 mode			SLOW, SLEEP mode		
				DV7CK = 0		DV7CK = 1			
				00	$f_c/2^{13}$	$f_s/2^5$	$f_s/2^5$		$f_s/2^5$
				01	$f_c/2^{12}$	$f_s/2^4$	$f_s/2^4$	$f_s/2^4$	
	10	$f_c/2^{11}$	$f_s/2^3$	$f_s/2^3$	$f_s/2^3$				
	11	$f_c/2^{10}$	$f_s/2^2$	$f_s/2^2$	$f_s/2^2$				

*Note: f_c ; High-frequency clock [Hz], f_s ; Low-frequency clock [Hz], *; Don't care*

Figure 2-15. Divider Output Control Register

Example: 1.95 kHz pulse output (at $f_c = 16$ MHz)

```

SET (P3DR).0 ; P30 output latch ← 1
LD (TBTCR), 00000000B ; DVQCK ← "00"
LD (TBTCR), 10000000B ; DVOEN ← "1"
    
```

Table 2-3. Divider Output Frequency (Example: at $f_c = 16.0$ MHz, $f_s = 32.768$ kHz)

DVQCK	Divider output frequency [Hz]		
	NORMAL 1/2, IDLE 1/2 mode		SLOW, SLEEP mode
	DV7CK = 0	DV7CK = 1	
00	1.953 k	1.024 k	1.024 k
01	3.906 k	2.048 k	2.048 k
10	7.813 k	4.096 k	4.096 k
11	15.625 k	8.192 k	8.192 k

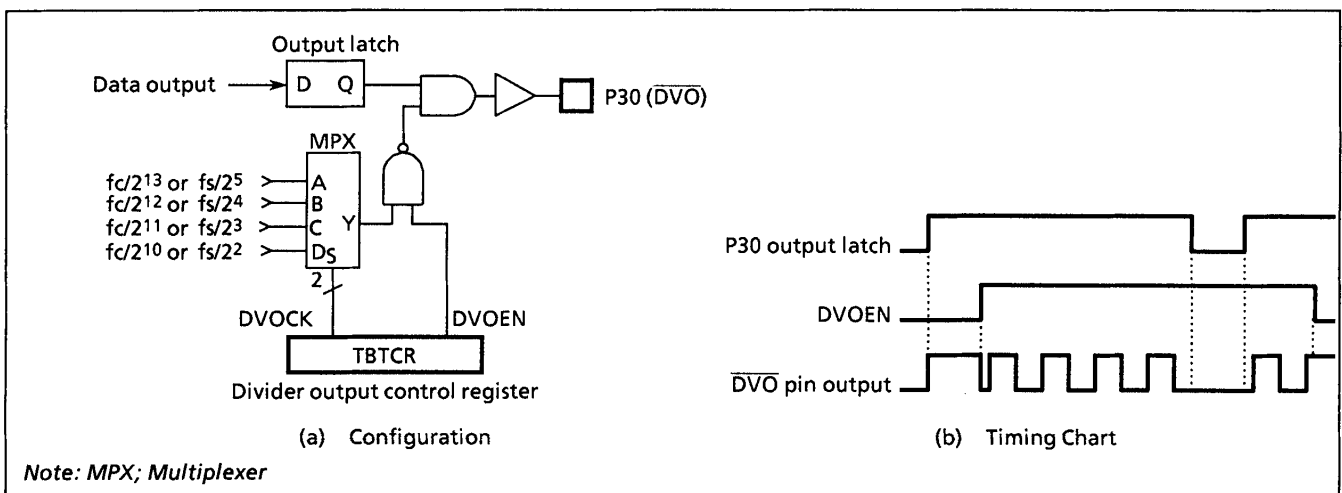


Figure 2-16. Divider Output

2.6 18-Bit Timer/Counter (TC1)

2.6.1 Configuration

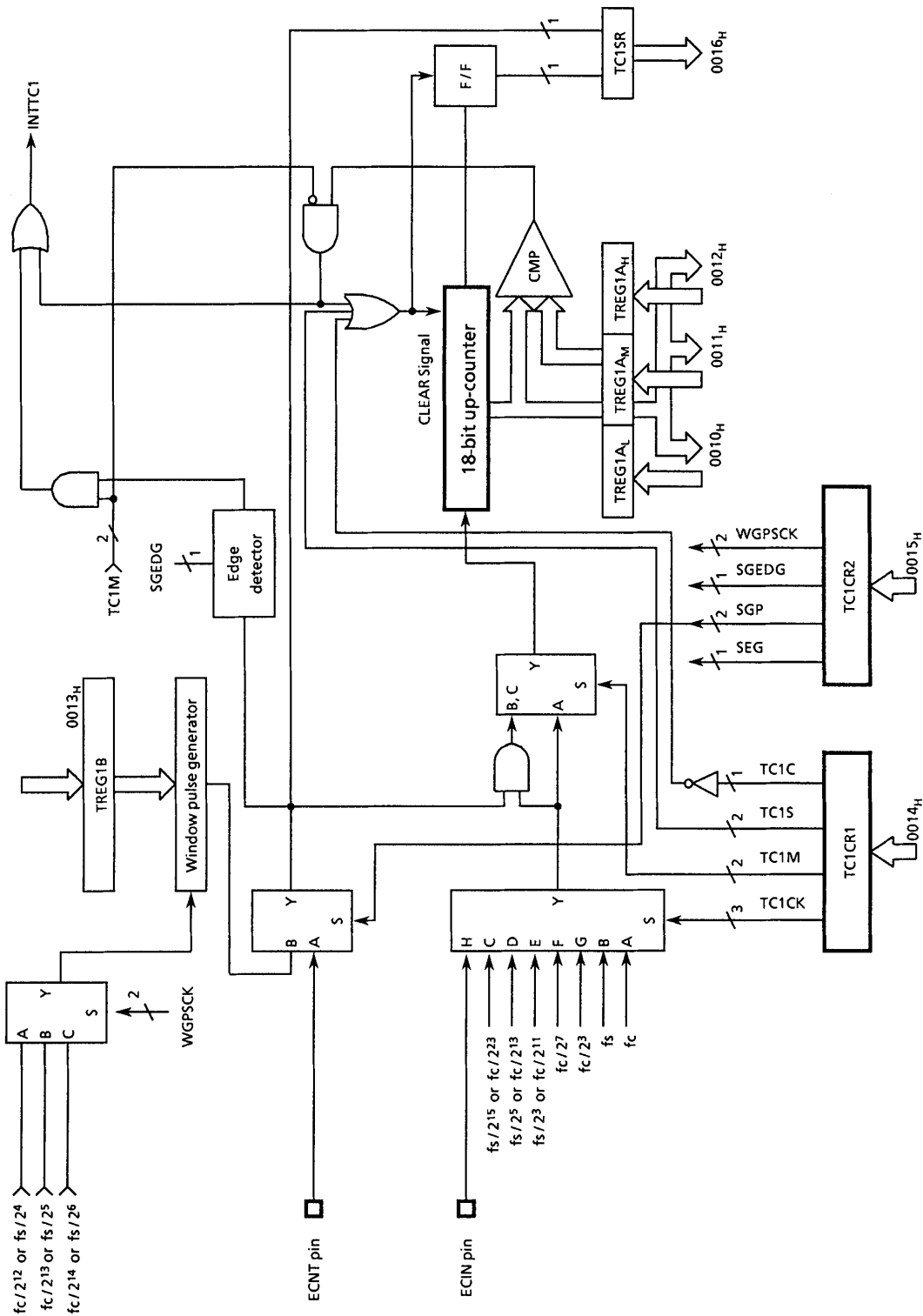


Figure 2-17. Timer/Counter 1

2.6.2 Control

The timer/counter 1 is controlled by a timer/counter 1 control registers (TC1CR1/TC1CR2), an 18-bit timer register (TREG1A), and an 8-bit internal window gate pulse setting register (TREG1B).

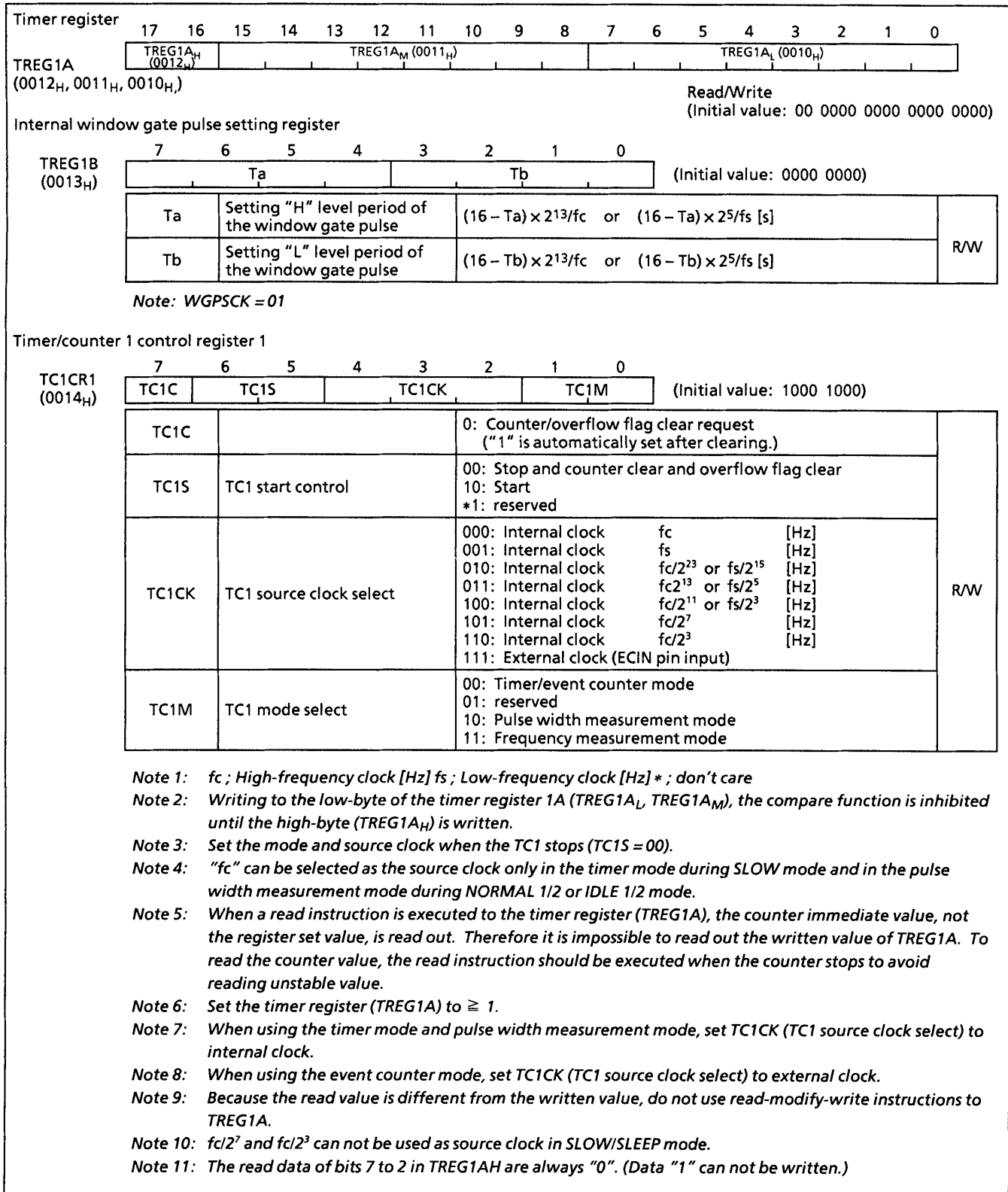


Figure 2-18. Timer Register/Window Gate Pulse Setting Register/Control Register of the TC1

Timer/counter 1 control register 2

	7	6	5	4	3	2	1	0	
TC1CR2 (0015 _H)	"0"	SGP	SGEDG	WGPSCK	"1"	"0"	(Initial value: 0000 00**)		

SGP	Window gate pulse select	00: ECNT input 01: Internal window gate pulse (TREG1B) 10: reserved 11: reserved	R/W
SGEDG	Window gate pulse interrupt edge select	0: Interrupts at the falling edge 1: Interrupts at the falling / rising edges	
WGPSCK	Window gate pulse source clock select	00: Select 2 ¹² / fc or 2 ⁴ / fs 01: Select 2 ¹³ / fc or 2 ⁵ / fs 10: Select 2 ¹⁴ / fc or 2 ⁶ / fs 11: reserved	

*Note 1: fc; High-frequency clock [Hz] fs; Low-frequency clock [Hz] *; Don't care*
Note 2: Set the mode, source clock, and edge (selection) when the TC1 stops (TC1S = 00).
Note 3: Be sure to write "1" to Bit 1 of TC1CR2, and "0" to Bit 0 and Bit 7 of TC1CR2.

TC1 Status register

	7	6	5	4	3	2	1	0	
TC1SR (0016 _H)	HECF	HEOVF	"0"	"0"	"0"	"0"	"0"	"0"	(Initial value: 0000 0000)

HECF	Operating Status monitor	0: Stop (during Tb) or disable 1: Under counting (during Ta)	Read only
HEOVF	Counter overflow monitor	0: No overflow 1: Overflow status	

Figure 2-19. Control Register of the TC1/Status Register

2.6.3 Function

TC1 has four operating modes. The timer mode of the TC1 is used at warm-up when switching from SLOW mode to NORMAL2 mode.

(1) Timer mode

In this mode, counting up is performed using the internal clock. The contents of TREG1A are compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared. Counting up resumes after the counter is cleared.

Table 2-4. Source Clock (internal clock) of Timer / Counter 1

Source clock				Resolution		Maximum time setting	
NORMAL1/2, IDLE1/2 mode		SLOW mode	SLEEP mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1						
fc / 2 ²³ [Hz]	fs / 2 ¹⁵ [Hz]	fs / 2 ¹⁵ [Hz]	fs / 2 ¹⁵ [Hz]	0.52 s	1 s	38.2 h	72.8 h
fc / 2 ¹³	fs / 2 ⁵	fs / 2 ⁵	fs / 2 ⁵	512 μs	0.98 ms	2.2 min	4.3 min
fc / 2 ¹¹	fs / 2 ³	fs / 2 ³	fs / 2 ³	128 μs	244 μs	0.5 min	1.07 min
fc / 2 ⁷	—	—	—	8 μs	—	2.1 s	—
fc / 2 ³	—	—	—	0.5 μs	—	131 ms	—
fc	—	fc (Note)	—	62.5 ns	—	16.4 ms	—
fs	—	—	—	—	30.5 μs	—	8 s

Note: When fc is selected for the source clock in SLOW mode, the lower bits 11 of TREG1A is invalid, and a match of the upper bits 7 makes interrupts.

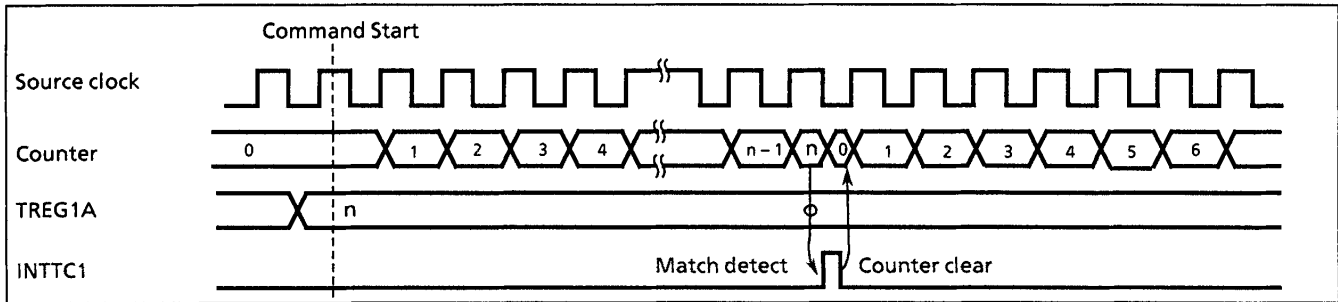


Figure 2-20. Timing Chart for Timer Mode

(2) Event Counter mode

It is a mode to count up at the falling edge of the ECIN pin input. The countents of TREG1A are compared with the contents of up-counter. If a match is found, an INTTC1 interrupt is generated, and the counter is cleared. Counting up resumes for ECIN pin input edge each after the counter is cleared. The maximum applied frequency is fc / 2⁴ [Hz] in NORMAL 1/2 or IDLE 1/2 mode and fs/2⁴ [Hz] in SLOW or SLEEP mode. Two or more machine cycles are required for both the "H" and "L" levels of the pulse width.

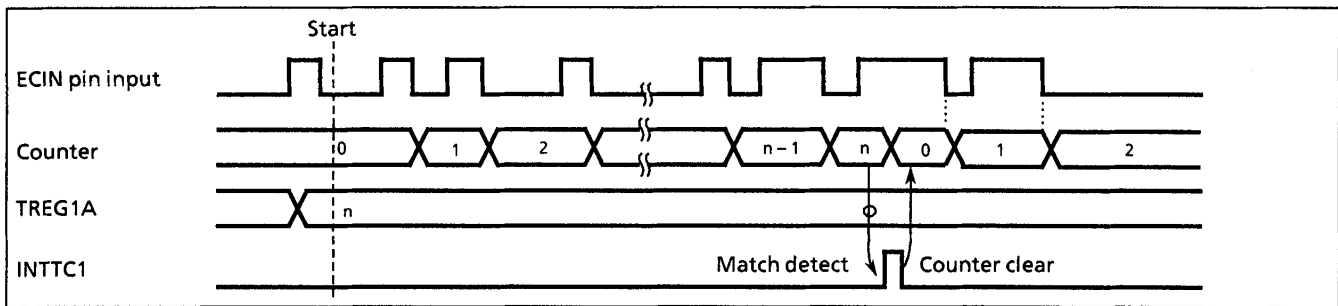


Figure 2-21. Event Counter Mode Timing Chart

(3) Pulse Width Measurement mode

In this mode, pulse widths are counted on the rising edge of logical AND-ed product between ECIN pin input (window pulse) and the internal clock. The internal clock is selected by TC1CK (bit 2, 3 and 4 in TC1CR1). An INTTC1 interrupt is generated at the falling edge of the window pulse or both rising and falling edges of the window pulse, that can be selected by SGEDG (bit 4 in TC1CR2). In the interrupt service program, read the contents of TREG1A while the count is stopped (ECIN pin is low), then clear the counter using TC1C (bit 7 in TC1CR1). When the counter is not cleared, counting up resumes by starting count-up. When TREG1A is counted up from 3FFFF_H to 00000_H, an overflow occurs. HEOVF (bit 6 in TC1SR) of the status register can monitor whether the overflows or not. HEOVF remains the old data until the counter is required to be cleared by TC1C.

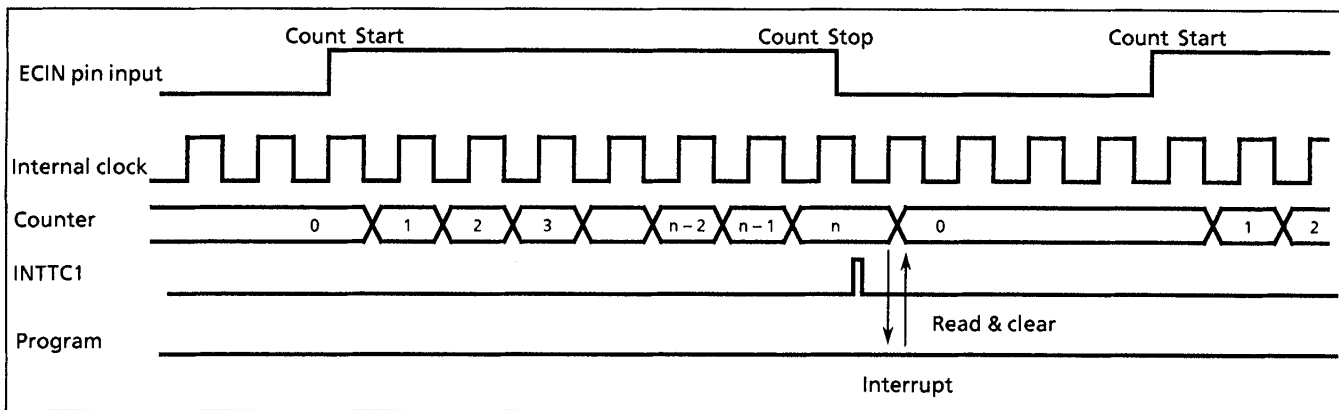


Figure 2-22. Pulse Width Measurement Mode Timing Chart

Note 1: INTTC1 interrupt occurs when ECIN input is "1" and TC1S of TC1CR1 is written to "00". According to the following step, when timer counter is stopped, INTTC1 interrupt latch should be cleared to "0".

```

TC1STOP:      ;
              DI                      ; Clear IMF
              CLR (EIRH). EF8         ; Clear EF8
              LD (TC1CR1), 00011010B ; Stop timer counter 1
              LD (ILH), 11111110B    ; Clear IL8
              SET (EIRH). EF8         ; SET EF8
              EI                      ; SET IMF
    
```

Note 2: When SGEDG (window gate pulse interrupt edge select) is set to both edges and ECIN pin input is "1" in the pulse width measurement mode, an INTTC1 interrupt is generated by setting TC1S (TC1 start control) to "10" (start).

Note 3: In the pulse width measurement mode, HECF (operating status monitor) cannot be used.

(4) Frequency Measurement mode

In this mode, the frequency of ECIN pin input pulse is measured. TC1CK is required to be set to the external clock. The edge of the input pulse is counted during “H” level of the window gate pulse selected by SGP (bit 5 and 6 in TC1CR2). Whether the input pulse is counted on the falling edge. An INTTC1 interrupt is generated on the falling edge or both the rising / falling edges of the window gate pulse, that can be selected by SGEDG (bit 4 in TC1CR2). To use ECNT terminal input as a window gate pulse, SGP (bit 5 and 6 in TC1CR2) should be set to “00”. In the interrupt service program, read the contents of TREG1A while the count is stopped (window gate pulse is low), then clear the counter using TC1C. When the counter is not cleared, counting up resumes by starting count-up. The window pulse status can be monitored by HECF of the status register. HEOVF of the status register can monitor whether the binary counter overflows or not. In the overflow flag status, a new data is not input until the counter clear requests.

- When the internal window gate pulse is selected, the window gate pulse is set as follows. The internal window gate pulse consists of “H” level period (Ta) that is counting time and “L” level period (Tb) that is counting stop time. Ta or Tb can be individually set by TREG1B. One cycle contains Ta + Tb.

Note 1: Because the internal window gate pulse is generated in synchronization with the internal divider, it may be delayed for a maximum of one cycle of the source clock (WGPSCK) immediately after start of the timer.

Note 2: Set the internal window gate pulse when the timer counter is not operating or during the Tb period. When Tb is overwritten during the Tb period, the update is valid from the next Tb period.

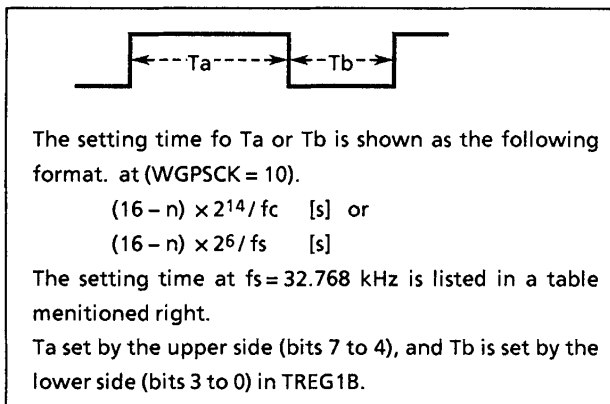


Figure 2-23. Window Gate Pulse Format

Table 2-5. Setting Ta and Tb (WGPSCK = 10, fs = 32.768 kHz)

Setting value	Setting time	Setting value	Setting time
0	31.25 ms	8	15.63 ms
1	29.30 ms	9	13.67 ms
2	27.34 ms	A	11.72 ms
3	25.39 ms	B	9.77 ms
4	23.44 ms	C	7.81 ms
5	21.48 ms	D	5.86 ms
6	19.53 ms	E	3.91 ms
7	17.58 ms	F	1.95 ms

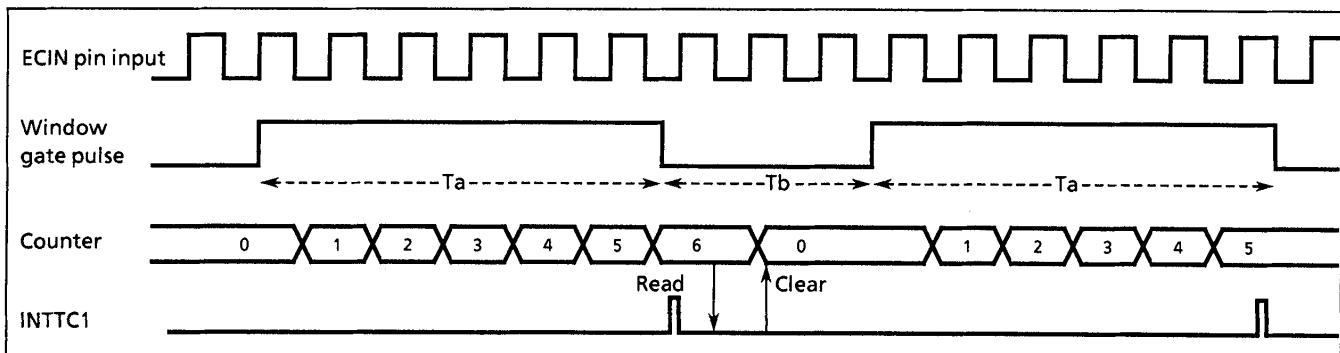


Figure 2-24. Timing Chart for the Frequency Measurement Mode (ECIN falling edge count, window gate pulse falling interrupt)

2.7 8-bit Timer/Counter (TC3, 4)

The TMP86C420/820 have four channels of 8-bit timer/counter (TC3, 4). These timer/counter are used as timer, event counter, PWM, PPG and PDO. These are also available as a 16-bit timer/counter by cascade connection.

2.7.1 Configuration

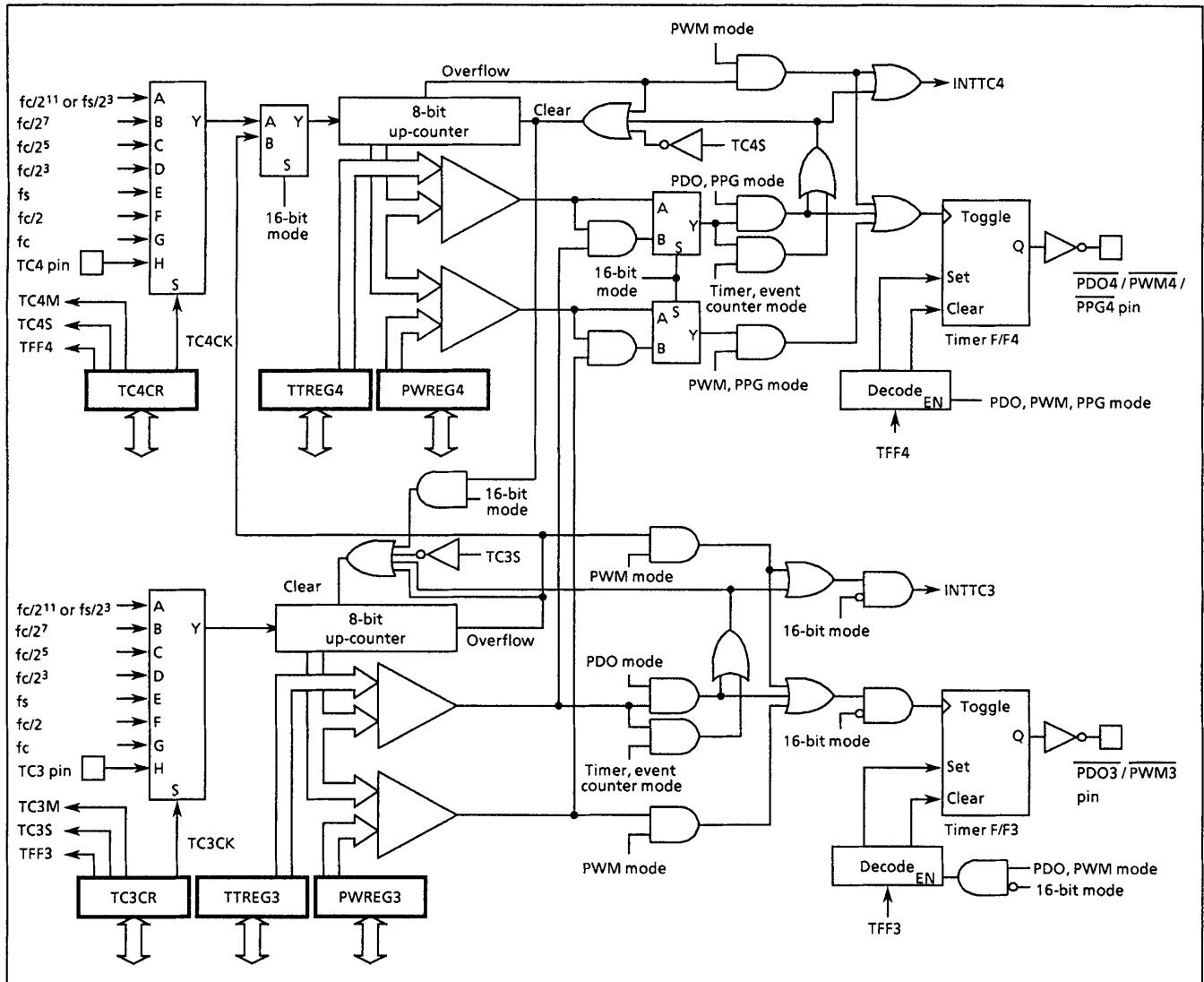


Figure 2-25. 8 bit Timer 3, 4

2.7.2 Control

The timer/counter 3 is controlled by a timer/counter 3 control register (TC3CR) and two 8-bit timer registers (TTREG3 and PWREG3).

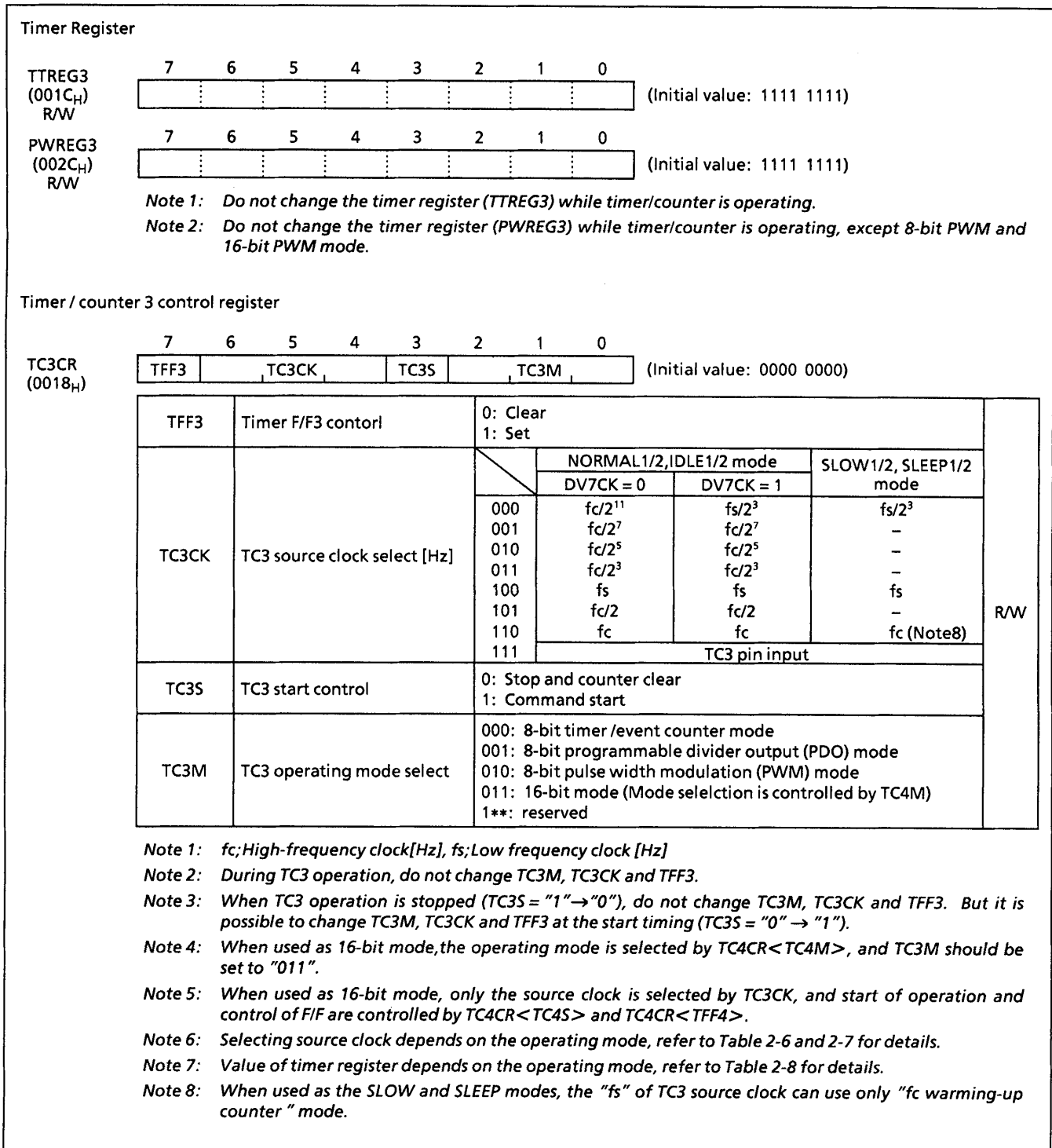


Figure 2-26. Timer 3 Register and Timer / Counter 3 Control Register

The timer/counter 4 is controlled by a timer/counter 4 control register (TC4CR) and two 8-bit timer registers (TTREG4 and PWREG4).

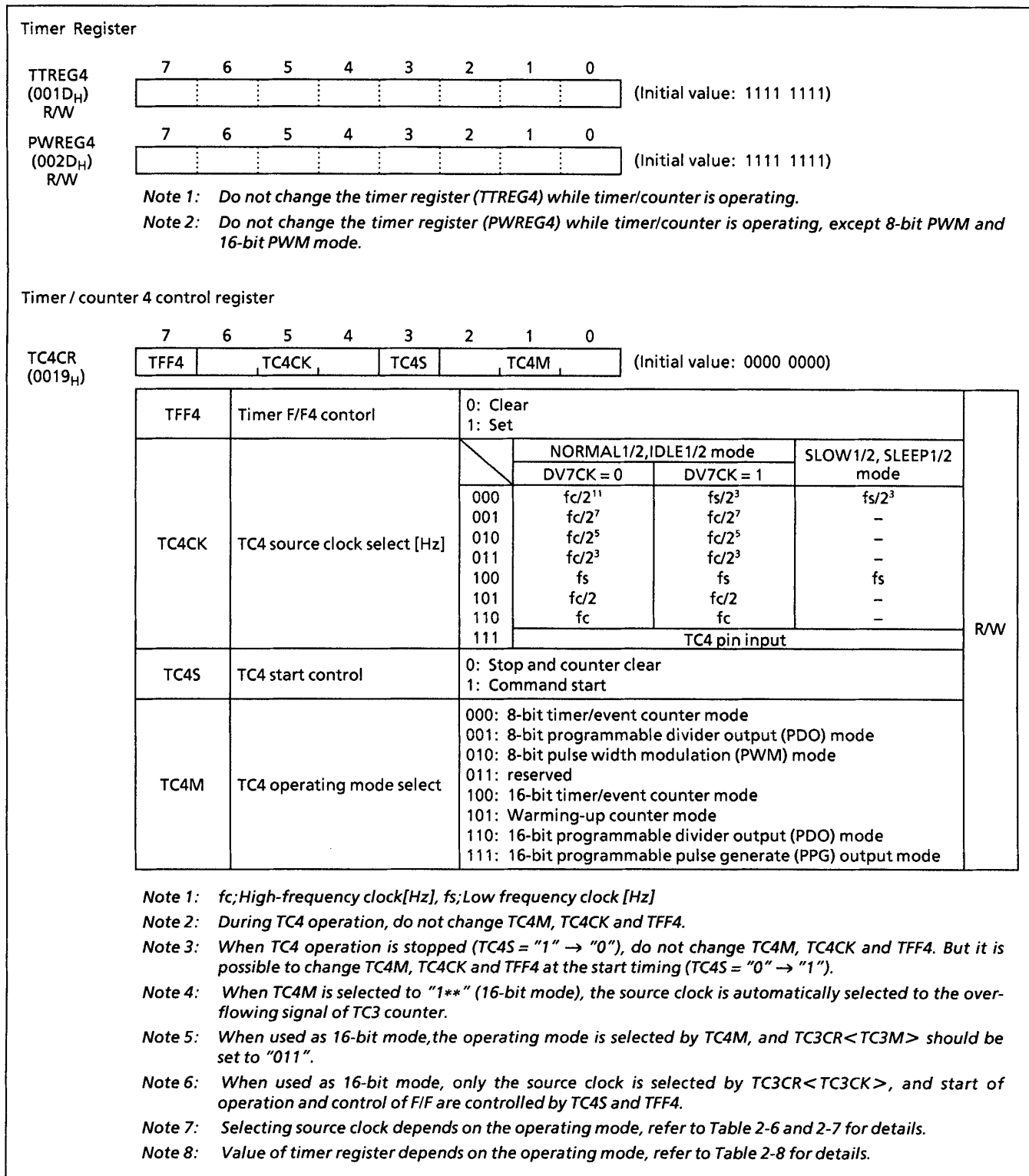


Figure 2-27. Timer 4 Register and Timer / Counter 4 Control Register

Table 2-6. Operating mode and available source clock (NORMAL1/2, IDLE1/2 mode)

Operating Mode	$fc/2^{11}$ or $fs/2^3$	$fc/2^7$	$fc/2^5$	$fc/2^3$	fs	$fc/2$	fc	TCi pin input
8-bit Timer	○	○	○	○	—	—	—	—
8-bit Event Counter	—	—	—	—	—	—	—	○
8-bit PDO	○	○	○	○	—	—	—	—
8-bit PWM	○	○	○	○	○	○	○	—
16-bit Timer	○	○	○	○	—	—	—	—
16-bit Event Counter	—	—	—	—	—	—	—	○
Warming-up Counter	—	—	—	—	○	—	—	—
16-bit PWM	○	○	○	○	○	○	○	○
16-bit PPG	○	○	○	○	—	—	—	○

Note 1: For 16-bit operation (16-bit Timer/Event Counter, Warming-up Counter, 16-bit PWM and 16-bit PPG), set its source clock on lower bits (TC3CK).

Note 2: $i = 3, 4$ (8-bit mode)
 $i = 3$ (16-bit mode)

Table 2-7. Operating mode and available source clock (Under SLOW1/2 mode, SLEEP1/2 mode)

Operating Mode	$fc/2^{11}$ or $fs/2^3$	$fc/2^7$	$fc/2^5$	$fc/2^3$	fs	$fc/2$	fc	TCi pin input
8-bit Timer	○	—	—	—	—	—	—	—
8-bit Event Counter	—	—	—	—	—	—	—	○
8-bit PDO	○	—	—	—	—	—	—	—
8-bit PWM	○	—	—	—	○	—	—	—
16-bit Timer	○	—	—	—	—	—	—	—
16-bit Event Counter	—	—	—	—	—	—	—	○
Warming-up Counter	—	—	—	—	—	—	○	—
16-bit PWM	○	—	—	—	○	—	—	○
16-bit PPG	○	—	—	—	—	—	—	○

Note 1: For 16-bit operation (16-bit Timer/Event Counter, Warming-up Counter, 16-bit PWM and 16-bit PPG), set its source clock on lower bits (TC3CK).

Note 2: $i = 3, 4$ (8-bit mode)
 $i = 3$ (16-bit mode)

Table 2-8. Restriction against the Rate for Comparing Registers

Operating Mode	Authorized Rate for Register
8-bit Timer/Event Counter	$1 \leq (TTREGn) \leq 255$
8-bit PDO	$1 \leq (TTREGn) \leq 255$
8-bit PWM	$2 \leq (PWREGn) \leq 254$
16-bit Timer/Event Counter	$1 \leq (TTREG4, 3) \leq 65535$
fc Warming-up Counter	$256 \leq (TTREG4, 3) \leq 65535$
16-bit PWM	$2 \leq (PWREG4, 3) \leq 65534$
16-bit PPG	$1 \leq (PWREG4, 3) < (TTREG4, 3) \leq 65535$ and $(PWREG4, 3) + 1 < (TTREG4, 3)$

Note: $n = 3, 4$

2.7.3 Function

Timer/Counter 3 and 4 have eight operating modes: 8-bit timer, 8-bit external trigger timer, 8-bit programmable divider output mode, 8-bit pulse width modulation output mode, 16-bit timer, 16-bit external trigger timer, 16-bit pulse width modulation output mode, 16-bit programmable pulse generator output mode.

16-bit timer mode can use Timer counter 3 and 4 by cascade connection.

(1) 8-Bit Timer Mode (Timer/Counter 3 and 4)

In this mode, counting up is performed using the internal clock. The contents of TTREGi are compared with the contents of up-counter. If a match is found, an INTTCi interrupt is generated, and the counter is cleared to "0". Counting up resumes after the counter is cleared.

Note 1: In the timer mode, always write TCjCR<TFfj> to "0". If TFFj is set to "1", unexpected pulse may be output from PDOj / PWMj / PPGj pin.

Note 2: In the timer mode, do not change the setting of timer registers (TTREGi) while timer/counter is operating. Since TTREGi is configured as one-stage register, a newly set value is immediately reflected on the timer register.

Note 3: j = 3, 4 i = 3, 4

Table 2-9. Timer/Counter 1 Source Clock (Internal Clock)

Source clock		SLOW1/2, SLEEP1/2 modes	Resolution		Maximum time setting	
NORMAL1/2, IDLE1/2 modes			At fc = 16 MHz	At fs = 32.768 kHz	At fc = 16 MHz	At fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
fc / 2 ¹¹ [Hz]	fs / 2 ³ [Hz]	fs / 2 ³ [Hz]	128 [μs]	244.14 [μs]	32.6 [ms]	62.3 [ms]
fc / 2 ⁷	fc / 2 ⁷	-	8 [μs]	-	2.0 [ms]	-
fc / 2 ⁵	fc / 2 ⁵	-	2 [μs]	-	510 [μs]	-
fc / 2 ³	fc / 2 ³	-	500 [ns]	-	127.5 [μs]	-

Example: Sets the timer mode with source clock fc/2⁷ [Hz] and generates an interrupt 80 μs later (at fc = 16 MHz).

```
LDW (TTREG4), 0AH ; Sets the timer register (80 μs ÷ 27/fc = 0AH)
DI
SET (EIRH).EF11 ; Enables INTTC4 interrupt
EI
LD (TC4CR), 00010000B ; Sets the 8-bit timer mode and source clock (fc/27)
LD (TC4CR), 00011000B ; Starts TC4
```

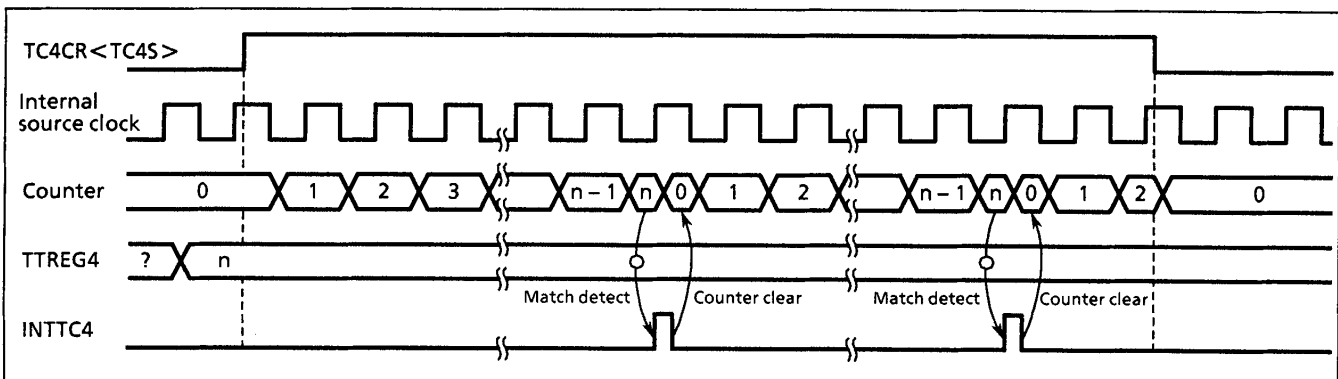


Figure 2-28. 8-Bit Timer Mode Timing Chart (In Case of Timer/Counter 4)

(2) 8-Bit Event Counter Mode (Timer/Counter 3 and 4)

In this mode, events are counted on the falling edge of TC_j pin input. The contents of TTREG_j are compared with the contents of up-counter. If a match is found, an INTTC_j interrupt is generated, and the counter is cleared. The maximum applied frequency is $f_c/2^4$ [Hz] in NORMAL1/2 or IDLE1/2 mode and $f_s/2^4$ [Hz] in SLOW1/2 or SLEEP1/2 mode. Two or more machine cycles are required for both the "H" and "L" levels of the pulse width.

Note 1: In the event counter mode, always write TC_jCR<TC₄S> to "0". If TFF_j is set to "1", unexpected pulse may be output from $\overline{PDO_j}$ / $\overline{PWM_j}$ / $\overline{PPG_j}$ pin.

Note 2: In the event counter mode, do not change the setting of timer registers (TTREG_j) while timer/counter is operating. Since TTREG_j is configured as one-stage register, a newly set value is immediately reflected on the timer register.

Note 3: $j = 3, 4$

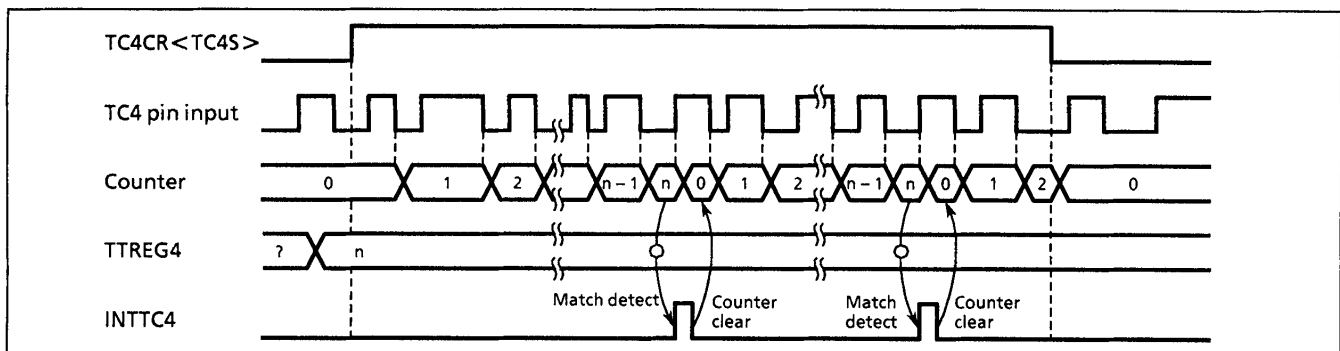


Figure 2-29. Event Counter Mode Timing Chart (In Case of Timer/Counter 4)

(3) 8-Bit Programmable Divider Output (PDO) Mode (Timer/Counter 3 and 4)

The internal clock is used for counting up. The contents of TTREG_j are compared with the contents of the up-counter. Timer F/F_j output is toggled and the counter is cleared each time a match is found. Timer F/F_j output is inverted and output to the $\overline{PDO_j}$ pin. When used as a this mode, respective output latch should be set to "1". This mode can be used for 50% duty pulse output. Timer F/F_j can be initialized by program, and it is initialized to "0" during reset. An INTTC_j interrupt is generated each time the $\overline{PDO_j}$ output is toggled.

Example: Output a 1024 Hz pulse (at $f_c = 16$ MHz = "0", in case of TC4)

```
SET (P3DR). 2 ; P32 output latch ← 1
LD (TTREG4), 7AH ; (1/1024 ÷ 27/fc) ÷ 2 = 7AH
LD (TC4CR), 00010001B ; Sets the 8-bit PDO mode and source clock (fc/27)
LD (TC4CR), 00011001B ; Starts TC4
```

Note 1: In the programmable divider output(PDO) mode, do not change the setting of timer registers (TTREG_j) while timer/counter is operating. Since TTREG_j is configured as one-stage register, a newly set value is immediately reflected on the timer register.

Note 2: If PDO output is stopped during output operation, the output state is maintained at the state immediately before timer/counter is stopped. For changing the level of $\overline{PDO_j}$ pin, modify TC_jCR<TFF_j> after timer/counter has been stopped. Do not execute halt of timer/counter and modification of TFF_j simultaneously.

Example: Fixes $\overline{PDO_j}$ output at high level after timer/counter is stopped

```
CLR (TCjCR).3 ; Stops timer/counter.
```

```
CLR (TCjCR).7 ; Sets  $\overline{PDO_j}$  output to high level output
```

Note 3: $j = 3, 4$

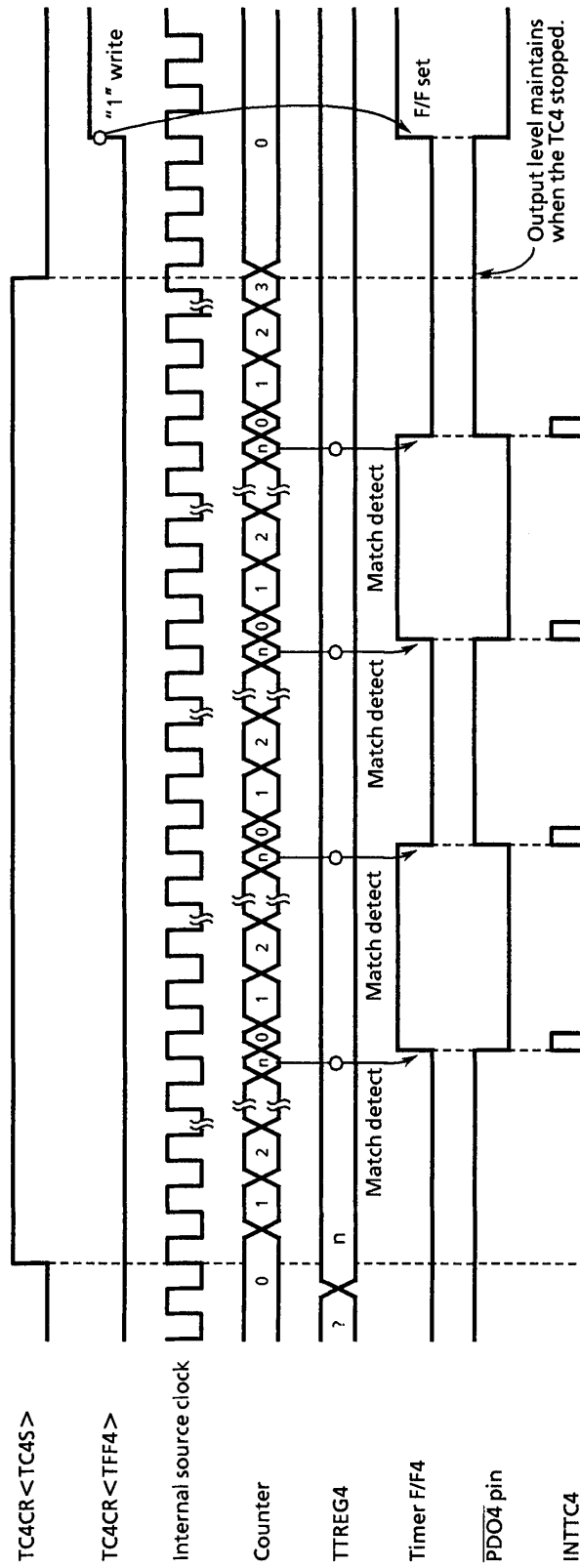


Figure 2-30. 8-Bit PDO Mode Timing Chart (In Case of Timer/Counter 4)

(4) 8-Bit Pulse Width Modulation (PWM) Output Mode (Timer/Counter 3 and 4)

PWM output with a resolution of 8 bits is possible. The internal clock is used for counting up. The contents of PWREG_i are compared with the contents of up-counter. If a match is found, the timer F/F_i output is toggled. The counter continues counting. And, when an overflow occurs, the timer F/F_i output is again toggled and the counter is cleared. Timer F/F_i output is inverted and output to the \overline{PWMi} pin. An INTTC_i interrupt is generated when an overflow occurs.

In PWM mode, because PWREG_i becomes a 2-stage registers with shift register, it is possible to change the setting value of PWREG_i while timer/counter is operating. Therefore, output can be altered continuously. The shift operation of PWREG_i to shift register is executed at the INTTC_i timing. While timer/counter is operating, the data by read instruction is not a setting value of PWREG_i but a value of shift register. Therefore, after writing to PWREG_i, the reading data of PWREG_i is previous value till INTTC_i is generated.

While timer/counter stops, written value to PWREG_i is shifted to shift register immediately.

Note 1: In PWM mode, write to the timer register PWREG_i immediately after an INTTC_i interrupt is generated (normally during the INTTC_i interrupt service routine). If writing to PWREG_i and INTTC_i interrupt occur at the same time, the unstable value being written is shifted. This may cause pulses different from the set value to be output until the next INTTC_i interrupt is generated.

Note 2: If PWM output is stopped during output operation, the output state is maintained at the state immediately before timer/counter is stopped. For changing the level of \overline{PWMi} , modify TCiCR<TFFi> after timer/counter has been stopped. Do not execute halt of timer/counter and modification of TFFi simultaneously.

Example: Fixes \overline{PWMi} output at high level after timer/counter is stopped

CLR (TCiCR).3 ; Stops timer/counter.

CLR (TCiCR).7 ; Sets \overline{PWMi} output to high level output

Note 3: Before starting STOP mode, disable PWM output. When the timer/counter is enabled and fc, fc/2 or fs is selected as the source clock, pulse is output from PWM pin during warming-up after releasing STOP mode.

Note 4: i = 3, 4

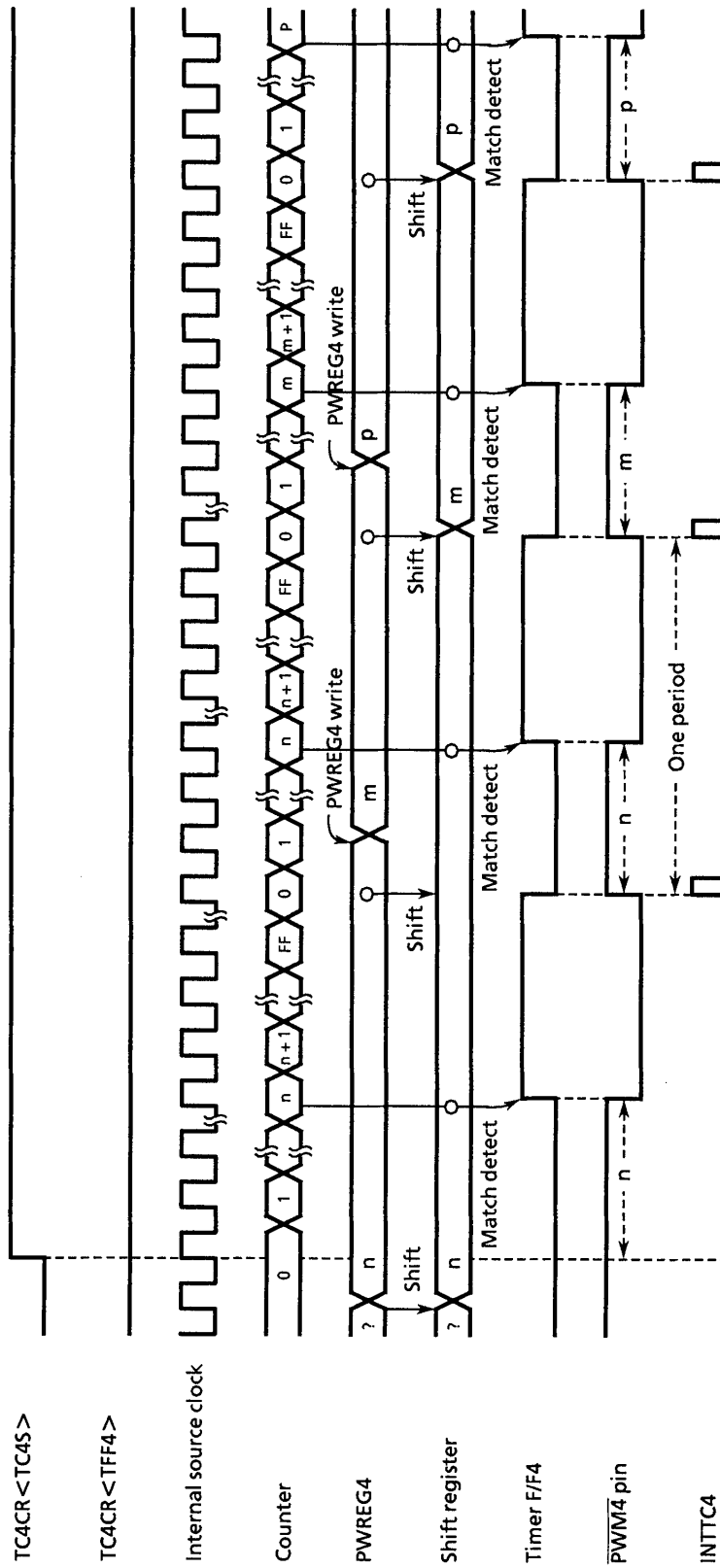


Figure 2-31. 8-Bit PWM Mode Timing Chart (In Case of Timer/Counter 4)

Table 2-10. PWM Output Mode

Source clock		SLOW1/2, SLEEP1/2 mode	Resolution		Maximum setting time	
NORMAL1/2, IDLE1/2 mode	fc = 16 MHz		fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz	
DV7CK = 0	DV7CK = 1					
fc/2 ¹¹ [Hz]	fs/2 ³ [Hz]	fs/2 ³ [Hz]	128 [μ s]	244.14 [μ s]	32.8 [ms]	62.5 [ms]
fc/2 ⁷	fc/2 ⁷	–	8 [μ s]	–	2.05 [ms]	–
fc/2 ⁵	fc/2 ⁵	–	2 [μ s]	–	512 [μ s]	–
fc/2 ³	fc/2 ³	–	500 [ns]	–	128 [μ s]	–
fs	fs	fs	30.5 [μ s]	30.5 [μ s]	7.81 [ms]	7.81 [ms]
fc/2	fc/2	–	125 [ns]	–	32 [μ s]	–
fc	fc	–	62.5 [ns]	–	16 [μ s]	–

(5) 16-Bit Timer Mode (Timer/counter 3 and 4)

In this mode, counting up is performed using the internal clock.

Timer/counter 3 and 4 are also available as a 16-bit timer mode by cascade connection.

a. 16 bit timer mode of Timer/counter 3 and 4

If a match is found, the INTTC4 interrupt is generated and the counter is cleared to "0". Counting up resumes after the counter is cleared. The timer register should write to the TTREG3 more first than TTREG4. The timer register must not write only either TTREG3 or TTREG4.

Note 1: In the timer mode, always write TCjCR<TFfj> to "0". If TFFj is set to "1", unexpected pulse may be output from P \overline{D} Oj / P \overline{W} Mj / P \overline{P} Gj pin.

Note 2: In the timer mode, do not change the setting of timer registers (TTREGi) while timer/counter is operating. Since TTREGi is configured as one-stage register, a newly set value is immediately reflected on the timer register.

Note 3: j = 3, 4 i = 3, 4

Table 2-11. Source Clock of 16-Bit Timer Mode

Source clock		SLOW1/2, SLEEP1/2 mode	Resolution		Maximum setting time	
NORMAL1/2, IDLE1/2 mode	At fc = 16 MHz		At fs = 32.768 kHz	At fc = 16 MHz	At fs = 32.768 kHz	
DV7CK = 0	DV7CK = 1					
fc/2 ¹¹	fs/2 ³ [Hz]	fs/2 ³	128 [μ s]	244.14 [μ s]	8.39 [s]	16 [s]
fc/2 ⁷	fc/2 ⁷	–	8 [μ s]	–	524.3 [ms]	–
fc/2 ⁵	fc/2 ⁵	–	2 [μ s]	–	131.1 [ms]	–
fc/2 ³	fc/2 ³	–	500 [ns]	–	32.8 [ms]	–

Example: Set the 16-bit timer mode with source clock fc/2⁷ [Hz] and generates an interrupt 300 [ms] later (at fc = 16 [MHz])

```
LDW (TTREG3), 927CH ; Sets the timer register (300 ms ÷ 27/fc = 927CH)
DI
SET (EIRH). EF11 ; Enable INTTC4 interrupt
EI
LD (TC3CR), 13H ; Sets the 16-bit timer mode (lower) and source clock
LD (TC4CR), 04H ; Sets the 16-bit timer mode (upper)
LD (TC4CR), 0CH ; Starts timer/counter
```

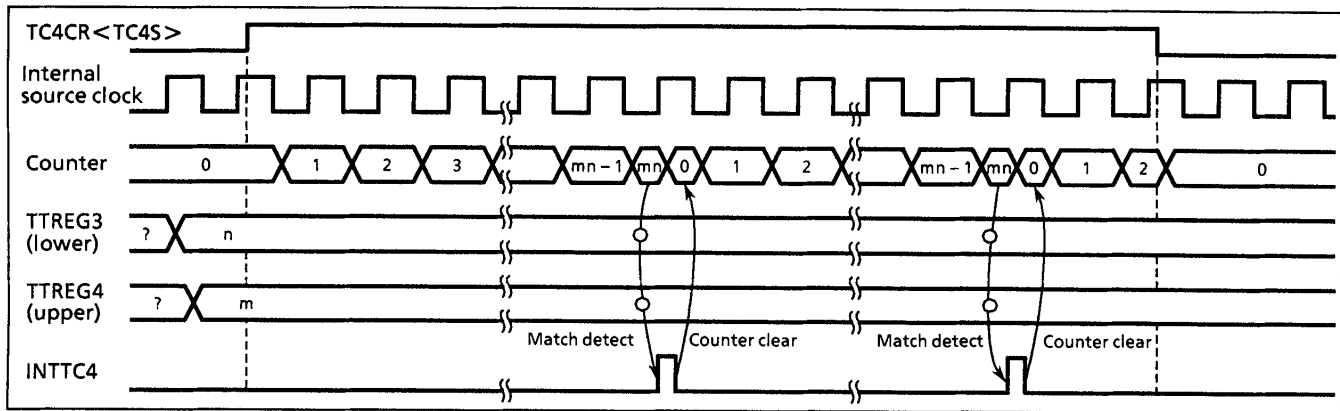


Figure 2-32. 16-bit Timer Mode Timing Chart (In Case of Timer/Counter 3 and 4)

(6) 16-Bit Event Counter Mode (Timer/counter 3 and 4)

In this mode, event are counted on the falling edge of the TC3 pin input. Timer/counter 3 and 4 are also available as a 16-bit Event counter mode by cascade connection.

a. 16 bit event counter mode of Timer/counter 3 and 4

If a match is found, the INTTC4 interrupt is generated and the counter is cleared to "0". After the counter is cleared, counting up resumes every falling edge of TC3 input. The maximum applied frequency is $fc/2^4$ [Hz] in NORMAL1/2 or IDLE1/2 mode and $fs/2^4$ [Hz] in SLOW1/2 or SLEEP1/2 mode. Two or more machine cycles are required for both the "H" and "L" levels of the pulse width. The timer register should write to the TTREG3 more first than TTREG4. The timer register must not write only either TTREG3 or TTREG4.

Note 1: In the event counter mode, always write $TCjCR<TFj>$ to "0". If TFj is set to "1", unexpected pulse may be output from $PDOj$ / $PWMj$ / $PPGj$ pin.

Note 2: In the event counter mode, do not change the setting of timer registers (TTREGj) while timer/counter is operating. Since TTREGj is configured as one-stage register, a newly set value is immediately reflected on the timer register.

Note 3: $j = 3, 4$

(7) 16-bit Pulse Width Modulation (PWM) Output Mode (Timer/counter 3 and 4)

PWM output with a resolution of 16 bits is possible. Timer/counter 3 and 4 are also available as a 16-bit PWM output mode by cascade connection.

a. 16 bit PWM output mode of Timer/counter 3 and 4

The contents of PWREG3/4 are compared with the contents of up-counter. If a match is found, the timer F/F4 output is toggled. The counter continues counting. And, when an overflow occurs, the timer F/F4 output is again toggled and the counter is cleared. Timer F/F4 output is inverted and output to the PWM4 pin. An INTTC4 interrupt is generated when an overflow occurs. When used as PWM4 pin, respective output latch should be set to "1". In PWM mode, because PWREG4/3 each becomes a 2-stage registers with shift register, it is possible to change the setting value of PWREG4/3 while timer/counter is operating. Therefore, output can be altered continuously. The shift operation of PWREG4/3 to shift register is executed at the INTTC4 timing. While timer/counter is operating, the data by read instruction is not a setting value of PWREG4/3 but a value of shift register. Therefore, after writing to PWREG4/3, the reading data of these registers is previous value till INTTC4 is generated.

While timer/counter stops, written value to PWREG4/3 is shifted to shift register immediately. When writing to PWREG4/3, always write to the lower side (PWREG3) and then the upper side (PWREG4) in that order. Writing to only lower side (PWREG3) or the upper side (PWREG4) has no effect.

Note 1: In PWM mode, write to the timer register PWREG 4, 3 immediately after an INTTC4 interrupt is generated (normally during the INTTC4 interrupt service routine). If writing to PWREG4, n and INTTC4 interrupt occur at the same time, the unstable value being written is shifted. This may cause pulses different from the set value to be output until the next INTTC4 interrupt is generated.

Note 2: If PWM output is stopped during output operation, the output state is maintained at the state immediately before timer/counter is stopped. For changing the level of $\overline{PWM4}$, modify TC4CR<TFF4> after timer/counter has been stopped. Do not execute halt of timer/counter and modification of TFF4 simultaneously.

Example: Fixes $\overline{PWM4}$ output at high level after timer/counter is stopped

CLR (TC4CR).3 ; Stops timer/counter

CLR (TC4CR).7 ; Sets $\overline{PWM4}$ output to high level output

Note 3: Before starting STOP mode, disable PWM output. When the timer/counter is enabled and f_c , $f_c/2$ or f_s is selected as the source clock, pulse is output from PWM pin during warming-up after releasing STOP mode.

Table 2-12. 16-Bit PWM Output Mode

Source clock		SLOW1/2, SLEEP1/2 mode	Resolution		Maximum setting time	
NORMAL1/2, IDLE1/2 mode			At $f_c = 16$ MHz	At $f_s = 32.768$ kHz	At $f_c = 16$ MHz	At $f_s = 32.768$ kHz
DV7CK = 0	DV7CK = 1					
$f_c/2^{11}$	$f_s/2^3$ [Hz]	$f_s/2^3$	128 [μ s]	244.14 [μ s]	8.39 [s]	16 [s]
$f_c/2^7$	$f_c/2^7$	–	8 [μ s]	–	524.3 [ms]	–
$f_c/2^5$	$f_c/2^5$	–	2 [μ s]	–	131.1 [ms]	–
$f_c/2^3$	$f_c/2^3$	–	500 [ns]	–	32.8 [ms]	–
f_s	f_s	f_s	30.5 [μ s]	30.5 [μ s]	2 [s]	2 [s]
$f_c/2$	$f_c/2$	–	125 [ns]	–	8.2 [ms]	–
f_c	f_c	–	62.5 [ns]	–	4.1 [ms]	–

Example: Extract the pulse, whose term and “high” width is 32.768 ms and 1ms respectively, from P32 width 16-bit PWM mode (at $f_c = 16$ MHz = “0”, DV7CK = 0)

SET (P3DR). 2 ; Sets P32 output data latch to “1”

LDW(PWREG3), 07D0H ; Sets pulse width

LD (TC3CR), 33H ; Sets the 16-bit PWM mode (lower) and source clock ($f_c/2^3$)

LD (TC4CR), 0D6H ; Sets the TFF4 to “1” and sets the 16-bit PWM mode (upper)

LD (TC4CR), 0DEH ; Starts timer/counter

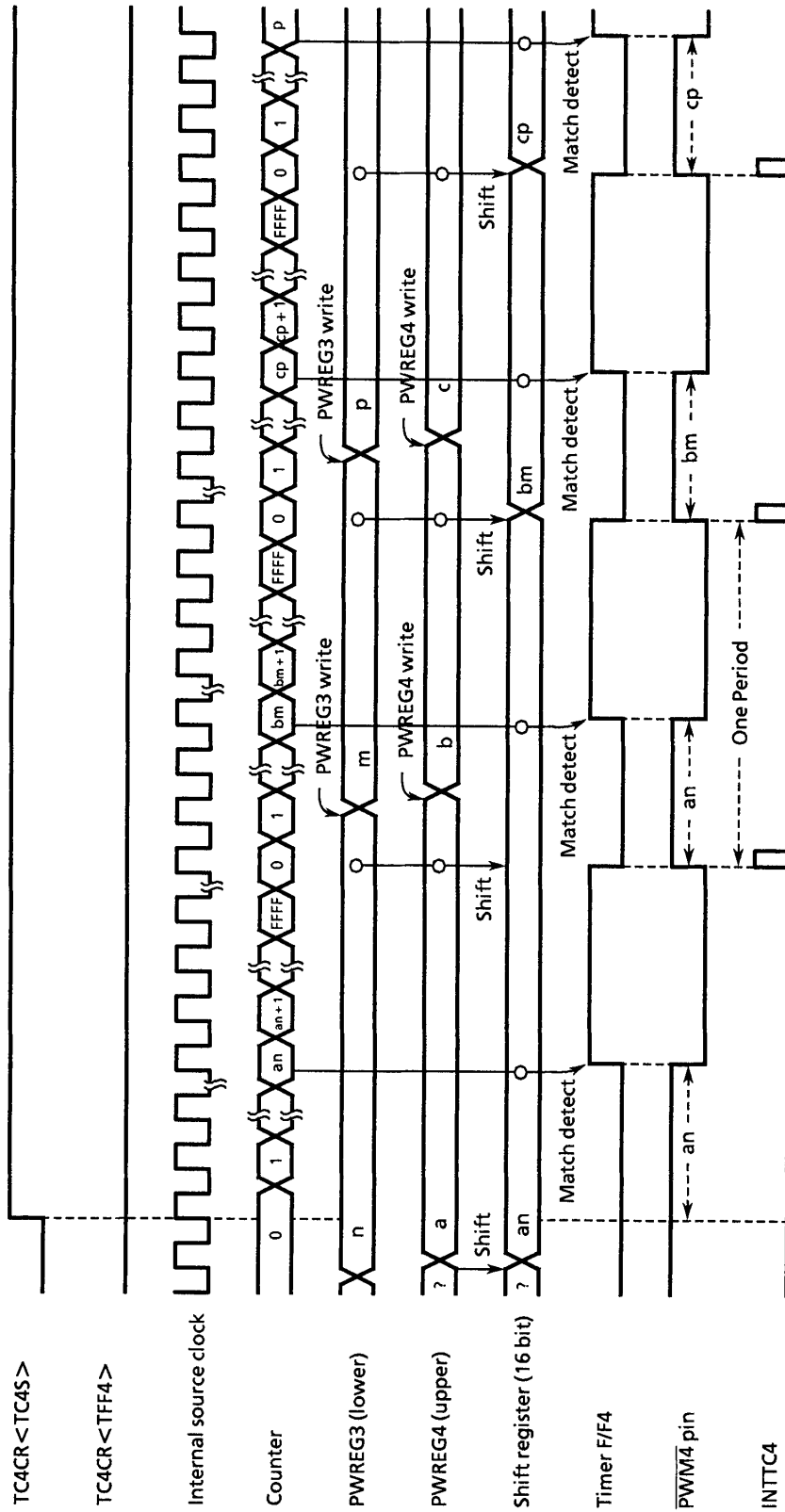


Figure 2-33. 16-Bit PWM Mode Timing Chart (In Case of Timer/Counter 3 and 4)

(8) 16-Bit Programmable Pulse Generate (PPG) output mode (Timer/counter 3 and 4)

PPG output with a resolution of 16 bits is possible. Timer/counter 3 and 4 are also available as a 16-bit PPG output mode by cascade connection.

a. 16-bit PPG output mode of Timer/counter 3 and 4

First, the contents of PWREG3/4 are compared with the contents of up-counter. If a match is found, the timer F/F4 output is toggled. Next, timer F/F4 is again toggled and the counter is cleared by matching with TTREG3/4. The INTTC4 interrupt is generated at this time.

When used as $\overline{PPG4}$ pin, respective output latch should be set to "1". During reset, the F/F4 is initialized to "0".

The F/F4 output is configured by TC4CR<TFF4>. Therefore, the $\overline{PPG4}$ can output either output high or output low at first time. The timer register should write to the PWREG3/TTREG3 more first than PWREG4/TTREG4. The timer register must not write only either PWREG3/TTREG3 or PWREG4/TTREG4.

Example: Extract the pulse, whose term and "high" width is 16.385 ms and 1ms respectively, from P32 with 16-bit PPG mode (at $f_c = 16$ MHz, $DV7CK = 0$)

```

SET (P3DR).2 ; Sets P32 output data latch to "1"
LDW (PWREG3), 07D0H ; Sets pulse width
LDW (TTREG3), 8002H ; Sets pulse term
LD (TC3CR), 33H ; Sets the 16-bit PPG mode (lower) and source clock ( $f_c/2^3$ )
LD (TC4CR), 0D7H ; Sets the TFF4 to "1" and sets the 16-bit PPG mode(upper)
LD (TC4CR), 0DFH ; Starts timer/counter

```

Note 1: In the programmable pulse generate (PPG) mode, do not change the setting of timer registers (PWREG_i, TTREG_i) while timer/counter is operating. Since PWREG_i, TTREG_i are configured as one-stage register, a newly set value is immediately reflected on the timer register.

Note 2: If PPG output is stopped during output operation, the output state is maintained at the state immediately before timer/counter is stopped. For changing the level of \overline{PPGj} , modify TCiCR<TFFi> after timer/counter has been stopped. Do not execute halt of timer/counter and modification of TFFj simultaneously.

Example: Fixes \overline{PPGj} output at high level after timer/counter is stopped

CLR (TCjCR).3 ; Stops timer/counter

CLR (TCjCR).7 ; Sets \overline{PPGj} output to high level output

Note 3: j = 4 i = 3, 4

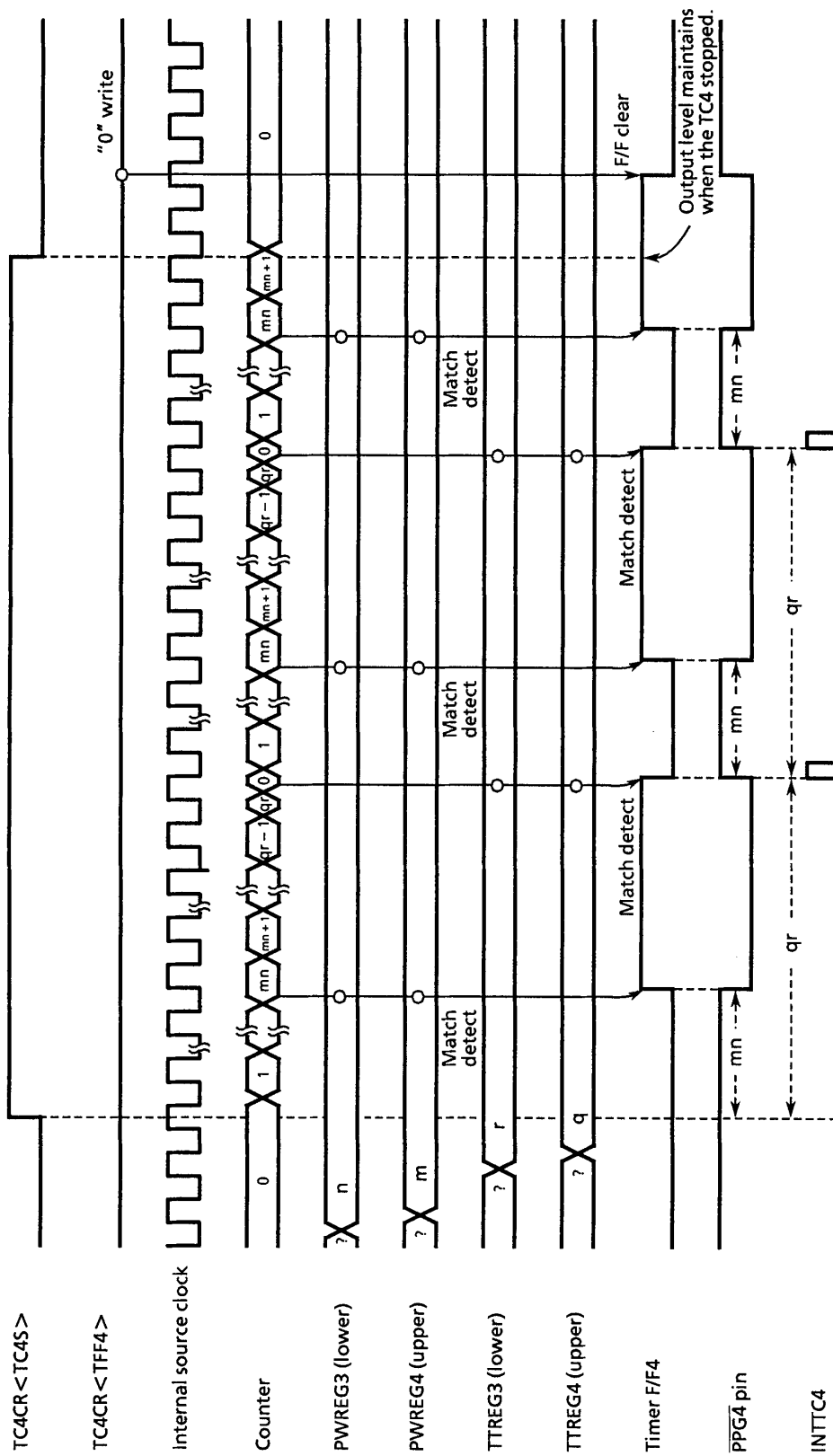


Figure 2-34. 16-Bit PPG Mode Timing Chart (In Case of Timer/Counter 3 and 4)

(9) Warming-up counter mode

In this mode, the warming-up period for switching the main system clock can be generated. Timer/counter 3 and 4 are used as a 16-bit timer by cascade connection.

There are 2 modes in warming-up counter mode, one is a mode from NORMAL to SLOW and the other is a mode from SLOW to NORMAL.

Note 1: In the warming-up mode, always write TCiCR<TFFi> to "0". If TFFi is set to "1", unexpected pulse may be output from \overline{PDOi} / \overline{PWMi} / \overline{PPGi} pin.

Note 2: In the warming-up mode, the lower 11 bits of TTREGm,n are ignored and an interrupt is generated by matching the upper 5 bits.

Note 3: i = 3, 4 m = 4 and n = 3

a. Warming-up counter mode for low-frequency (NORMAL1→NORMAL2→SLOW2→SLOW1)

In this mode, it can obtain the warming-up period till the oscillation for low-frequency (fs) is stabilized.

Before timer/counter is started, turn on low-frequency oscillation by setting SYSCR2<XTEN> to "1".

After timer/counter is started by setting TCmCR<TCmS>, the contents of TTREGm,n are compared with the contents of up-counter. If a match is found, an INTTCm interrupt is generated, and the counter is cleared to "0".

In the interrupt service program, stop the timer/counter and change the system clock to low-frequency clock by setting SYSCR2<SYSCK> to "1".

After that, halt the high-frequency oscillation by clearing SYSCR2<XEN> to "0".

Table 2-13. Warming-up period for low-frequency oscillation
(at fs = 32.768 kHz)

Min (at TTREGm, n = 0800H)	Max (at TTREGm, n = F800H)
62.5 ms	1.94 s

Example: Switching to the SLOW1 mode after low-frequency clock has stabilized by using TC4, 3.

```

SET   (SYSCR2).6      ; SYSCR2<XTEN> ← "1"
LD    (TC3CR), 43H    ; TFF3 = "0", fs for source clock, sets 16-bit mode
LD    (TC4CR), 05H    ; TFF4 = "0", sets warming-up counter mode
LD    (TTREG3), 8000H ; sets warming-up time (depend on oscillator characteristics)
DI                                         ; IMF ← "0"
SET   (EIRH).3        ; Enables INTTC4
EI                                         ; IMF ← "1"
SET   (TC4CR). 3      ; Starts TC4, 3
:
:
PINTTC4: CLR (TC4CR).3 ; Stops TC4, 3
SET   (SYSCR2).5      ; SYSCR2<SYSCK> ← "1"
                        ; (Switches the main system clock to the low-frequency clock)
CLR   (SYSCR2).7      ; SYSCR2<XEN> ← "0" (Turns off low-frequency oscillation)
RETI
:
:
VINTTC4: DW  PINTTC4   ; INTTC4 vector table

```

b. Warming-up counter mode for high-frequency(SLOW1→SLOW2→NORMAL2→NORMAL1)

In this mode, it can obtain the warming-up period till the oscillation for high-frequency (fc) is stabilized.

Before timer/counter is started, turn on high-frequency oscillation by setting SYSCR2<XEN> to "1".

After timer/counter is started by setting TCmCR<TCmS>, the contents of TTREGm,n are compared with the contents of up-counter. If a match is found, an INTTCm interrupt is generated, and the counter is cleared to "0".

In the interrupt service program, stop the timer/counter and change the system clock to high-frequency clock by clearing SYSCR2<SYSCK> to "0".

After that, halt the low-frequency oscillation by clearing SYSCR2<XTEN> to "0".

Table 2-14. Warming-up period for high-frequency (at fc = 16 MHz)

Min (at TTREGm, n = 0800H)	Max (at TTREGm, n = F800H)
128 μ s	3.97 ms

Example: Switching to the NORMAL1 mode after high-frequency clock has stabilized by using TC4, 3.

```

SET   (SYSCR2).7       ; SYSCR2<XEN> ← "1"
LD    (TC3CR), 63H     ; TFF3 = "0", fc for source clock, sets 16-bit mode
LD    (TC4CR), 05H     ; TFF4 = "0", sets warming-up counter mode
LD    (TTREG3), 0F800H ; Sets warming-up time (depend on oscillator characteristics)
DI                                         ; IMF ← "0"
SET   (EIRH).3         ; Enables INTTC4
EI                                         ; IMF ← "1"
SET   (TC4CR).3        ; Starts TC4, 3
:
:
PINTTC4: CLR (TC4CR).3 ; Stops TC4, 3
CLR   (SYSCR2).5       ; SYSCR2<SYSCK> ← "0"
                                   (Switches the main system clock to the high-frequency clock)
CLR   (SYSCR2).6       ; SYSCR2<XTEN> ← "0"
                                   (Turns off high-frequency oscillation)
RETI
:
:
VINTTC4: DW   PINTTC4   ; INTTC4 vector table
    
```

2.8 Serial Interface (SIO)

The TMP86C420/820 have one clocked-synchronous 8-bit serial interface. Serial interface has an 8-byte transmit and receive data buffer that can automatically and continuously transfer up to 64 bits of data.

The serial interface is connected to external devices via pins P16 (SO), P15 (SI), P17 (\overline{SCK}). The serial interface pins are also used as port P1. When these pins are used as serial interface pins, the correspondence output latch should be set to "1". In the transmit mode, pin P15 can be used as normal I/O port, and in the receive mode, the pin P16 can be used as normal I/O ports.

2.8.1 Configuration

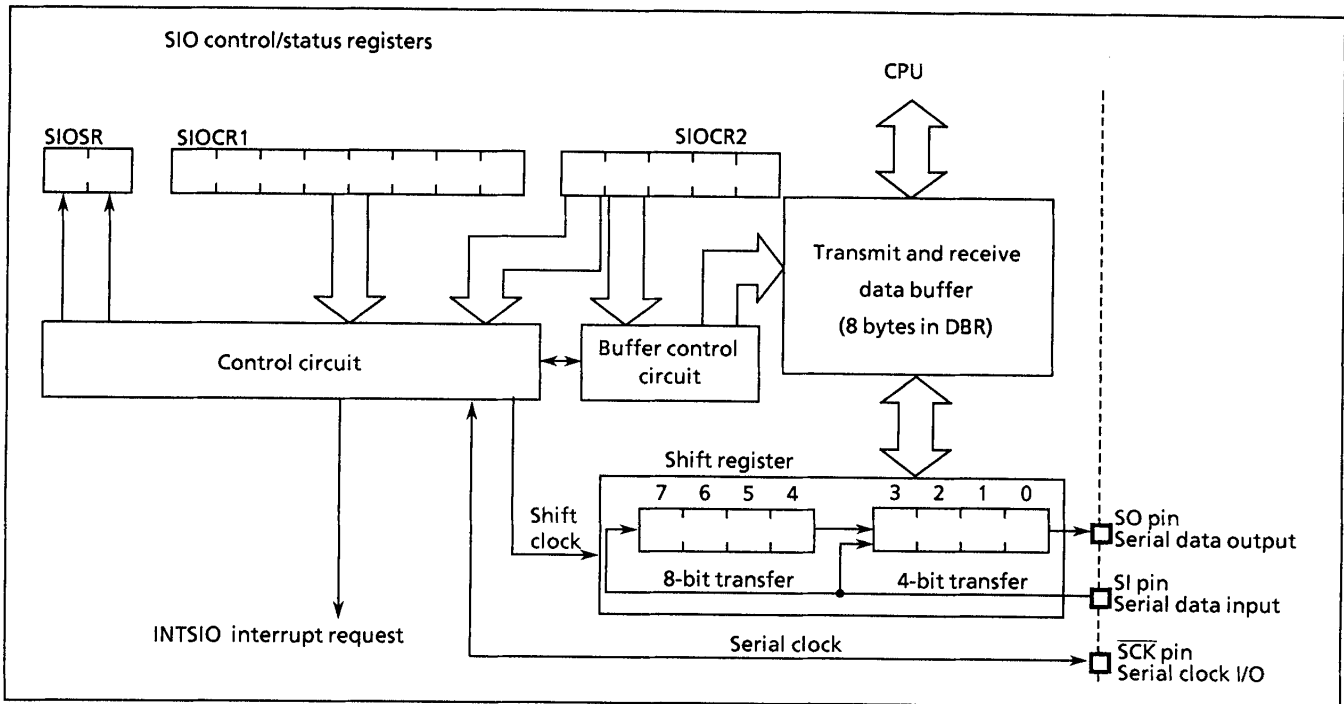


Figure 2-35. Serial Interfaces

2.8.2 Control

The serial interface is controlled by SIO control registers (SIOCR1/SIOCR2). The serial interface status can be determined by reading SIO status register (SIOSR).

The transmit and receive data buffer is controlled by the BUF (bits 2-0 in SIOCR2). The data buffer is assigned to address 0F90H to 0F97H for SIO in the DBR area, and can continuously transfer up to 8 words (bytes or nibbles) at one time. When the specified number of words has been transferred, a buffer empty (in the transmit mode) or a buffer full (in the receive mode or transmit/receive mode) interrupt (INTSIO) is generated.

When the internal clock is used as the serial clock in the 8-bit receive mode and the 8-bit transmit/receive mode, a fixed interval wait can be applied to the serial clock for each word transferred. Four different wait times can be selected with WAIT (bits 4 and 3 in SIOCR2).

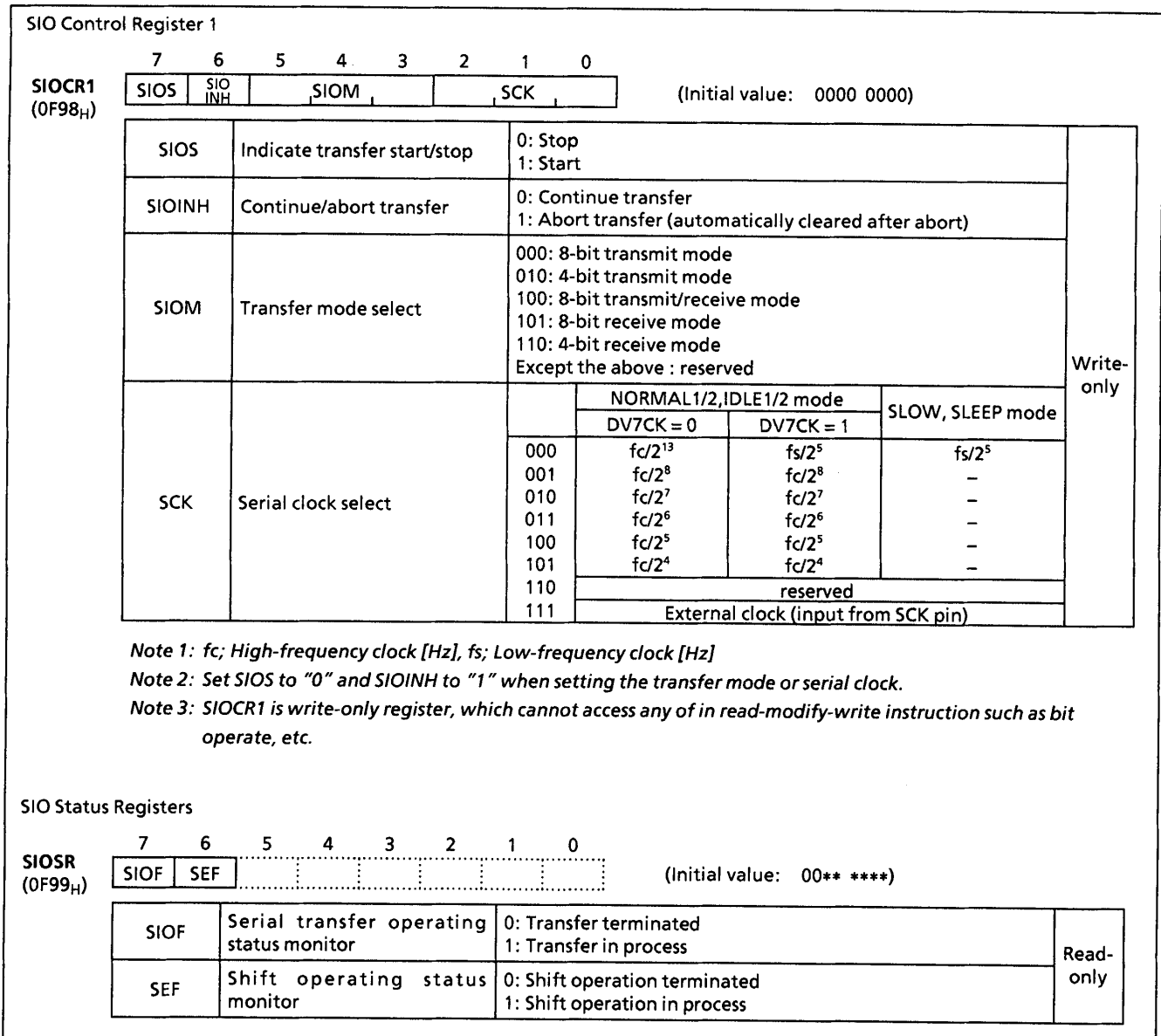


Figure 2-36. SIO Control Register and Status Register (1/2)

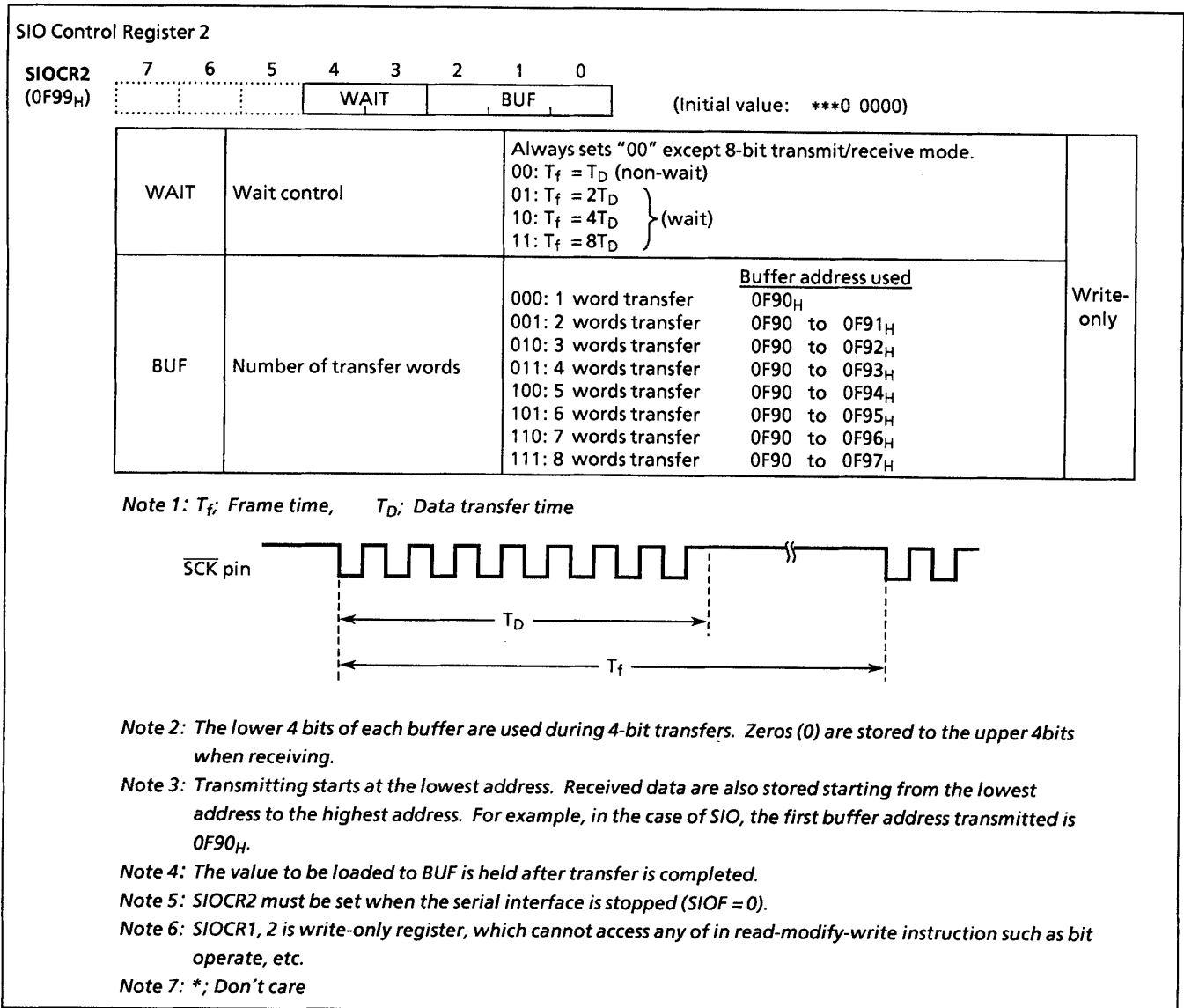


Figure 2-37. SIO Control Register and Status Register (2/2)

(1) Serial Clock

a. Clock Source

SIOCR1 <SCK> is able to select the following:

① Internal Clock

Any of seven frequencies can be selected. The serial clock is output to the outside on the $\overline{\text{SCK}}$ pin. The $\overline{\text{SCK}}$ pin goes high when transfer starts.

When data writing (in the transmit mode) or reading (in the receive mode or the transmit/receive mode) cannot keep up with the serial clock rate, there is a wait function that automatically stops the serial clock and holds the next shift operation until the read/write processing is completed.

Table 2-15. Serial Clock Rate

SCK	NORMAL 1/2, IDLE 1/2 modes				SLOW, SLEEP modes	
	DV7CK = 0		DV7CK = 1		clock	baud rate
	clock	baud rate	clock	baud rate		
000	$fc/2^{13}$	1.91 Kbps	$fs/2^5$	1024 bps	$fs/2^5$	1024 bps
001	$fc/2^8$	61.04 Kbps	$fc/2^8$	61.04 Kbps	-	-
010	$fc/2^7$	122.07 Kbps	$fc/2^7$	122.07 Kbps	-	-
011	$fc/2^6$	244.14 Kbps	$fc/2^6$	244.14 Kbps	-	-
100	$fc/2^5$	488.28 Kbps	$fc/2^5$	488.28 Kbps	-	-
101	$fc/2^4$	976.56 Kbps	$fc/2^4$	976.56 Kbps	-	-
110	-	-	-	-	-	-
111	External		External		External	

1 Kbit = 1024 bit
($fc = 16 \text{ MHz}$, $fs = 32.768 \text{ kHz}$)

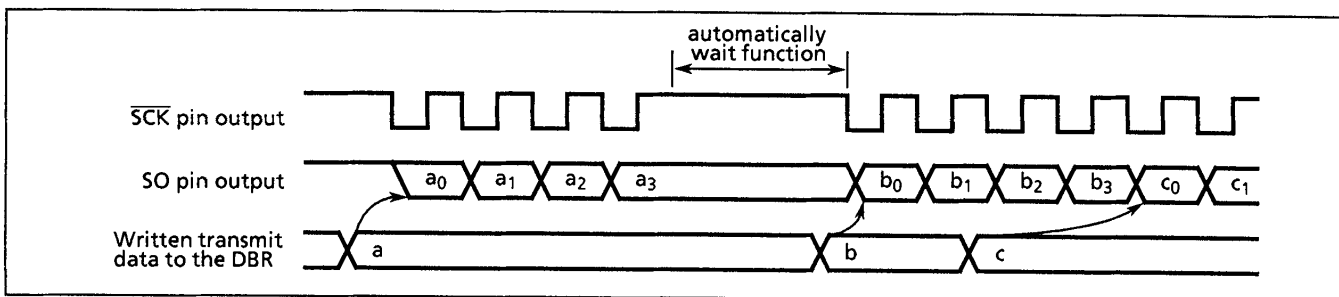
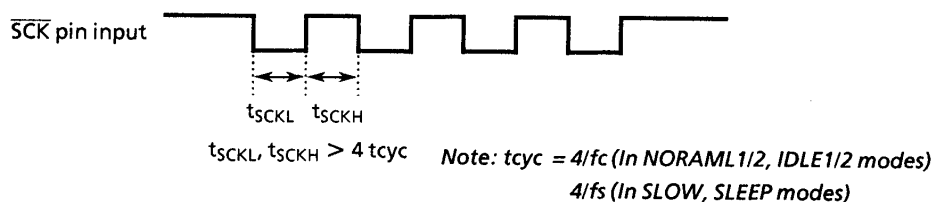


Figure 2-38. Clock Source (Internal Clock)

② External Clock

An external clock connected to the $\overline{\text{SCK}}$ pin is used as the serial clock. In this case, the P17 ($\overline{\text{SCK}}$) must be set to the input mode. To ensure shifting, a pulse width of at least 4 machine cycles is required. This pulse is needed for the shift operation to execute certainly. Actually, there is necessary processing time for interrupting, writing, and reading. The minimum pulse is determined by setting the mode and the program.



b. Shift edge

The leading edge is used to transmit, and the trailing edge is used to receive.

① Leading Edge

Transmitted data are shifted on the leading edge of the serial clock (falling edge of the \overline{SCK} pin input/output).

② Trailing Edge

Received data are shifted on the trailing edge of the serial clock (rising edge of the \overline{SCK} pin input/output).

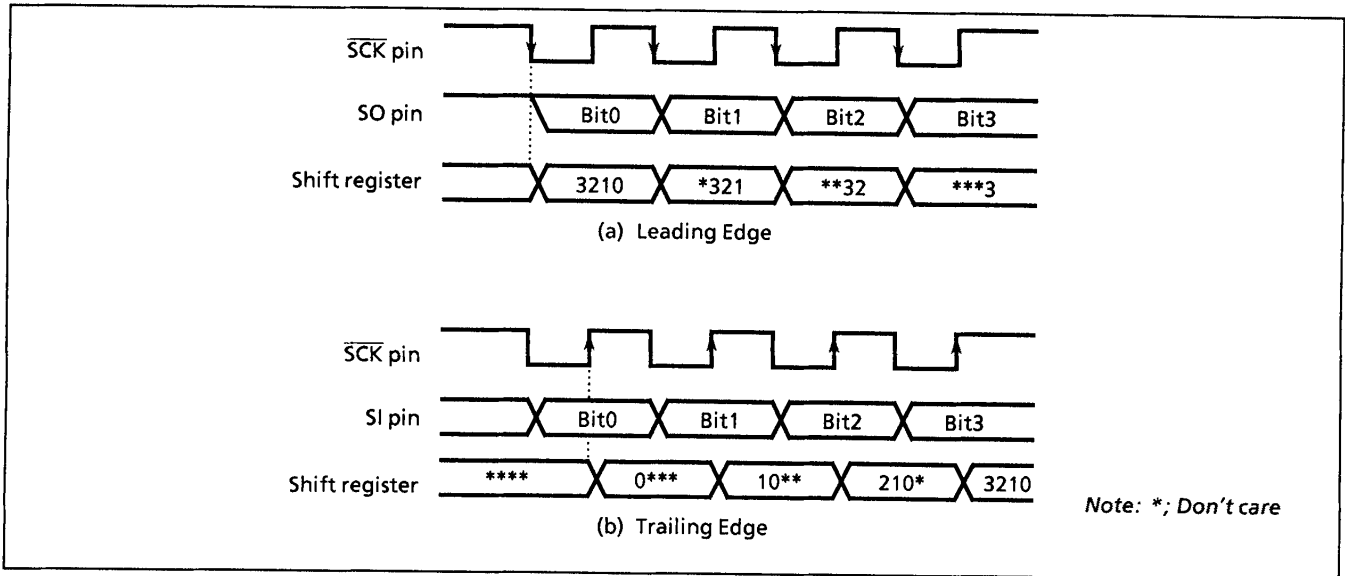


Figure 2-39. Shift Edge

(2) Number of Bits to Transfer

Either 4-bit or 8-bit serial transfer can be selected. When 4-bit serial transfer is selected, only the lower 4 bits of the transmit/receive data buffer register are used. The upper 4 bits are cleared to "0" when receiving.

The data is transferred in sequence starting at the least significant bit (LSB).

(3) Number of Words to Transfer

Up to 8 words consisting of 4 bits of data (4-bit serial transfer) or 8 bits (8-bit serial transfer) of data can be transferred continuously. The number of words to be transferred is loaded to SIOCR2 < BUF > .

An INTSIO interrupt is generated when the specified number of words has been transferred. If the number of words is to be changed during transfer, the serial interface must be stopped before making the change. The number of words can be changed during automatic-wait operation of an internal clock. In this case, the serial interface is not required to be stopped.

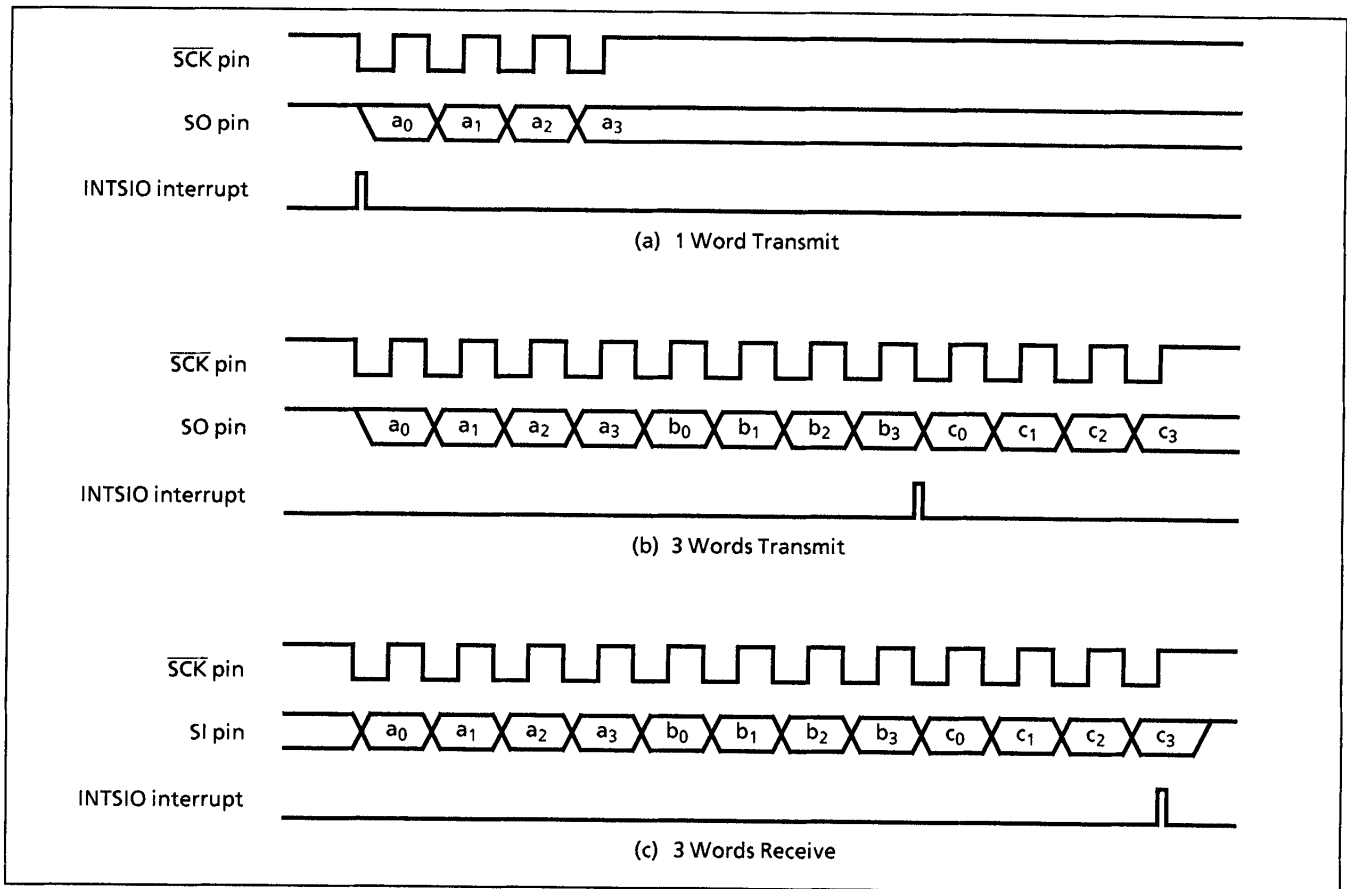


Figure 2-40. Number of Bits to Transfer (Example : 4-bit serial transfer)

2.8.3 Transfer mode

SIOCR1<SIOM> is used to select the transmit, receive, or transmit/receive mode.

(1) 4-bit and 8-bit Transmit Modes

In these modes, the SIOCR1 is set to the transmit mode and then the data to be transmitted first are written to the data buffer registers (DBR). After the data are written, the transmission is started by setting SIOCR1<SIOS> to "1". The data are then output sequentially to the SO pin in synchronous with the serial clock, starting with the least significant bit (LSB). As soon as the LSB has been output, the data are transferred from the data buffer register to the shift register. When the final data bit has been transferred and the data buffer register is empty, an INTSIO (buffer empty) interrupt is generated to request the next transmitted data.

When the internal clock is used, the serial clock will stop and an automatic-wait will be initiated if the next transmitted data are not loaded to the data buffer register by the time the number of data words specified with the SIOCR2<BUF> has been transmitted. Writing even one word of data cancels the automatic-wait; therefore, when transmitting two or more words, always write the next word before transmission of the previous word is completed.

Note: Automatic-waits are also canceled by writing to a DBR not being used as a transmit data buffer register; therefore, during SIO do not use such DBR for other applications. For example, when 3 words are transmitted, do not use the DBR of the remained 5 words.

When an external clock is used, the data must be written to the data buffer register before shifting next data. Thus, the transfer speed is determined by the maximum delay time from the generation of the interrupt request to writing of the data to the data buffer register by the interrupt service program.

The transmission is ended by clearing SIOCR1<SIOS> to "0" or setting SIOCR1<SIOINH> to "1" in buffer empty interrupt service program. That the transmission has ended can be determined from the status of SIOSR<SIOF> because SIOSR<SIOF> is cleared to "0" when a transfer is completed.

When SIOCR1<SIOINH> is set, the transmission is immediately ended and SIOSR<SIOF> is cleared to "0".

When an external clock is used, it is also necessary to clear SIOCR1<SIOS> to "0" before shifting the next data; otherwise, dummy data will be transmitted and the operation will end.

If it is necessary to change the number of words, SIOCR1<SIOS> should be cleared to "0", then SIOCR2<BUF> must be rewritten after confirming that SIOSR<SIOF> has been cleared to "0".

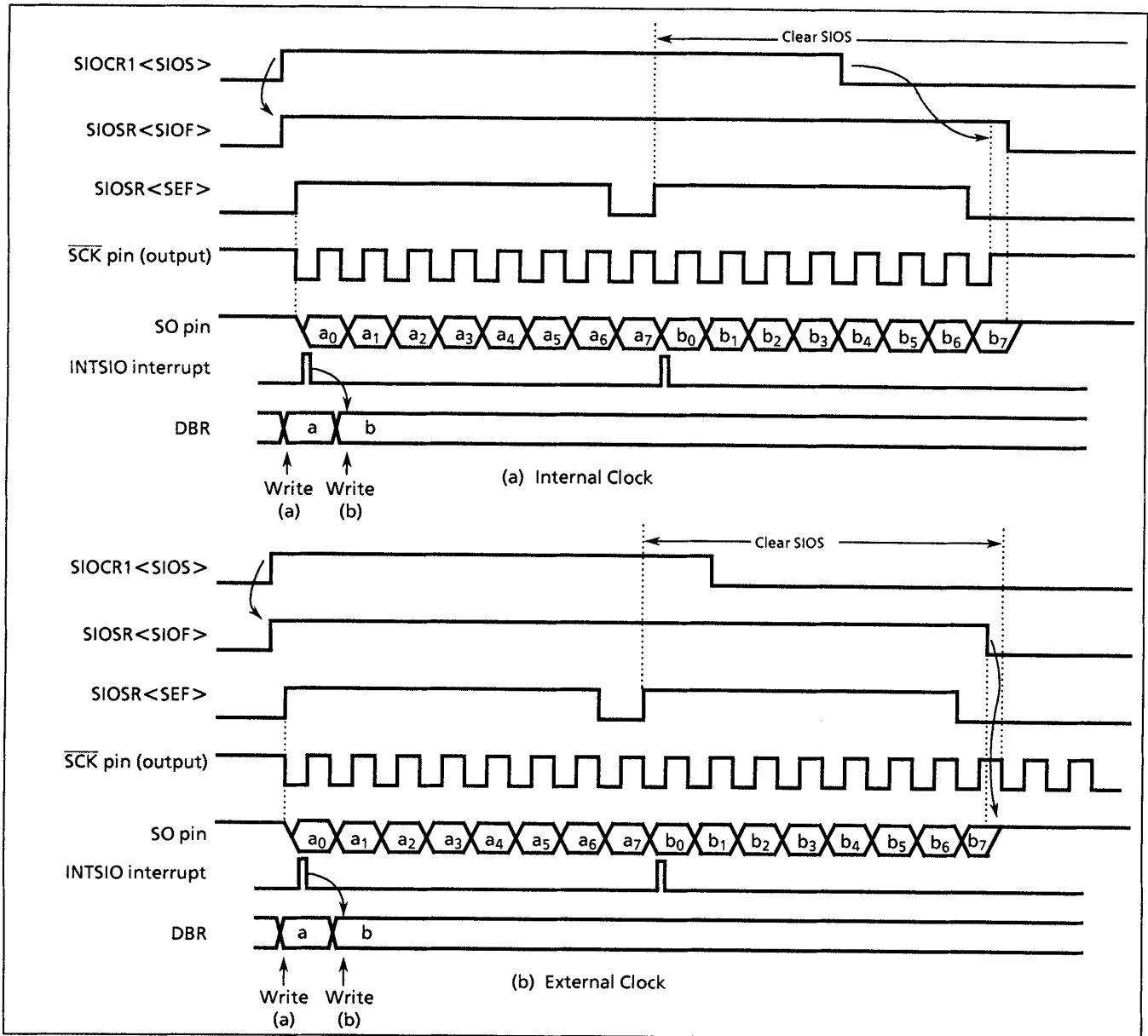


Figure 2-41. Transfer Mode (Example: 8-bit, 1 Word Transfer)

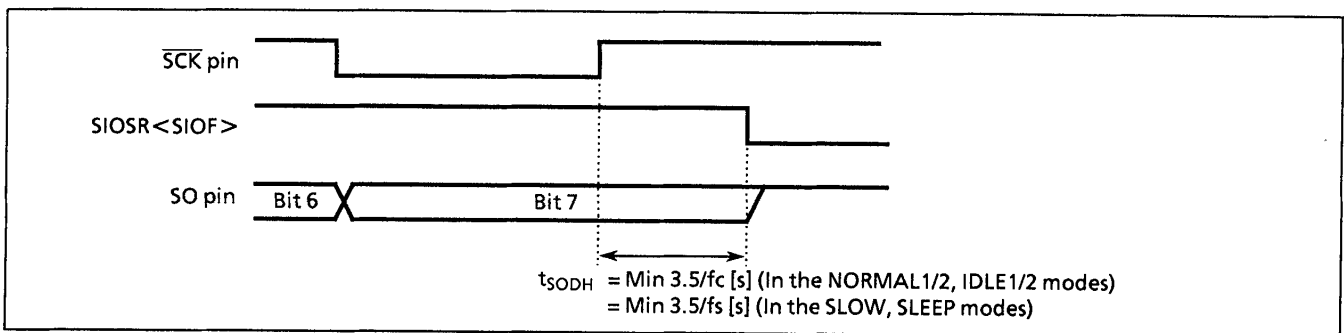


Figure 2-42. Transmitted Data Hold Time at End of Transmit

(2) 4-bit and 8-bit receive modes

After setting the control registers to the receive mode, set SIOCR1<SIOS> to "1" to enable receiving. The data are then transferred to the shift register via the SI pin in synchronous with the serial clock. When one word of data has been received, it is transferred from the shift register to the data buffer register (DBR). When the number of words specified with the SIOCR2<BUF> has been received, an INTSIO (buffer full) interrupt is generated to request that these data be read out. The data are then read from the data buffer registers by the interrupt service program.

When the internal clock is used, and the previous data are not read from the data buffer register before the next data are received, the serial clock will stop and an automatic-wait will be initiated until the data are read. A wait will not be initiated if even one data word has been read.

Note: Waits are also canceled by reading a DBR not being used as a received data buffer register is read; therefore, during SIO do not use such DBR for other applications.

When an external clock is used, the shift operation is synchronized with the external clock; therefore, the previous data are read before the next data are transferred to the data buffer register. If the previous data have not been read, the next data will not be transferred to the data buffer register and the receiving of any more data will be canceled. When an external clock is used, the maximum transfer speed is determined by the delay between the time when the interrupt request is generated and when the data received have been read.

The receiving is ended by clearing SIOCR1<SIOS> to "0" or setting SIOCR1<SIOINH> to "1" in buffer full interrupt service program. When SIOCR1<SIOS> is cleared, the current data are transferred to the buffer. After SIOCR1<SIOS> cleared, the receiving is ended at the time that the final bit of the data has been received. That the receiving has ended can be determined from the status of SIOSR<SIOF>. SIOSR<SIOF> is cleared to "0" when the receiving is ended. After confirmed the receiving termination, the final receiving data is read. When SIOCR1<SIOINH> is set, the receiving is immediately ended and SIOSR<SIOF> is cleared to "0". (The received data is ignored, and it is not required to be read out.)

If it is necessary to change the number of words in external clock operation, SIOCR1<SIOS> should be cleared to "0" then SIOCR2<BUF> must be rewritten after confirming that SIOSR<SIOF> has been cleared to "0".

If it is necessary to change the number of words in internal clock, during automatic-wait operation which occurs after completion of data receiving, SIOCR2<BUF> must be rewritten before the received data is read out.

Note: The buffer contents are lost when the transfer mode is switched. If it should become necessary to switch the transfer mode, end receiving by clearing SIOCR1<SIOS> to "0", read the last data and then switch the transfer mode.

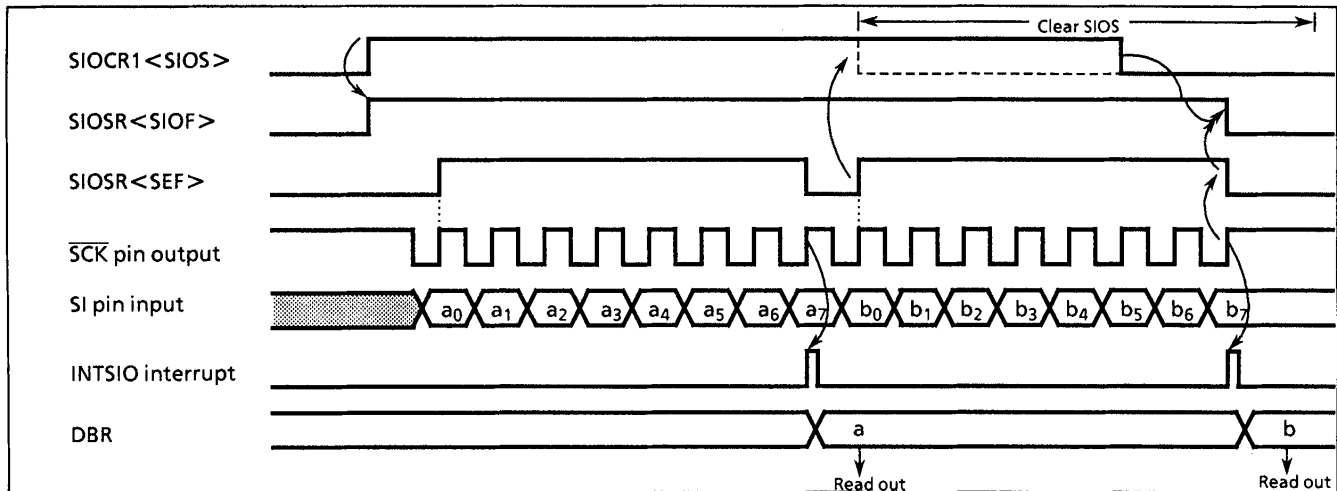


Figure 2-43. Receive Mode (Example: 8-bit, 1 word, internal clock)

(3) 8-bit transmit / receive mode

After setting the control registers to the 8-bit transmit / receive mode, write the data to be transmitted first to the data buffer registers (DBR). After that, enable transceiving by setting <SIOS> to "1". When transmitting, the data are output from the SO pin at leading edges of the serial clock. When receiving, the data are input to the SI pin at the trailing edges of the serial clock. 8-bit data are transferred from the shift register to the data buffer register. An INTSIO interrupt is generated when the number of data words specified with the <BUF> has been transferred. The interrupt service program reads the received data from the data buffer register and then writes the data to be transmitted. The data buffer register is used for both transmitting and receiving; therefore, always write the data to be transmitted after reading the received data.

When the internal clock is used, a wait is initiated until the received data are read and the next data are written. A wait will not be initiated if even one data word has been written.

Note: The wait is also canceled by writing to a DBR not being used as a transmit data buffer registers; therefore, during SIO do not use such DBR for other applications.

When an external clock is used, the shift operation is synchronized with the external clock; therefore, it is necessary to read the received data and write the data to be transmitted next before starting the next shift operation. When an external clock is used, the transfer speed is determined by the maximum delay between generation of an interrupt request and the received data are read and the data to be transmitted next are written.

The transmit/receive operation is ended by clearing SIOCR1<SIOS> to "0" or setting SIOSR<SIOINH> to "1" in interrupt service program.

When SIOCR1<SIOINH> is set, the transmit/receive operation is immediately ended and SIOSR<SIOF> is cleared to "0".

If it is necessary to change the number of words in external clock operation, SIOCR1<SIOS> should be cleared to "0", then SIOCR2<BUF> must be rewritten after confirming that SIOSR<SIOF> has been cleared to "0".

If it is necessary to change the number of words in internal clock, during automatic-wait operation which occurs after completion of transmit/receive operation, SIOCR2<BUF> must be rewritten before reading and writing of the receive/transmit data.

Note: The buffer contents are lost when the transfer mode is switched. If it should become necessary to switch the transfer mode, end receiving by clearing SIOCR1<SIOS> to "0", read the last data and then switch the transfer mode.

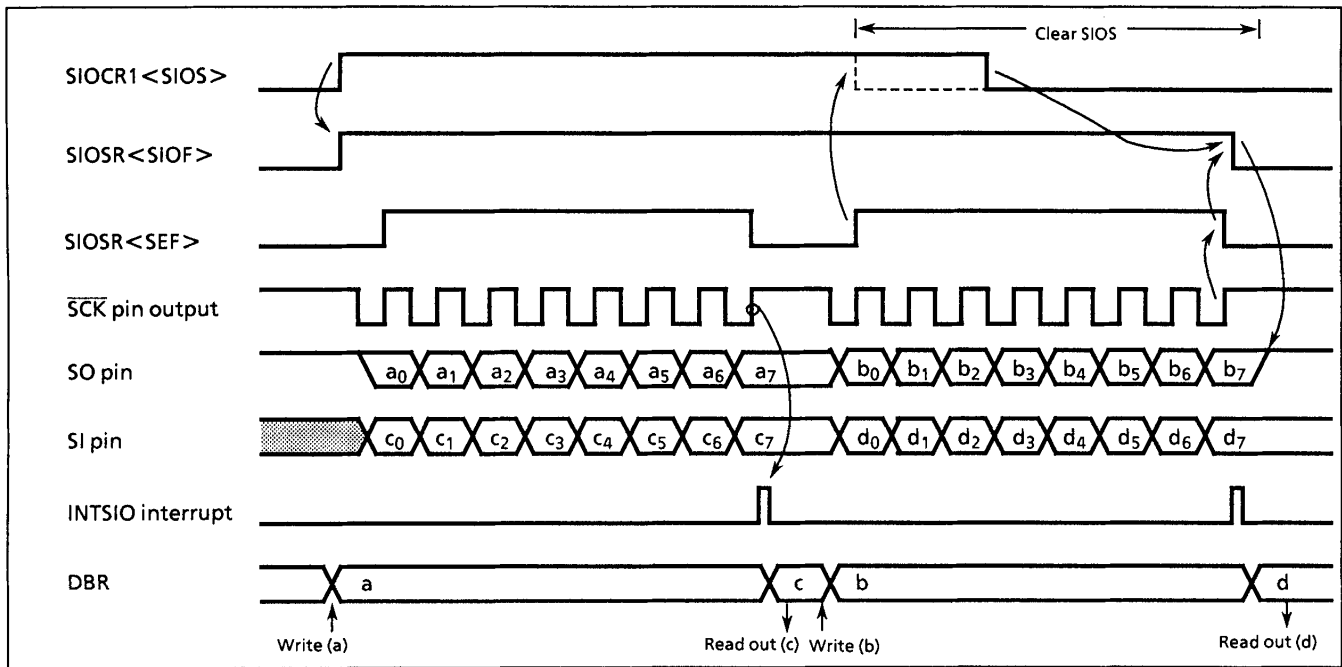


Figure 2-44. Transmit/Receive Mode (Example: 8-bit, 1word, internal clock)

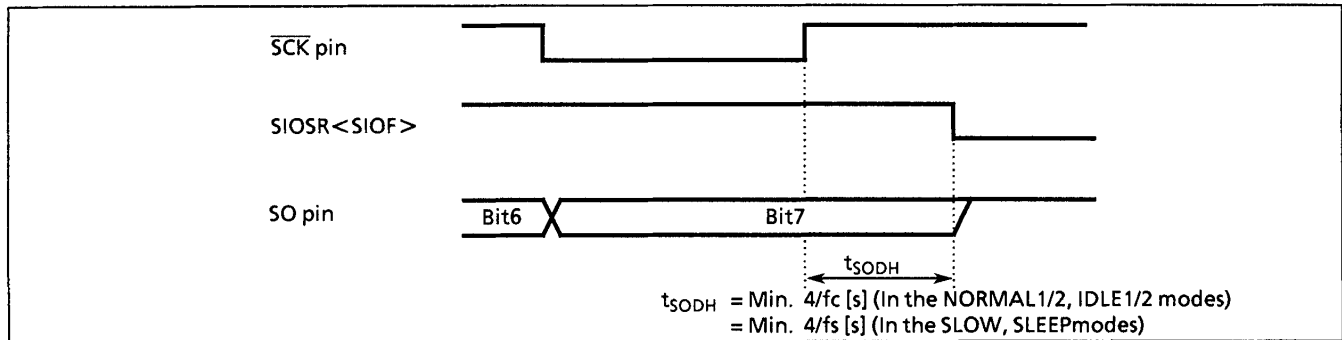


Figure 2-45. Transmitted Data Hold Time at End of Transmit/Receive

2.9 8-Bit AD Converter (ADC)

The TMP86C420/820 have a 8-bit successive approximation type AD converter.

2.9.1 Configuration

The circuit configuration of the 8-bit AD converter is shown in Figure 2-46.

It consists of control registers ADCCR1 and ADCCR2, converted value registers ADCDR1 and ADCDR2, a DA converter, a sample-and-hold circuit, a comparator, and a successive comparison circuit.

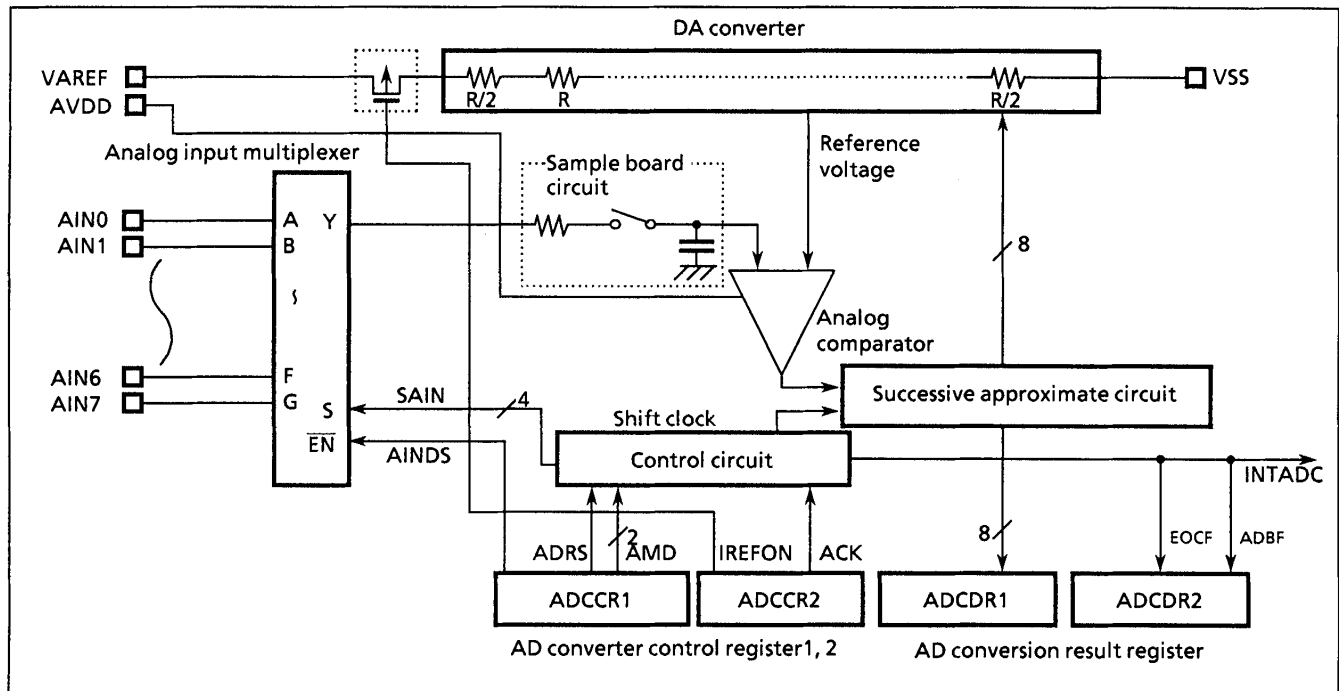


Figure 2-46. AD Converter (ADC)

2.9.2 Register Configuration

The AD converter consists of the following four registers:

- AD converter control register 1 (ADCCR1)
- AD converter control register 2 (ADCCR2)
- AD converted value register 1/2 (ADCDR1/ADCDR2)

(1) AD converter control register 1 (ADCCR1)

This register selects the analog channels and operation mode (software start) in which to perform AD conversion and controls the AD converter as it starts operating.

(2) AD converter control register 2 (ADCCR2)

This register selects the AD conversion time and controls the connection of the DA converter (ladder resistor network).

(3) AD converted value register1 (ADCDR1)

This register is used to store the digital value after being converted by the AD converter.

(4) AD converted value register2 (ADCDR2)

This register monitors the operating status of the AD converter.

The AD converter control register configurations are shown in Figures 2-47 and 2-48.

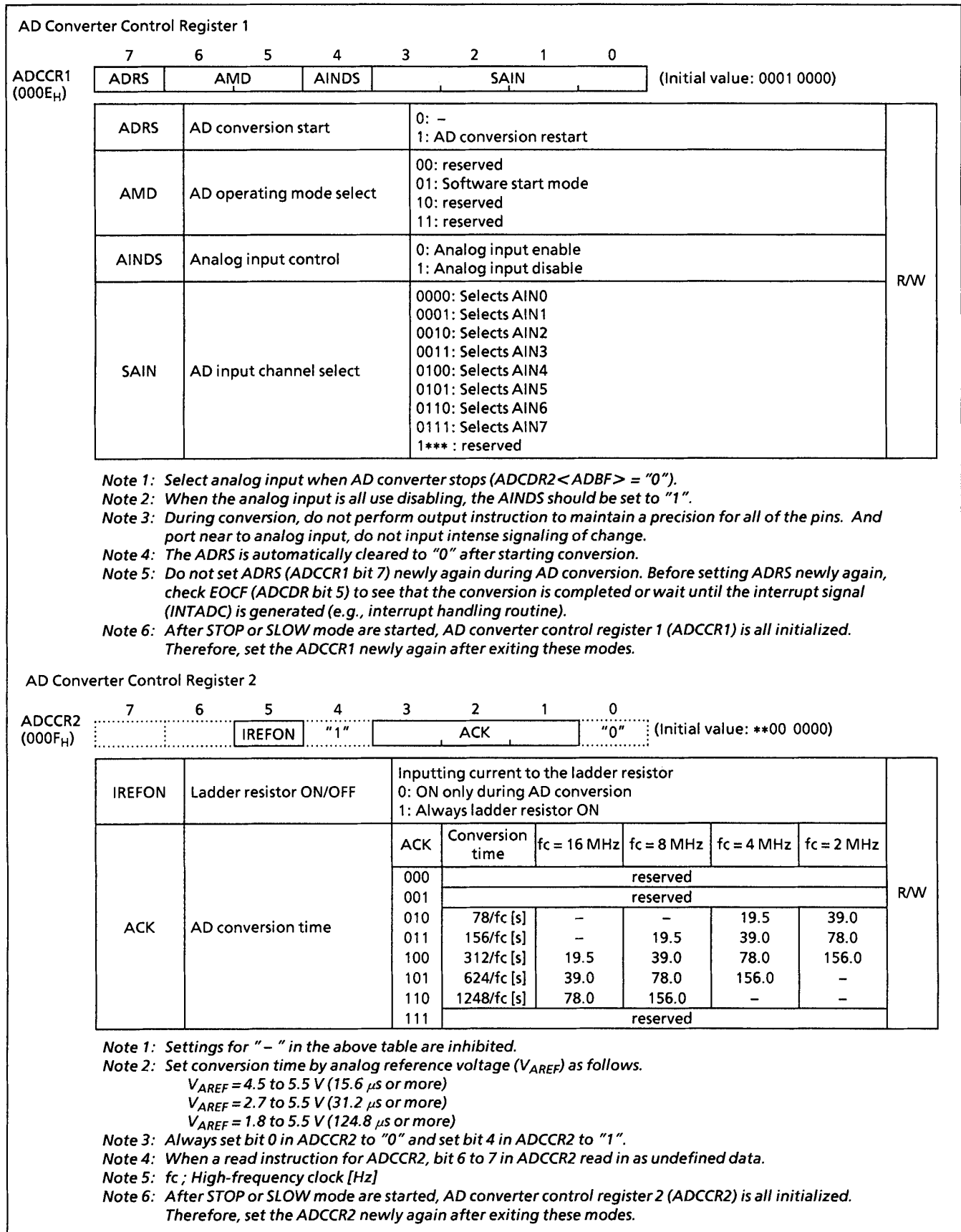


Figure 2-47. AD Converter Control Register

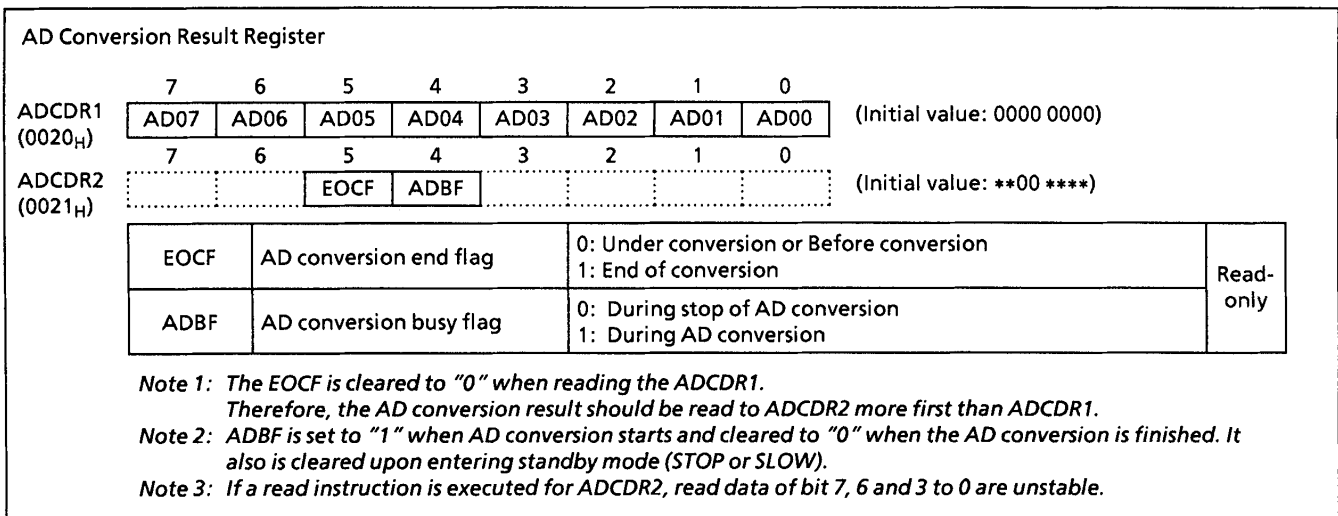


Figure 2-48. AD Converter Result Register

2.9.3 AD Converter Operation

- (1) Set up the AD converter control register 1 (ADCCR1) as follows:
 - Choose the channel to AD convert using AD input channel select (SAIN).
 - Specify analog input enable for analog input control (AINDS).
 - Specify AMD for the AD converter control operation mode (software mode only).
- (2) Set up the AD converter control register 2 (ADCCR2) as follows:
 - Set the AD conversion time using AD conversion time (ACK). For details on how to set the conversion time, refer to Note 2 for AD converter control register 2.
 - Choose IREFON for DA converter control.
- (3) After setting up (1) and (2) above, set AD conversion start (ADRS) of AD converter control register 1 (ADCCR1) to "1". If software start mode has been selected, AD conversion starts immediately.
- (4) After an elapse of the specified AD conversion time, the AD converted value is stored in AD converted value register 1 (ADCDR1) and the AD conversion finished flag (EOCF) of AD converted value register 2 (ADCDR2) is set to "1", upon which time AD conversion interrupt INTADC is generated.
- (5) EOCF is cleared to "0" by a read of the conversion result. However, if reconverted before a register read, although EOCF is cleared the previous conversion result is retained until the next conversion is completed.

2.9.4 AD Converter Operation Modes

(1) Software start mode

After setting AMD (ADCCR1 bits 5, 6) to "01" (software start mode), set ADRS (ADCCR1 bit 7) to "1". AD conversion of the voltage at the analog input pin specified by SAIN (ADCCR1 bits 0-3) is thereby started.

After completion of the AD conversion, the conversion result is stored in AD converted value registers (ADCDR1) and at the same time EOCF (ADCDR2 bit 5) is set to 1, the AD conversion finished interrupt (INTADC) is generated.

ADRS is automatically cleared after AD conversion has started. Do not set ADRS (ADCCR1 bit 7) newly again (restart) during AD conversion. Before setting ADRS newly again, check EOCF (ADCDR bit 5) to see that the conversion is completed or wait until the interrupt signal (INTADC) is generated (e.g., interrupt handling routine).

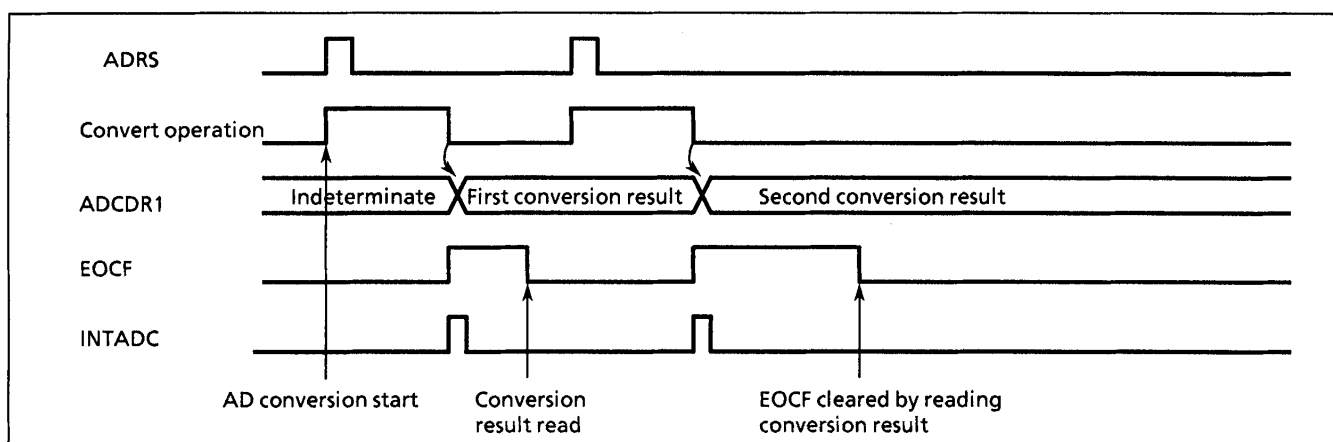


Figure 2-49. Operation in Software Start Mode

2.9.5 STOP and SLOW modes during AD conversion

When standby mode (STOP or SLOW mode) is entered forcibly during AD conversion, the AD convert operation is suspended and the AD converter is initialized (ADCCR1 and ADCCR2 are initialized to initial value). Also, the conversion result is indeterminate. (Conversion results up to the previous operation are cleared, so be sure to read the conversion results before entering standby mode.) When restored from standby mode, AD conversion is not automatically restarted, so it is necessary to restart AD conversion. Note that since the analog reference voltage is automatically disconnected, there is no possibility of current flowing into the analog reference voltage.

2.9.6 Analog Input Voltage and AD Conversion Result

Example: After selecting the conversion time of 19.5 μ s at 16 MHz and the analog input channel AIN4 pin, perform AD conversion once. After checking EOCF, read the converted value and store the 8-bit data in address 009FH on RAM. The operation mode is software start mode.

```

; AIN SELECT
LD (P6DR), 00000000B ; P6DR bit 4 = 0
LD (P6CR), 00000000B ; P6CR bit 4 = 0
LD (ADCCR1), 00100100B ; Select AIN4
LD (ADCCR2), 11011000B ; Select conversion time (312/fc) and operation mode
; AD CONVERT START
SET (ADCCR1). 7 ; ADRS = 1
SLOOP: TEST (ADCCR2). 5 ; EOCF = 1 ?
JRS T, SLOOP
; RESULT DATA READ
LD A, (ADCDR1)
LD (9FH), A
    
```

The analog input voltage is corresponded to the 8-bit digital value converted by the AD as shown in Figure 2-50.

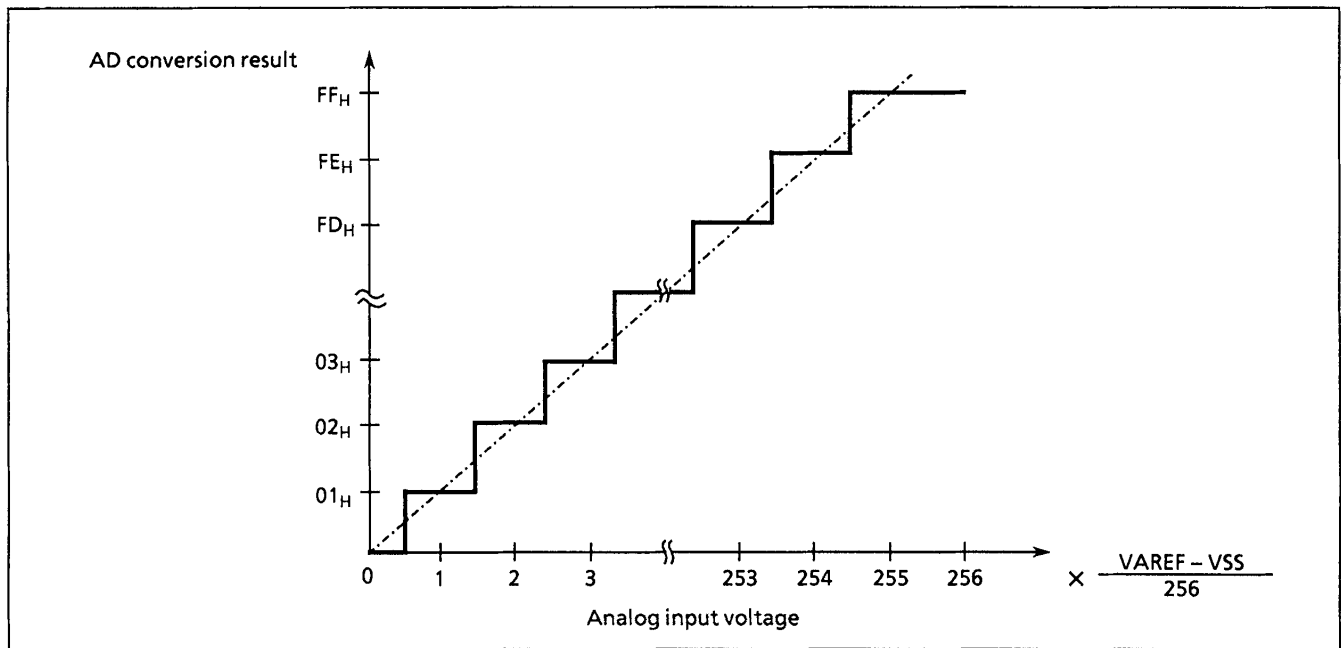


Figure 2-50. Analog Input Voltage and AD Conversion Result (typ.)

2.9.7 Precautions about AD Converter

(1) Analog input pin voltage range

Make sure the analog input pins (AIN0 to AIN7) are used at voltages within VSS below VAREF. If any voltage outside this range is applied to one of the analog input pins, the converted value on that pin becomes uncertain. The other analog input pins also are affected by that.

(2) Analog input shared pins

The analog input pins (AIN0 to AIN7) are shared with input/output ports. When using any of the analog inputs to execute AD conversion, do not execute input/output instructions for all other ports. This is necessary to prevent the accuracy of AD conversion from degrading. Not only these analog input shared pins, some other pins may also be affected by noise arising from input/output to and from adjacent pins.

(3) Noise countermeasure

The internal equivalent circuit of the analog input pins is shown in Figure 2-51. The higher the output impedance of the analog input source, more easily they are susceptible to noise. Therefore, make sure the output impedance of the signal source in your design is 5 k Ω or less. Toshiba also recommends attaching a capacitor external to the chip.

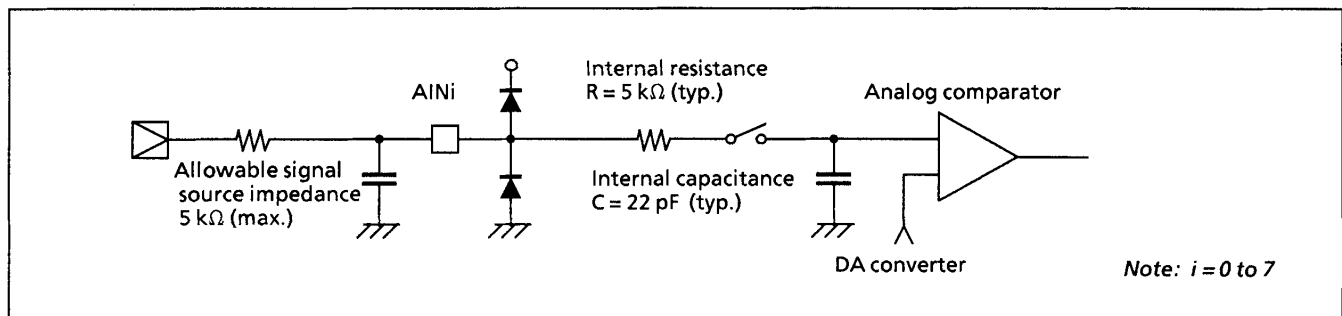


Figure 2-51. Analog Input Equivalent Circuit and Example of Input Pin Processing

2.10 Key-On Wake-Up (KWU)

In the TMP86C420/820, the STOP mode must be released by not only P20 ($\overline{INT5}$ / \overline{STOP}) pin but also P64 to P67 pins.

When the STOP mode is released by P64 to P67 pins, the P20 ($\overline{INT5}$ / \overline{STOP}) pin needs to be used.

2.10.1 Configuration

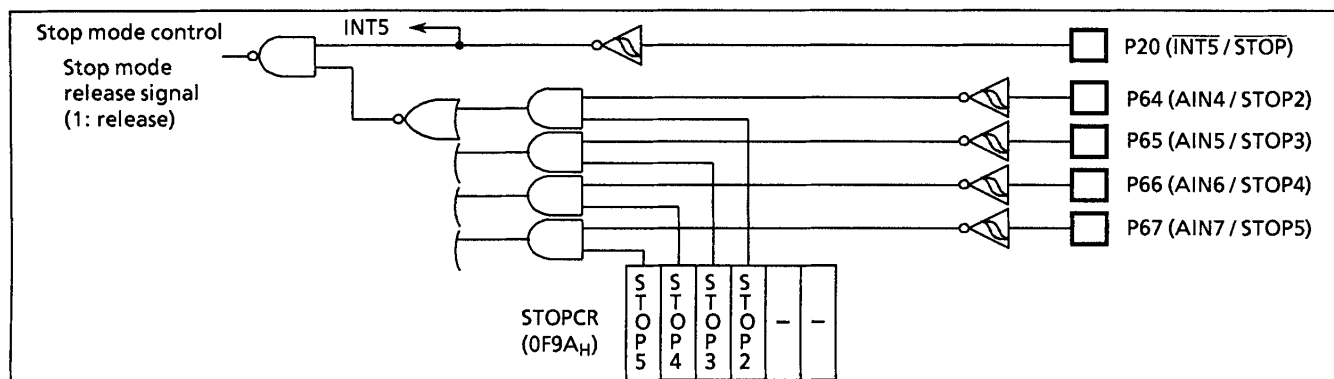


Figure 2-52. Stop Mode Control Circuit

Note: \overline{STOP} pin doesn't have the control register such as STOPCR, so when STOP mode is released by STOPx (x ; 2 to 5), \overline{STOP} pin should be used as STOP function.

2.10.2 Control

P64 to P67 (STOP2 to STOP5) pin can controlled by Key-On Wake-Up control register (STOPCR). It can be configured as enable/disable in one-bit unit. When those pins are used by STOP mode release, those pins must be set input mode (P6CR, P6DR, ADCCR1).

STOP mode can be entered by setting up the System Control Register1 (SYSCR1), and can be exited by detecting the falling edge on STOP2 to 5 pins, which are enabled by STOPCR, for releasing STOP mode (Note 1). Also, because each level of the STOP2 to 5 can be confirmed by reading P6DR, check all STOP2 to 5 pins that is enabled by STOPCR before the STOP mode is started (Note 2).

Note 1: When the STOP mode release by edge mode ($SYSCR1<RELM> = "0"$), prohibit input from STOP2 to STOP5 or must be set "1" level into STOP2 to STOP5 pins.

Note 2: When the \overline{STOP} pin input is high or STOP2 to STOP5 pin input which is enabled by STOPCR is low, executing an instruction which starts STOP mode will not place in STOP mode but instead will immediately start the release sequence (warm-up).

Key-On Wake-Up control register									
STOPCR (0F9AH)	7	6	5	4	3	2	1	0	
	STOP5	STOP4	STOP3	STOP2	-	-	-	-	(Initial value: 0000 ****)
	STOP2	Stop mode released by P64 port	0: Disable 1: Enable		write-only				
	STOP3	Stop mode released by P65 port	0: Disable 1: Enable						
	STOP4	Stop mode released by P66 port	0: Disable 1: Enable						
	STOP5	Stop mode released by P67 port	0: Disable 1: Enable						

Figure 2-53. Key-On Wake-Up control register

2.11 LCD Driver

The TMP86C420/820 each have a driver and control circuit to directly drive the liquid crystal device (LCD). The pins to be connected to LCD are as follows:

- ① Segment output port 8 pins (SEG7 to SEG0)
- ② Segment output or P1, P5, P7 input / output port 24 pins (SEG31 to SEG8)
- ③ Common output port 4 pins (COM3 to COM0)

In addition, C0, C1, V1, V2, V3 pin are provided for the LCD driver's booster circuit.

The devices that can be directly driven is selectable from LCD of the following drive methods:

- ① 1 / 4 Duty (1 / 3 Bias) LCD Max 128 Segments (8-segment×16 digits)
- ② 1 / 3 Duty (1 / 3 Bias) LCD Max 96 Segments (8-segment×12 digits)
- ③ 1 / 2 Duty (1 / 2 Bias) LCD Max 64 Segments (8-segment× 8 digits)
- ④ Static LCD Max 32 Segments (8-segment× 4 digits)

2.11.1 Configuration

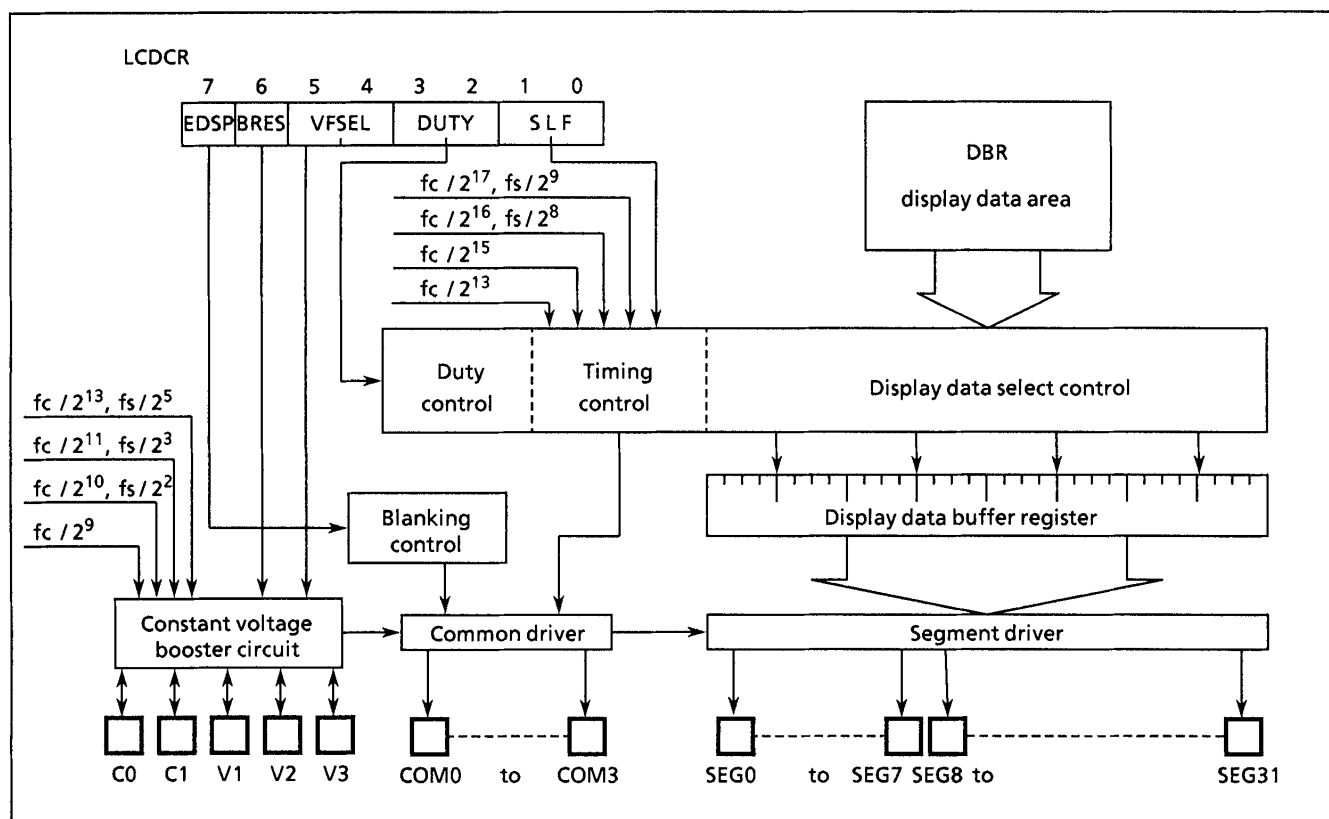


Figure 2-54. LCD Driver

2.11.2 Control

The LCD driver is controlled using the LCD control register (LCDCR). The LCD driver's display is enabled using the EDSP.

		7	6	5	4	3	2	1	0		
LCDCR (0028 _H)		EDSP		BRES		VFSEL		DUTY		SLF	
		(Initial value: 0000 0000)									
SLF	Selection of LCD frame frequency	00: $f_c/2^{17}$ or $f_s/2^9$ [Hz] 01: $f_c/2^{16}$ or $f_s/2^8$ 10: $f_c/2^{15}$ 11: $f_c/2^{13}$									
DUTY	Selection of driving methods	00: 1/4 Duty (1/3 Bias) 01: 1/3 Duty (1/3 Bias) 10: 1/2 Duty (1/2 Bias) 11: Static									
VFSEL	Selection of boost frequency	00: $f_c/2^{13}$ or $f_s/2^5$ [Hz] 01: $f_c/2^{11}$ or $f_s/2^3$ 10: $f_c/2^{10}$ or $f_s/2^2$ 11: $f_c/2^9$									
BRES	Booster circuit control	0: Disable (use divider resistance) 1: Enable									
EDSP	LCD Display Control	0: Blanking 1: Enables LCD display (Blanking is released)									

R/W

Note: When <BRES>(Booster circuit control) is set to "0", $V_{DD} \geq V_3 \geq V_2 \geq V_1 \geq V_{SS}$ should be satisfied. When <BRES> is set to "1", $5.5[V] \geq V_3 \geq V_{DD}$ should be satisfied. If these conditions are not satisfied, it not only affects the quality of LCD display but also may damage the device due to over voltage of the port.

Figure 2-55. LCD Driver Control Register

(1) LCD driving methods

As for LCD driving method, 4 types can be selected by DUTY (bit 3 to bit 2 of LCDCR). The driving method is initialized in the initial program according to the LCD used.

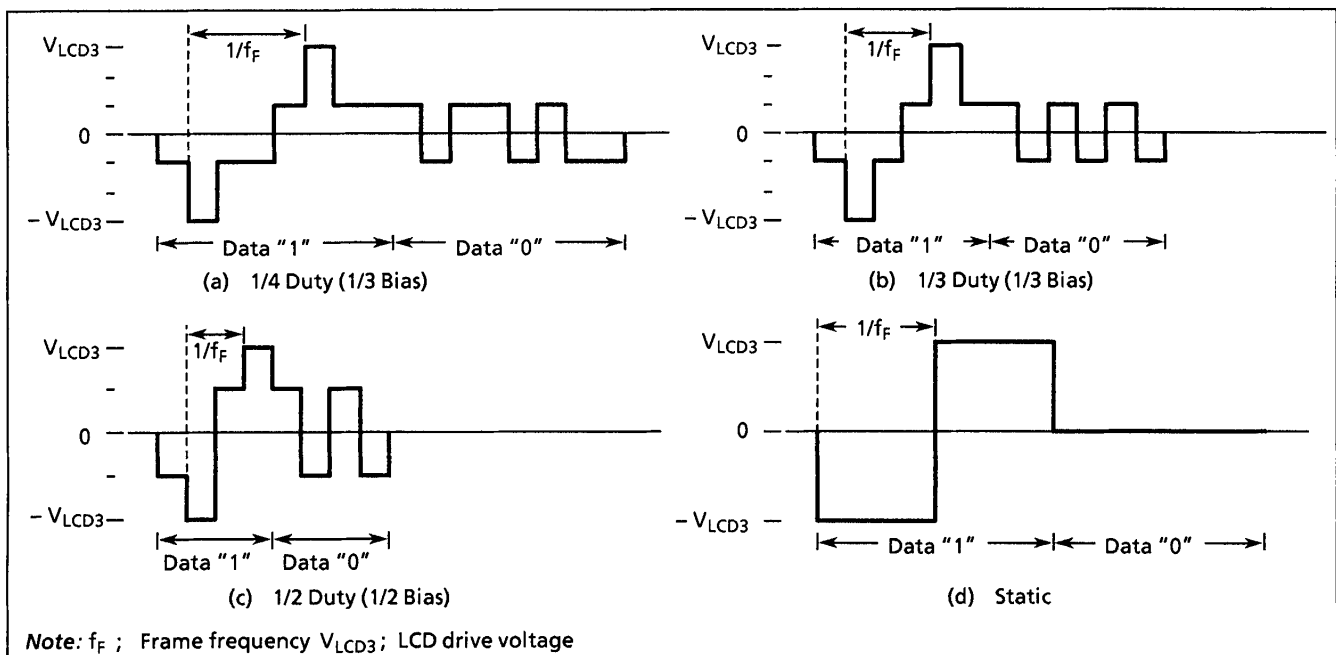


Figure 2-56. LCD Drive Waveform (COM - SEG pins)

(2) Frame frequency

Frame frequency (f_F) is set according to driving method and base frequency as shown in the following Table 2-16. The base frequency is selected by SLF (bit 1 and 0 of LCDCR) according to the frequency f_c and f_s of the basic clock to be used.

Table 2-16. Setting of LCD Frame Frequency

(a) At the single clock mode. At the dual clock mode (DV7CK = 0).

SLF	Base frequency [Hz]	Frame frequency [Hz]			
		1/4 Duty	1/3 Duty	1/2 Duty	Static
00	$\frac{f_c}{2^{17}}$	$\frac{f_c}{2^{17}}$	$\frac{4}{3} \cdot \frac{f_c}{2^{17}}$	$\frac{4}{2} \cdot \frac{f_c}{2^{17}}$	$\frac{f_c}{2^{17}}$
	($f_c = 16$ MHz)	122	163	244	122
	($f_c = 8$ MHz)	61	81	122	61
01	$\frac{f_c}{2^{16}}$	$\frac{f_c}{2^{16}}$	$\frac{4}{3} \cdot \frac{f_c}{2^{16}}$	$\frac{4}{2} \cdot \frac{f_c}{2^{16}}$	$\frac{f_c}{2^{16}}$
	($f_c = 8$ MHz)	122	163	244	122
	($f_c = 4$ MHz)	61	81	122	61
10	$\frac{f_c}{2^{15}}$	$\frac{f_c}{2^{15}}$	$\frac{4}{3} \cdot \frac{f_c}{2^{15}}$	$\frac{4}{2} \cdot \frac{f_c}{2^{15}}$	$\frac{f_c}{2^{15}}$
	($f_c = 4$ MHz)	122	163	244	122
	($f_c = 2$ MHz)	61	81	122	61
11	$\frac{f_c}{2^{13}}$	$\frac{f_c}{2^{13}}$	$\frac{4}{3} \cdot \frac{f_c}{2^{13}}$	$\frac{4}{2} \cdot \frac{f_c}{2^{13}}$	$\frac{f_c}{2^{13}}$
	($f_c = 1$ MHz)	122	163	244	122

Note: f_c ; High-frequency clock [Hz]

(b) At the dual clock mode (DV7CK = 1 or SYSCK = 1)

SLF	Base frequency [Hz]	Frame frequency [Hz]			
		1/4 Duty	1/3 Duty	1/2 Duty	Static
00	$\frac{f_s}{2^9}$	$\frac{f_s}{2^9}$	$\frac{4}{3} \cdot \frac{f_s}{2^9}$	$\frac{4}{2} \cdot \frac{f_s}{2^9}$	$\frac{f_s}{2^9}$
	($f_s = 32.768$ kHz)	64	85	128	64
01	$\frac{f_s}{2^8}$	$\frac{f_s}{2^8}$	$\frac{4}{3} \cdot \frac{f_s}{2^8}$	$\frac{4}{2} \cdot \frac{f_s}{2^8}$	$\frac{f_s}{2^8}$
	($f_s = 32.768$ kHz)	128	171	256	128

Note: f_s ; Low-frequency clock [Hz]

(3) Booster circuit for LCD driver

The LCD voltage booster pin can select the booster circuit or the divider resistance.

The booster circuit control is selected by BRES (bit 6 in LCDCR).

The booster circuit boosts the output voltage for the segment/common signal by double (V2) and triple (V3) in relation to the on-chip output voltage (1 V typ.).

When used as the divider resistance, the V1, V2 and V3 pins are input by divider voltage of external supply.

When used as the booster circuit, the VLCD setting should be composed to 1/3 bias.

The selection of boost frequency is selected by SLFR (bit 1 to 0 in LCDCR).

Selecting the fast frequency using the SLFR in the command register (LCDCR) raises the drive capability of segment/common.

Table 2-17 shows the V3 pin current capacity and Boosting Frequency.

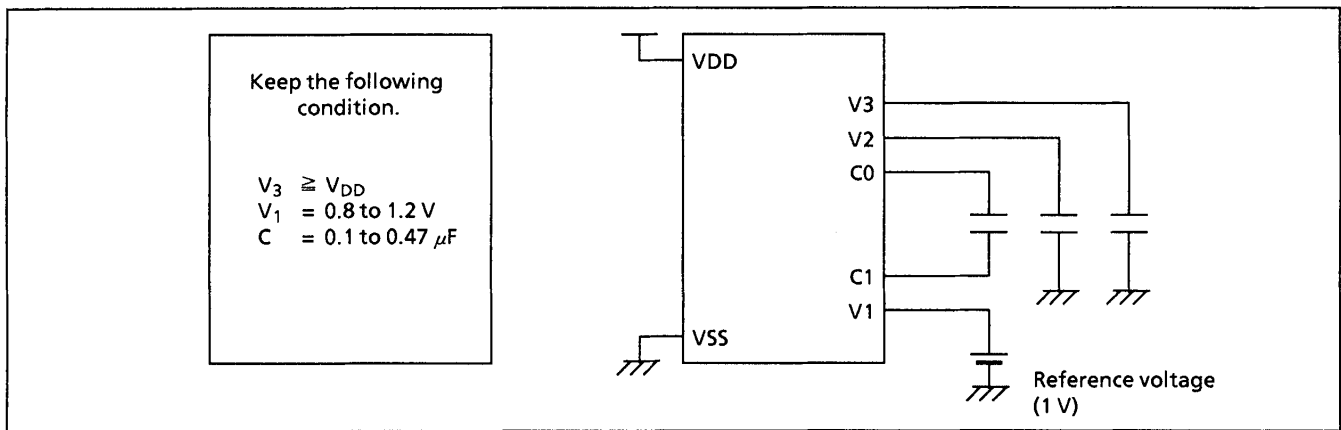


Figure 2-57. Example of a Booster Circuit (LCDCR <BRES> = "1")

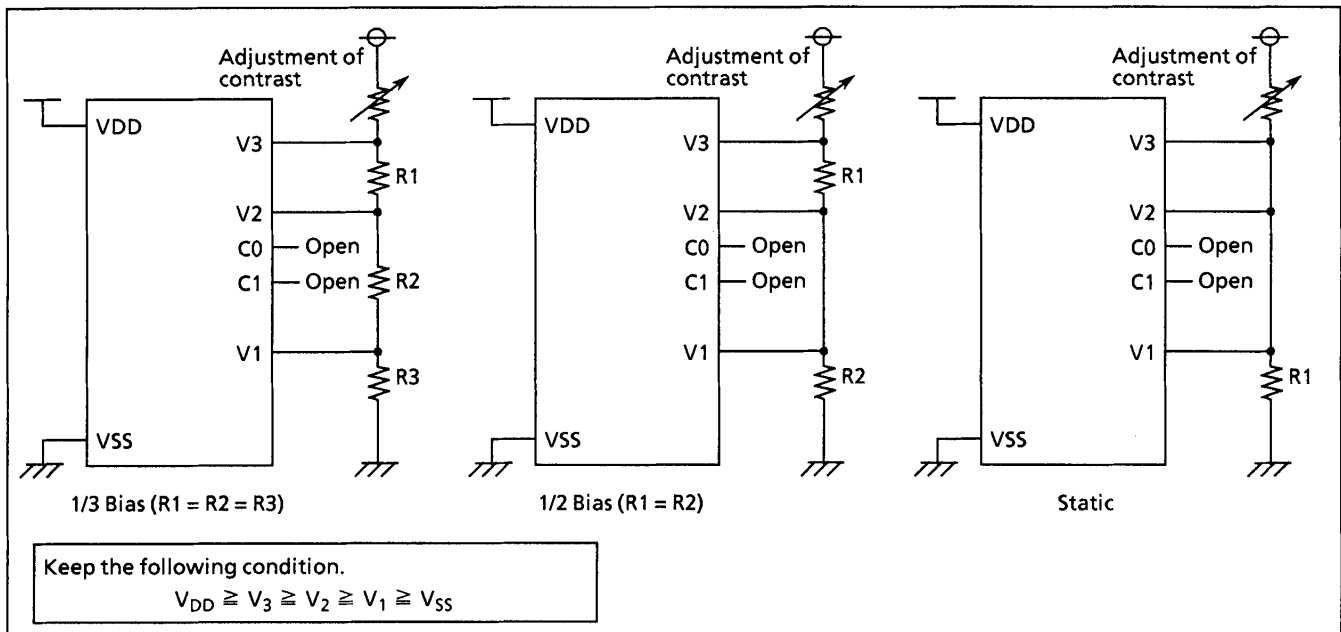


Figure 2-58. Example of Divider Resistance (LCDCR <BRES> = "0")

Table 2-17. V3 Pin Current Capacity and Boosting Frequency (typ.)

VFSEL	Boosting frequency	fc = 16 MHz	fc = 8 MHz	fc = 4 MHz	fs = 32.768 kHz
00	$fc/2^{13}$ or $fs/2^5$	- 37 mV/ μ A	- 80 mV/ μ A	- 138 mV/ μ A	- 76 mV/ μ A
01	$fc/2^{11}$ or $fs/2^3$	- 19 mV/ μ A	- 24 mV/ μ A	- 37 mV/ μ A	- 23 mV/ μ A
10	$fc/2^{10}$ or $fs/2^2$	- 17 mV/ μ A	- 19 mV/ μ A	- 24 mV/ μ A	- 18 mV/ μ A
11	$fc/2^9$	- 16 mV/ μ A	- 17 mV/ μ A	- 19 mV/ μ A	—

Note 1: The current capacity is the amount of voltage that falls per 1 μ A

Note 2: The boosting frequency should be selected depending on your LCD panel.

Note 3: For the reference pin V1, a current capacity ten times larger than the above is recommended to ensure stable operation.

For example, when the boosting frequency is $fc/2^9$ (at $fc = 8$ MHz), - 1.7 mV/ μ A or more is recommended for the current capacity of the reference pin V1.

2.11.3 LCD Display Operation

(1) Display data setting

Display data is stored to the display data area (assigned to address 0F80 to 0F8FH) in the DBR. The display data which are stored in the display data area is automatically read out and sent to the LCD driver by the hardware. The LCD driver generates the segment signal and common signal according to the display data and driving method. Therefore, display patterns can be changed by only over writing the contents of display data area by the program. Figure 2-59 shows the correspondence between the display data area and SEG/COM pins.

LCD light when display data is "1" and turn off when "0". According to the driving method of LCD, the number of pixels which can be driven becomes different, and the number of bits in the display data area which is used to store display data also becomes different.

Therefore, the bits which are not used to store display data as well as the data buffer which corresponds to the addresses not connected to LCD can be used to store general user process data (see Table 2-18.)

Note: The display data memory contents become unstable when the power supply is turned on ; therefore, the display data memory should be initialized by an initiation routine.

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0F80H	SEG1			SEG0				
81	SEG3			SEG2				
82	SEG5			SEG4				
83	SEG7			SEG6				
84	SEG9			SEG8				
85	SEG11			SEG10				
86	SEG13			SEG12				
87	SEG15			SEG14				
88	SEG17			SEG16				
89	SEG19			SEG18				
8A	SEG21			SEG20				
8B	SEG23			SEG22				
8C	SEG25			SEG24				
8D	SEG27			SEG26				
8E	SEG29			SEG28				
8F	SEG31			SEG30				
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Figure 2-59. LCD Display Data Area (DBR)

Table 2-18. Driving Method and Bit for Display Data

Driving methods	Bit 7/3	Bit 6/2	Bit 5/1	Bit 4/0
1 / 4 Duty	COM3	COM2	COM1	COM0
1 / 3 Duty	-	COM2	COM1	COM0
1 / 2 Duty	-	-	COM1	COM0
Static	-	-	-	COM0

Note: - ; This bit is not used for display data

(2) Blanking

Blanking is enabled when EDSP is cleared to "0".

Blanking turns off LCD through outputting a GND level to SEG/COM pin.

When in STOP mode, EDSP is cleared to "0" and automatically blanked. To redisplay LCD after exiting STOP mode, it is necessary to set EDSP back to "1".

Note: During reset, the LCD segment outputs (SEG0 to SEG7) and LCD common outputs are fixed "0" level. But the multiplex terminal (P1, P5 and P7 ports) of input / output port and LCD segment output becomes high impedance. Therefore, when the reset input is long remarkably, ghost problem may appear in LCD display.

2.11.4 Control Method of LCD Driver

(1) Initial setting

Figure 2-60 shows the flowchart of initialization.

Example: To operate a 1/4 duty LCD of 32 segments \times 4 commons at frame frequency $f_c/2^{16}$ [Hz]

```
LD(LCDCR), 0000001B ; Sets LCD driving method and frame frequency.
                    ; Boost frequency
LD(P1LCR), 0FFH    ; Sets P1 port as segment output .
                    ; Sets the initial value of display data.
                    ;
LD(LCDCR), 1000001B ; Display enable
```

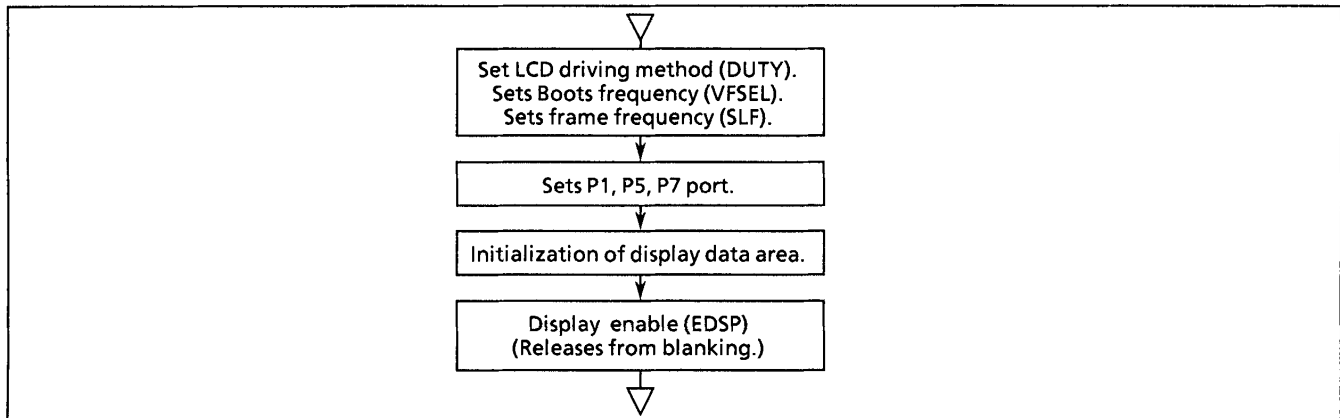


Figure 2-60. Initial Setting of LCD Driver

(2) Store of display data

Generally, display data are prepared as fixed data in program memory and stored in display data area by load command.

Example 1: To display using 1/4 duty LCD a numerical value which corresponds to the LCD data stored in data memory at address 80H (when pins COM and SEG are connected to LCD as in Figure 2-61), display data become as shown in Table 2-19.

```
LD    A, (80H)
ADD   A, TABLE - $ - 7
LD    HL, 0F80H
LD    W, (PC + A)
LD    (HL), W
RET
```

```
TABLE: DB    11011111B, 00000110B,
            11100011B, 10100111B,
            00110110B, 10110101B,
            11110101B, 00010111B,
            11110111B, 10110111B
```

SNEXT:

Note: DB is a byte data definition instruction.

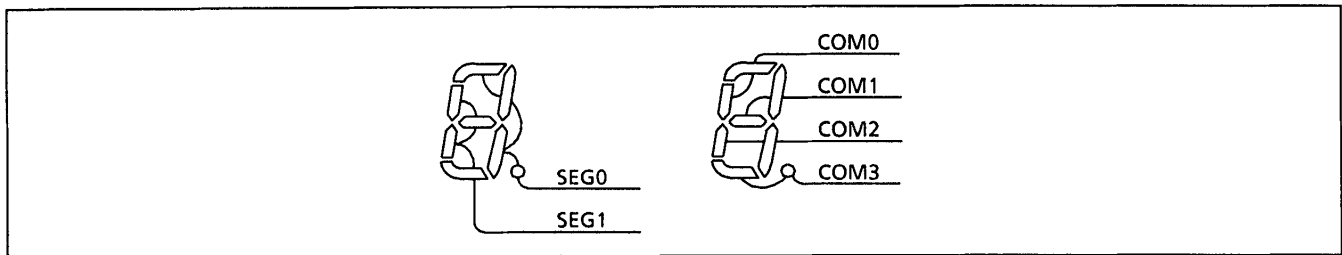


Figure 2-61. Example of COM, SEG Pin Connection (1/4 Duty)

Table 2-19. Example of Display Data (1/4 Duty)

No.	Display	Display data	No.	Display	Display data
0	0.	11011111	5	5	10110101
1	1	00000110	6	6	11110101
2	2	11100011	7	7	00000111
3	3	10100111	8	8	11110111
4	4	00110110	9	9	10110111

Example 2 : Table 2-19 shows an example of display data which are displayed using 1/2 duty LCD in the same way as Table 2-20. The connection between pins COM and SEG are the same as shown in Figure 2-62.

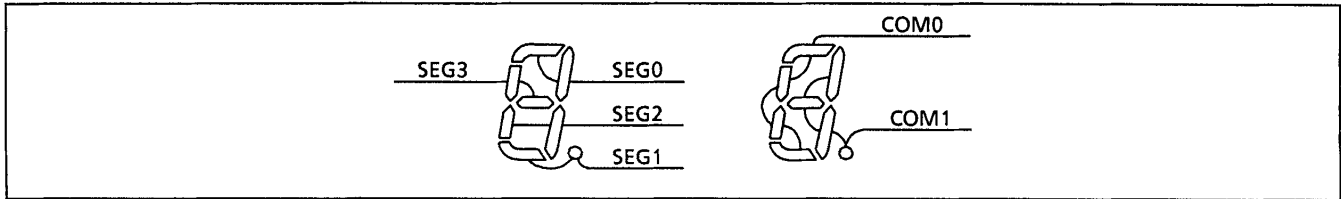


Figure 2-62. Example of COM, SEG Pin Connection

Table 2-20. Example of Display Data (1/2 Duty)

Number	Display data		Number	Display data	
	High order address	Low order address		High order address	Low order address
0	**01**11	**01**11	5	**11**10	**01**01
1	**00**10	**00**10	6	**11**11	**01**01
2	**10**01	**01**11	7	**01**10	**00**11
3	**10**10	**01**11	8	**11**11	**01**11
4	**11**10	**00**10	9	**11**10	**01**11

Note: *; Don't care

(3) Example of LCD drive output

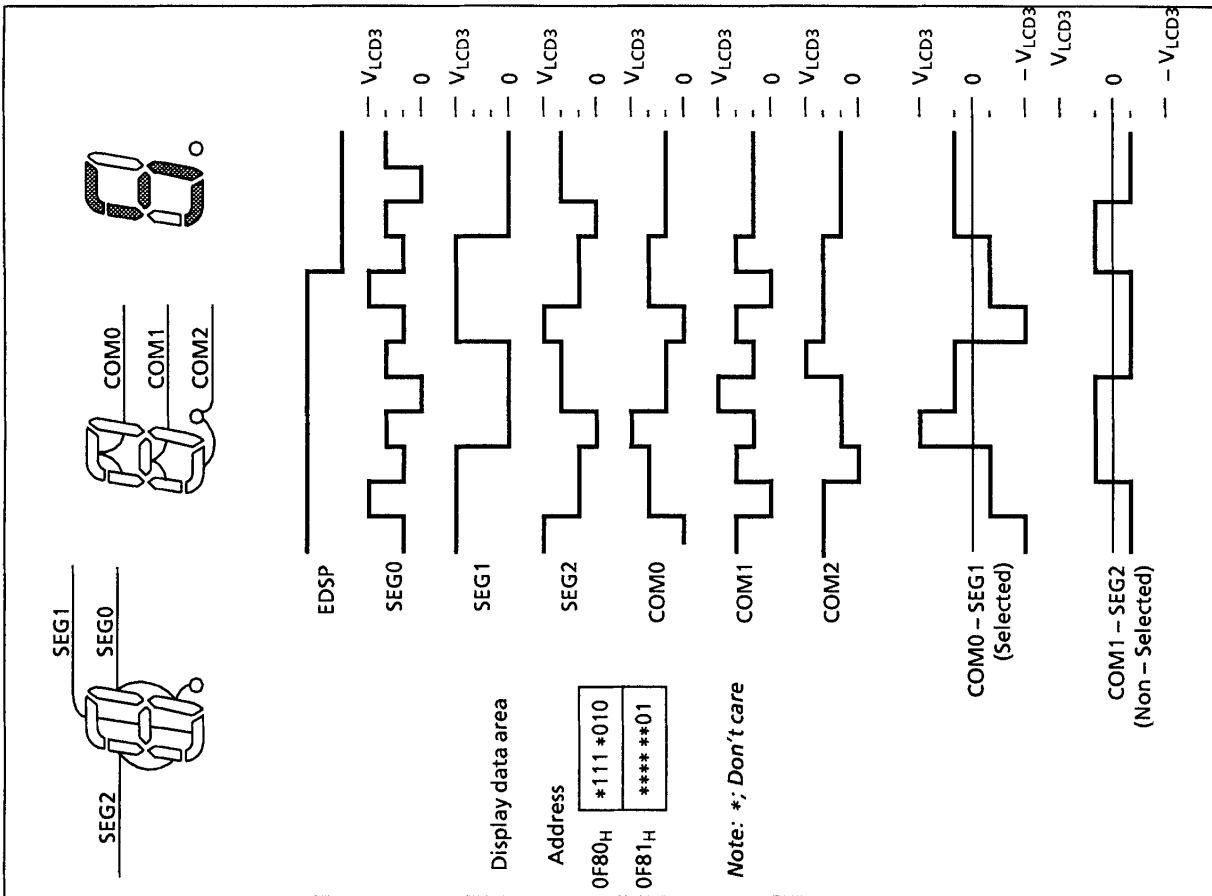


Figure 2-64. 1/3 Duty (1/3 Bias) Drive

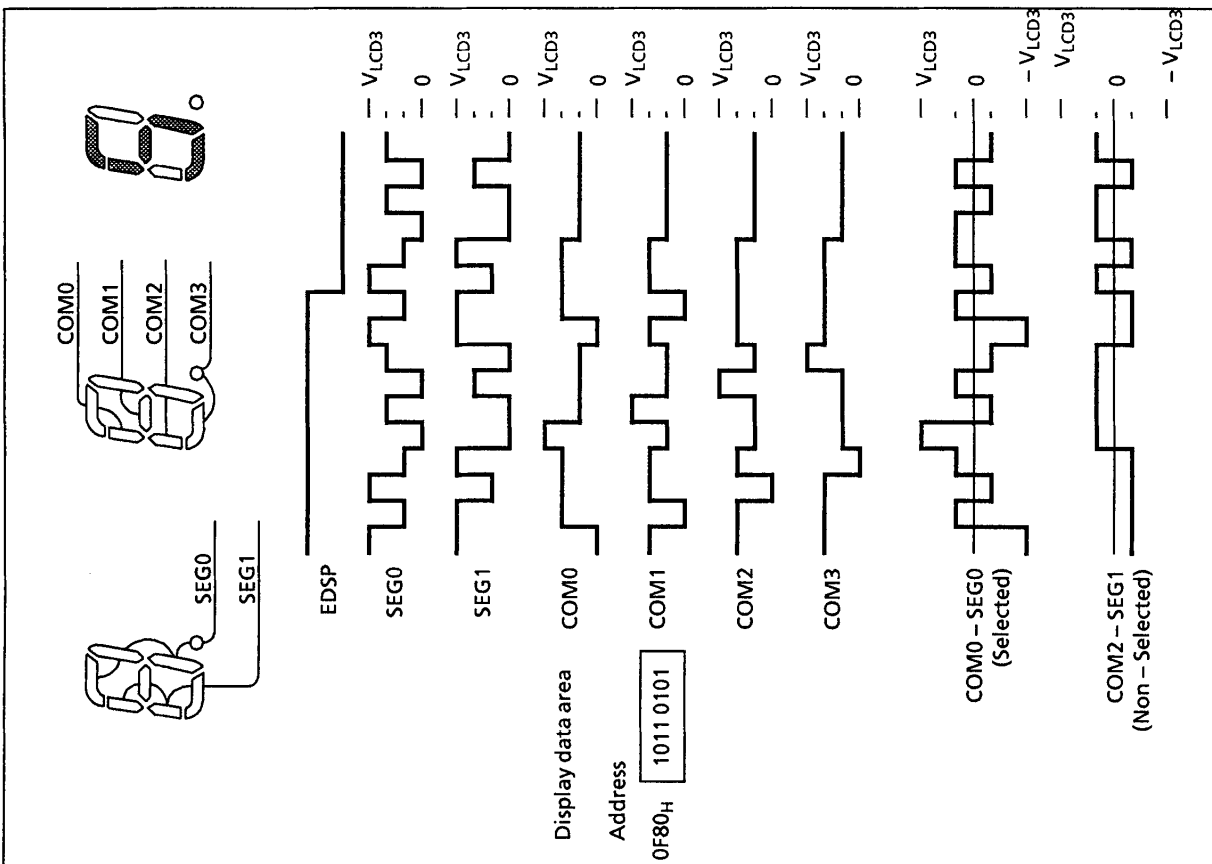


Figure 2-63. 1/4 Duty (1/3 Bias) Drive

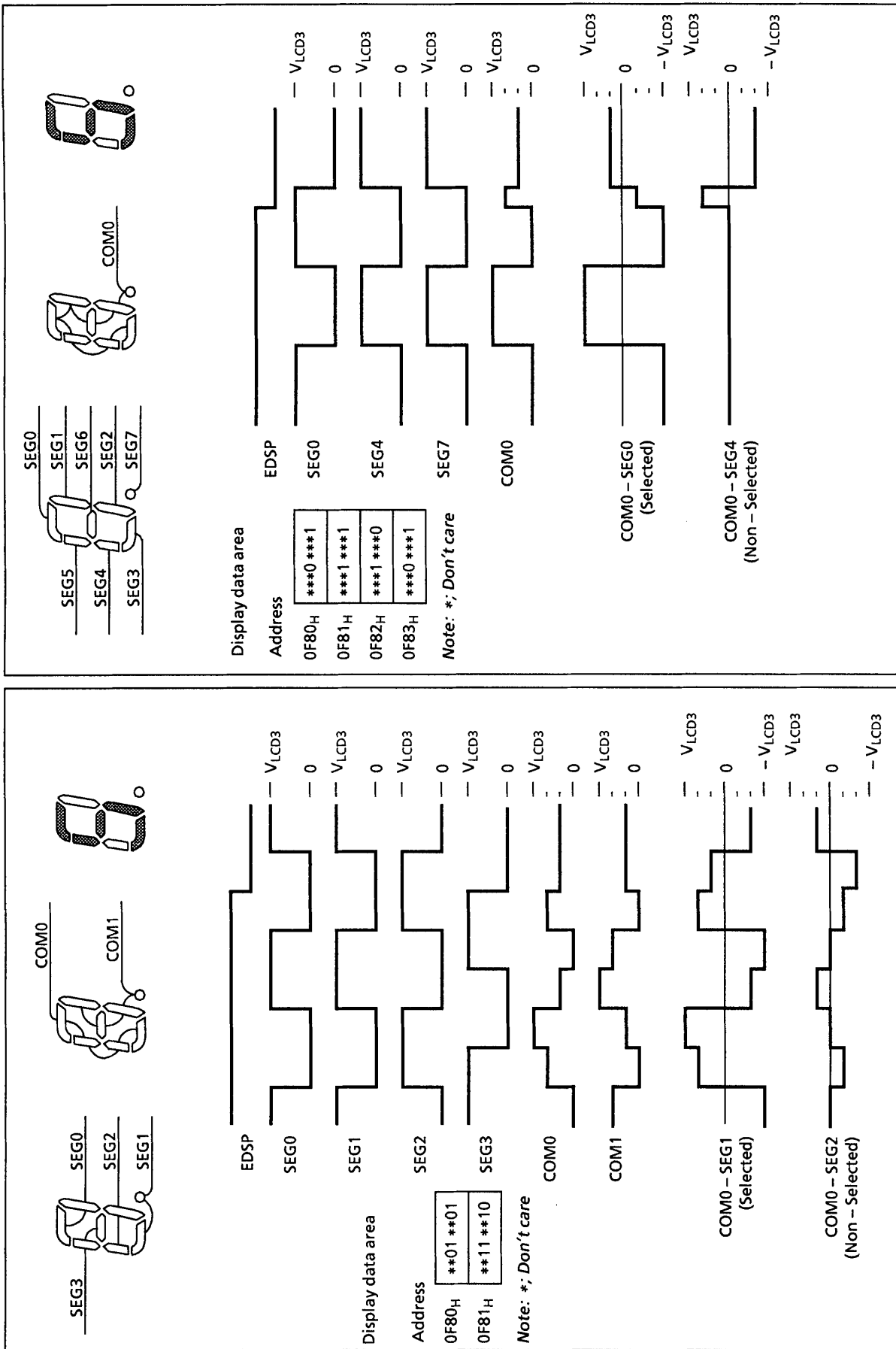


Figure 2-66. Static Drive

Figure 2-65. 1/2 Duty (1/3 Bias) Drive

Input / Output Circuitry

(1) Control Pins

The input/output circuitries of the TMP86C420/820 control pins are shown below.

Control Pin	I/O	Input / Output Circuitry	Remarks
XIN XOUT	Input Output		Resonator connecting pins (high-frequency) $R_f = 1.2\text{ M}\Omega$ (typ.) $R_o = 1.0\text{ k}\Omega$ (typ.)
XTIN XTOUT	Input Output	<p>Normal 1 mode</p> <p>Normal 2 mode</p>	Resonator connecting pins (Low-frequency) $R_f = 6\text{ M}\Omega$ (typ.) $R_o = 220\text{ k}\Omega$ (typ.)
$\overline{\text{RESET}}$	I/O		Sink open drain output Hysteresis input Pull-up resistor $R_{IN} = 220\text{ k}\Omega$ (typ.)
$\overline{\text{STOP}}/\overline{\text{INT5}}$	Input		Hysteresis input
TEST	Input		Pull-down resistor $R_{IN} = 70\text{ k}\Omega$ (typ.)

Note: The TEST pin of the TMP86PM29A does not have a pull-down register. Fix the TEST pin at low-level.

(2) Input / Output Ports

Port	I/O	Input / Output Circuitry	Remarks
P1	I/O	<p>initial "High-Z"</p>	<p>Sink open drain output Hysteresis input</p>
P5 P7	I/O	<p>initial "High-Z"</p>	<p>Sink open drain output</p>
P2	I/O	<p>initial "High-Z"</p>	<p>Sink open drain output Hysteresis input</p>
P3	I/O	<p>initial "High-Z"</p>	<p>Sink open drain or C-MOS output Hysteresis input</p> <p>High current output (Nch) (Programable port option)</p>
P6	I/O	<p>initial "High-Z"</p>	<p>Tri-state I/O Hysteresis input</p>

Note: Port P1, P5 and P7 are sink open drain output. But they are also used as a segment output of LCD. Therefore, absolute maximum ratings of port input voltage should be used in -0.3 to $V_{DD} + 0.3$ volts.

Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V _{DD}		- 0.3 to 6.5	V
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	
Output Voltage	V _{OUT1}		- 0.3 to V _{DD} + 0.3	
Output Current (Per 1 pin)	I _{OUT1}	P3, P6 Port	- 1.8	mA
	I _{OUT2}	P1, P2, P5, P6, P7 Port	3.2	
	I _{OUT3}	P3 Port	30	
Output Current (Total)	ΣI _{OUT1}	P1, P2, P5, P6, P7 Port	60	
	ΣI _{OUT2}	P3 Port	80	
Power Dissipation [T _{opr} = 85°C]	PD		350	
Soldering Temperature (time)	T _{sld}		260 (10 s)	°C
Storage Temperature	T _{stg}		- 55 to 125	
Operating Temperature	T _{opr}		- 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition ($V_{SS} = 0\text{ V}$, $T_{opr} = -40\text{ to }85^{\circ}\text{C}$)

Parameter	Symbol	Pins	Condition	Min	Max	Unit	
Supply Voltage	V_{DD}		$f_c = 16\text{ MHz}$	NORMAL1, 2 mode	4.5	5.5	V
				IDLE0, 1, 2 mode			
			$f_c = 8\text{ MHz}$	NORMAL1, 2 mode	2.7		
				IDLE0, 1, 2 mode			
			$f_c = 4.2\text{ MHz}$	NORMAL1, 2 mode	1.8		
				IDLE0, 1, 2 mode			
$f_s = 32.768\text{ kHz}$	SLOW1, 2 mode	1.8					
	SLEEP0, 1, 2 mode						
			STOP mode				
Input high Level	V_{IH1}	Except Hysteresis input	$V_{DD} \geq 4.5\text{ V}$	$V_{DD} \times 0.70$	V_{DD}	V	
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$			
	V_{IH3}			$V_{DD} < 4.5\text{ V}$			$V_{DD} \times 0.90$
Input low Level	V_{IL1}	Except Hysteresis input	$V_{DD} \geq 4.5\text{ V}$	0	$V_{DD} \times 0.30$	V	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$		
	V_{IL3}				$V_{DD} < 4.5\text{ V}$		$V_{DD} \times 0.10$
Clock Frequency	f_c	XIN, XOUT	$V_{DD} = 1.8\text{ to }5.5\text{ V}$	1.0	4.2	MHz	
			$V_{DD} = 2.7\text{ to }5.5\text{ V}$		8.0		
			$V_{DD} = 4.5\text{ to }5.5\text{ V}$		16.0		
	f_s	XTIN, XTOUT		30.0	34.0	kHz	

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics ($V_{SS} = 0\text{ V}$, $T_{opr} = -40\text{ to }85^{\circ}\text{C}$)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	$V_{DD} = 5.5\text{ V}$, $V_{IN} = 5.5\text{ V} / 0\text{ V}$	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-state					
	I_{IN3}	$\overline{\text{RESET}}$, $\overline{\text{STOP}}$					
Input Resistance	R_{IN1}	TEST Pull-Down		–	70	–	k Ω
	R_{IN2}	$\overline{\text{RESET}}$ Pull-Up		100	220	450	
Output Leakage Current	I_{LO}	Sink Open Drain, Tri-state	$V_{DD} = 5.5\text{ V}$, $V_{OUT} = 5.5\text{ V} / 0\text{ V}$	–	–	± 2	μA
Output High Voltage	V_{OH2}	C-MOS, Tri-st Port	$V_{DD} = 4.5\text{ V}$, $I_{OH} = -0.7\text{ mA}$	4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P3 Port	$V_{DD} = 4.5\text{ V}$, $I_{OL} = 1.6\text{ mA}$	–	–	0.4	V
Output Low Current	I_{OL}	High Current Port (P3 Port)	$V_{DD} = 4.5\text{ V}$, $V_{OL} = 1.0\text{ V}$	–	20	–	mA
Supply Current in NORMAL 1, 2 mode	I_{DD}		$V_{DD} = 5.5\text{ V}$ $V_{IN} = 5.3 / 0.2\text{ V}$ $f_c = 16\text{ MHz}$ $f_s = 32.768\text{ kHz}$	–	7.5	9	mA
Supply Current in IDLE 0, 1, 2 mode				–	5.5	6.5	
Supply Current in SLOW 1 mode			μA	$V_{DD} = 3.0\text{ V}$ $V_{IN} = 2.8\text{ V} / 0.2\text{ V}$ $f_s = 32.768\text{ kHz}$ LCD driver is not enable.	–	18	42
Supply Current in SLEEP 1 mode					–	16	25
Supply Current in SLEEP 0 mode					–	12	20
Supply Current in STOP mode					$V_{DD} = 5.5\text{ V}$ $V_{IN} = 5.3\text{ V} / 0.2\text{ V}$	–	0.5

Note 1: Typical values show those at $T_{opr} = 25^{\circ}\text{C}$, $V_{DD} = 5\text{ V}$

Note 2: Input current (I_{IN1} , I_{IN2}); The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.

AD Conversion Characteristics

($V_{SS} = 0.0 \text{ V}$, $4.5 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$, $T_{opr} = -40 \text{ to } 85^\circ\text{C}$)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		$A_{VDD} - 1.5$	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit	A_{VDD}		V_{DD}			V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}		3.0	–	–	V
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 5.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	–	0.6	1.0	mA
Non linearity Error		$V_{DD} = A_{VDD} = 5.0 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $V_{AREF} = 5.0 \text{ V}$	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

($V_{SS} = 0.0 \text{ V}$, $2.7 \text{ V} \leq V_{DD} < 4.5 \text{ V}$, $T_{opr} = -40 \text{ to } 85^\circ\text{C}$)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		$A_{VDD} - 1.5$	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit	A_{VDD}		V_{DD}			V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}		2.5	–	–	V
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 4.5 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	–	0.5	0.8	mA
Non linearity Error		$V_{DD} = A_{VDD} = 2.7 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $V_{AREF} = 2.7 \text{ V}$	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

($V_{SS} = 0.0 \text{ V}$, $2.0 \text{ V} \leq V_{DD} < 2.7 \text{ V}$, $T_{opr} = -40 \text{ to } 85^\circ\text{C}$) Note 5

($V_{SS} = 0.0 \text{ V}$, $1.8 \text{ V} \leq V_{DD} < 2.0 \text{ V}$, $T_{opr} = -10 \text{ to } 85^\circ\text{C}$) Note 5

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		$A_{VDD} - 0.9$	–	A_{VDD}	V
Power Supply Voltage of Analog Control Circuit	A_{VDD}		V_{DD}			V
Analog Reference Voltage Range (Note 4)	ΔV_{AREF}	$1.8 \text{ V} \leq V_{DD} < 2.0 \text{ V}$	1.8	–	–	V
		$2.0 \text{ V} \leq V_{DD} < 2.7 \text{ V}$	2.0	–	–	
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{AREF}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	$V_{DD} = A_{VDD} = V_{AREF} = 2.7 \text{ V}$ $V_{SS} = 0.0 \text{ V}$	–	0.3	0.5	mA
Non linearity Error		$V_{DD} = A_{VDD} = 1.8 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $V_{AREF} = 1.8 \text{ V}$	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to "2.9.2 Register Configuration".

Note 3: Please use input voltage to AIN input Pin in limit of $V_{AREF} - V_{SS}$.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: $\Delta V_{AREF} = V_{AREF} - V_{SS}$

Note 5: When AD is used with $V_{DD} < 2.7 \text{ V}$, the guaranteed temperature range varies with the operating voltage.

AC Characteristics (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	NORMAL 1, 2 mode	0.25	-	4	μs
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	-	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	tw _{cH}	For external clock operation (XIN input) f _c = 16 MHz	-	31.25	-	ns
Low Level Clock Pulse Width	tw _{cL}					
High Level Clock Pulse Width	tw _{cH}	For external clock operation (XTIN input) f _c = 32.768 kHz	-	15.26	-	μs
Low Level Clock Pulse Width	tw _{cL}					

(V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	NORMAL 1, 2 mode	0.5	-	4	μs
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	-	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	tw _{cH}	For external clock operation (XIN input) f _c = 8 MHz	-	62.5	-	ns
Low Level Clock Pulse Width	tw _{cL}					
High Level Clock Pulse Width	tw _{cH}	For external clock operation (XTIN input) f _c = 32.768 kHz	-	15.26	-	μs
Low Level Clock Pulse Width	tw _{cL}					

(V_{SS} = 0 V, V_{DD} = 1.8 to 2.7 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	t _{cy}	NORMAL 1, 2 mode	0.95	-	4	μs
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	-	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	tw _{cH}	For external clock operation (XIN input) f _c = 4.2 MHz	-	119.05	-	ns
Low Level Clock Pulse Width	tw _{cL}					
High Level Clock Pulse Width	tw _{cH}	For external clock operation (XTIN input) f _c = 32.768 kHz	-	15.26	-	μs
Low Level Clock Pulse Width	tw _{cL}					

Timer Counter 1 input (ECIN) Characteristics (V_{SS} = 0 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit	
TC1 input (ECIN input)	t _{TC1}	Frequency measurement mode V _{DD} = 4.5 to 5.5 V	Single edge count	-	-	16	MHz
		Frequency measurement mode V _{DD} = 2.7 to 4.5 V	Single edge count	-	-	8	
		Frequency measurement mode V _{DD} = 1.8 to 2.7 V	Single edge count	-	-	4.2	

Recommended Oscillating Conditions - 1

($V_{SS} = 0\text{ V}$, $V_{DD} = 4.5\text{ to }5.5\text{ V}$, $T_{opr} = -40\text{ to }85^\circ\text{C}$)

PARAMETER	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	16 MHz	MURATA	CSA16.00MXZ040	10 pF	10 pF
		8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF		
		CST4.19MGW	30 pF (built-in)	30 pF (built-in)		
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	SII	VT-200	6 pF	6 pF

Recommended Oscillating Conditions - 2

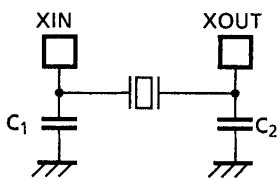
($V_{SS} = 0\text{ V}$, $V_{DD} = 2.7\text{ to }5.5\text{ V}$, $T_{opr} = -40\text{ to }85^\circ\text{C}$)

PARAMETER	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
		CST4.19MGW	30 pF (built-in)	30 pF (built-in)		

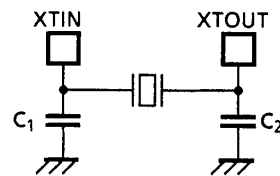
Recommended Oscillating Conditions - 3

($V_{SS} = 0\text{ V}$, $V_{DD} = 1.8\text{ to }5.5\text{ V}$, $T_{opr} = -40\text{ to }85^\circ\text{C}$)

PARAMETER	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant	
					C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

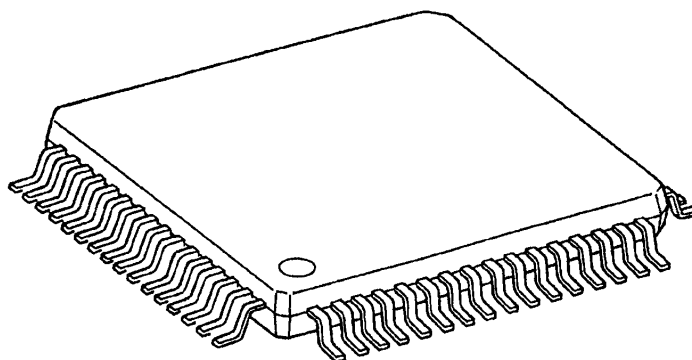
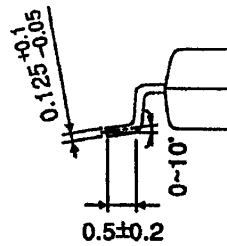
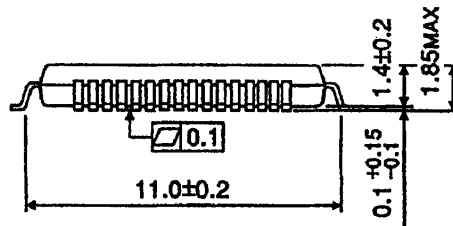
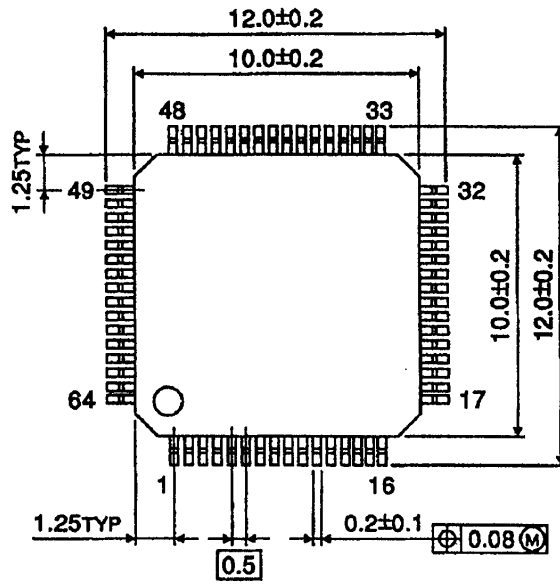
Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

For up-to-date information, please refer to the following URL;

<http://www.murata.co.jp/search/index.html>

P-LQFP64-1010-0.50

Unit: mm



P-QFP64-1414-0.80A

Unit: mm

