

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

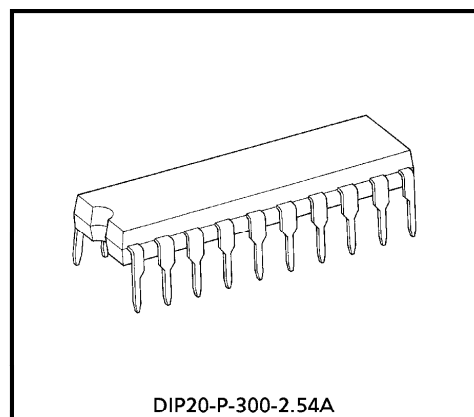
TD62C851P, TD62C852P

8BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER / LATCH DRIVERS

The TD62C851P and TD62C852P are monolithic circuits designed to be used together with Bi-CMOS integrated circuits. The devices consist of a 8bit shift register, 8bit latches, and 8 output circuits (integral clamp diodes for switching inductive loads).

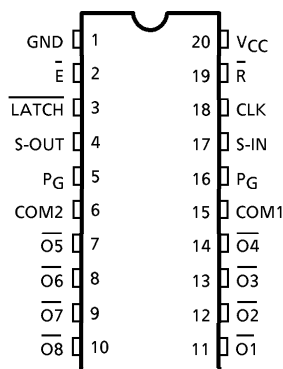
FEATURES

- 8bit serial-in parallel-out shift register / latch driver (Bi-CMOS process)
- Output sustaining voltage ; 50V
- Output current ; TD62C851P 200mA / ch (Low saturation type)
TD62C852P 500mA / ch (darlington type)
- Built-in output clamp diodes
- CMOS compatible inputs
- Package ; DIP20-P-300A



DIP20-P-300-2.54A
Weight : 2.25g (Typ.)

PIN CONNECTION (TOP VIEW)



961001EBA2

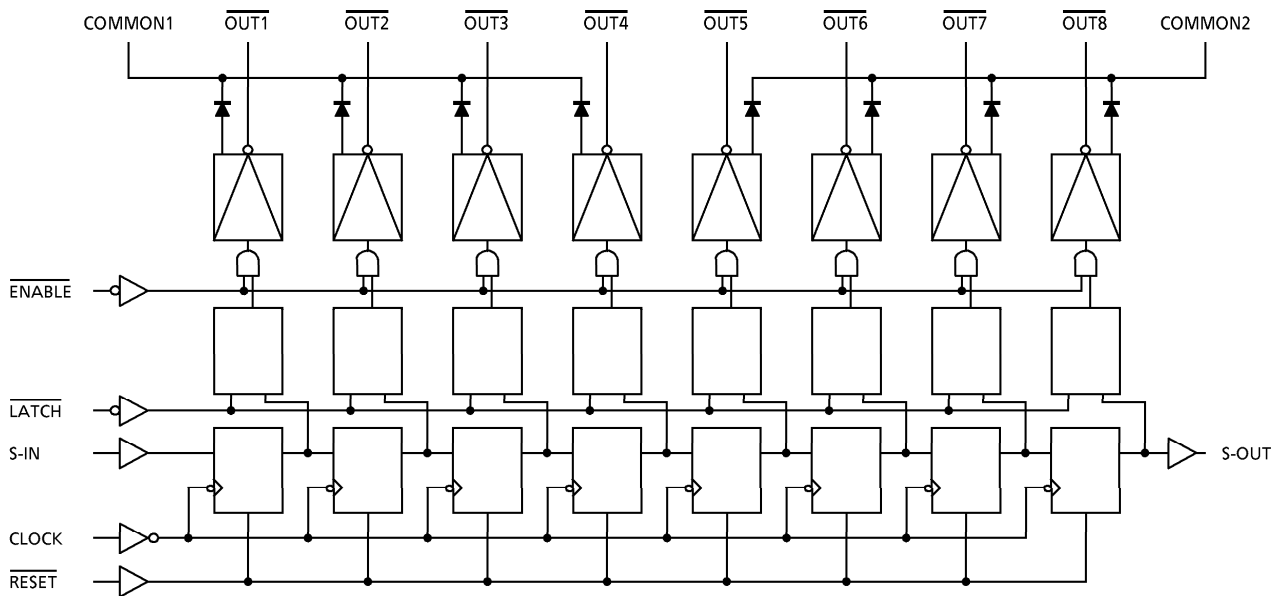
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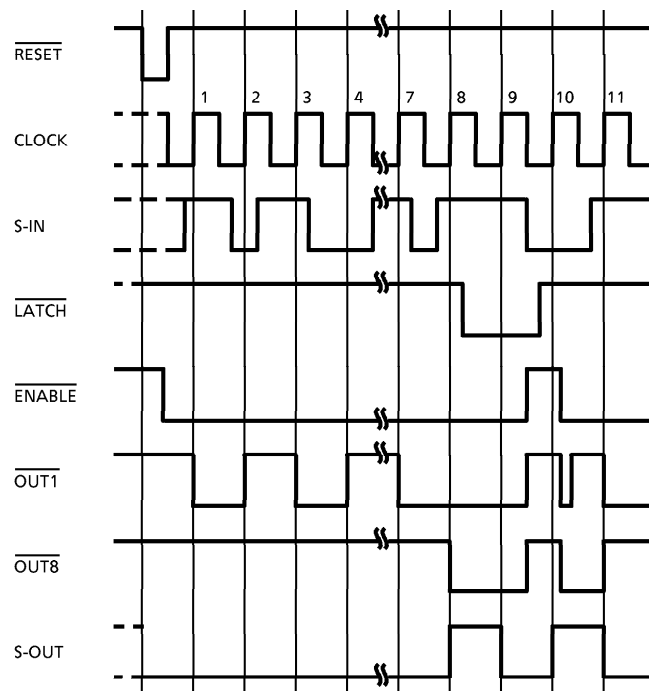
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BLOCK DIAGRAM

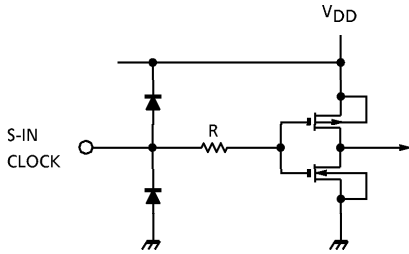


TIMING DIAGRAM

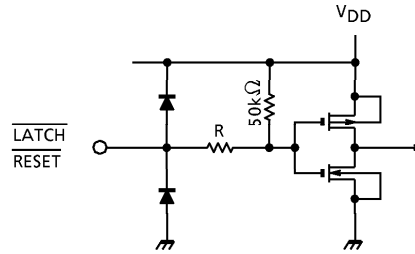


EQUIVALENT OF INPUTS AND OUTPUTS

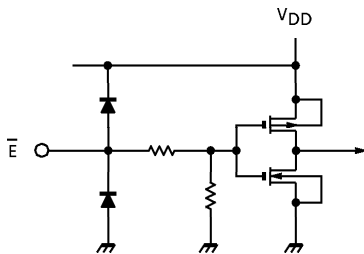
S-IN, clock terminal equivalent circuits



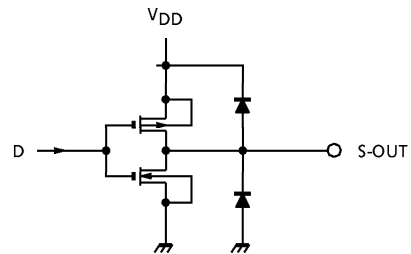
$\overline{\text{LATCH}}$, $\overline{\text{RESET}}$ terminal equivalent circuits



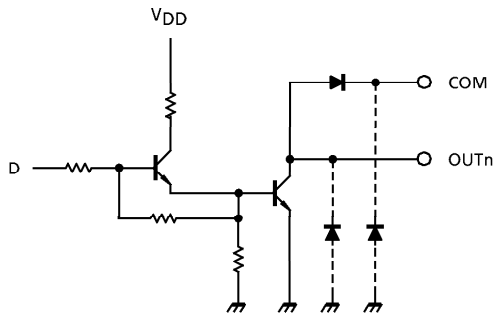
$\overline{\text{ENABLE}}$ terminal equivalent circuits



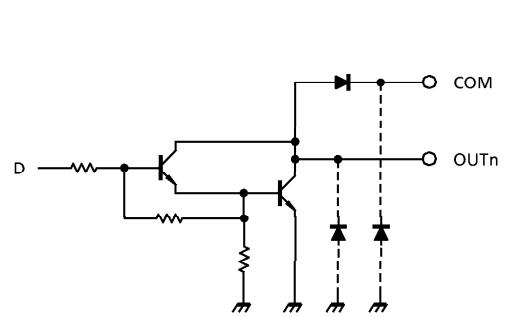
S-OUT terminal equivalent circuits



Output terminal equivalent circuits
(TD62C851P)



Output terminal equivalent circuits
(TD62C852P)



(Note) The output parasitic diode cannot be used as clamp diode.

TRUTH TABLE

CK	\bar{E}	\bar{R}	$\overline{\text{LATCH}}$	S-IN	OUT		S-OUT
					O1	$\overline{O_n-1}$	
	L	H	H	L	OFF	$\overline{O_n-1}$	Q7
	L	H	H	H	ON	$\overline{O_n-1}$	Q7
	L	H	L	(*)	NC	NC	Q7
	H	H	(*)	(*)	OFF	NC	Q7
	(*)	(*)	(*)	(*)	NC	NC	Q7
(*)	(*)	L	H	(*)	OFF	OFF	L
(*)	H		L	(*)	NC	NC	L

CK = CLOCK
 \bar{E} = ENABLE
 \bar{R} = RESET
 $\overline{\text{LATCH}}$ = LATCH
 S-IN = SERIAL IN
 OUT = PARALLEL OUT
 S-OUT = SERIAL OUT

(*) = DON'T CARE
 NC = NO CHANGE
 L = LOW LEVEL
 H = HIGH LEVEL

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	- 0.3~7.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	- 0.5~50	V
Output Current	TD62C851P	200	mA / ch
	TD62C852P	500	
Input Voltage	V_{IN}	~0.4~ $V_{DD} + 0.3$	V
Power Dissipation	P_D	1.47	W
Operating Temperature	T_{opr}	- 40~85	°C
Storage Temperature	T_{stg}	- 55~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -40~85°C)

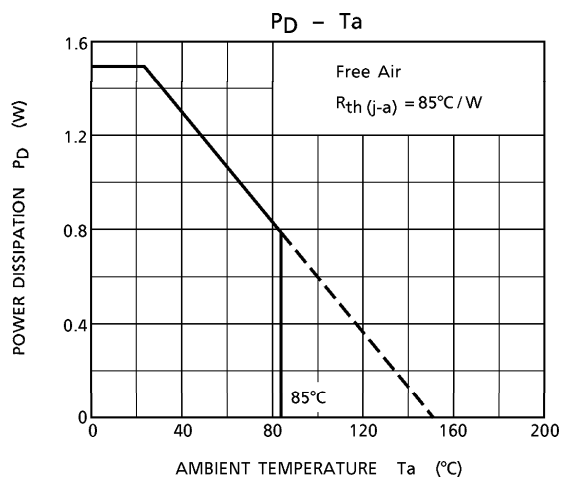
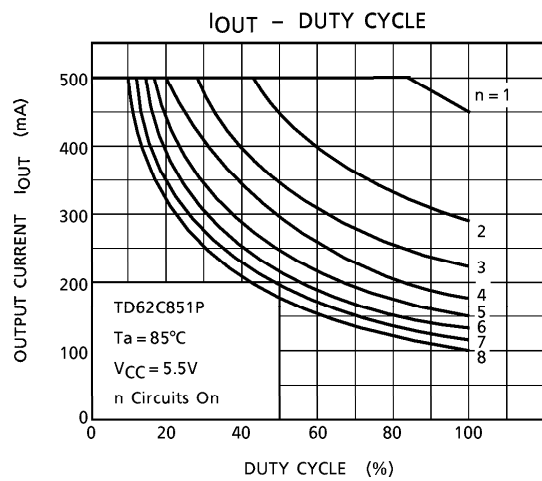
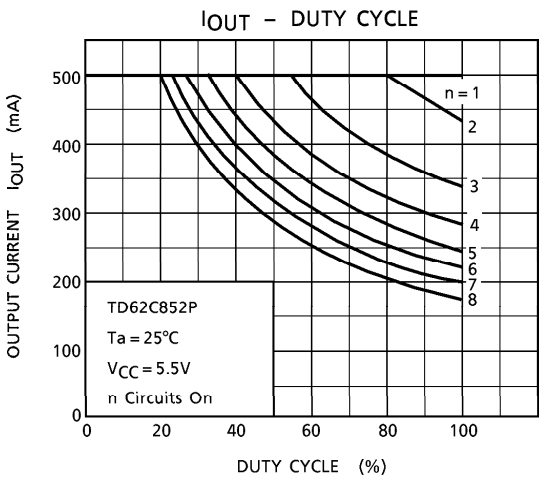
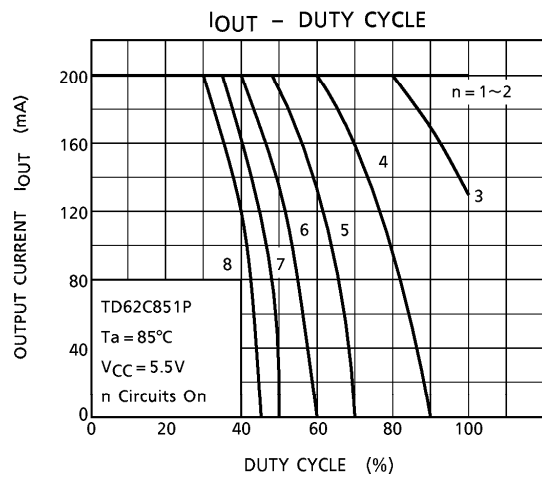
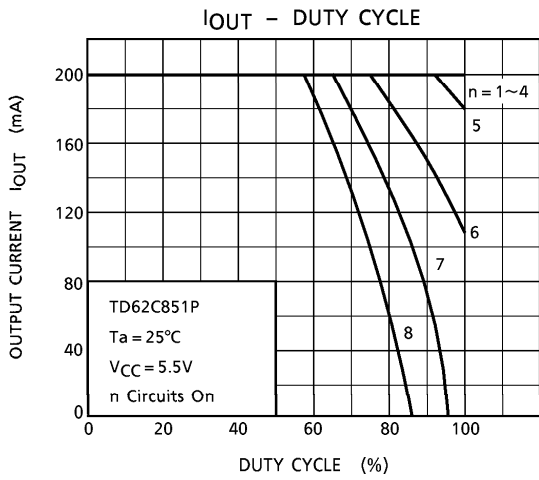
CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage		V_{DD}	—	4.5	5.0	5.5	V	
Input Voltage		V_{IN}	—	0	—	V_{DD}	V	
Output Current ("H" Level)	S-OUT	I_{OH}	Ta = 25°C	—	—	-0.4	mA	
Output Voltage ("L" Level)	$\overline{O_n}$	V_{OH}	—	0	—	50	V	
Output Current ("L" Level)	S-OUT	I_{OL}	—	—	—	0.4	mA / ch	
			DC 1 circuit, Ta = 25°C	0	—	160		
			8 circuit on T _{pw} = 25ms Ta = 85°C V _{DD} = 5.5V	Duty = 10%	0	—		160
				Duty = 40%	0	—		95
			DC 1 circuit, Ta = 25°C	0	—	400		
			8 circuit on T _{pw} = 25ms Ta = 85°C V _{DD} = 5.5V	Duty = 10%	0	—		400
Duty = 50%	0	—		170				
Clock Frequency		f _{CLOCK}	—	1.5	—	—	MHz	
Clock Pulse Width		f _w CLOCK	—	0.33	—	—	μs	
Data Set Up Time		t _{setup}	—	100	—	—	ns	
Data Hold Time		t _{hold}	—	100	—	—	ns	
Clamp Diode Reverse Voltage		V _R	—	0	—	50	V	
Clamp Diode Forward Current	TD62C851P	I _F	—	0	—	160	mA	
	TD62C852P		—	0	—	400		

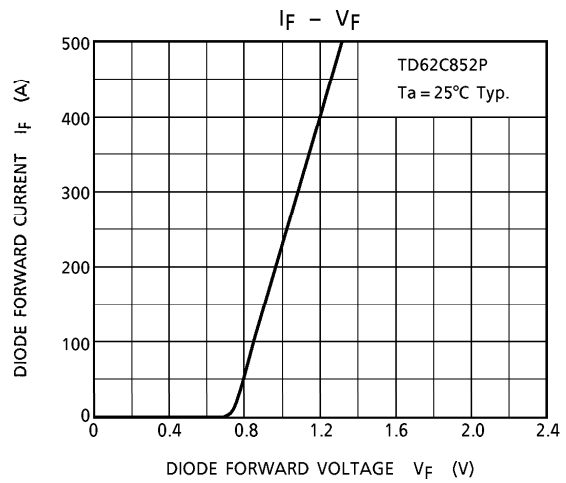
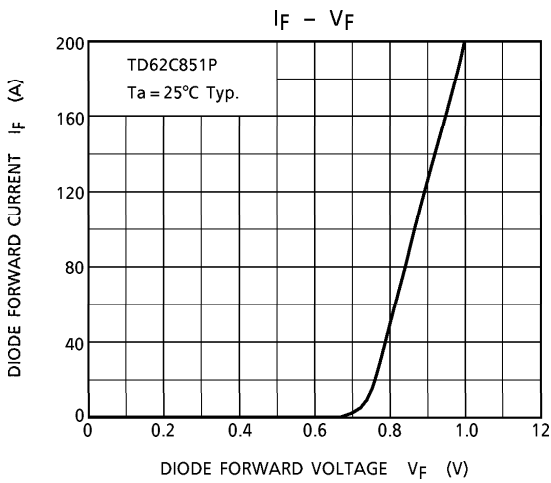
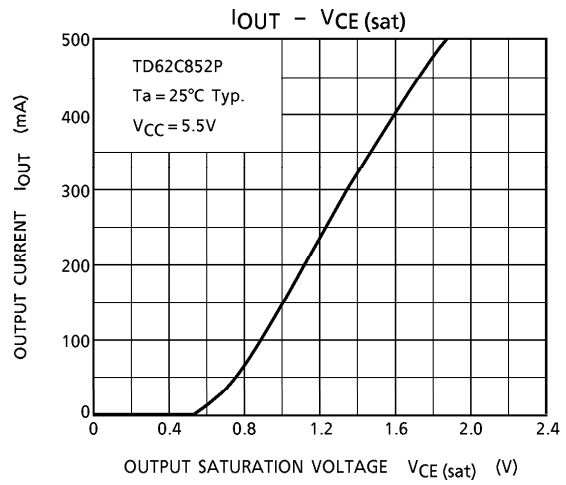
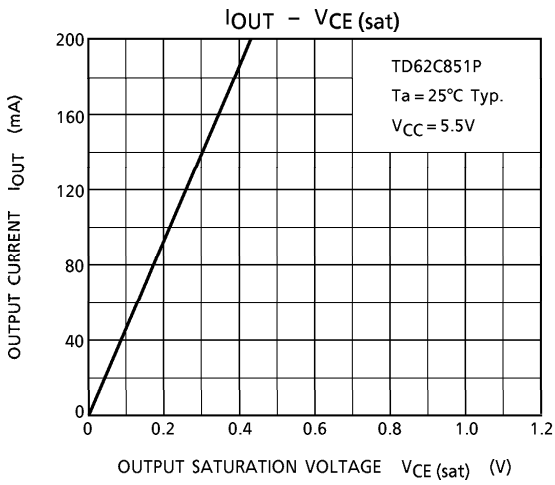
ELECTRICAL CHARACTERISTICS (Ta = -40~85°C)

CHARACTERISTIC		SYM-BOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT			
Input Voltage	"H" Level	V _{IH}	—	—	0.7 V _{DD}	—	—	V			
	"L" Level	V _{IL}	—	—	—	—	0.3 V _{DD}				
Input Current	"H" Level	I _{IH}	—	ENABLE, V _{DD} = 5.5V V _{IH} = V _{DD}	28	55	110	μA			
	"L" Level	I _{IL}	—	LATCH, RESET V _{DD} = 5.5V, V _{IL} = GND	-55	-110	-275				
		I _{IN}	—	CLOCK, S-IN V _{IN} = V _{CC} or GND	—	—	±1.0				
Output Voltage	"H" Level	S-OUT	V _{OH}	—	V _{DD} = 4.5V I _{OH} = -10μA	3.9	4.1	—	V		
	"L" Level	S-OUT	V _{OL}	—	V _{DD} = 4.5V	I _{OL} = 0.8mA	—	0.2	0.4	V	
		On				I _{OL} = 100mA	—	0.29	0.50		
						I _{OL} = 160mA	—	0.39	0.65		
						I _{OL} = 250mA	—	1.24	1.90		
I _{OL} = 400mA	—		1.54	2.30							
Output Current	"H" Level	On	I _{OH}	—	V _{DD} = 5.5V, V _{OH} = 50.0V	—	—	100	μA		
Operating Supply Current			I _{DD1}	—	V _{DD} = 5.5V Ta = 25°C	ENABLE = "H" f _{CLK} = 1MHz Output open DATA = 1 / 2 f _{CLK}	—	130	200	mA	
			I _{DD2}				—	2.0	5.0		
			TD62C851P				I _{DD3}	—	35		40
								TD62C851P	—		1.0
Clamp Diode Reverse Current		I _R	—	V _R = 50V	—	—	50	μA			
Clamp Diode Forward Voltage	TD62C851P	V _F	—	I _F = 160mA	—	1.0	2.0	V			
	TD62C852P			I _F = 400mA	—	1.5	2.0				

SWITCHING CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time	Low-to-High	CK-S-OUT	t _{pLH}	V _{DD} = 5.0V, V _{IH} = 5.0V V _{IL} = 0V, Duty = 50% R _L = { 300Ω (TD62C851P) 120Ω (TD62C852P) }	—	0.40	0.65	μs
		CK-On			—	1.80	3.00	
		L-On			—	2.10	3.50	
		R-On			—	1.50	2.50	
		E-On			—	1.50	2.50	
	High-to-Low	CK-S-OUT	t _{pHL}		—	0.33	0.55	
		CK-On			—	0.41	0.70	
		L-On			—	0.30	0.50	
		R-S-OUT			—	0.25	0.42	
		E-On			—	0.21	0.35	
Maximum Clock Frequency		f _{MAX}	—	1.5	2.0	—	MHz	
Minimum Pulse Width	CLOCK	t _{wCK}	—	—	250	330	ns	
	LATCH	t _{wL}		—	116	160		
	RESET	t _{wR}		—	107	140		
Data Set Up Time		t _{setup}	—	—	30	60	ns	
Data Hold Time		t _{hold}	—	—	14	40		
Maximum Clock Rise Time		t _r	—	—	70	—	ns	
Maximum Clock Fall Time		t _f	—	—	70	—		



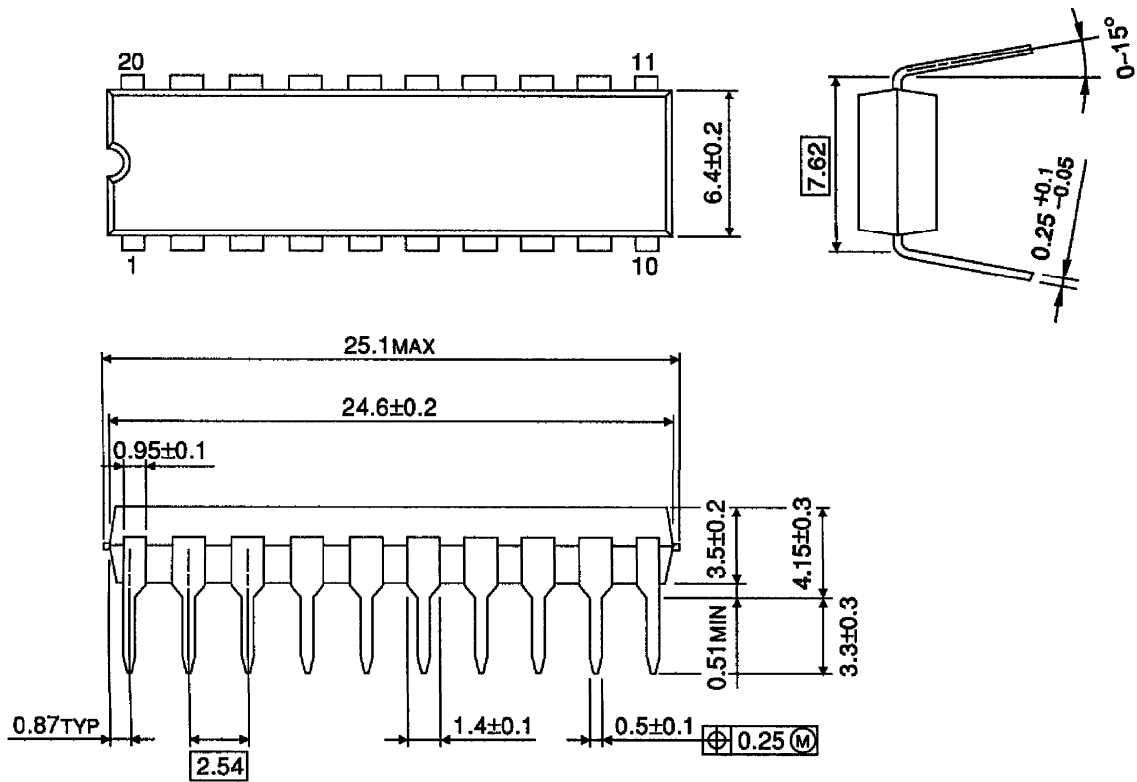


PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING
DIP20-P-300-2.54A

Unit : mm



Weight : 2.25g (Typ.)