MICROPROCESSOR SUPERVISOR
WITH WATCHDOG TIMER

FEATURES

- **Fully Programmable Reset Threshold**
- **Fully Programmable Reset Period**
- **Fully Programmable Watchdog Period**
- **2% Accurate Reset Threshold**
- **Input Voltage Down to 2 V**
- **Input 18-μA Maximum Input Current**
- **Reset Valid Down to 1 V**

DESCRIPTION

The UCCx946 is designed to provide accurate microprocessor supervision, including reset and watchdog functions. During power up, the device asserts a reset signal $\overline{\text{RES}}$ with VDD as low as 1 V. The reset signal remains asserted until the VDD voltage rises and remains above the reset threshold for the reset period. Both reset threshold and reset period are programmable by the user.

The UCCx946 is also resistant to glitches on the VDD line. Once $\overline{\text{RES}}$ has been deasserted, any drops below the threshold voltage need to be of certain time duration and voltage magnitude to generate a reset signal. These values are shown in Figure 1. An I/O line of the microprocessor may be tied to the watchdog input (WDI) for watchdog functions. If the I/O line is not toggled within a set watchdog period, programmable by the user, WDO is asserted. The watchdog function is disabled during reset conditions.

The UCCx946 is available in 8-pin SOIC(D), 8-pin PDIP (N) and 8-pin TSSOP(PW) packages to optimize board space.

UDG–02192

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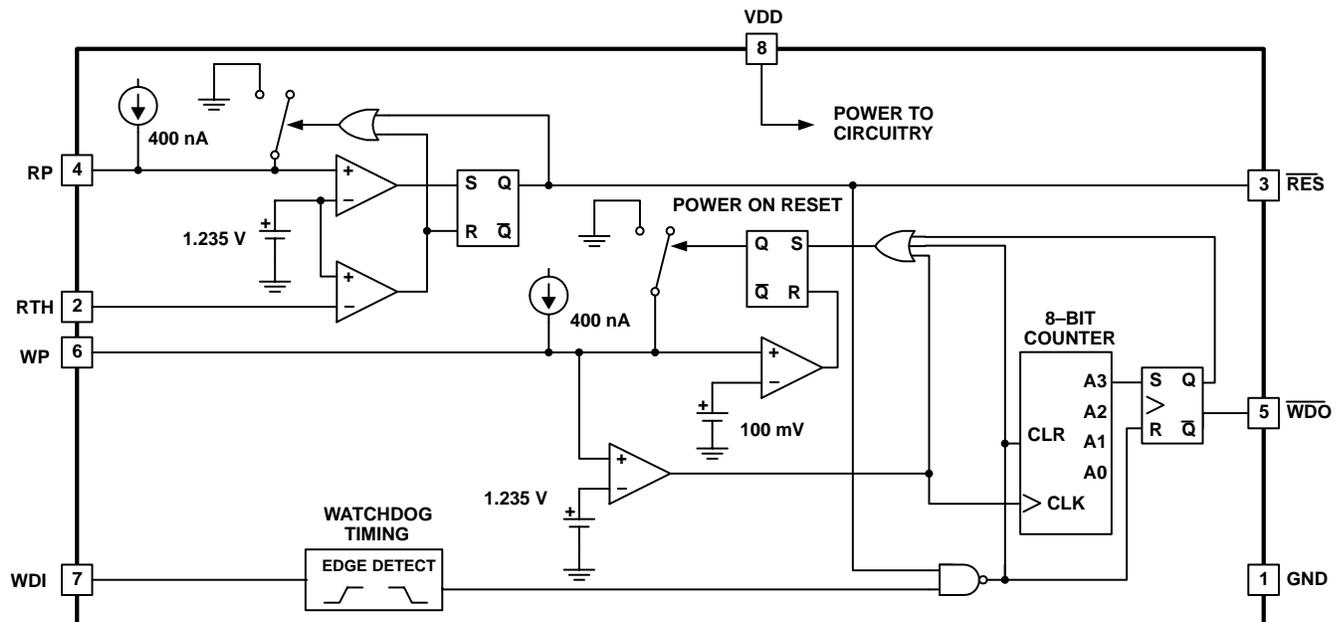
UCC2946
UCC3946

ORDERING INFORMATION

T_A	PACKAGED DEVICES[3]		
	(D)	**(N)**	**(PW)**
−40°C to 95°C	UCC2946D	UCC2946N	UCC2946PW
0°C to 70°C	UCC3946D	UCC3946N	UCC3946PW

[1] The D and PW packages are also available taped and reeled. Add an R suffix to the device type (i.e., UCC2946DR) for quantities of 3,000 devices per reel.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

	UCC2946 UCC3946	**UNIT**
Input voltage range, V_{IN}	10	V
Junction temperature range, T_J	−55 to 150	
Storage temperature, T_{stg}	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300	

[1] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Voltages are with respect to GND. Currents are positive into, and negative out of the specified terminal.

D PACKAGE
(TOP VIEW)

```
GND   [ 1      8 ]  VDD
RTH   [ 2      7 ]  WDI
RES   [ 3      6 ]  WP
RP    [ 4      5 ]  WDO
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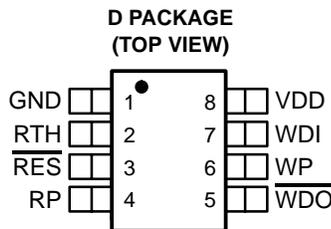
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
GND	1	–	Ground reference for the device
RES	3	O	This pin is high only if the voltage on the RTH has risen above 1.235 V. Once RTH rises above the threshold, this pin remains low for the reset period. This pin asserts low and remains low if the RTH voltage dips below 1.235 V for an amount of time determined by Figure 1.
RTH	2	I	This input compares its voltage to an internal 1.25-V reference. By using external resistors, a user can program any desired reset threshold.
RP	4	I	This pin allows the user to program the reset period by adjusting an external capacitor.
VDD	8	I	Supply voltage for the device.
WDI	7	I	This pin is the input to the watchdog timer. If this pin is not toggled or strobed within the watchdog period, WDO is asserted.
WDO	5	O	This pin is the watchdog output. This pin is asserted low if the WDI pin is not strobed or toggled within the watchdog period.
WP	6	I	This pin allows the user to program the watchdog period by adjusting an external capacitor.

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ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C and 2.0 V ≤ V_{DD} ≤ 5.5 V for the UCC3946, T_A = –40°C to 95°C and 2.1 V ≤ V_{DD} ≤ 5.5 V for the UCC2946, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{DD} Operating voltage	UCC2946		2.1		5.5	V
	UCC3946		2.0		5.5	
I_{DD} Supply current	UCC2946			12	18	µA
	UCC3946			10	18	
$V_{DD(min)}$ Minimum operating voltage[1]	UCC2946				1.1	V
	UCC3946				1.0	
RESET SECTION						
Reset threshold voltage	UCC2946	V_{DD} rising	1.170	1.235	1.260	V
	UCC3946		1.190	1.235	1.260	
Threshold hysteresis				15		mV
I_{LEAK} Input leakage current					5	nA
V_{OH} High-level output voltage		I_{SOURCE} = 2 mA	V_{DD}–0.3			V
V_{OL} Low-level output voltage		I_{SINK} = 2 mA			0.1	
	UCC2946	I_{SINK} = 20 µA, VDD = 1 V			0.4	
	UCC3946				0.2	
VDD-to-output delay time		VDD = –1 mV/µs		120		µs
Reset period	UCC2946	C_{RP} = 64 nF	140	200	320	ms
	UCC3946		160	200	260	
WATCHDOG SECTION						
V_{IH} High-level input voltage, WDI			0.7×V_{DD}			V
V_{IL} Low-level input voltage, WDI					0.3×V_{DD}	
Watchdog period	UCC2946	C_{RP} = 64 nF	0.96	1.60	2.56	s
	UCC3946		1.12	1.60	2.08	
Watchdog pulse width			50			ns
V_{OH} High-level output voltage		I_{SOURCE} = 2 mA	V_{DD}–0.3			V
V_{OL} Low-level output voltage		I_{SINK} = 2 mA			0.1	

(1) Minimum supply voltage where $\overline{RES}$ is considered valid.

APPLICATION INFORMATION

The UCCx946 supervisory circuit provides accurate reset and watchdog functions for a variety of microprocessor applications. The reset circuit prevents the microprocessor from executing code during undervoltage conditions, typically during power-up and power-down. In order to prevent erratic operation in the presence of noise, voltage glitches where voltage amplitude and time duration are less than the values specified in Figure 1 are ignored.

**OVERDRIVE VOLTAGE WITH RESPECT TO
RESET THRESHOLD
vs
DELAY TO OUTPUT LOW ON R$_{ESB}$**
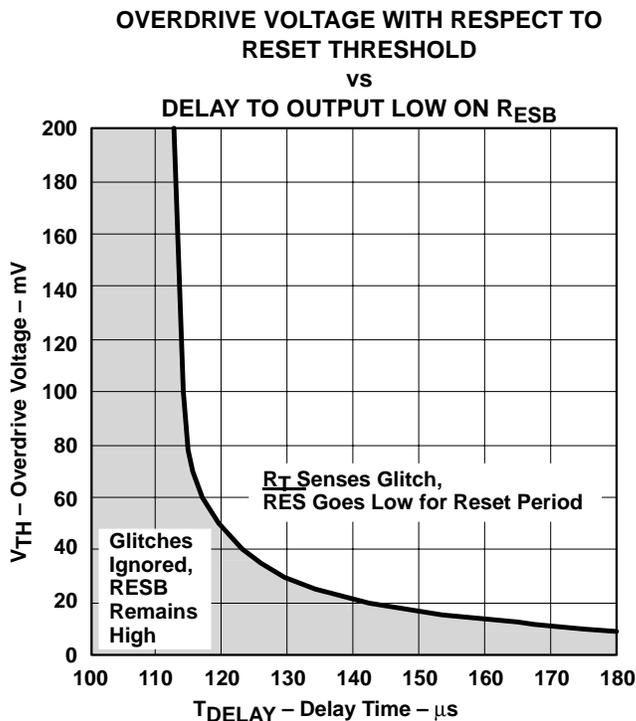
Figure 1.

The watchdog circuit monitors the microprocessor's activity, if the microprocessor does not toggle WDI during the programmable watchdog period $\overline{WDO}$ goes low, alerting the microprocessor's interrupt of a fault. The $\overline{WDO}$ pin is typically connected to the non-maskable input of the microprocessor so that an error recovery routine can be executed.

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APPLICATION INFORMATION

PROGRAMMING THE RESET VOLTAGE AND RESET PERIOD

The UCCx946 allows the reset trip voltage to be programmed with two external resistors. In most applications VDD is monitored by the reset circuit, however, the design allows voltages other than VDD to be monitored. Referring to Figure 2, the voltage below which reset is asserted is determined by:

$$V_{RESET} = 1.235 \times \left(\frac{R1 + R2}{R2} \right)$$

(1)

In order to keep quiescent currents low, resistor values in the megaohm range can be used for R1 and R2. A manual reset can be easily implemented by connecting a momentary push switch in parallel with R2. $\overline{RES}$ is ensured to be low with VDD voltages as low as 1 V.

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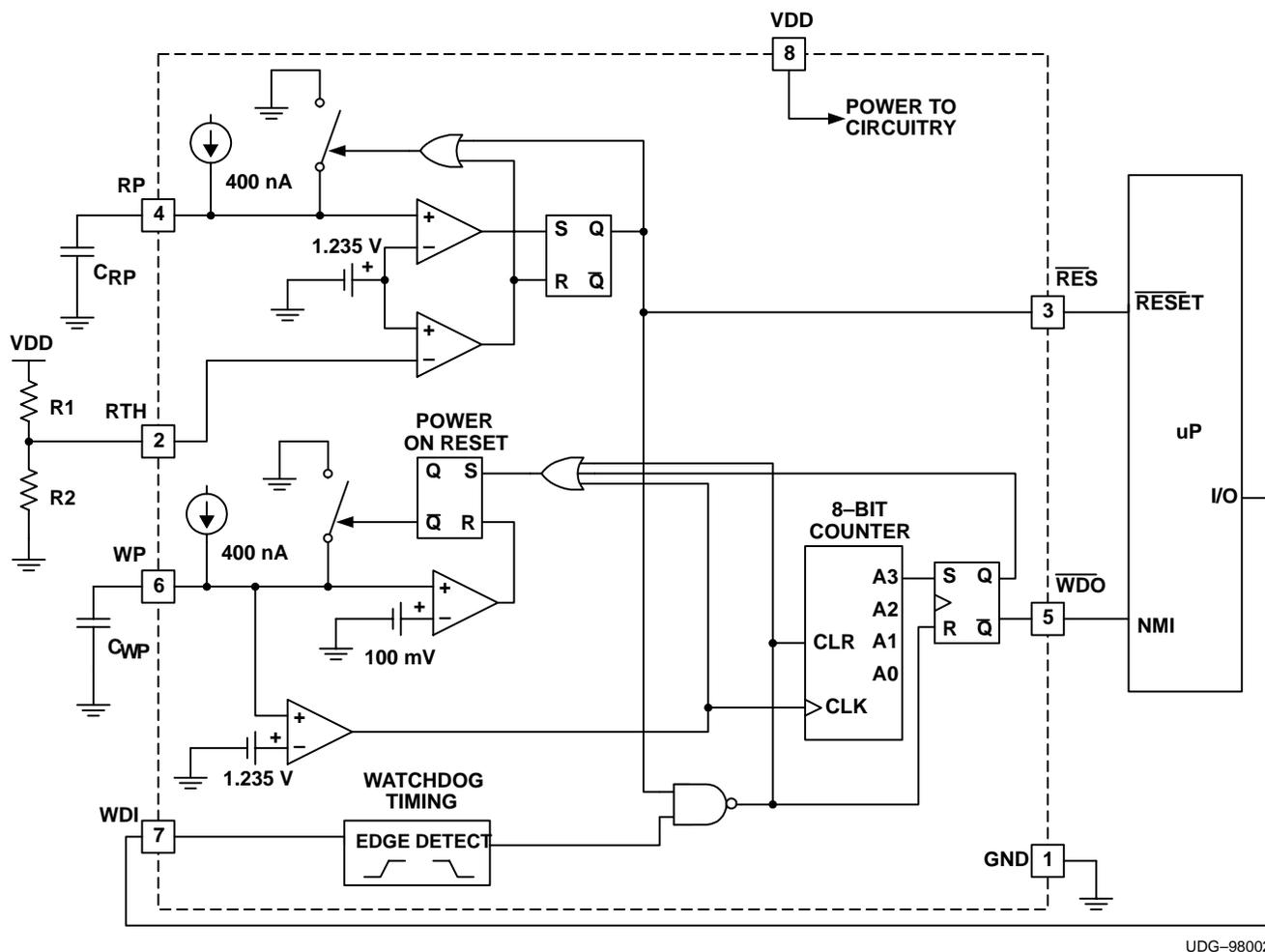
Figure 2. Typical Application Diagram

APPLICATION INFORMATION

Once VDD rises above the programmed threshold, $\overline{\text{RES}}$ remains low for the reset period defined by:

$$T_{RP} = 3.125 \times C_{RP} \tag{2}$$

where T_{RP} is time in milliseconds and C_{RP} is capacitance in nanofarads. C_{RP} is charged with a precision current source of 400 nA, a high-quality, low-leakage capacitor (such as an NPO ceramic) should be used to maintain timing tolerances. Figure 3 illustrates the voltage levels and timings associated with the reset circuit.
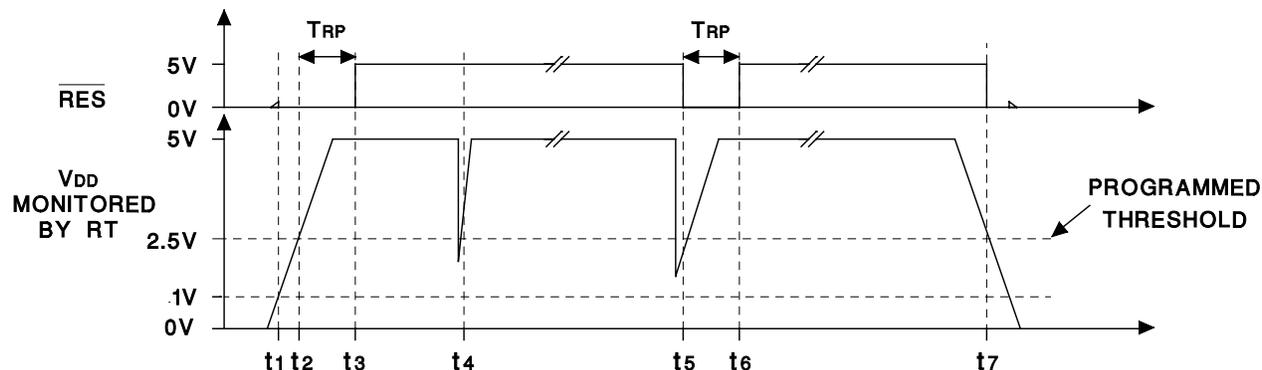
UDG–97067

t1: VDD > 1 V, $\overline{\text{RES}}$ is ensured low.
t2: VDD > programmed threshold, $\overline{\text{RES}}$ remains low for TRP.
t3: T_{RP} expires, $\overline{\text{RES}}$ pulls high.
t4: Voltage glitch occurs, but is filtered at the RTH pin, $\overline{\text{RES}}$ remains high.
t5: Voltage glitch occurs whose magnitude and duration is greater than the RTH filter, $\overline{\text{RES}}$ is asserted for TRP.
t6: On completion of the TRP pulse the RTH voltage has returned and $\overline{\text{RES}}$ is pulled high.
t7: VDD dips below threshold (minus hysteresis), $\overline{\text{RES}}$ is asserted.

Figure 3. Reset Circuit Timings

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APPLICATION INFORMATION

PROGRAMMING THE WATCHDOG PERIOD

The watchdog period is programmed with C_{WP} as follows:

$$T_{WP} = 25 \times C_{WP} \qquad (3)$$

where T_{WP} is in milliseconds and C_{WP} is in nanofarads. A high-quality, low-leakage capacitor should be used for C_{WP}. The watchdog input WDI must be toggled with a high-to-low or low-to-high transition within the watchdog period to prevent $\overline{WDO}$ from assuming a logic level low. $\overline{WDO}$ maintains the low logic level until WDI is toggled or $\overline{RES}$ is asserted. If at any time $\overline{RES}$ is asserted, $\overline{WDO}$ assumes a high logic state and the watchdog period be reinitiated. Figure 4 illustrates the timings associated with the watchdog circuit.
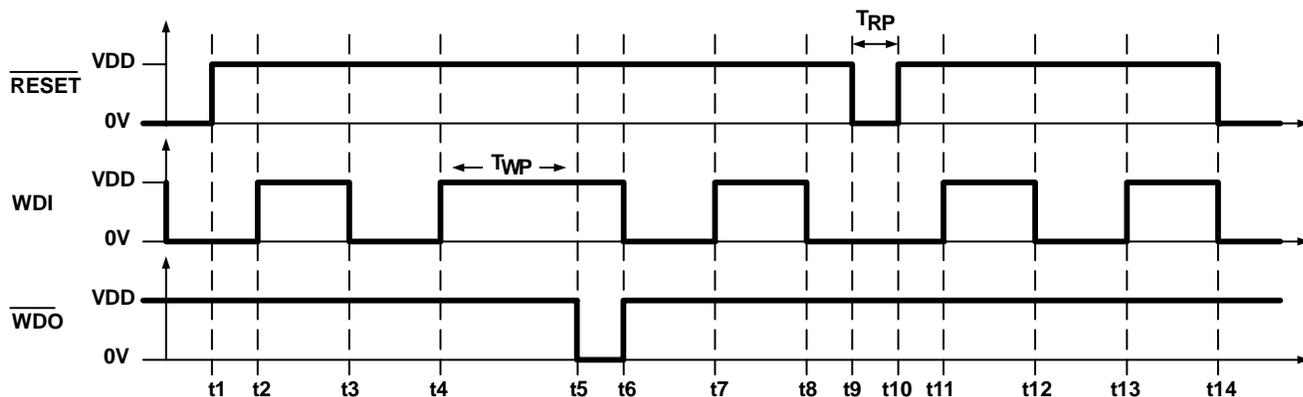
UDG−98007

t1: Microprocessor is reset.
t2: WDI is toggled some time after reset, but before TWP expires.
t3: WDI is toggled before T_{WP} expires.
t4: WDI is toggled before T_{WP} expires.
t5: WDI is not toggled before TWP expires and $\overline{WDO}$ asserts low, triggering the microprocessor to enter an error recovery routine.
t6: The microprocessor's error recovery routine is executed and WDI is toggled, reinitiating the watchdog timer.
t7: WDI is toggled before T_{WP} expires.
t8: WDI is toggled before T_{WP} expires.
t9: $\overline{RES}$ is momentarily triggered, $\overline{RES}$ is asserted low for T$\overline{RP}$.
t10: Microprocessor is reset, $\overline{RES}$ pulls high.
t11: WDI is toggled some time after reset, but before T_{WP} expires.
t12: WDI is toggled before T_{WP} expires.
t13: WDI is toggled before T_{WP} expires.
t14: VDD dips below the reset threshold, $\overline{RES}$ is asserted.

Figure 4. Watchdog Circuit Timings

APPLICATION INFORMATION

CONNECTING $\overline{\text{WDO}}$ TO $\overline{\text{RES}}$

In order to provide design flexibility, the reset and watchdog circuits in the UCCx946 have separate outputs. Each output independently drives high or low, depending on circuit conditions explained previously.

In some applications, it may be desirable for either the $\overline{\text{RES}}$ or $\overline{\text{WDO}}$ to reset the microprocessor. This can be done by connecting $\overline{\text{WDO}}$ to $\overline{\text{RES}}$. If the pins try to drive to different output levels, the low output level dominates. Additional current flows from VDD to GND during these states. If the application cannot support additional current (during fault conditions), $\overline{\text{RES}}$ and $\overline{\text{WDO}}$ can be connected to the inputs of an OR gate whose output is connected to the microprocessor's reset pin.

LAYOUT CONSIDERATIONS

A 0.1-µF capacitor connected from VDD to GND is recommended to decouple the UCCx946 from switching transients on the VDD supply rail.

Since RP and WP are precision current sources, capacitors C_{RP} and C_{WP} should be connected to these pins with minimal trace length to reduce board capacitance. Care should be taken to route any traces with high voltage potential or high speed digital signals away from these capacitors.

Resistors R1 and R2 generally have a high ohmic value, traces associated with these parts should be kept short in order to prevent any transient producing signals from coupling into the high impedance RTH pin.

TYPICAL CHARACTERISTICS

THRESHOLD RESISTANCE vs AMBIENT TEMPERATURE

Figure 5.

INPUT CURRENT vs INPUT VOLTAGE

Figure 6.
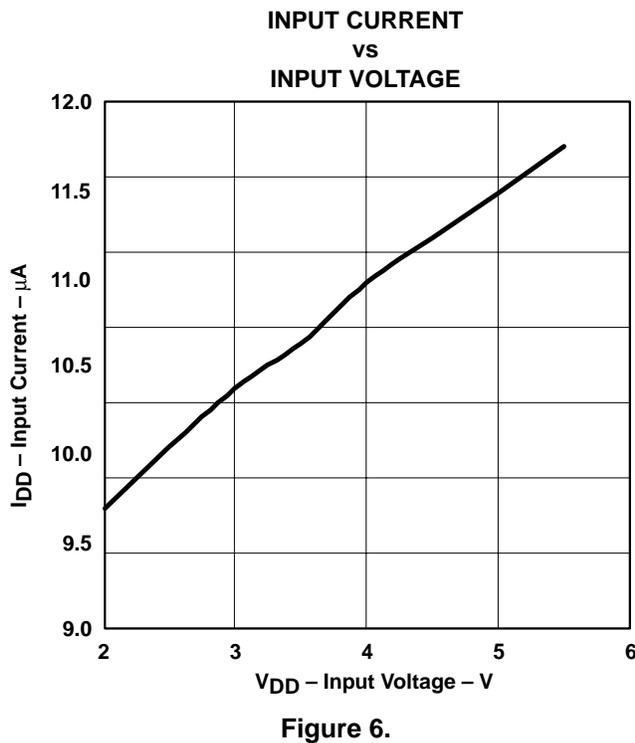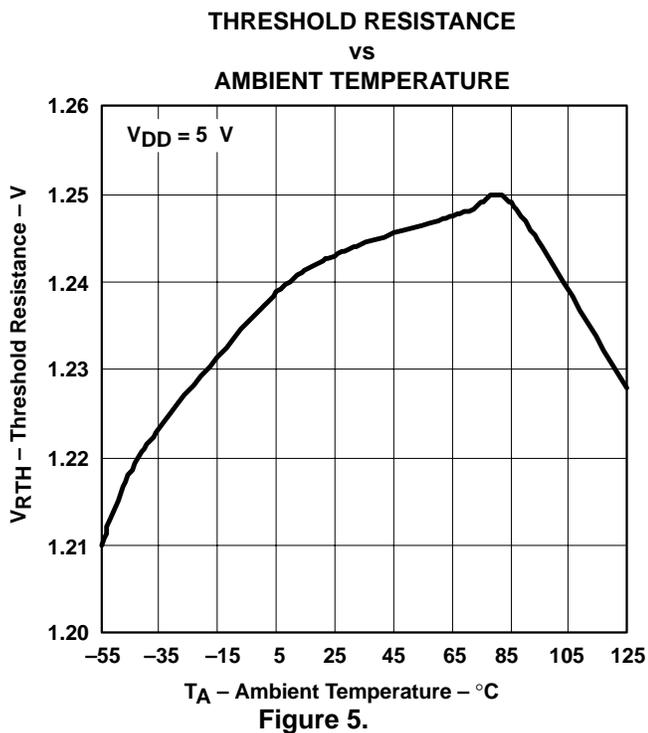
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