

# **Regulating Pulse Width Modulator**

# FEATURES

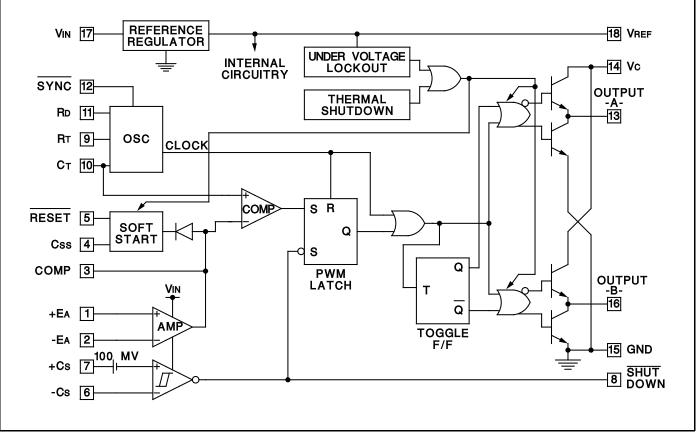
- Reduced Supply Current
- Oscillator Frequency to 600kHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 200mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports
- 5 Volt Operation (VIN = VC = VREF = 5.0V)

# DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non- "A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

Five volt (5V) operation is possible for "logic level" applications by connecting VIN, Vc and VREF to a precision 5V input supply. Consult factory for additional information.



### **BLOCK DIAGRAM**

# ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Note 1: Values beyond which damage may occur.

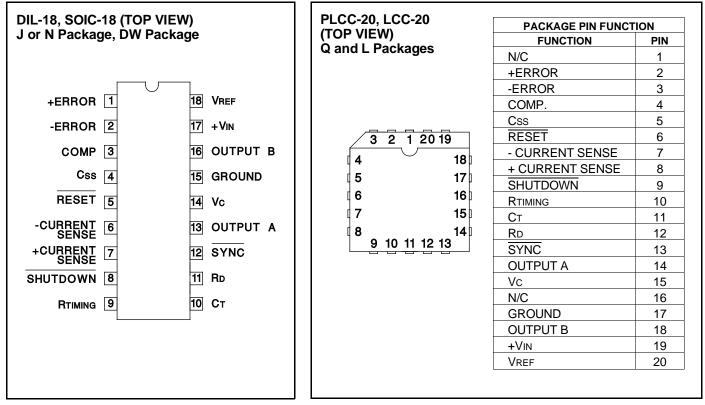
Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.

#### **RECOMMENDED OPERATING CONDITIONS**

(Note 3)
Input Voltage+7V to +35V
Collector Supply Voltage +4.5V to +35V
Sink/Source Load Current (each output) 0 to 100mA
Reference Load Current
Oscillator Frequency Range 1Hz to 600kHz
Oscillator Timing Resistor
Oscillator Timing Capacitor 400pF to 20µF
Available Deadtime Range at 40kHz 1% to 50%
Operating Ambient Temperature Range
UC1526A
UC2526A
UC3526A 0°C to +70°C
Note 3: Range over which the device is functional and
parameter limits are guaranteed

parameter limits are guaranteed.

#### **CONNECTION DIAGRAMS**



# UC1526A UC2526A UC3526A

PARAMETER	TEST CONDITIONS	UC152	26A / UC	2526A	UC3526A			
		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Reference Section (Note 4)								
Output Voltage	TJ = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+VIN = 7 to 35V		2	10		2	15	mV
Load Regulation	I∟ = 0 to 20mA		5	20		5	20	mV
Temperature Stability	Over Operating TJ (Note 5)		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	Vref = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
RESET Output Voltage	VREF = 3.8V		0.2	0.4		0.2	0.4	V
	VREF = 4.7V	2.4	4.7		2.4	4.8		V
Oscillator Section (Note 6)		•		- <u>1</u>			-	•
Initial Accuracy	TJ = +25°C		±3	±8		±3	±8	%
Voltage Stability	+VIN = 7 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating TJ (Note 5)		2	6		1	3	%
Minimum Frequency	RT = 150kΩ, CT = 20 $\mu$ F (Note 5)			1			1	Hz
Maximum Frequency	$R_T = 2k\Omega$ , $C_T = 470pF$	550			650			kHz
Sawtooth Peak Voltage	+VIN = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+VIN =7V	0.5	1.0		0.5	1.0		V
SYNC Pulse Width	$T_J = 25^{\circ}C$ , $R_L = 2.7k\Omega$ to $V_{REF}$		1.1			1.1		μs
Error Amplifier Section (No	te 7)							
Input Offset Voltage	$R_S \le 2k\Omega$		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	$RL \geq 10 M \Omega$	64	72		60	72		dB
HIGH Output Voltage	VPIN 1 - VPIN 2 $\geq 150 mV,$ Isource = $100 \mu A$	3.6	4.2		3.6	4.2		V
LOW Output Voltage	VPIN 2 - VPIN 1 $\geq$ 150mV, ISINK = 100 $\mu$ A		0.2	0.4		0.2	0.4	V
Common Mode Rejection	$Rs \leq 2k\Omega$	70	94		70	94		dB
Supply Voltage Rejection	+VIN = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 6)								
Minimum Duty Cycle	VCOMPENSATION = $+0.4V$			0			0	%
Maximum Duty Cycle	VCOMPENSATION = $+3.6V$	45	49		45	49		%
Digital Ports (SYNC, SHUTE	DOWN, and RESET)							
HIGH Output Voltage	ISOURCE = $40\mu A$	2.4	4.0		2.4	4.0		V
LOW Output Voltage	ISINK = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	VIH = +2.4V		-125	-200		-125	-200	μA
LOW Input Current	VIL = +0.4V		-225	-360		-225	-360	μA
Shutdown Delay	From Pin 8, TJ = 25°C		160			160		ns
Current Limit Comparator (	Note 8)		<b>1</b>				<b>1</b>	
Sense Voltage	$Rs \leq 50 \Omega$	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	μA
Shutdown Delay	From pin 7, 100mV Overdrive, TJ = 25°C		260			260		ns

ELECTRICAL CHARACTERISTICS: +VIN = 15V, and over operating ambient temperature, unless otherwise specified TA = TJ.

Note 4: IL = 0mA.

Note 5: Guaranteed by design, not 100% tested in production. Note 6: Fosc = 40kHz, ( $R\tau$  = 4.12k $\Omega \pm 1$ %,  $C\tau$  = 0.01 $\mu$ F $\pm 1$ %,  $R_D$  = 0  $\Omega$ ). Note 7: VCM = 0 to +5.2V

Note 8: VCM = 0 to +12V. Note 9: VC = +15V.

Note  $10:V_{IN} = +35V$ ,  $R_T = 4.12k_{\Omega}$ .

PARAMETER	TEST CONDITIONS		UC1526A UC2526A			UC3526A		
		MIN	TYP	MAX	MIN	TYP	MAX	1
Soft-Start Section	•		-	-1	•	•		-
Error Clamp Voltage	RESET = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	RESET = +2.4V	50	100	150	50	100	150	μA
Output Drivers (Each Output	it) (Note 9)							
HIGH Output Voltage	ISOURCE = 20mA	12.5	13.5		12.5	13.5		V
	ISOURCE = 100mA	12	13		12	13		V
LOW Output Voltage	ISINK = 20mA		0.2	0.3		0.2	0.3	V
	ISINK = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	Vc = 40V		50	150		50	150	μA
Rise Time	C∟ = 1000pF (Note 5)		0.3	0.6		0.3	0.6	μs
Fall Time	C∟ = 1000pF (Note 5)		0.1	0.2		0.1	0.2	μs
Cross-Conduction Charge	Per cycle, TJ = 25°C		8			8		nC
Power Consumption (Note 1	10)							
Standby Current	SHUTDOWN = +0.4V		14	20		14	20	mA

ELECTRICAL CHARACTERISTICS: +VIN = 15V, and over operating ambient temperature, unless otherwise specified TA = TJ.

Note 4:  $I_L = 0mA$ .

Note 5: Guaranteed by design, not 100% tested in production.

Note 6: Fosc = 40kHz, ( $R\tau = 4.12k\Omega \pm 1\%$ ,  $C\tau = 0.01\mu F \pm 1\%$ ,

 $R_D = 0 \Omega$ ).

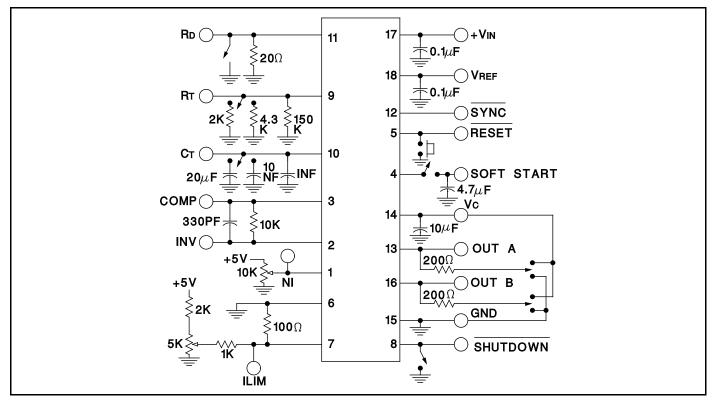
Note 7: VCM = 0 to +5.2V

Note 8: VCM = 0 to +12V.

Note 9: Vc = +15V.

Note  $10:V_{IN} = +35V$ ,  $R_T = 4.12k_{\Omega}$ .

# **Open Loop Test Circuit UC1526A**



# **APPLICATIONS INFORMATION**

#### **Voltage Reference**

The reference regulator of the UC1526A is based on a precision band-gap reference, internally trimmed to  $\pm 1\%$  accuracy. The circuitry is fully active at supply voltages above +7V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

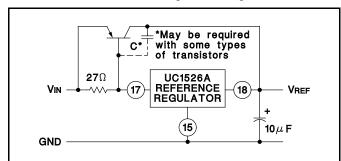


Figure 1. Extending Reference Output Current

#### **Under-Voltage Lockout**

The under-voltage lockout circuit protects the UC1526A and the power devices it controls from inadequate supply voltage, If +VIN is too low, the circuit disables the output drivers and holds the RESET pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to 3VBE or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the RESET pin, allowing a normal soft-start. The comparator has 350mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls RE-SET LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526A can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

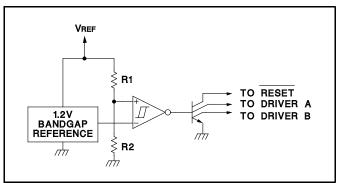


Figure 2. Under-Voltage Lockout Schematic Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526A, the under-voltage lockout circuit holds RESET LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, RESET will go HIGH. Q1 turns off, allowing the internal 100 $\mu$ A current source to charge Cs. Q2 clamps the error amplifier output to 1VBE above the voltage on Cs. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

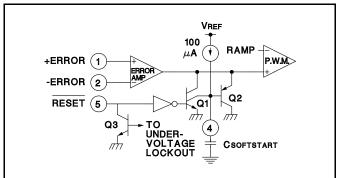


Figure 3. Soft-Start Circuit Schematic Digital Control Ports

The three digital control ports of the UC1526A are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is <u>pulled</u> LOW to activate the particular function. Driving SYNC LOW initiates a discharge cycle in the oscillator. Pulling SHUTDOWN LOW immediately inhibits all PWM output pulses. Holding RESET LOW discharges the soft-start

# **APPLICATIONS INFORMATION (cont.)**

capacitor. The logic threshold is +1.1V at  $+25^{\circ}C$ . Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

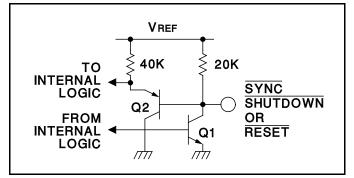


Figure 4. Digital Control Port Schematic

#### Oscillators

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD=  $0\Omega$  (pin 11 shorted to ground) select values for RT and CT from the graph on page 4 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +Vc terminal is the same as the oscillator frequency.

2. If more dead time is required, select a larger value of RD. At 40kHz dead time increases by  $400ns/\Omega$ .

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526A can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the SYNC frequency.

A periodic LOW logic pulse approximately 0.5µs wide at

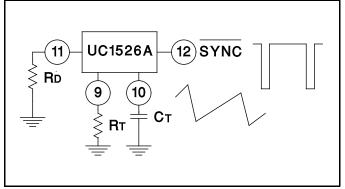
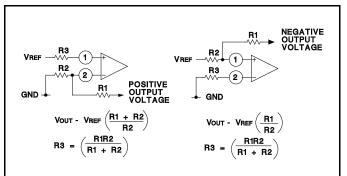


Figure 5. Oscillator Connections and Waveforms

the SYNC pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master and all SYNC terminals are likewise connected to the SYNC pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminal may be either left open or grounded.





#### **Error Amplifier**

The error amplifier is a transconductance design, with an output impedance of  $2M\Omega$ . Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

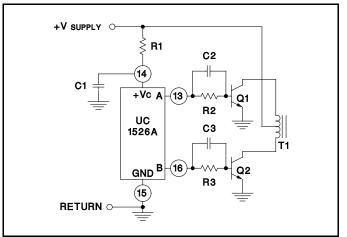
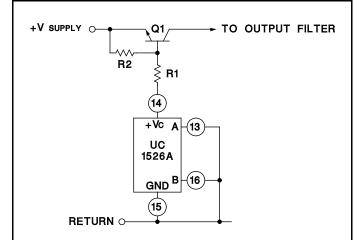


Figure 7. Push-Pull Configuration

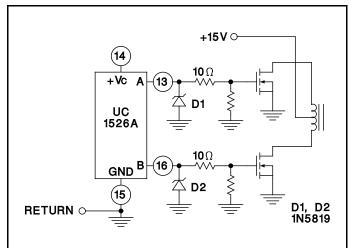
#### APPLICATIONS INFORMATION (cont.) Output Drivers

The totem pole output drivers of the UC1526A are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +Vc, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the



+Vc terminal to ground during switching; however, improved design has limited this cross-conduction period to less than 50ns. Capacitor decoupling at Vc is recommended and careful grounding of Pin 15 is needed to insure that high peak sink currents from a capacitive load do not cause ground transients.

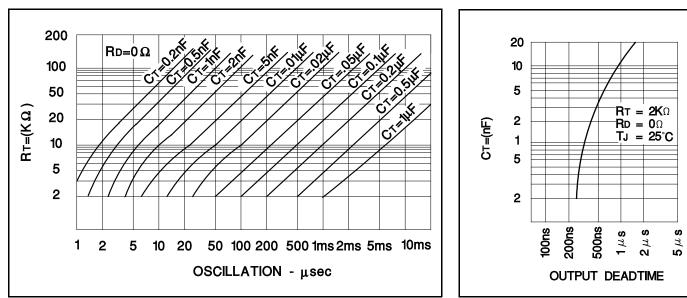


**OUTPUT BLANKING** 

Figure 9. Driving N-Channel Power MOSFETs

#### **TYPICAL CHARACTERISTICS**

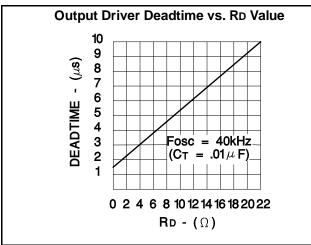
Figure 8. Single-Ended Configuration

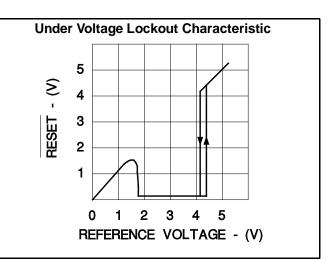


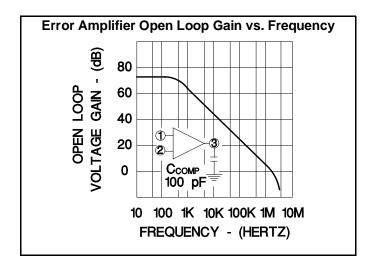
# **OSCILLATOR PERIOD vs RT and CT**

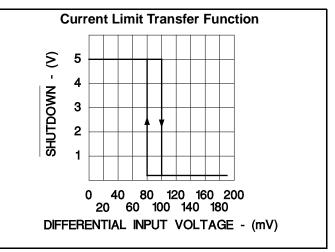
UC1526A UC2526A UC3526A

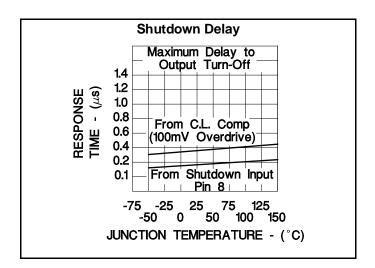
### TYPICAL CHARACTERISTICS (Cont.)

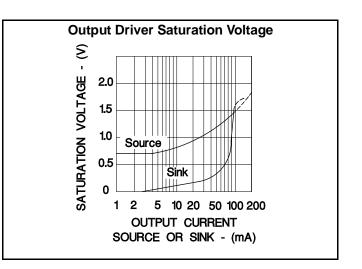












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