

3.5-GHz Integrated IF Up-Converter

FEATURES

- Low Phase Noise
- High Dynamic Range Image-Reject Downconverter
- Selectable IF Filters
- Internal or External AGC Control With Peak Detector and Voltage Reference
- Analog Gain Control Range
- Direct Interface to A/D
- Dual VCO/PLL With On-Chip Resonator For Double Down-Conversion Architecture
- S-Band LO Frequency Range:
 - TRF1112: 1818 to 2268 MHz
 - TRF1212: 2818-MHz to 3382-MHz
- UHF LO Frequency Range: 360 to 456 MHz
- Phase Noise is 0.5 RMS Typ 100 Hz to 1 MHz
- Rx Noise Figure of 5 dB, Typ
- UHF LO Tuning Step Size of 125 kHz
- Typical Gain of 90 dB, Including 15-dB Loss IF2 SAW Filter
- Input Third Order Intercept Point > 0 dBm
- Input 1-dB Compression Point > -10 dBm
- Gain Control Range of 90 dB Typ

DESCRIPTION

The TRF1112 / TRF1212 are UHF-VHF down converters with integrated UHF and S-band frequency synthesizers for radio applications in the 2 GHz to 4 GHz range. The device integrates an image reject mixer, IF gain blocks, automatic gain control (AGC), and two complete phase locked loop (PLL) circuits including: VCOs, resonator circuit, varactors, dividers, and phase detectors.

The TRF1112 / TRF1212 are designed to function as part of Texas Instruments 2.5-GHz and 3.5-GHz complete radio chipsets, respectively. In the chipset, two chips function together to double-down-convert RF frequencies to an IF frequency that is suitable for most baseband modem ADCs. The TRF1112 / TRF1212 performs the second down conversion from the first IF frequency (480 MHz typical) to a final IF frequency (20-50 MHz). The radio chipset features sufficient linearity, phase noise and dynamic range to work in single carrier or multi-carrier, line-of-sight or non-line-of-sight, IEEE standard 802.16, BWIF, or proprietary systems. Due to the modular nature of the chipset, it is ideal for use in systems that employ transmit or receive diversity.

DEVICE INFORMATION

LPCC-48 PACKAGE
(TOP VIEW)

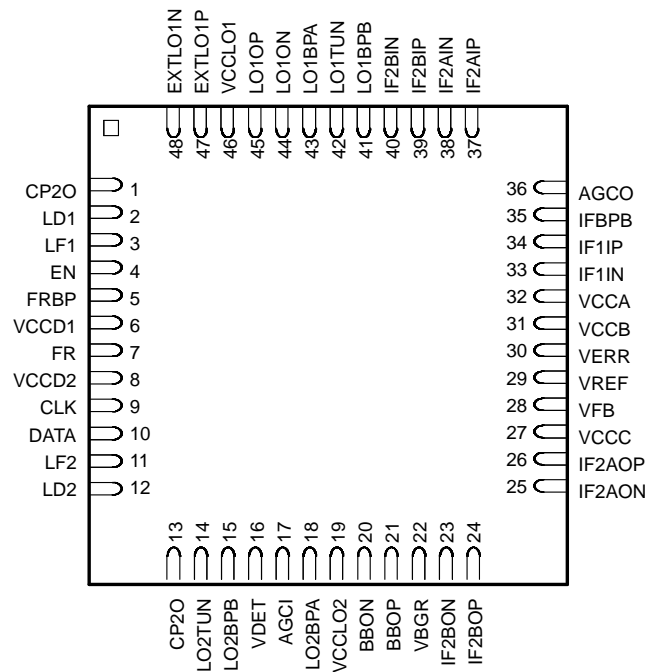


Figure 1. TRF1112 / TRF1212 Pin Out

PRODUCT PREVIEW



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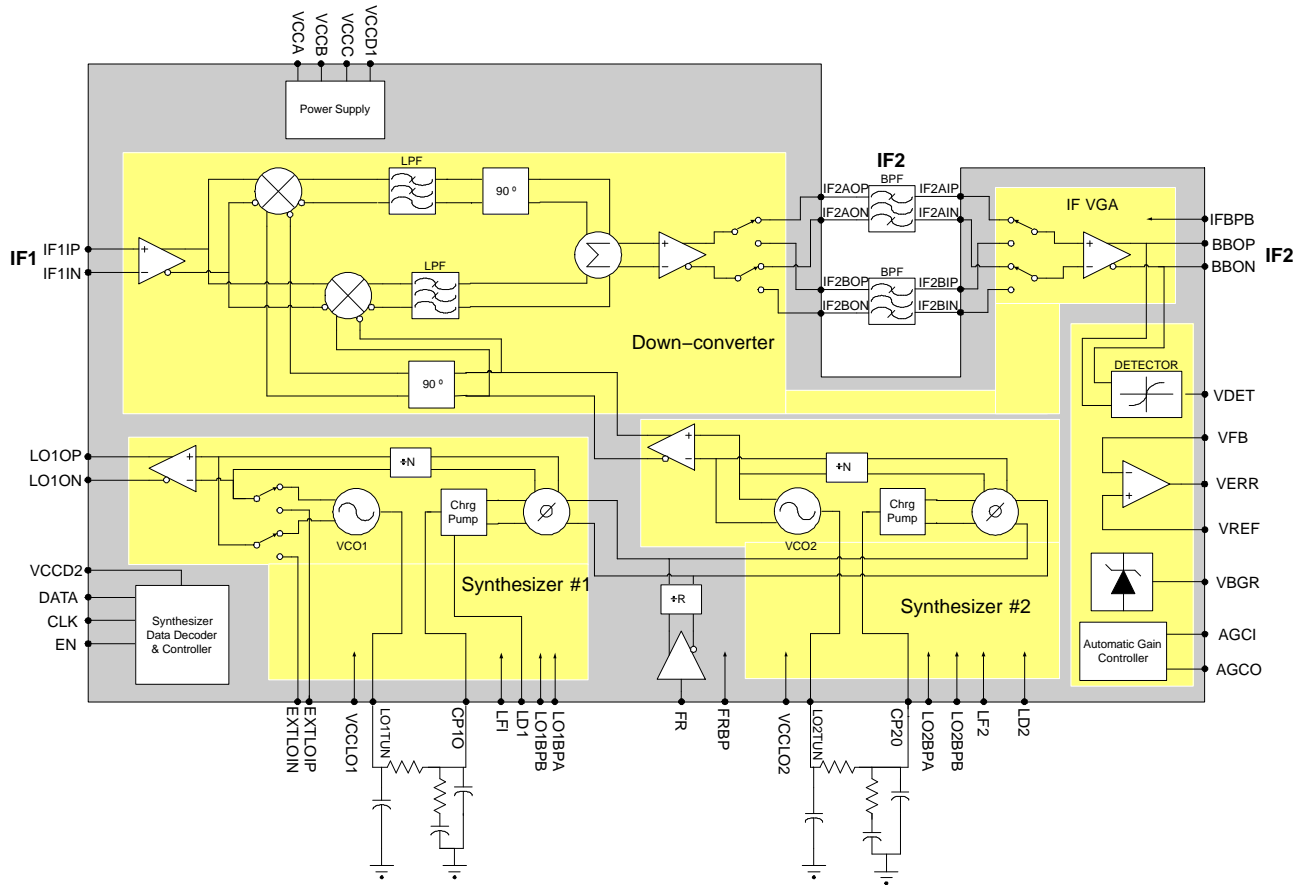


Figure 2. Block Diagram

PRODUCT PREVIEW

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