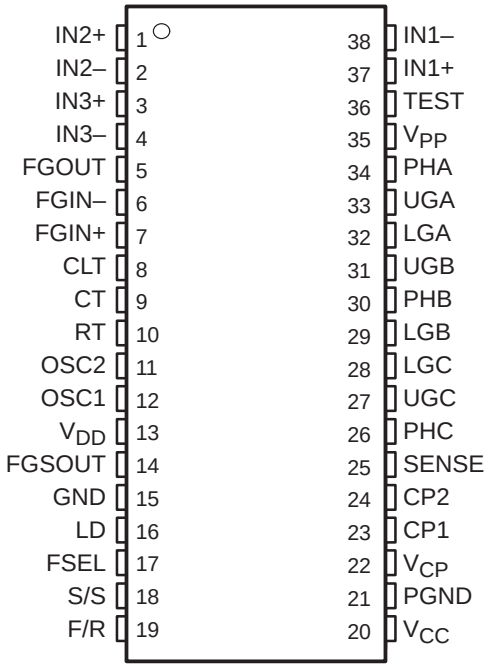
- **Precision Phase Lock Loop Motor – RPM Control With Embedded DSP Filter Algorithm for Loop Compensation**
- **EEPROM Registers for User Adjustment of PLL Loop Gain and DSP Filter Coefficients (Pole/Zero)**
- **Crystal Oscillator With EEPROM Adjustable Divide-By for Versatile PLL Timebase**
- **Standalone Operation With No Host Processor Needed**
- **RPM Lock Detection/Reporting (±5% Window)**
- **Synchronous Rectification, Enabled (TPIC43T01) Disabled (TPIC43T02)**
- **Stalled Motor Timer/Shutdown**
- **High-Side Current Limiting**
- **High-Side Over-Current Shutdown**
- **Differential Hall Effect Position Sensor Inputs/Decode Provide Commutation Control**
- **Differential Variable Reluctance Speed Sensor Inputs**
- **Gate Drive for Six External N-Channel Power FETs in Three Half-H Configuration**
- **Charge Pump to Develop High-Side Gate Drive Voltage**
- **5 V Regulator – Designed for 10 mA External Current**
- **8 to 28 V Supply Voltage**
- **Small Outline Surface-Mount Package**

DA PACKAGE
(TOP VIEW)



description

The TPIC43T01/02 is a monolithic motor control integrated circuit designed to provide RPM control to a 3-phase brushless dc motor. The device provides two analog sensor input ports which include a speed sensor interface and a Hall effect position interface. The speed feedback interface consists of an FG amplifier to receive an external sinusoidal signal from a variable reluctance pickup and convert it to a digital speed signal for the control circuit. When the motor speed is outside a ±5% window of the reference signal, an out-of-lock condition is declared. The Hall ffect sensor input section receives low-level differential voltages from external naked Hall elements and converts them to digital position reference signals for the control circuit for commutation control.

The core of the control circuit implements a digital signal processing algorithm consisting of a digital integrator and filter with user adjustable parameters to optimize the closed loop performance of the control system. The device contains an internal EEPROM to set integrator gain and digital filter coefficients. In addition, Texas Instruments provides a PC based Windows™ compatible software package to input the motor and system characteristics and convert them to control parameters for the TPIC43T01/02. The software generates a JEDEC compatible file to program the device through a third party device programmer.

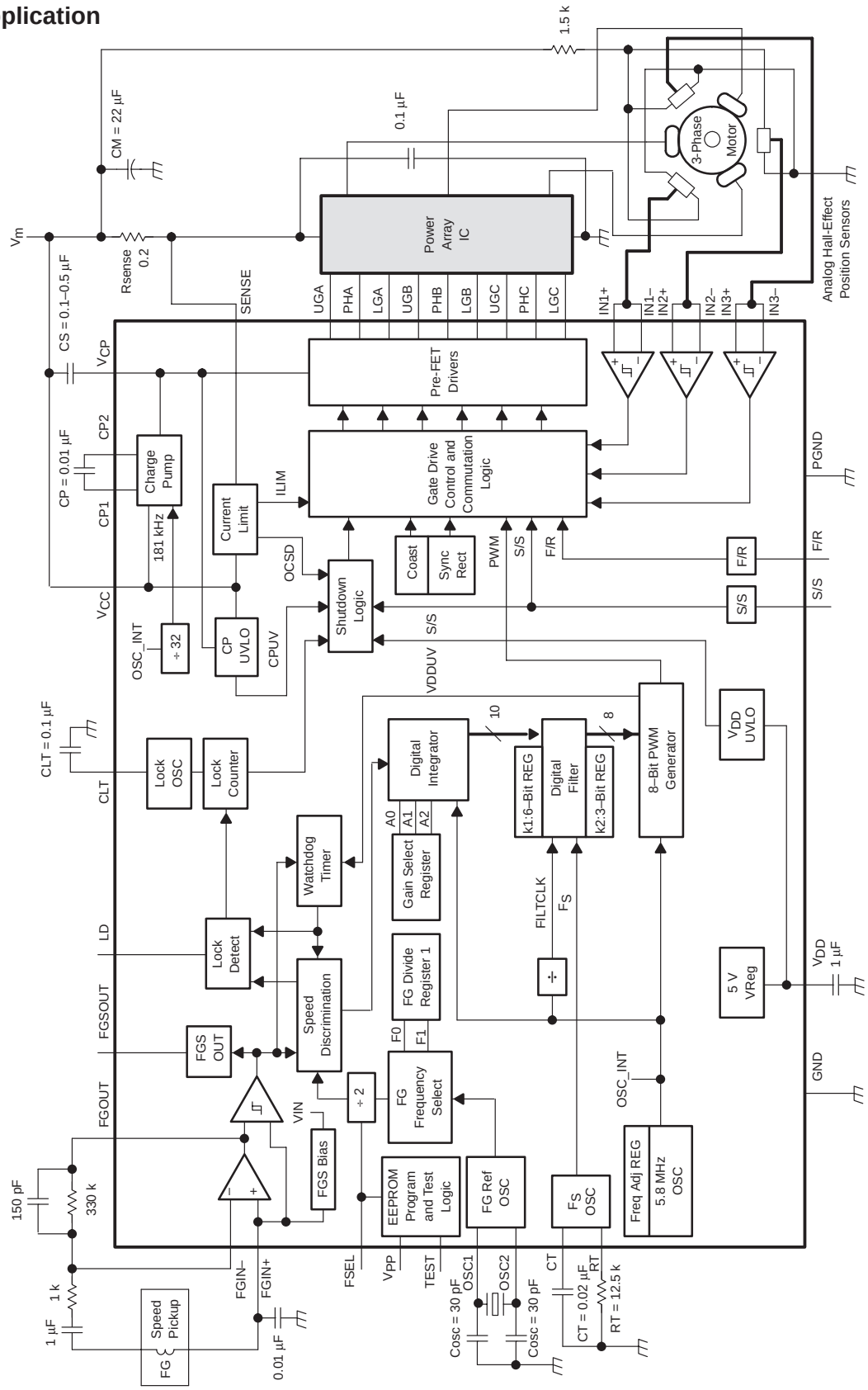
description (continued)

The TPIC43T01/02 provides pre-drive outputs to control six external N-channel FET switches connected in a 3-half H-bridge configuration to drive a 3-phase dc motor. A companion TI Power+ Arrays™ device is available, the TPIC1310 3-half H-bridge power array, to provide up to 2.5 A motor drive capability. The TPIC1310 is a monolithic gate protected DMOS power array available in the TI 15-pin PowerFLEX™ power package. The TPIC43T01/02 gate drive outputs are designed to also drive discrete N-channel power FETs.

The TPIC43T01/02 provides onboard supervisory and shutdown logic to protect the device and motor from fault conditions. Oscillators, charge pump, and voltage regulators have been integrated into the TPIC43T01/02 to minimize the number of external discrete components required to support the motor system.

Power+ Arrays and PowerFLEX are trademarks of Texas Instruments Incorporated.

typical application



Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
CLT	8	I	Capacitor lock timer. CLT is a timing capacitor for the lock detect timer oscillator.
CP1	23	O	Charge pump. CP1 is the switched capacitor output number 1.
CP2	24	O	Charge pump. CP2 is the switched capacitor output number 2.
CT	9	I	Timing capacitor. CT is the timing capacitor for the filter oscillator.
F/R	19	I	Forward/Reverse. F/R is the forward/reverse direction data input.
FGIN–	6	I	FGIN– is a inverting amplifier input.
FGIN+	7	O	FGIN+ is a noninverting amplifier input.
FGOUT	5	O	FGOUT is a amplifier output.
FGSOUT	14	O	FGSOUT is a buffered FGS comparator output.
FSEL	17	I	Frequency select. FSEL is a frequency select input.
GND	15		Ground
IN1–	38	I	Hall amplifier 1 inverting input
IN1+	37	I	Hall amplifier 1 noninverting input
IN2–	2	I	Hall amplifier 2 inverting input
IN2+	1	I	Hall amplifier 2 noninverting input
IN3–	4	I	Hall amplifier 3 inverting input
IN3+	3	I	Hall amplifier 3 non-inverting input
LD	16	O	Lock Detect. LD is an active low, open-drain output.
LGA	32	I	Lower gate drive A
LGB	29	I	Lower gate drive B
LGC	28	I	Lower gate drive C
OSC1	12	I	Crystal oscillator input 1. OSC1 is an external OSC input.
OSC2	11	I	Crystal oscillator input 2. OSC2 is an external OSC input.
PGND	21		PGND is the lower gate drive turnoff circuitry GND return.
PHA	34	I	Phase A return
PHB	30	I	Phase B return
PHC	26	I	Phase C return
RT	10	O	RT is the charge/discharge current setting resistor for filter and lock timer oscillators.
S/S	18	I	Stop/Start. S/S = low to start.
SENSE	25	I	Current limit sense. SENSE is the high-side current limit sense input.
TEST	36	I	Test enable
UGA	33	I	Upper gate drive A
UGB	31	I	Upper gate drive B
UGC	27	I	Upper gate drive C
V_{CC}	20	I	Supply voltage
V_{CP}	22	O	Charge-pump voltage source. V_{CP} requires a storage capacitor.
V_{DD}	13	O	5 V Supply output
V_{PP}	35	I	EEPROM programming voltage input

absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . 8 V to 30 V
Motor drive voltage, $V_{(motor)}$ . . . . . 30 V
Charge pump output voltage, $V_{CP(max)}$, ($V_{CP} - V_{CC}$) . . . . . V_{CC} + 20 V
Operating virtual junction temperature range, T_J . . . . . 0°C to 150°C
Thermal resistance, junction to ambient, $R_{\theta JA}$ . . . . . 121°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The device will function, but may not meet all electrical specifications over this voltage range.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	18	24	28	V
Extended supply voltage range, (see Note 1)	8		18	V
Operating case temperature, T_C	0		70	°C

NOTE 1: The device will function, but may not meet all electrical specifications over this voltage range.

EEPROM programming

		MIN	TYP	MAX	UNIT
V_{PP} setup time, $t_{su}(V_{PP})$	See Figure 20	2			µs
V_{PP} pulse width duration, $t_w(V_{PP})$	See Figure 20	5			ms
V_{PP} rise time, $t_r(V_{PP})$	See Figure 20	2		3	ms
V_{PP} fall time, $t_f(V_{PP})$	See Figure 20	2		3	ms

electrical characteristics, T_C = 25°C, V_{CC} = 24V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ccq}	V_{DD} quiescent current	S/S low, V_{CC} = 28 V, $I_{(VCP)}$ = 2 mA		10	18	mA
		S/S high, V_{CC} = 28 V, $I_{(VCP)}$ = 0 mA		5	10	

V_{DD} undervoltage lockout

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DD(uvlo)}$	V_{DD} under-voltage lockout threshold voltage		2.5	3.1	4	V
V_{hys}	V_{DD} under-voltage lockout threshold voltage hysteresis			1.1		V

5 V regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Output voltage	I_O = –10 mA	4.75	5	5.25	V
$V_{(REGIN)}$	Line regulation	V_{CC} = 8 V to 28 V		0	50	mV
$V_{(REGOUT)}$	Load regulation	I_O = 0 to –10 mA		20	100	mV

electrical characteristics, T_C = 25°C, V_{CC} = 24V (unless otherwise noted) (continued)

charge pump

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(CP)}$	Output voltage	I_O = –1.5 mA, V_{CC} = 18 V to 28 V, CP = 0.01 µF, CS = 0.1 µF, S/S = high	V_{CC} + 14	V_{CC} + 15	V_{CC} + 17	V
		I_O = –1.5 mA, V_{CC} = 8 V, CP = 0.01 µF, CS = 0.1 µF, S/S = high		V_{CC} + 5.5		V
$V_{(CP–uvlo)}$	Under voltage lockout	I_O = –1.5 mA, V_{CC} = 8 V to 28 V, S/S = high (VCP forced externally)	V_{CC} + 5	V_{CC} + 6	V_{CC} + 7	V
$V_{hys(CP)}$	Under voltage lockout hysteresis	I_O = –1.5 mA, V_{CC} = 8 V to 28 V, S/S = high (VCP forced externally)		0.6		V

FG signal conditioning

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IO(FG)}$	Amplifier input offset voltage	Measured at FGOUT		0.5	±7	mV
$I_{IB(FG)}$	Amplifier input bias current	Measured at FGIN–		0.02	±1	µA
$V_{OH(FG)}$	Amplifier high level output voltage	$I_{(FG)}$ = –200 µA, I_{DD} = 0	V_{DD}–500 mV	V_{DD}–350 mV		V
$V_{OL(FG)}$	Amplifier low level output voltage	$I_{(FG)}$ = 200 µA, I_{DD} = 0		100	500	mV
A_V	Amplifier open-loop gain (see Note 2)		45			dB
$V_{(FGsens)}$	FG input sensitivity (see Note 2)	100 x Gain, at 2 kHz,	3			mV
$V_{(FGbias)}$	FG bias voltage	I_{FG} = 0 µA, I_{DD} = 0	2.375	2.5	2.625	V
$V_{IT+(FGOUT)}$	FG comparator positive threshold	FGOUT with respect to $V_{(FGIN+)}$, See Figure 8	215	250	285	mV
$V_{IO(FGOUT)}$	FG comparator offset voltage	FGOUT with respect to $V_{(FGIN+)}$, See Figure 8		0.8	±7	mV
$V_{OL(FGSOUT)}$	FGSOUT open drain saturation voltage	I_O = 2 mA		0.4	0.7	V
$I_{lkg(FGSOUT)}$	FGSOUT leakage current	V_O = 5 V		0.08	10	µA

NOTE 2: Design target only. Not tested in production.

Hall sensor signal conditioning

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IB(HL)}$	Input bias current (see Note 2)				±4	µA
$V_{ICR(HL)}$	Common-mode input voltage range (see Note 3)		1.5		3.5	V
$V_{IT+(HL)}$	Input positive threshold voltage	With respect to $V_{(CM)}$, 1.5 kΩ in series with both inputs, See Figure 9	4	8	12	mV
$V_{IT–(HL)}$	Input negative threshold voltage	With respect to V_{CM}, 1.5 kΩ in series with both inputs, See Figure 9	–4	–8	–12	mV

NOTES: 2. Design target only. Not tested in production.
3. Not measured, forced during testing.

FG reference crystal oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(OSC1)}$	OSC1 input upper threshold (see Note 3)		2.7			V
$V_{IT–(OSC1)}$	OSC1 input lower threshold (see Note 3)				1	V

NOTES: 3. Not measured, forced during testing.

electrical characteristics, T_C = 25°C, V_{CC} = 24V (unless otherwise noted) (continued)

digital filter $f_{(s)}$ RC oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ref(RT)}$	RT reference voltage	$I_{(RT)}$ = –160 μA	0.19 V_{DD}	0.2 V_{DD}	0.21 V_{DD}	V
$V_{IT+(CT)}$	CT upper threshold voltage			0.7 V_{DD}		V
$V_{IT–(CT)}$	CT lower threshold voltage			0.3 V_{DD}		V
$V_{(CT)}$	CT amplitude		1.9	2	2.1	V
$I_{(CT)}$	CT charge/discharge current	Measured at $V_{IT+(CT)}$ and $V_{IT–(CT)}$	1.8 $I_{(RT)}$	±2 $I_{(RT)}$	2.2 $I_{(RT)}$	A

lock detection timer

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(CLT)}$	CLT upper threshold voltage			0.7 V_{DD}		V
$V_{IT–(CLT)}$	CLT lower threshold voltage			0.3 V_{DD}		V
$V_{(CLT)}$	CLT amplitude		1.9	2	2.1	V
$I_{(CLT)}$	CLT charge/discharge current	Measured at $V_{IT + (CLT)}$ and $V_{IT–(CLT)}$	1.9 $I_{(RT)}$	±2 $I_{(RT)}$	2.3 $I_{(RT)}$	A

high side gate drive

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Clamp voltage	UGX to PHX, $I_{(UGX)}$ = –100 μA	14	16	19	V
$V_{DS(UGX)}$	Source voltage drop	$I_{(UGX)}$ =–10 mA, VCP = V_{CC} + 17 V, Measure VCP – $V_{(UGX)}$, V_{CC} = 18 V		1	1.2	V
$Vsink_{(UGX)}$	Sink voltage drop @10 mA	$I_{(UGX)}$=10 mA, $V_{(PHx)}$= 0, Measure $V_{(UGX)}$ – $V_{(PHx)}$, V_{CC} = 18 V		1.8	2	V
$Vsink_{(UGX)}$	Sink voltage drop @100 uA	$I_{(UGX)}$=10 mA, $V_{(PHx)}$ = 0, Measure $V_{(UGX)}$ – $V_{(PHx)}$, V_{CC} = 18 V		0.56	0.7	V

low side gate drive

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(REG15)}$	High level output voltage	V_{CC} = 18 to 28 V, $I_{(LGX)}$ = 0	14	16	19	V
		V_{CC} = 8 to 18 V, $I_{(LGX)}$ = 0	7.9	8	18	V
$V_{source(LGX)}$	Source voltage	$I_{(LGX)}$ = –10 mA, with respect to PGND, V_{CC} = 18 V	12	14.5		V
$V_{DS(LGX)}$	Sink voltage drop	$I_{(LGX)}$ = 10 mA, with respect to PGND, V_{CC} = 18 V		0.6	1	V

current limit control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(lim)}$	Limit threshold voltage	V_{CC} – $V_{(SENSE)}$	0.46	0.5	0.54	V

over-current shutdown control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(ocsd)}$	Detection threshold voltage	V_{CC} – $V_{(SENSE)}$	0.9	1	1.1	V

EEPROM programming

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PP}	V_{PP} programming voltage		12	13	15	V
$R_{(VPP)}$	V_{PP} pulldown resistance	V_{PP} = 1 V	15	23	35	kΩ

electrical characteristics, T_C = 25°C, V_{CC} = 24V (unless otherwise noted) (continued)

digital input pins

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Digital input high level input voltage	Interface from 3.3 V controller	2.2			V
V_{IL}	Digital input low level input voltage	Interface from 3.3 V controller			1.1	V
$I_{(pullup)}$	Digital input pullup current, S/S, FSEL	V_{IN} = 2.2 V	–9	–14	–18	µA
$I_{(F/R)}$	Digital input pulldown current, F/R	V_{IN} = 1.1 V	17.5	27	35	µA
$I_{(TEST)}$	TEST input pulldown current	V_{IN} = 1.1 V	130	200	250	µA

switching characteristics, T_C = 25°C, V_{CC} = 24 V

charge pump

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(CP)}$	Switching frequency			180		kHz
		T_C = 0 to 70°C	140		220	kHz

FG signal conditioning

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Gain bandwidth (see Note 2)			200		kHz

NOTE 2. Design target only. Not tested in production.

FG reference crystal oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Crystal frequency range (see Note 2)		5	6.87	10	MHz
$f_{(OSC1)}$	OSC1 frequency range	OSC1 driven externally, see FG Reference Oscillator section	1		10	MHz

NOTE 2. Design target only. Not tested in production.

PWM control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(PWM)}$	PWM frequency			22.7		kHz
		T_C = 0 to 70°C	18		27	
$t_{(DT)}$	Gate drive dead time control	See Figure 3	1		3.2	µs

digital filter $f_{(s)}$ RC oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(CT)}$	Oscillator frequency (see Note 2)			1/(2 × RT × CT) ±10%		Hz

NOTE 2. Design target only. Not tested in production.

lock detection timer

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(CLT)}$	CLT oscillator frequency (see Note 2)			1/(2 × RT × CLT) ±10%		Hz

NOTE 2. Design target only. Not tested in production.

lock detection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LD_{ERR}†	Lock detect threshold			±5		%

† Non JEDEC symbol.

switching characteristics, T_C = 25°C, V_{CC} = 24 V (continued)

current limit control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(DG)}$	Deglitch blanking time	$V_{(SENSE)} - V_L \geq 100$ mV, See Figure 1	0.5	3.7	6.5	µs

over-current shutdown control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(OCSD)}$	Response time	See Figure 2	0.5	1.5	2.5	µs

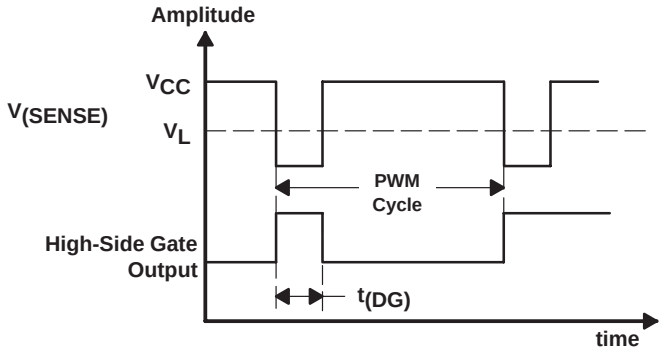


Figure 1. Current Limit Deglitch Blanking Time

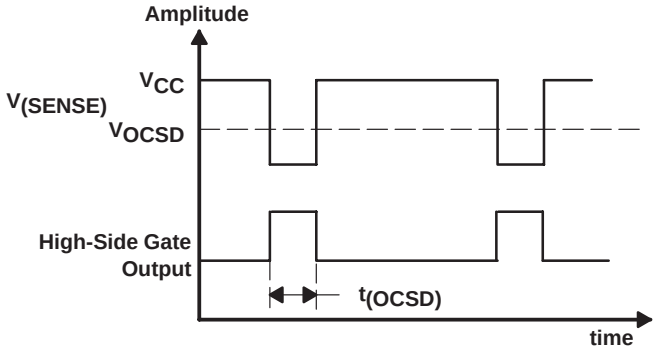


Figure 2. Over-Current Shutdown Response Time

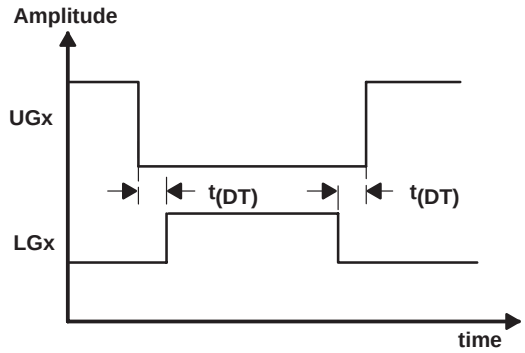


Figure 3. Gate Drive Deadtime

PRINCIPLES OF OPERATION

voltage regulator

The TPIC43T01/02 receives an 8 to 28 V supply voltage at the V_{CC} pin and generates an internal 5 V, V_{DD}, supply for the internal analog and digital logic. An external terminal for V_{DD} is provided for a required external 1 μF compensation capacitor. The regulator can also supply up to 10 mA current from the V_{DD} pin to external circuitry.

oscillators

internal oscillator

The device generates an internal 5.8 MHz clock to supply a frequency input to internal control blocks as presented in Figure 4. No external components are required.

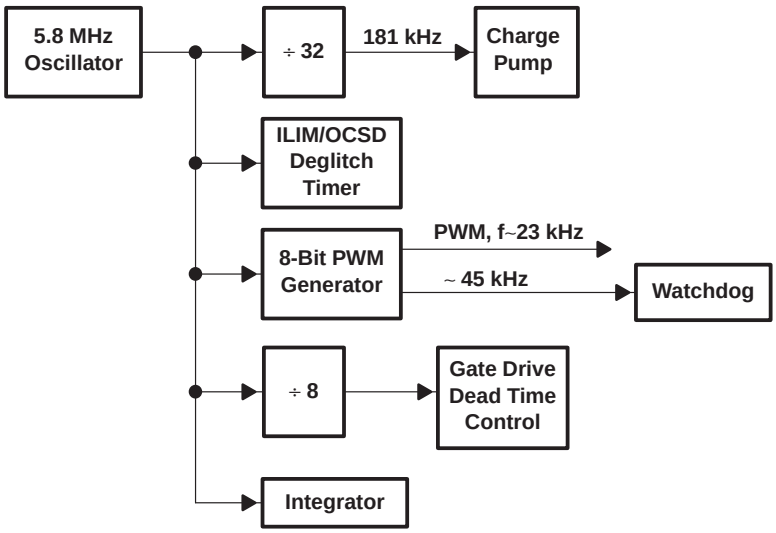


Figure 4. 5.8 MHz Internal Oscillator Fanout

FG reference oscillator

The FG reference oscillator provides a clock to the FG frequency control section of the device. The oscillator requires an external 5 to 10 MHz crystal to select the primary frequency. The user can alternatively input a 1 to 10 MHz signal from a signal generator to the OSC1 input to replace the external crystal. Two EEPROM bits allow programming four different crystal oscillator divide-by values for controlling the FG reference frequency. The FSEL pin provides an additional divide-by-2 for on-the-fly FG frequency (RPM) selection. Table 1 shows the divide-by count and resulting FG reference frequency based on the two EEPROM bits (address 1, bits 0–1) and the FSEL pin input level.

PRINCIPLES OF OPERATION

Table 1. FG Reference Frequency

EEPROM ADDR 1, BIT 1	EEPROM ADDR 1, BIT 0	FSEL INPUT	PRE-DIVIDER DIVIDE BY	TOTAL $f_{(osc)}$ DIVIDE-BY	FG $f_{(ref)}$ @$f_{(osc)}$		
					1 MHZ	5 MHZ	10 MHZ
0	0	1	3	3072	326	1628	3256
0	0	0	6	6144	163	814	1628
0	1	1	4	4096	244	1221	2441
0	1	0	8	8192	122	610	1221
1	0	1	6	6144	163	814	1628
1	0	0	12	12,288	81	407	814
1	1	1	8	8192†	122	610	1221
1	1	0	16	16,384†	61	305	610

† Equals default value

sampling frequency for the digital filter, $f_{(S)}$, oscillator

An external resistor (RT) and capacitor (CT) must be connected from the respective RT and CT terminals to GND to set the sampling frequency for the digital filter. Charge/discharge current at terminal CT will nominally be $\pm 2 \times$ (1V/RT). Nominal period is determined by the formula: $T_{(CT)} = 2 \times RT \times CT$ (see Figure 5).

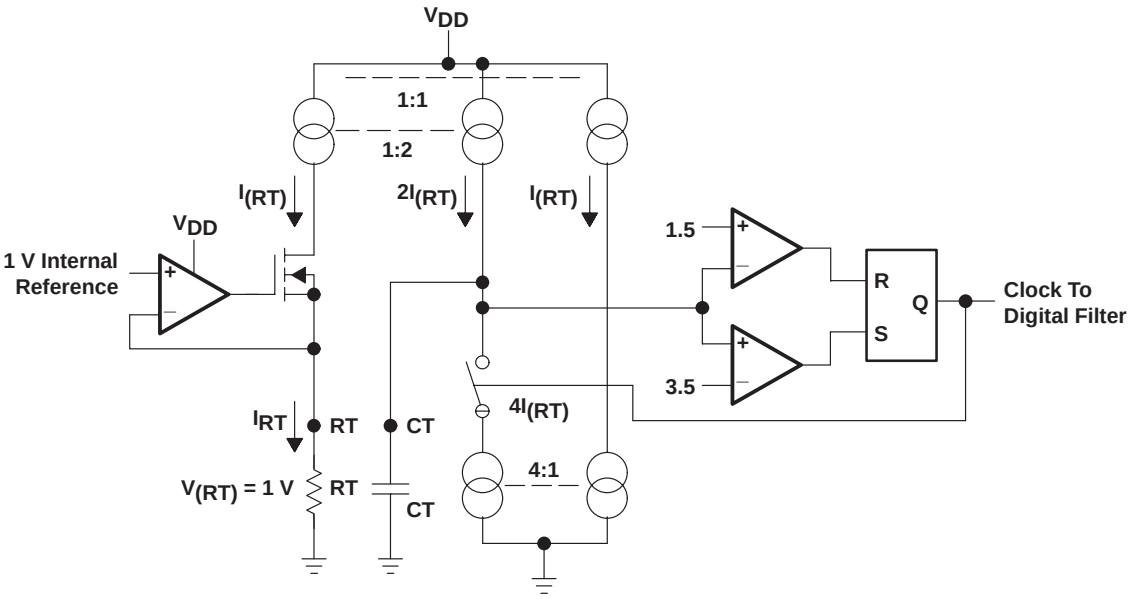


Figure 5. Digital Filter Sampling Clock Generation

PRINCIPLES OF OPERATION

lock timer oscillator/counter

Overall lock timer functionality is implemented by the combination of the oscillator and counter. The lock timer oscillator is identical to the sampling frequency oscillator. The external resistor (RT) is used as the current setting reference for both blocks. An external capacitor must be connected from the CLT terminal to GND to set the period, $T_{(CLT)}$, of the lock timer oscillator. The nominal period is determined by the formula: $T_{CLT} = 2 \times RT \times CLT$. When an out-of-lock signal is generated by the lock detect block (see lock detect section), the lock timer counter will count at the frequency of the lock timer oscillator. Should the out-of-lock signal remain for the duration of the counter completing 1023 counts, a lock timer time-out signal will then be generated which the shutdown logic block will respond to (see shutdown section). The lock timer time-out is thus set by $T_{CLT} \times 1023$.

power-up clear

An under-voltage lockout and power-up clear are provided to ensure FET drive outputs are set to a known state during power-up. The device is held in a CLEAR state until the following three conditions are met:

1. $V_{DD} > V_{DD(uvlo)}$, after which a power-up clear (PUC) time will begin.
2. The PUC timer counts 3 cycles of internal 20 kHz signal (internal 5.8 MHz ÷ 255), or ≅ 132 µs.
3. The charge pump voltage, $V_{(CP)}$, has charged to at least V_{CC} + 5 V.

shutdown

The scheme for shutdown includes monitoring two conditions and latching the device in a CLEAR state should an abnormal condition occur. Once shutdown is latched, the S/S input must be cycled high then low, or power cycled OFF then ON to release shutdown and resume normal operation. If an abnormal condition still exists after the S/S pin has been cycled, the device will relatch shutdown. A 1 on either S/S or V_{DD} pins will clear the lock timer. A V_{DD} under-voltage-lockout detect will force a global clear. (see Table 2 and Figure 6).

Table 2. Shutdown Conditions

LATCHED SHUTDOWN CONDITIONS		UNLATCHED SHUTDOWN CONDITIONS		S/S	INTERNAL CLR	LT LTCLR	GATE OUTPUTS
OCSD	LT	CP UV	V_{DD} UVLO	INPUT			
X	X	X	X	H	0	0	0
X	X	X	$V_{DD} < V_{DD(uvlo)}$	X	0	0	0
$V_{(SENSE)} < V_{(OCSD)}$	Out of Lock < $t_{(LT)}$	$V_{O(CP)} > V_{(CPUV)}$	$V_{DD} > V_{DD(uvlo)}$ + 3 counts	H↓L	1	1	1
X	X	VCP < $V_{(CPUV)}$ for > $t_{(DG)}$	X	X	X	X	0
$V_{(SENSE)} > V_{(OCSD)}$ for > $t_{(DG)}$	X	X	X	X	X	X	0
X	Out of Lock > $t_{(LT)}$	X	X	L	X	1	0

PRINCIPLES OF OPERATION

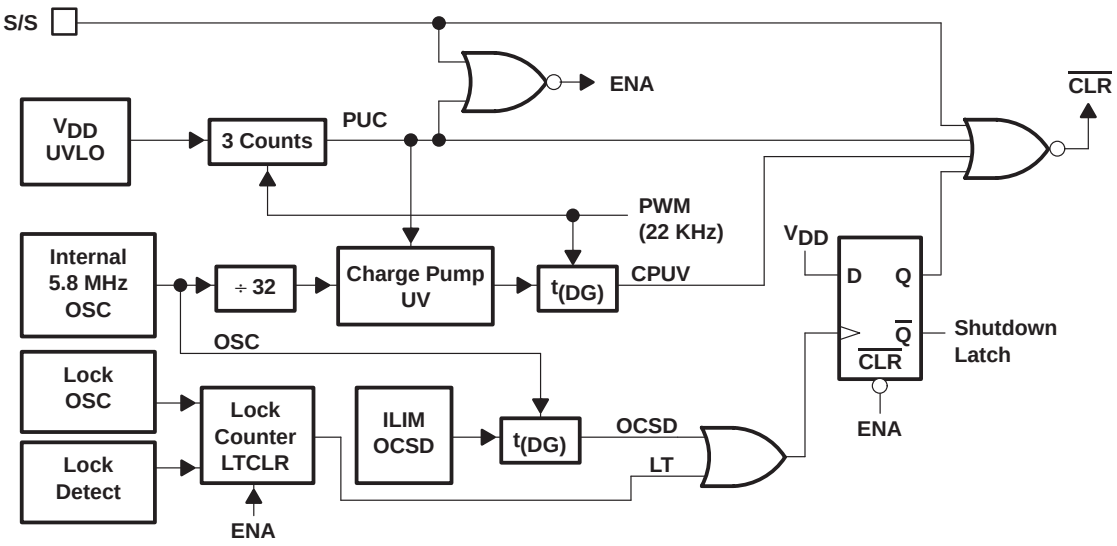


Figure 6. Shutdown Logic Block Diagram

FG amplifier

The FG amplifier amplifies the ac signal from the FG variable-reluctance pickup and converts it to a digital signal for internal use in the FG frequency control loop (see Figure 7). Figure 8 illustrates the generation of the FGSOUT signal in the FG amplifier section. Two comparators driving an RS latch are used with the upper comparator threshold (taken from the 5 V V_{DD} band-gap buffer circuit feedback resistor string), while the lower comparator threshold is connected to the FG bias voltage. This provides controlled hysteresis above the FGIN+ amplifier input reference voltage and zero-crossing detection at the input reference voltage.

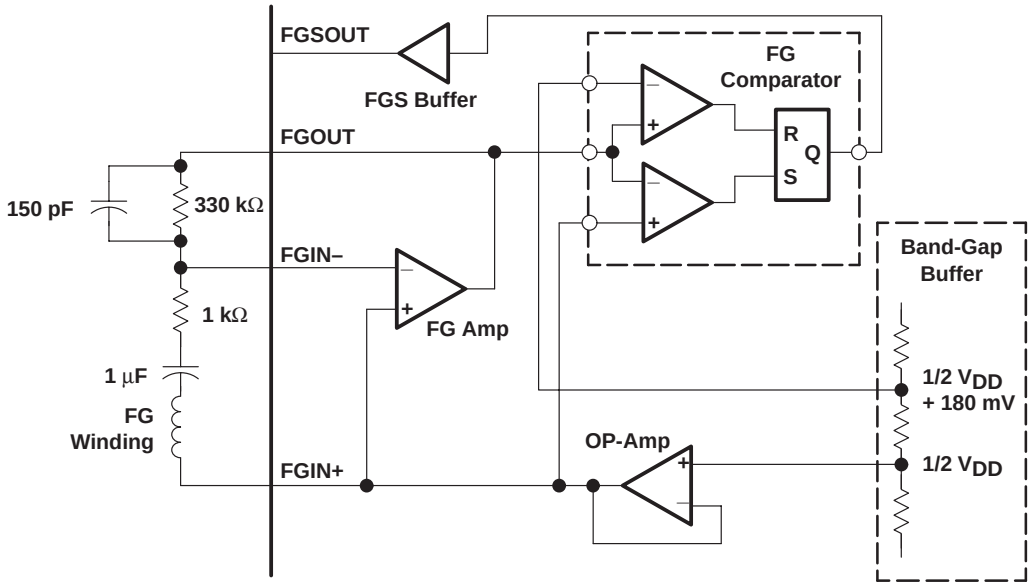


Figure 7. FG Signal Conditioning Schematic

PRINCIPLES OF OPERATION

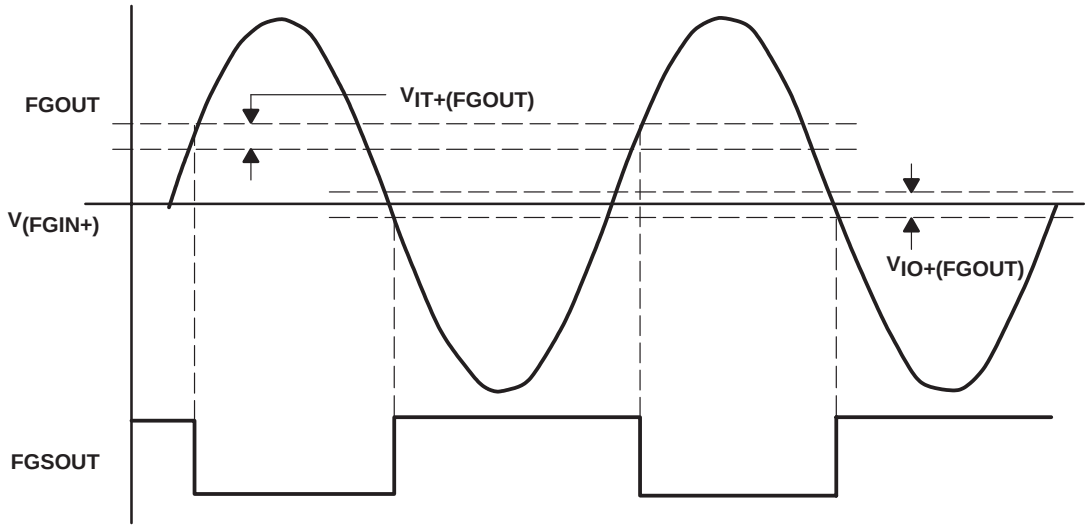


Figure 8. FG Signal Conditioning Block Waveforms

lock detect

The lock detect circuit monitors FGSOUT and flags when it is within ±5% of $f_{(ref)}$. The circuit counts the number of FG reference clocks which occur between the rising edges of FGSOUT to determine whether motor speed has reached the locking range. When a lock occurs, the LD terminal transitions low. When the FGSOUT frequency is not within the ± 5% of $f_{(ref)}$ window, an internal *out-of-lock* signal is generated for the lock timer block (see *lock timer* section).

Hall signal conditioning

The Hall signal conditioning block receives the low-level differential voltage from naked Hall elements and implements symmetric threshold detection and hysteresis for noise rejection. The circuit has nominal input voltage thresholds of ±7 mV at the INx+ pin with respect to the INx– pin. The common-mode input voltage range is 1.5 V to 3.5 V (see Figure 9).

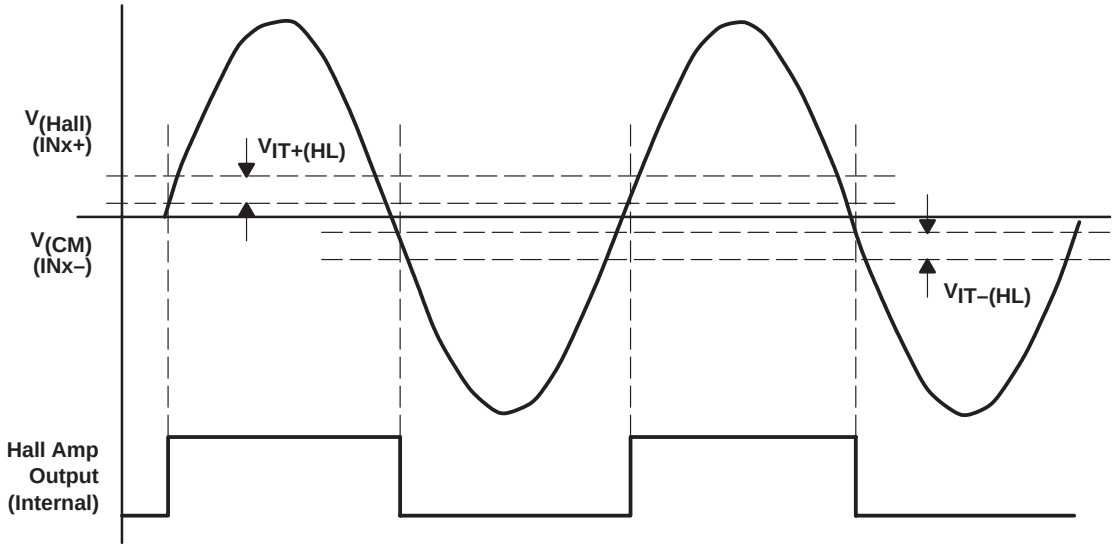


Figure 9. Hall Signal Conditioning Waveforms

PRINCIPLES OF OPERATION

rotor position sensing/commutation control

To electronically commutate the three phases, the state of the three Hall-effect sensors is decoded to drive the correct phases based on desired motor rotational direction and rotor position. This is accomplished by decoding the Hall sensor gray-code with the F/R input condition as described in Table 3. If all three Hall inputs are detected as identical states, this is an illegal condition and the device turns all outputs OFF.

Table 3. Hall Position Sensor Input Gray-Code Logic

COMMUTATION	F/R = LOW			F/R = HIGH			PHASE A		PHASE B		PHASE C	
STEP	IN1	IN2	IN3	IN1	IN2	IN3	UPPER	LOWER	UPPER	LOWER	UPPER	LOWER
A	L	L	H	H	H	L			PWM	Note 4		ON
B	L	H	H	H	L	L	PWM	Note 4				ON
C	L	H	L	H	L	H	PWM	Note 4		ON		
D	H	H	L	L	L	H				ON	PWM	Note 4
E	H	L	L	L	H	H		ON			PWM	Note 4
F	H	L	H	L	H	L		ON	PWM	Note 4		
Illegal	L	L	L	L	L	L	all OFF					
Illegal	H	H	H	H	H	H	all OFF					

NOTE 4: For the Half-H in which GUx is being switched by PWM, the complimentary LGx can be EEPROM programmed by a single bit to enable or disable synchronous rectification during $t_{(OFF)}$ of each PWM cycle. This allows configuration of the device for applications where synchronous rectification can or cannot be used.

digital PWM operation

In Table 3, the term PWM represents the pulse-width-modulation duty-cycle. PWM switching is implemented with the upper gate drive such that recirculation occurs in the lower external FET during the OFF portion of each period. Coast mode is enabled or disabled using EEPROM address 0, bit 4. Synchronous rectification mode is enabled or disabled using EEPROM address 0, bit 3.

An 8-bit digital PWM circuit uses an internal 5.8 Mhz oscillator as an input frequency. Each PWM period is defined by 255 ($2^8 - 1$) intervals where the number of ON intervals is controlled by the value of an 8-bit binary input word from the digital filter output. The PWM generator is implemented such that duty cycle is:

$$\text{Duty cycle} = \frac{n}{\left(2^8 - 1\right)} = \frac{n}{255}$$

Where:

n = decimal equivalent of the 8-bit binary input word

coast mode, (EEPROM address 0, bit 4, default = H)

When coast function is enabled (EEPROM address 0, bit 4 = H), the device uses a special mode to control speed of the motor when it exceeds the selected reference speed. Referring to Figure 10, when FGSOUT frequency exceeds $f_{(ref)}$ by 5%, resulting in a loss of lock detect, the high-side FET gate drives (UGx) are disabled and the low-side FET drives (LGx) continue to sequence as per the commutation table. This will continue until FGSOUT frequency drops below $f_{(ref)}$, which re-enables the high-side gate drives. The coast mode will override synchronous rectification mode if both are enabled (see following) after the FSGOUT signal exceeds $f_{(ref)}$.

PRINCIPLES OF OPERATION

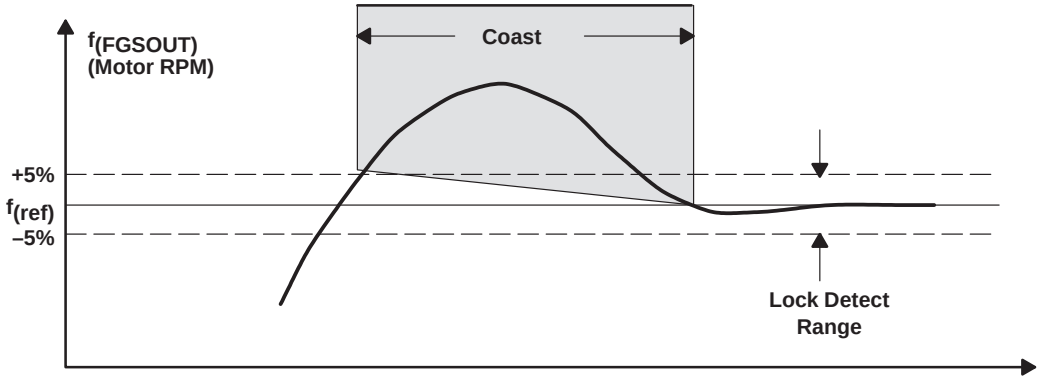


Figure 10. Coast Mode Operation

synchronous rectification mode (EEPROM address 0, bit 3, default = H for TPIC43T01, default = L for TPIC43T02)

The TPIC43T01 is set up with synchronous rectification enabled. With synchronous rectification enabled (EEPROM address 0, bit 3 = H), the complimentary LGx of the phase being pulse-width-modulated will turn ON inversely to UGx during each PWM cycle. This provides a low resistance path through the low-side FET, operating in inverse, for recirculating inductive current of the motor winding. This technique improves drive efficiency over allowing the inductive energy to recirculate through the FET's drain-body diode. Dead-time will be controlled in each half-H between upper to lower and lower to upper transitions to prevent high current conduction directly through the power FETs. During this dead-time, recirculation current, due to load inductance, will occur in the lower FET body diode. After dead-time, the complimentary LGx will be turned on, thus reducing power dissipation by using the lower FET in inverse to produce a lower voltage drop across $r_{DS(ON)}$ than would occur across V_F of the FET drain-body diode (see Figure 11).

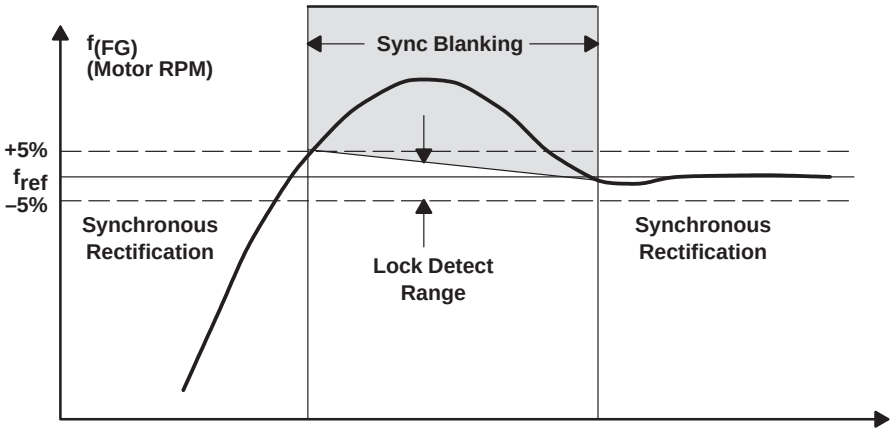


Figure 11. Synchronous Rectification/Coast Mode Operation

The TPIC43T02 is set up with synchronous rectification disabled. With synchronous rectification disabled (EEPROM address 0, bit 3 = L), the complimentary LGx will stay low during the OFF time of UGx, and inductive current will thus recirculate through the lower external FET drain-body diode for the duration of $t_{(OFF)}$.

PRINCIPLES OF OPERATION

digital integrator gain selections

In Table 4, EEPROM bits can be set for different clocking rates of the digital integrator. In effect, this allows for different integrator gain, thereby allowing the user to optimize loop performance (see Figure 12). The integrator circuit actually utilizes 14 bits with a 4-bit pre-integrator prior to the 10 bits which are output to the digital filter. This design increases resolution in the error detected by the speed discriminator while reducing the bit-count output to the digital filter.

Table 4. Digital Integrator Gain Selection Table

EEPROM ADDR 0 BIT 2	EEPROM ADDR 0 BIT 1	EEPROM ADDR 0 BIT 0	INTEGRATOR INPUT FREQUENCY DIVIDE DOWN	INTEGRATOR GAIN ADJUST	TYPICAL INTEGRATOR INPUT FREQUENCY
0	0	0	÷ 1†	0 dB	5.8 MHz
0	1	0	÷ 2	–6 dB	2.9 MHz
0	0	1	÷ 3	–9.5 dB	1.93 MHz
1	0	0	÷ 4	–12 dB	1.45 MHz
0	1	1	÷ 6	–15.5 dB	967 kHz
1	1	0	÷ 8	–18 dB	725 kHz
1	0	1	÷ 12	–21.5 dB	483 kHz
1	1	1	÷ 16	–24 dB	363 kHz

† Default setting for integrator clock.

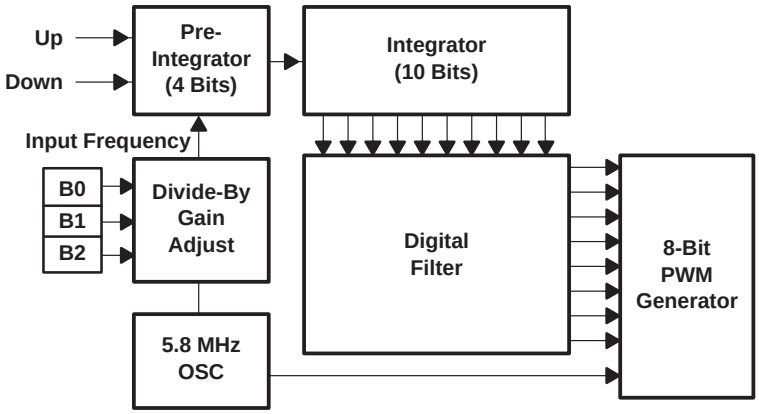


Figure 12. Integrator Implementation

PRINCIPLES OF OPERATION

digital filter coefficients

The two digital filter coefficients can be set by programming the EEPROM to select the pole and zero for the digital filter. The pole and zero values are directly proportional to the digital filter sample rate, $T_{(S)}$, and the filter gain is independent of $T_{(S)}$. The adjustment range of $T_{(S)}$ is from 250 μs to 1 ms (see Figure 13). The K1 lead coefficient value is stored in bits 2–7 of Address 1 as a BCD equivalent of the K1 coefficient. K1 has a range from 0 to 63, with a default setting of 28. See Table 5 for a typical range of pole and zero frequencies at $T_{(S)}$ = 500 μs. The K2 coefficient value is stored in bits 5–7 of Address 0 (see Table 6 and Figure 14).

The gain of the digital filter is given by the equation:

$$\text{OUT} = \frac{\text{IN} \times [128 \times Z - \text{K2}] \times 0.25}{Z - \text{K1}/128}$$

Where:

Z represents a delay of one period of the $f_{(S)}$ sampling clock.

The scaling factor of 0.25 in the above equation accounts for the difference in word lengths in the integrator (10 bits), the filter (17 bits) and the PWM generator (8 bits).

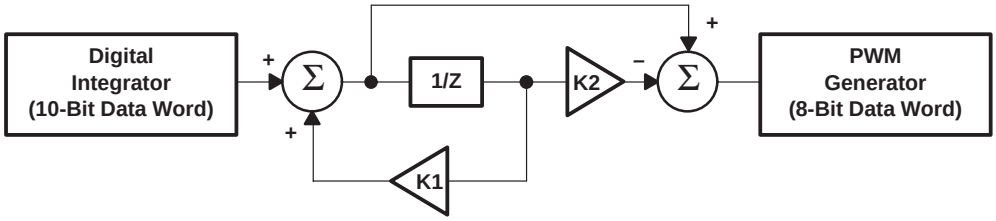


Figure 13. Digital Filter System Diagram

Table 5. Filter Zero and Gain as a Function of K2, Ts = 500 μs

K2	K1 = 14 (POLE = 704 Hz)		K1 = 28 (POLE = 483 Hz)		K1 = 56 (POLE = 263 Hz)	
	ZERO (Hz)	GAIN	ZERO (Hz)	GAIN	ZERO (Hz)	GAIN
127	6.2	0.28	4.8	0.32	3.7	0.45
126	12.4	0.28	9.7	0.32	7.3	0.45
125	18.4	0.42	14.5	0.48	11	0.68
124	24.7	0.28	19.3	0.32	14.6	0.45
123	30.9	0.35	24.2	0.4	18.3	0.56
122	37.1	0.42	29	0.48	21.9	0.68
121	43.3	0.25	33.9	0.28	25.6	0.39
120	49.4	0.28	38.7	0.32	29.2	0.45

PRINCIPLES OF OPERATION

Table 6. Digital Coefficient Truth Table

EEPROM ADDR 0 BIT 7	EEPROM ADDR 0 BIT 6	EEPROM ADDR 0 BIT 5	K2 COEFFICIENT
0	0	0	120
0	0	1	121
0	1	0	122
0	1	1	123
1	0	0	124†
1	0	1	125
1	1	0	126
1	1	1	127

† Default setting for the digital filter coefficient

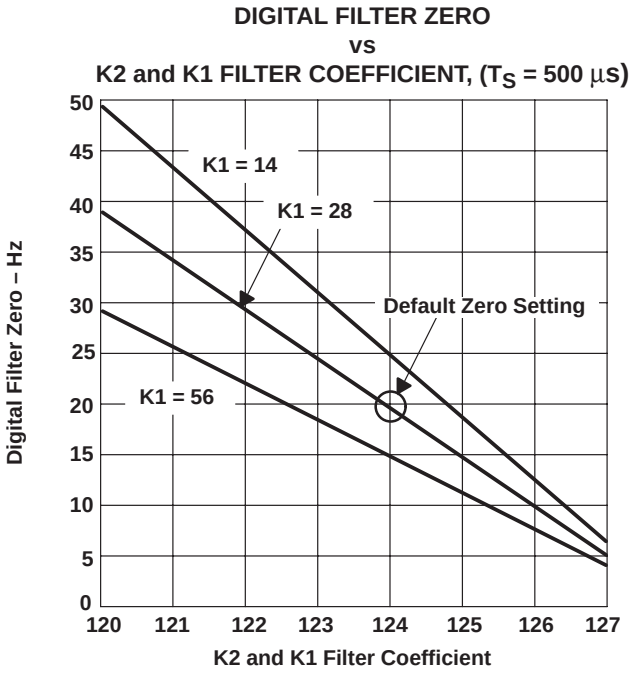


Figure 14. Digital Filter Coefficient

FG watchdog

The FG watchdog monitors FGOUT output, allowing an internal timer to count until a transition in FGOUT occurs and clears the counter. Should timer time-out occur by reaching a count equivalent to 25 ms (512 counts of the PWM clock), two actions are taken: 1) speed discriminator UP error output is set to 100%; 2) lock detect is set and lock timer begins counting (see *lock timer oscillator/counter* section). These actions ensure the digital integrator counts up (increasing motor drive PWM) at startup of the system, or, if the FG signal is lost during operation and if no detection of an FG period of < 25 ms occurs for the duration of the lock timer, the IC will go into shutdown mode, disabling the motor drive (see *shutdown* section).

PRINCIPLES OF OPERATION

current limit/over-current shutdown

Referring to Figure 15, two comparators monitor the voltage drop across an external current sensing resistor, $R_{(SENSE)}$. The sensed voltage, $V_{(SENSE)}$, is then compared against two V_{CC} referred voltages, V_L and $V_{(OCSD)}$. When $V_{(SENSE)}$ exceeds V_L, the ILIM comparator outputs a high level. When $V_{(SENSE)}$ exceeds $V_{(OCSD)}$, the OCSD comparator also outputs a high level. The combination of these two comparator outputs is then used in conjunction with a deglitch or blanking timer to discriminate between a high di/dt, short-duration current spike. This spike is commonly caused by reverse recover time (t_{rr}) current at the start of each PWM cycle and a portion of the current waveform with lower di/dt. The lower di/dt is controlled by the L/R time constant of the motor winding (see Figure 16). A comparator is also used to detect over current conditions caused by a shorted-load or shorted phase-winding to GND (see Figure 17).

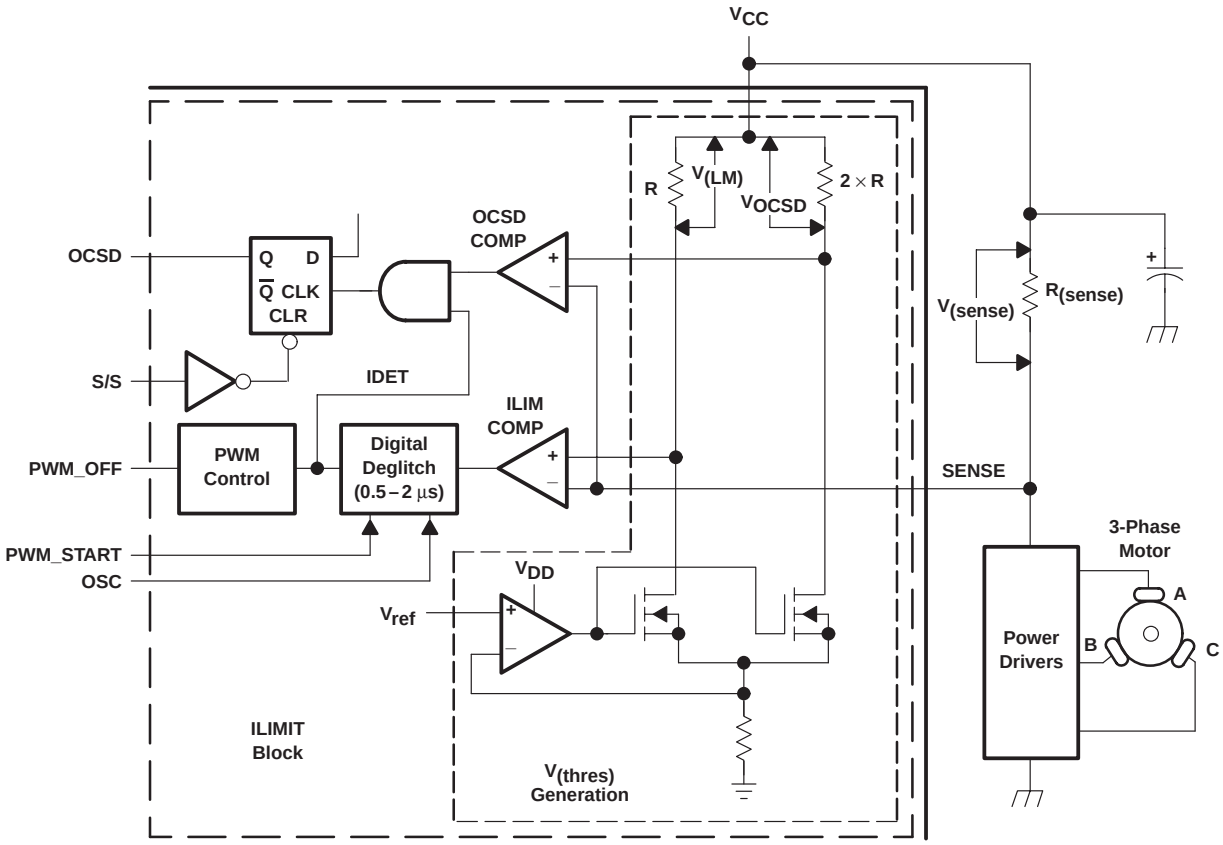


Figure 15. ILIMIT/OCSD Diagram

PRINCIPLES OF OPERATION

current limit/over-current shutdown (continued)

The deglitch timer prevents the ILIM COMP high from being recognized unless it occurs for the duration of the timer, after which a high IDET level occurs. This IDET level is used to terminate, or latch off the upper gate drive being driven by PWM for the remainder of the PWM interval. This ILIM latch and deglitch timer clears at the start of each new PWM cycle; thus, a cycle-by-cycle PWM controlled current limit is implemented.

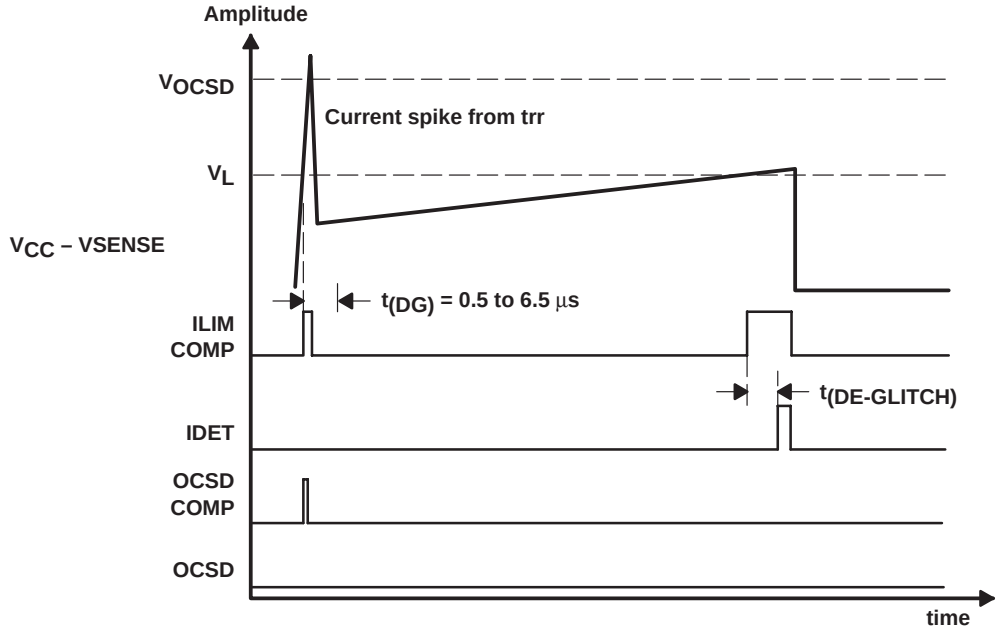


Figure 16. Normal Motor Current Waveform With trr Spike at Start of PWM Cycle

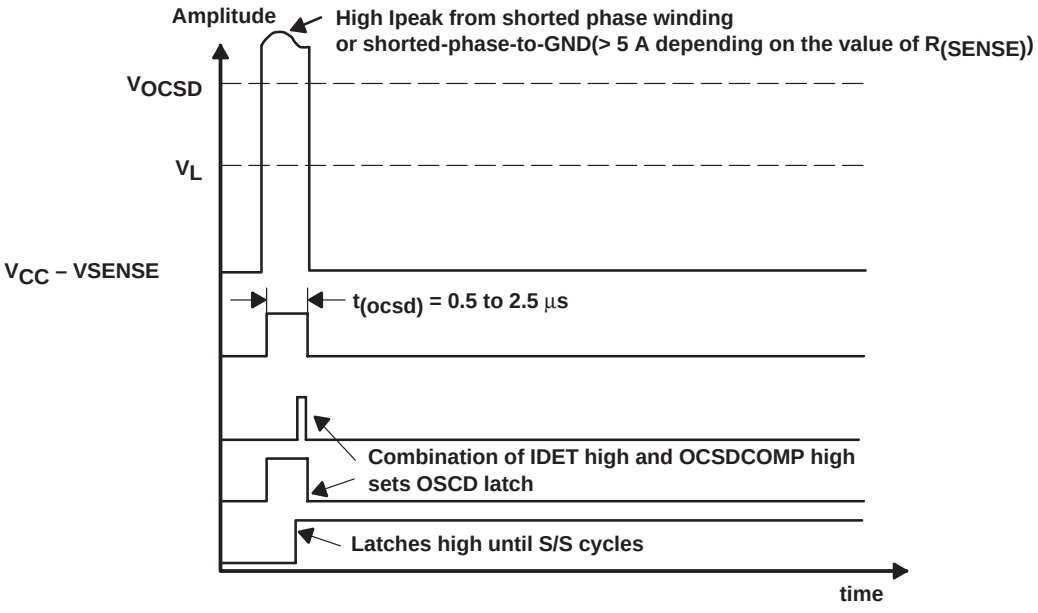


Figure 17. Motor Current Waveform With Shorted Phase Winding or Shorted Phase to GND

PRINCIPLES OF OPERATION

EEPROM registers

There are two user configurable EEPROM bit registers accessible through the serial test interface when the device is configured in TEST mode. This mode is enabled when the TEST pin is held high at 5 V. Once the device is placed in TEST mode, either register can be programmed by transmitting a 16-bit word. The first three bits of this transmission are the address and R/W for the register the user wishes to modify. The next five bits must be held low, and the remaining eight bits are configuration bits. Each register must be programmed independently, i.e. once the register value is written, the V_{PP} pin must immediately be taken to 13.5 V in the manner described in the *EEPROM Programming* section. The two EEPROM registers are summarized in Table 7. A detailed definition outlining the function of each bit in the EEPROM is presented in the respective functional description sections of this specification (see Notes 5 and 6).

Table 7. EEPROM Register Definition

ADDR	EEPROM REGISTER CONFIGURATION BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	K2 Coefficient			Coast Enable	Synchronous Rectification	Integrator Gain Select		
TPIC43T01 default	1	0	0	1	1	0	0	0
TPIC43T02 default	1	0	0	1	0	0	0	0
1	K1 Coefficient						FG Frequency Select	
TPIC43T01 default	0	1	1	1	0	0	1	1
TPIC43T02 default	0	1	1	1	0	0	1	1

NOTES: 5. Bit 0 in the EEPROM register definition table corresponds to D0 and E0 in the serial protocol sequence.
6. Data read out of the EEPROM corresponds to the contents of the register at the time it is read. (A register can be read after programming it in order to verify that the EEPROM was programmed properly.)

serial test interface

User-programmable functions are controlled using two 16-bit EEPROM registers. These registers are programmed by placing the device in program/test mode by pulling the TEST pin high and transferring data using the serial interface. Pins 14 and 17–19 are multipurpose pins, which are configured for serial test mode when the TEST pin is high (see Table 8).

Table 8. Serial Test Interface Pin Definition

PIN NAME	PIN NO.	PIN DESCRIPTION
SO	14	Serial data output. SO is an output terminal that reads data from the EEPROM.
SCLK	17	Serial clock. SCLK clocks the shift register. Serial data is clocked into the serial data input (SI) port on the rising edge of the serial clock. Serial output data is clocked out of the serial data output (SO) port on the rising edge of the serial clock.
SIENB	18	Serial transfer enable. A low to high transition on the SIENB pin enables the serial interface to send or receive data (see Figure 2). The SIENB signal must be taken low after 16 bits of data has been transferred to insure data has been loaded into the proper bit locations. During program mode, the V_{PP} input is strobed after SIENB is taken low to program the EEPROM.
SI	19	Serial input. SI is an input terminal to load the EEPROM input register.
V_{PP}	35	EEPROM program voltage. V_{PP} transfers data from the EEPROM input register to the respective address location.
TEST	36	Serial interface/test mode enable. TEST is taken high to enable the serial interface.

PRINCIPLES OF OPERATION

EEPROM programming

Figure 18 presents the sequence of events required to program the onboard EEPROM. To begin the procedure, the device must be placed into test mode by setting V_{PP} to GND, TEST to V_{DD} and V_{CC} > 8 V. The SIENB input must transition high to enable the serial input port (see Figure 19). Serial data is clocked into SI on the rising edges of SCLK. Sixteen bits of data must be transferred during each serial transfer and SIENB must be set to 0 after the sixteenth clock. The first two bits transferred select the EEPROM address to be manipulated. Address bit A0 is the least significant bit (LSB). The third bit sets the interface into read or write mode. A 1 selects a read operation from the EEPROM and a 0 selects a write operation to the EEPROM. Set the next five unused bits to 0. The next 8 bits of data are used for write operations, and are unused and should be set to zero for read operations. The definition of the data word is presented in Table 7. SIENB must be set to 0 after the 16-bit transfer has been completed. When new data is being programmed into the EEPROM, the V_{PP} pin must transition to 13.5 V for at least 5 ms and then back to GND (see Figure 20). This completes the serial transfer and programming sequence. Another transfer can begin using the same procedure. Only one register can be programmed at a time. The TEST pin must be set to 0 after programming has been completed to disable the serial test mode and reconfigure the multipurpose pins for normal operation.

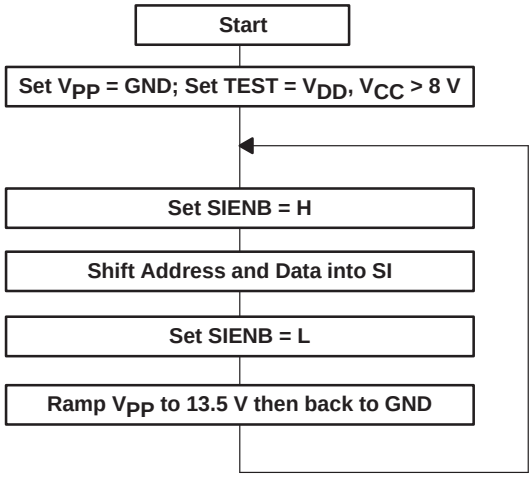


Figure 18. Recommended EEPROM Programming Sequence

PRINCIPLES OF OPERATION

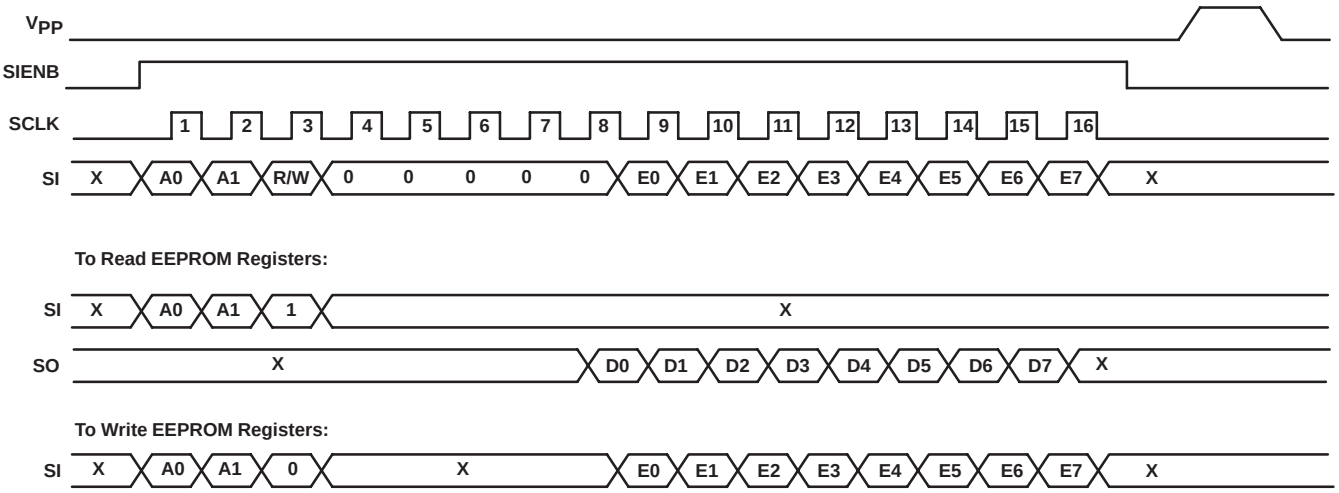


Figure 19. Serial Protocol

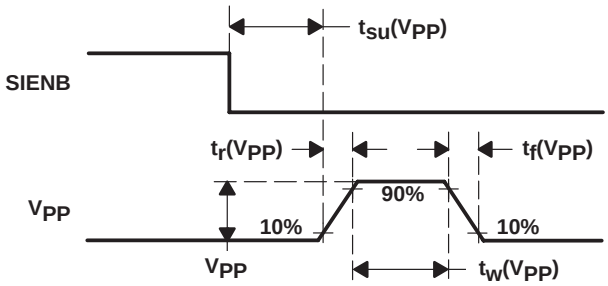


Figure 20. V_{PP} Programming Waveforms

PRINCIPLES OF OPERATION

charge pump

An external charge pump capacitor (CP) is connected across the CP1 and CP2 pins. An external storage capacitor (CS) with a typical value of 0.01 μF is connected from V_{CP} to V_{CC} (see *functional block diagram*). The charge pump output, V_{CP}, powers the high-side gate drive circuitry for the pre-FET drivers. An internal CPUV monitors the voltage between V_{CP} and V_{CC} and disables all outputs through a signal to the global shutdown circuit until $V_{CP} - V_{CC} \geq 5$ V. The V_{CP} voltage level is internally regulated to V_{CC} + 15 V (typical).

pre-FET drivers

The TPIC43T01/02 contains three pre-FET driver blocks, each with an upper and lower gate drive for driving the gates of two external power NMOS FETs configured as a half H-power stage (see Figure 21). The TPIC43T01/02 is designed to drive the TI TPIC1310 Power+ Array, but it is capable of driving discrete N-channel FET devices as well. Each pre-FET gate output is capable of sourcing at least 60 mA peak current and sinking at least 100 mA peak of current. The lower gate drive outputs provide V_{GS} to the external FET from 14 to 20 V. The upper gate drive outputs drive the external FET gate from V_{CP} and provide V_{GS} voltage protection (clamp UGx pin with respect to Phx pin) to prevent the gate voltage from exceeding 19 V and damaging the external FET in the event of a shorted-load or shorted-phase winding to ground.

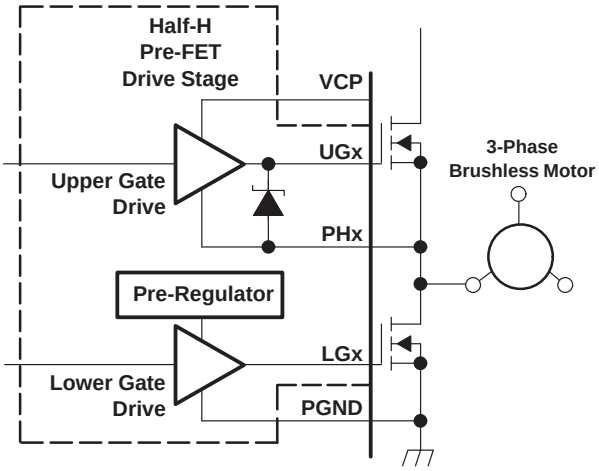
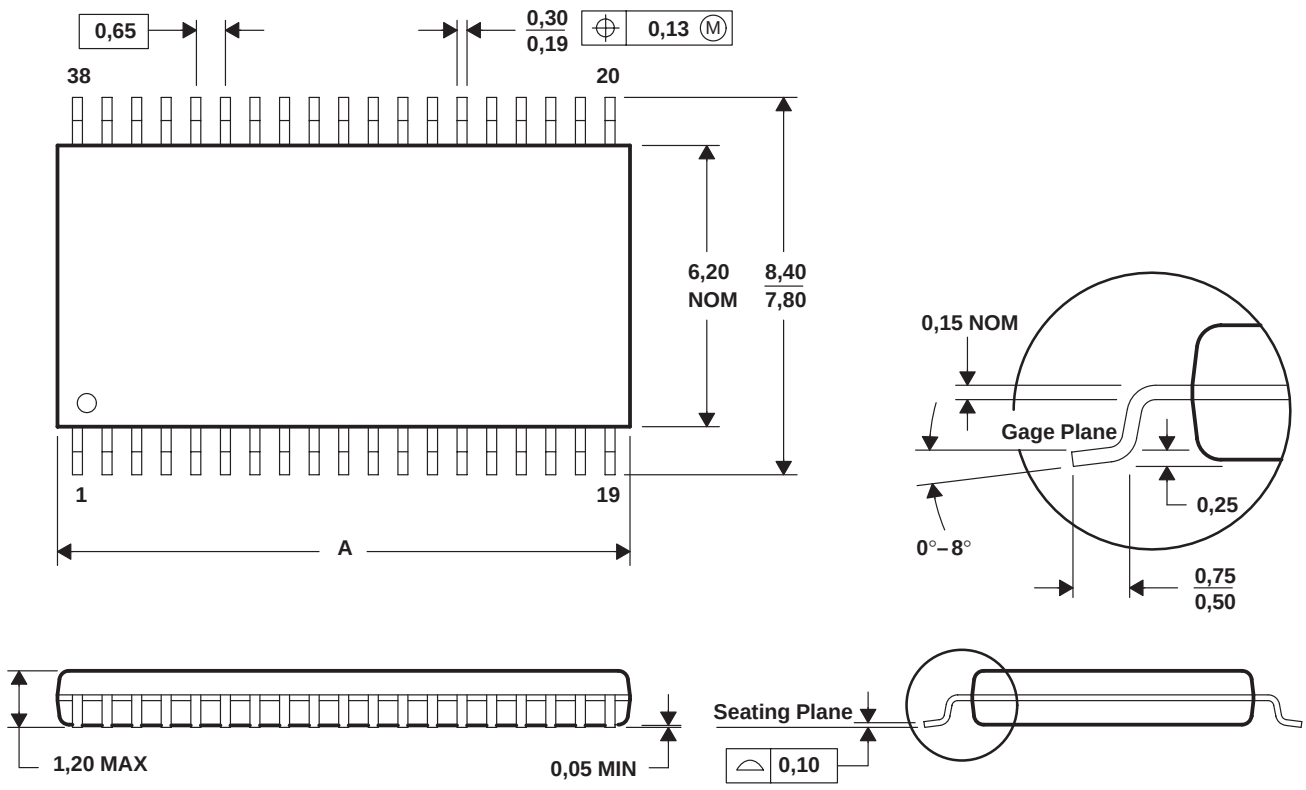


Figure 21. Pre-FET Driver Output Stage

MECHANICAL DATA

DA (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

38 PIN SHOWN



DIM \ PINS **	28	30	32	38
A MAX	9,80	11,10	11,10	12,60
A MIN	9,60	10,90	10,90	12,40

4040066/C 10/95

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.
D. Falls within JEDEC MO-153

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