- **Complete Discrete Multitone (DMT)-Based Asymmetric Digital Subscriber Line (ADSL) Coder/Decoder (Codec) Solution**
- **Complies With ANSI T1.413, Issue 2 and ITU G.992.1**
- **Supports up to 8-Mbit/s Downstream and 800-kbit/s Upstream Duplex**
- **Integrated 14-Bit Converter for Transmitter/Receiver**
- **Integrated Transmit/Receive (TX/RX) Channel Filters**
- **Integrated TX/RX Attenuation/Gain**
- **Integrated Reference**
- **High-Speed Parallel Interface**
- **2s-Complement Data Format**
- **Selectable 2.2-MSPS or 4.4-MSPS Parallel Data Transfer Rate**
- **Serial Configuration Port**
- **Eight General-Purpose (GP) Output Terminals**
- **Supports Multiple-Channel Configuration**
- **Single 3.3-V Supply**
- **Hardware/Software Power Down**
- **–40°C to 85°C Operation**
- **Packaged in 100-Pin Plastic Quad Flatpack**

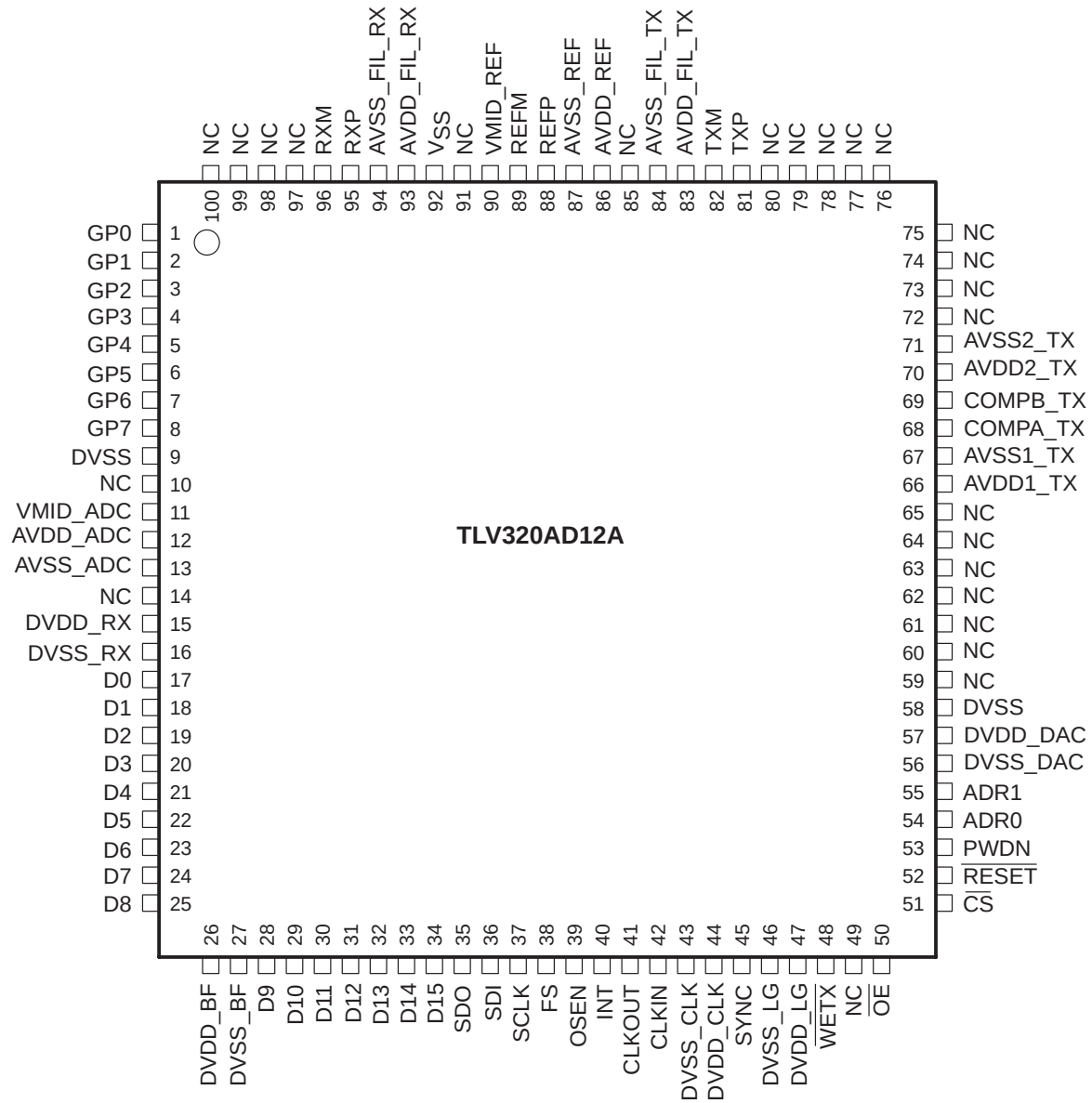
description

The TLV320AD12A is a high-speed coder/decoder (codec) for central office-side (CO) discrete-multitone (DMT) asymmetric-digital subscriber line (ADSL) access that supports ANSI Std T1.413, Issue 2 and ITU G.992.1. The codec is a low-power device comprised of five major functional blocks: transmitter (TX), receiver (RX), clock, reference, and host interface.

The transmit channel consists of a 25.875-kHz to 1.104-MHz digital band-pass filter, a 14-bit, 8.832-MSPS DAC, a 1.104-MHz analog low-pass filter, and a transmit attenuator. The receiver channel consists of a two programmable-gain-amplifier stages (PGA), a 138-kHz analog low-pass filter, a 14-bit, 4.416-MSPS ADC, a 138-kHz digital low-pass filter. An onboard reference circuit generates 1.5-V reference voltage for the converters.

The codec has two interface ports: a parallel port for data transfer, and a serial port for control. The parallel port is 16 bits wide, and is reserved for moving data between the codec and a DSP, such as the TMS320C6XX. Configuration is done via the serial port. A special interface scheme enables multichannel system design. The TLV320AD12A can be powered down via a dedicated terminal or through software control to reduce heat dissipation. Additionally, there is a general-purpose (GP) port consisting of eight output terminals for control of external circuitry.

PZ PACKAGE
(TOP VIEW)



No connection (leave open)

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
ADR0 ADR1	54 55	I	Serial-port chip ID address. ADR0 is the least significant bit.
AVDD_ADC	12	I	Analog-to-digital converter (ADC) analog power supply
AVDD1_TX	66	I	TX-channel analog power supply 1
AVDD2_TX	70	I	TX-channel analog power supply 2
AVDD_FIL_RX	93	I	RX-channel filter analog power supply
AVDD_FIL_TX	83	I	TX-channel filter analog power supply
AVDD_REF	86	I	Reference analog power supply
AVSS_ADC	13	I	ADC analog ground
AVSS1_TX	67	I	TX-channel analog ground 1
AVSS2_TX	71	I	TX-channel analog ground 2
AVSS_FIL_RX	94	I	RX-channel filter analog ground
AVSS_FIL_TX	84	I	TX-channel filter analog ground
AVSS_REF	87	I	Reference analog ground
CLKIN	42	I	35.328-MHz external oscillator clock input
CLKOUT	41	O	4.416-MHz clock output
COMPA_TX	68	I	TX-channel decoupling capacitor input A (add 500 pF X7R ceramic capacitor to AVDD1_TX)
COMPB_TX	69	I	TX-channel decoupling capacitor input B (add 1-μF X7R ceramic capacitor to AVDD1_TX)
$\overline{CS}$	51	I	Parallel-port chip select
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	34 33 32 31 30 29 28 25 24 23 22 21 20 19 18 17	I/O	(MSB) Parallel-port data. D0 is the least significant bit. (LSB)
DVDD_BF	26	I	Digital I/O buffer power supply
DVDD_CLK	44	I	Digital clock power supply
DVDD_DAC	57	I	Digital power supply for digital-to-analog converter (DAC)
DVDD_LG	47	I	Digital logic power supply
DVDD_RX	15	I	Digital power supply for RX channel
DVSS	9, 58	I	Digital ground
DVSS_BF	27	I	Digital I/O buffer ground
DVSS_CLK	43	I	Digital clock ground
DVSS_DAC	56	I	Digital ground for DAC
DVSS_LG	46	I	Digital logic ground

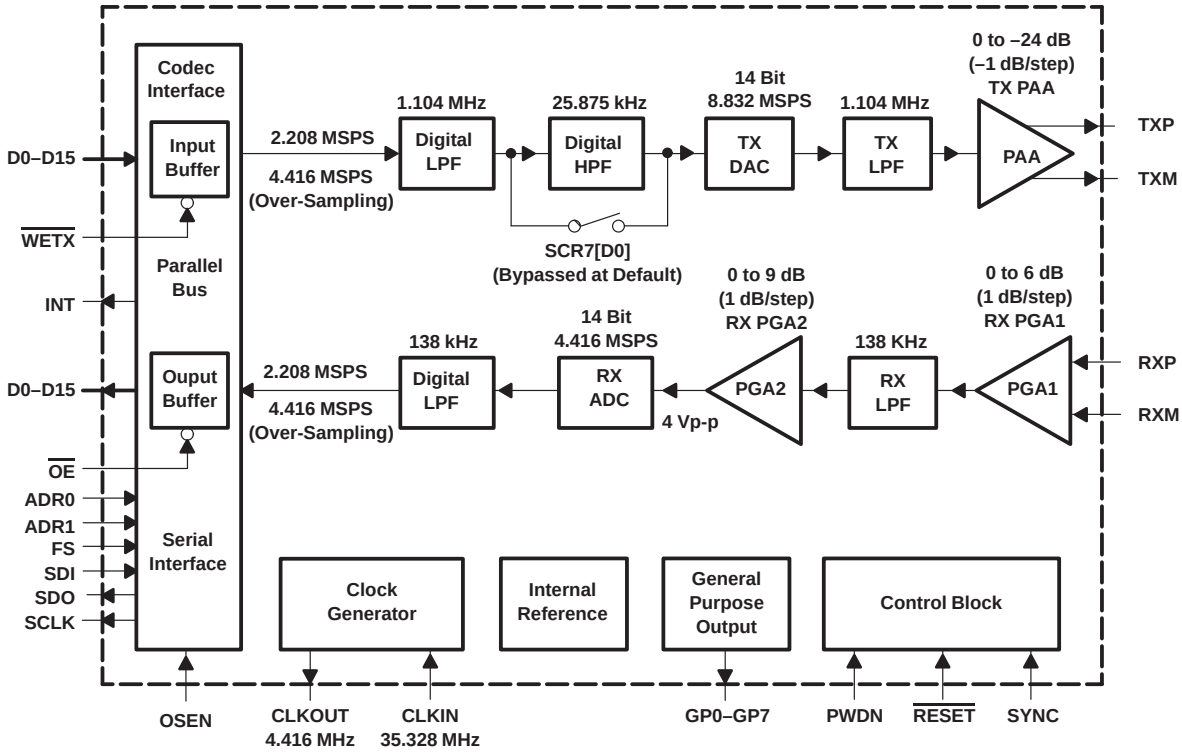
† I = input, O = output, I/O = 3-state input/output

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O†	DESCRIPTION
DVSS_RX	16	I	Digital ground for RX channel
FS	38	I	Frame sync input
GP7 GP6 GP5 GP4 GP3 GP2 GP1 GP0	8 7 6 5 4 3 2 1	O	General-purpose output port
INT	40	O	Data rate clock output (INT is 4.416 MHz when OSEN = 1, 2.208 MHz when OSEN = 0)
NC	10, 14, 49, 59, 60, 61, 62, 63, 64, 65, 72, 73, 74, 75, 76, 77, 78, 79, 80, 85, 91, 97, 98, 99, 100		No connection. All the NC pins should be left open.
$\overline{OE}$	50	I	Parallel-port output enable from host processor
OSEN	39	I	Over-sampling enable input. OSEN = 1 enables oversampling mode (INT = 4.416 MHz)
PWDN	53	I	Power-down input. When PWDN = 0, the device is in normal operating mode. When PWDN = 1, the device is in hardware power-down mode.
REFM	89	O	Decoupling reference voltage minus. Add 10-µF tantalum and 0.1-µF X7R ceramic capacitors to AVSS_REFP. The normal dc voltage at this terminal is 0.5 V. See figure 7 for the configuration.
REFP	88	O	Decoupling reference voltage plus. Add 10-µF tantalum and 0.1-µF X7R ceramic capacitors to AVSS_REFM. The normal dc voltage at this terminal is 2.5 V. See figure 7 for the configuration.
$\overline{RESET}$	52	I	Hardware system reset. An low level will reset the device.
RXM	96	I	Receive RX input minus. RXM is self-biased to AVDD_FIL_RX/2.
RXP	95	I	Receive RX input plus. RXP is self-biased to AVDD_FIL_RX/2.
SCLK	37	O	Serial clock output
SDI	36	I	Serial data input
SDO	35	O	Serial data output
SYNC	45	I	SYNC pulse for clock synchronization. A high pulse to the pin synchronizes the internal clock operation. The default state of the pin is low. Refer to Figure 3 for detail. Tie the SYNC terminal to the DVSS_LG terminal for autosynchronization.
TXM	82	O	Transmit output minus
TXP	81	O	Transmit output plus
VMID_ADC	11	O	Decoupling 1.5 V for ADC. Add 10-µF tantalum, and 0.1-µF X7R ceramic capacitors to AVSS_ADC.
VMID_REF	90	O	Decoupling 1.5 V reference voltage. Add 10-µF tantalum, and 0.1-µF X7R ceramic capacitors to AVSS_REF.
V_{SS}	92	I	Substrate. Connect V_{SS} to analog ground.
$\overline{WETX}$	48	I	Parallel-port write enable for TX channel from host processor

† I = input, O = output, I/O = 3-state input/output

functional block diagram



functional description

The TLV320AD12A is a low-power device consisting of transmitter, receiver, clock, reference, and host interface (see the functional block diagram). It is designed to be paired with the TLV320AD11A remote terminal-side (RT) codec.

The TLV320AD12A transmit channel consists of a 1.104-MHz digital low-pass filter (LPF), a 25.875-kHz high-pass filter (HPF) that can be enabled, a 14-bit, 8.832-megabyte samples-per-second (MSPS) digital-to-analog converter (DAC), a 1.104-MHz analog LPF, and a programmable amplifier attenuator (PAA). The receive channel consists of a two-stage programmable gain amplifier (PGA), a 138-kHz analog LPF, a 14-bit, 4.416-MSPS analog-to-digital converter (ADC), and a 138-kHz digital LPF. An onboard reference circuit generates a 1.5-V reference for the converters.

transmit channel

The transmit channel contains a high-performance, 14-bit DAC that operates at an 8.832 MHz sampling rate and provides a 4× oversampling to reduce the DAC noise. The low-pass filter limits the output of the transmitter to 1.104 MHz. The programmable attenuator, with a range of 0 dB to 24 dB in –1-dB steps, drives the external ADSL line driver. The TX HPF can be enabled by software control as shown in the functional block diagram.

receive channel

The receive channel contains a high-performance, 14-bit ADC that operates at a 4.416-MHz sampling rate and provides 16x oversampling to reduce the antialiasing noise. The two PGAs reduce the dynamic-range requirement of the high-resolution ADC. The two LPFs limit the input signal bandwidth to 138 kHz.

functional description (continued)

clock generation

The clock generator provides the necessary clock signals for the device. The external oscillator specifications are:

- 3.3-V supply
- 35.328 MHz, ±50 PPM
- 60/40 minimum duty cycle (50/50 is optimum)

Table 1 describes the major clocks generated internally.

Table 1. Clock Description

CLOCK	FREQUENCY (MHz)	
	OSEN = 0	OSEN = 1
INT	2.208	4.416
CLKOUT	4.416	4.416
SCLK	4.416	4.416

INT

The interrupt (INT) to the host processor is 4.416 MHz when OSEN = 1 and 2.208 MHz when OSEN = 0.

CLKOUT

The 4.416-MHz clock output (CLKOUT) is synchronous with the master clock (35.328 MHz).

SCLK

The serial clock (SCLK) output, used in the serial codec interface, has a fixed frequency of 4.416 MHz and is synchronous with the master clock (35.328 MHz).

parallel interface

The TLV320AD12A codec has a 16-bit parallel interface for TX and RX data. The input and output buffers (see diagram) are updated at either 2.208 MSPS or 4.416 MSPS (over-sampling mode). Strobes $\overline{OE}$ and $\overline{WETX}$ (from the host transceiver) are edge-triggered signals. Incoming data is registered on the rising edge of $\overline{WETX}$. Output data from the codec is enabled after the falling edge of $\overline{OE}$, and is disabled after the rising edge of $\overline{OE}$. The INT cycle time is hardware configurable for either 4.416 MHz (OSEN = 1), or 2.208 MHz (OSEN = 0).

For the 16-bit parallel data, D0 is the LSB and D15 is the MSB. The parallel TX and RX data contains 16 valid bits. All 16 bits are used in the digital filtering.

keep-out zones (KOZs)

The last clock input (CLKIN cycle) before a transition of CLKOUT is defined as a keep-out zone (KOZ). These zones are reserved for sampling of analog signals. All digital I/Os (except CLKIN) should be quiet during these keep-out zones.

oversampling mode

The OSEN pin selects 2× oversampling mode (INT running at 4.416 MHz), or 1× oversampling mode (INT running at 2.208 MHz).

serial interface

The serial port is used for codec configuration and register reading. The word length is 16 bits. Two hardware-configuration terminals, ADR1 and ADR0, are used to configure the device identification (ID). Up to four codecs can be identified for each common serial port.

serial interface (continued)

The master codec (ADR[1:0] = 00) provides SCLK to the host processor. The SCLK terminals on the other codecs are left unconnected. All the codecs in a multicodec system should be synchronized by SYNC pin so that their SCLK signals are in phase—even though the slave's SCLKs are not being used. This ensures proper latching of the data to the codec.

SCLK is a continuously-running 4.416-MHz fixed-frequency clock. The clock is synchronized to the codec internal events and CLKOUT (to the host), so the KOZs can be observed. A host DSP can drive the FS (synchronized to the CLKOUT from codec) into the codec to initiate a 16-bit serial I/O frame.

general-purpose (GP) port

The GP port provides eight outputs. Each output is capable of delivering 0.5 mA for control of external circuitry such as LEDs, gain control, and power down.

internal voltage reference

The built-in reference provides the needed reference voltage and current to individual analog blocks. It is also brought out to external terminals for noise decoupling.

register programming

See Figure 4 for timing and format details.

Table 2. System Control Register (SCR)

REGISTER		MODE	FUNCTION
NAME	ADDRESS S3, S2, S1, S0		
SCR0	0000	R	D6: chip ID = 1
		W	D0: software reset (self clearing). D1–D7 reserved.
SCR1	0001	R/W	D[4:0]= transmit-channel PAA control.
SCR2	0010	R/W	D[3:0] = receive-channel PGA2 control.
SCR3	0011	R/W	D[2:0] = receive-channel PGA1 control.
SCR4	0100		Reserved
SCR5	0101		Reserved
SCR6	0110	R/W	D[7:0] = general-purpose output control.
SCR7	0111	R/W	Miscellaneous control (set to 1 to enable) D0: enable TX DHPF (25.875 kHz) D1: software power-down RX channel with reference on D2: software power-down TX channel with reference on D3: analog loopback. TXP and TXM are internally connected to RXP and RXM. D4: digital loopback. RX channel digital output is internally connected to TX channel digital input. D5: TX parallel interface (read-back) test mode enable D6–D7: reserved
SCR8	1000	R/W	Reserved
SCR9	1001	R/W	D[7:0] = receive-channel offset word [7:0]
SCR10	1010	R/W	D[7:0] = receive-channel offset word [15:8]

NOTES: 1. All blank bits should be filled with 0s during register write operation.
2. All registers, except for chip ID, are set to 0 at power on.

register programming (continued)

SCR0 – system control register Address:0000b contents at reset: 01000000b

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	1	0	0	0	0	0	0	40	Chip ID = 1 (read only)
0	1	0	0	0	0	0	1	41	S/W reset (self clearing). All control registers are set to reset content.

SCR1 – TX PAA control register Address:0001b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	TX PAA gain = 0 dB
0	0	0	0	0	0	0	1	01	TX PAA gain = –1 dB
0	0	0	0	0	0	1	0	02	TX PAA gain = –2 dB
0	0	0	0	0	0	1	1	03	TX PAA gain = –3 dB
0	0	0	0	0	1	0	0	04	TX PAA gain = –4 dB
0	0	0	0	0	1	0	1	05	TX PAA gain = –5 dB
0	0	0	0	0	1	1	0	06	TX PAA gain = –6 dB
0	0	0	0	0	1	1	1	07	TX PAA gain = –7 dB
0	0	0	0	1	0	0	0	08	TX PAA gain = –8 dB
0	0	0	0	1	0	0	1	09	TX PAA gain = –9 dB
0	0	0	0	1	0	1	0	0A	TX PAA gain = –10 dB
0	0	0	0	1	0	1	1	0B	TX PAA gain = –11 dB
0	0	0	0	1	1	0	0	0C	TX PAA gain = –12 dB
0	0	0	0	1	1	0	1	0D	TX PAA gain = –13 dB
0	0	0	0	1	1	1	0	0E	TX PAA gain = –14 dB
0	0	0	0	1	1	1	1	0F	TX PAA gain = –15 dB
0	0	0	1	0	0	0	0	10	TX PAA gain = –16 dB
0	0	0	1	0	0	0	1	11	TX PAA gain = –17 dB
0	0	0	1	0	0	1	0	12	TX PAA gain = –18 dB
0	0	0	1	0	0	1	1	13	TX PAA gain = –19 dB
0	0	0	1	0	1	0	0	14	TX PAA gain = –20 dB
0	0	0	1	0	1	0	1	15	TX PAA gain = –21 dB
0	0	0	1	0	1	1	0	16	TX PAA gain = –22 dB
0	0	0	1	0	1	1	1	17	TX PAA gain = –23 dB
0	0	0	1	1	0	0	0	18	TX PAA gain = –24 dB
–	–	–	–	–	–	–	–	19–FF	Reserved (see Note 3)

NOTE 3: The performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.

programming (continued)

SCR2 – RX PGA2 control register Address:0010b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	RX PGA2 = 0 dB
0	0	0	0	0	0	0	1	01	RX PGA2 = 1 dB
0	0	0	0	0	0	1	0	02	RX PGA2 = 2 dB
0	0	0	0	0	0	1	1	03	RX PGA2 = 3 dB
0	0	0	0	0	1	0	0	04	RX PGA2 = 4 dB
0	0	0	0	0	1	0	1	05	RX PGA2 = 5 dB
0	0	0	0	0	1	1	0	06	RX PGA2 = 6 dB
0	0	0	0	0	1	1	1	07	RX PGA2 = 7 dB
0	0	0	0	1	0	0	0	08	RX PGA2 = 8 dB
0	0	0	0	1	0	0	1	09	RX PGA2 = 9 dB
–	–	–	–	–	–	–	–	0A–FF	Reserved (see Note 3)

NOTE 3: The performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.

SCR3 – RX PGA1 control register Address:0011b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0	0	0	0	0	0	0	0	00	RX PGA1 = 0 dB
0	0	0	0	0	0	0	1	01	RX PGA1 = 1 dB
0	0	0	0	0	0	1	0	02	RX PGA1 = 2 dB
0	0	0	0	0	0	1	1	03	RX PGA1 = 3 dB
0	0	0	0	0	1	0	0	04	RX PGA1 = 4 dB
0	0	0	0	0	1	0	1	05	RX PGA1 = 5 dB
0	0	0	0	0	1	1	0	06	RX PGA1 = 6 dB
–	–	–	–	–	–	–	–	06 – FF	Reserved (see Note 3)

NOTE 3: The performance of the codec for invalid combination of bits is not guaranteed and such combinations should not be used. The user should make no assumption that the code bits will saturate to a maximum or minimum value or wrap around to a valid combination.

SCR6 – general-purpose output data register Address:0110b contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
0/1	–	–	–	–	–	–	–		GP7 = low(0)/high(1)
–	0/1	–	–	–	–	–	–		GP6 = low(0)/high(1)
–	–	0/1	–	–	–	–	–		GP5 = low(0)/high(1)
–	–	–	0/1	–	–	–	–		GP4 = low(0)/high(1)
–	–	–	–	0/1	–	–	–		GP3 = low(0)/high(1)
–	–	–	–	–	0/1	–	–		GP2 = low(0)/high(1)
–	–	–	–	–	–	0/1	–		GP1 = low(0)/high(1)
–	–	–	–	–	–	–	0/1		GP0 = low(0)/high(1)

programming (continued)

SCR7 – miscellaneous control register 1 Address:0111b Contents at reset: 00000000b

D7	D6	D5	D4	D3	D2	D1	D0	REGISTER VALUE (HEX)	DESCRIPTION
–	–	–	–	–	–	–	1		Enable TX digital high–pass filter (25.875 kHz)
–	–	–	–	–	–	1	–		S/W power-down RX channel
–	–	–	–	–	1	–	–		S/W power-down TX channel
–	–	–	–	1	–	–	–		Analog loop-back (see Note 4)
–	–	–	1	–	–	–	–		Digital loop-back (see Note 5)
–	–	1	–	–	–	–	–		TX parallel interface (read-back) test mode enable (see Note 6)
0	0	–	–	–	–	–	–		Reserved

NOTES: 4. Analog loop-back: Analog output pins (TXP/TXM) are internally connected to RXP/RXM.
5. Digital loop-back: RX digital output buffer (16–bit word) is internally connected to the TX digital input buffer.
6. The input digital data is read back from RX output buffer without going through DAC converter.

SCR9 – RX offset control register[7:0] Address:1001b contents at reset: 00000000b

SCR10 – RX offset control register [15:8] Address:1010b contents at reset: 00000000b.

These two registers are combined together to form a 16-bit word in 2s-complement data format. The 16-bit word is used to adjust the RX channel DC offset error. The 16-bit RX ADC data will perform a plus operation with the 16-bit word before it is sent to the receive output buffer.

device initialization time

The TLV320AD12A completes all calibration and initialization in less than 1 second. This includes time for reference setting (~950 μs), one serial frame rest after power up, four serial frames for TX/RX gain select, and time for calibration of the DAC (256 × 113 ns). Each 16-bit frame requires up to 5 μs for completion. The host processor initiates this process upon a successful power-on condition, or recovery from a power-down mode.

power down

Both hardware and software power-down modes are provided. All of the digital interfaces and references are operative when the codec is in the software power-down mode. Power down of either or both the TX and RX channels can be invoked through software control. A logic 1 on the power-down (PWDN) input shuts down the codec completely.

multiple-channel configuration

The TLV320AD12A is designed with multiple-channel configuration capability. Up to four devices can be designed in a system. Each device works at 2.208 MSPS and shares the parallel data bus as selected by the chip select ($\overline{CS}$) signal. The serial bus is shared using different configurations of ADR1 and ADR0 for each device. When the host device sends a control command through the serial bus, ADR1 and ADR0 (D14 and D13) are decoded by each codec. Only the corresponding codec responds to the serial bus. All SYNCs need to be connected together. The host device needs to send a pulse to all codecs to synchronize the operation.

power supply grouping recommendation

The following power supply grouping is recommended for best performance of this device. Ferrite beads are used to separate group 1, 2, and 3 if the same 3.3-V analog power source is shared.

- Group 1. AVDD1_TX, AVDD2_TX, AVDD_FIL_TX

programming (continued)

- Group 2. AVDD_FIL_RX, AVDD_ADC
- Group 3. AVDD_REF
- Group 4. DVDD_BF, DVDD_CLK, DVDD_DAC, DVDD_LG, DVDD_RX

application information

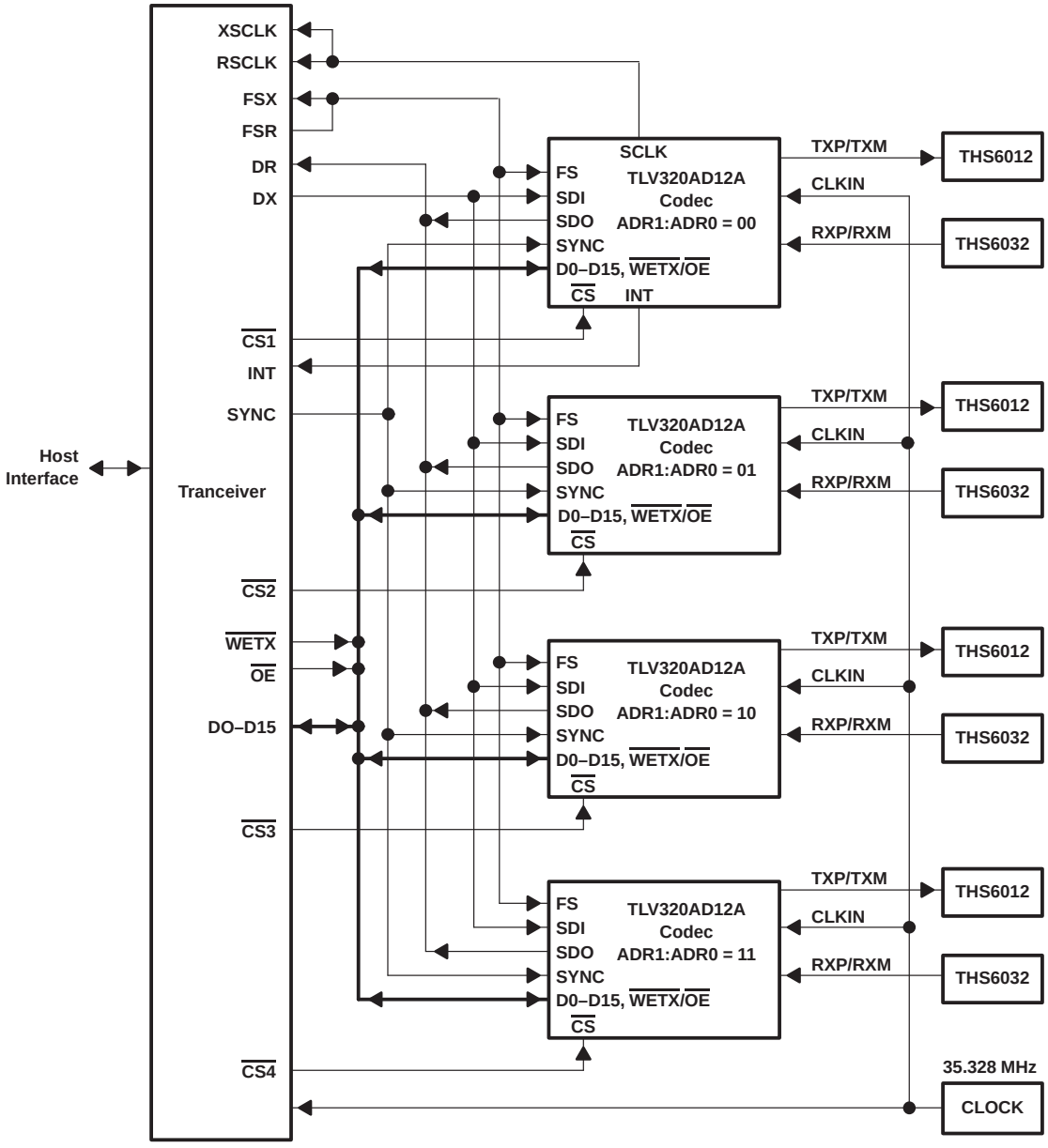


Figure 1. AD12 Multichannel Codec Configuration

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, AV_{DD} to AGND, DVDD to DGND . . . . . –0.3 V to 4.5 V
Analog input voltage range to AGND . . . . . –0.3 V to AVDD + 0.3 V
Digital input voltage range . . . . . –0.3 V to DVDD+ 0.3 V
Operating virtual-junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supply

		MIN	NOM	MAX	UNIT
Supply voltage	AVDD_FIL_TX, AVDD1_TX, AVDD2_TX, AVDD_FIL_RX, AVDD_ADC; AVDD_REF	3	3.3	3.6	V
	DVDD_BF, DVDD_CLK, DVDD_LG, DVDD_RX, DVDD_DAC	3	3.3	3.6	

digital inputs

	MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	

analog input

		MIN	NOM	MAX	UNIT
Analog input signal range	AVDD_FIL_RX = 3.3 V. The input signal is measured single-ended.		AVDD_FIL_RX/2±0.75		V
	AVDD_FIL_RX = 3.3 V. The input signal is measured differentially.		3		Vp-p

clock

		MIN	NOM	MAX	UNIT
Input clock frequency	DVDD_CLK=3.3 V		35.328		MHz
Input clock duty cycle			50%		

electrical characteristics over recommended operating free-air temperature range, typical at T_A = 25°C, f_{MCLKIN} = 35.328 MHz, analog power supply = 3.3 V, digital power supply = 3.3 V (unless otherwise noted)

TX channel (measured differentially, PAA = 0 dB, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Signal bandwidth			1104		kHz
	Conversion rate			8.832		MHz
	Effective number of bits (ENOB)			12		
	Channel gain error	43.125 kHz at –1 dB		–1		dB
	PAA step-gain error				0.1	dB
	Crosstalk	RX to TX channel		–67		dB
	Group delay			5		µs
	Power supply rejection ratio (PSRR)	Input = multitone at –10 dB (see Note 9)		60		dB
	Full-scale output voltage	Load = 4000 Ω (differentially), single-ended measured		AVDD_TX/2±0.75		V
		Load = 4000 Ω (differentially), differentially measured		3		Vp-p
AC Performance						
SNR	Signal-to-noise ratio	43.125 kHz at –3 dB (see Note 7)		74		dB
THD	Total harmonic distortion ratio			84		
TSNR	Signal-to-noise + harmonic distortion ratio			73		
MT	Missing-tone test (see Note 8)	120.750 kHz (missing tone)	65			dB
		750.375 kHz (missing tone)	65			
Channel Frequency Response (refer to Figure 5)						
	Gain relative to gain at 100 kHz (25.875 kHz DHPF is bypassed)	500 kHz	0.1		–1.5	dB
		1000 kHz	0.1		–1.5	dB
		1400 kHz	–1.5			dB
		1700 kHz	–7.2			dB

NOTES: 7. 250 tones input signal, 25.875 to 1104 kHz, 4.3125 kHz/step, 0 dB
8. Multitone signal (kHz): 30, 60, 200, 300, 500, 600, 700, 800, 1000
9. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential output with this input condition is 3 Vpp.

reference outputs (see Note 10)

			MIN	NOM	MAX	UNIT
REFP	REF plus output voltage	AVDD_REF = 3.3 V		2.5		V
REFM	REF minus output voltage			0.5		
VMID_REF	REF mid output voltage			1.5		
VMID_ADC	Receive channel mid-input voltage			1.5		

NOTE 10: All the reference outputs should not be used as voltage source.

digital inputs

			MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = –0.5 mA			0.6	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted), typical at T_A = 25°C, f_{CLKIN} = 35.328 MHz, analog power supply = 3.3 V, digital power supply = 3.3 V (unless otherwise noted) (continued)

RX channel (measured differentially, PGA1 = PGA2 = 0 dB, unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Signal bandwidth			138		kHz
	Conversion rate			4.416		MHz
	Integral nonlinearity (INL)			±0.8		
	Gain error			–1		dB
	PGA step gain error	PGA1 (0 to 6 dB in 1-dB/steps)		0		dB
		PGA2 (0 to 9 dB in 1-dB/steps)		0		
	DC offset			1.5		mV
	Crosstalk	TX to RX channel		–73		dB
	Group delay			6		µs
	Common-mode rejection ratio (CMRR)	43.125 kHz at –10dB		114		dB
	Power supply rejection ratio (PSRR)	Input = multitone at –10 dB (see Note 13		80		dB
	Analog input self-bias dc voltage			AVDD_FIL_RX/2		V
	Input impedance			10		kΩ
AC Performance						
SNR	Signal-to-noise ratio	43.125 kHz at –3 dB (see Note 11)		77		dB
THD	Total harmonic distortion ratio			84		
TSNR	Signal-to-noise + harmonic distortion ratio			76		
MT	Missing-tone test (see Note 112	120.750 kHz (missing tone)	65			dB
Channel Frequency Response (see Figure 6)						
	Gain relative to gain at 30 kHz	50 kHz		–0.4	0.25	dB
		138 kHz		–3.1	0.25	
		200 kHz		–16		
		400 kHz		–57		

NOTES: 11. 27 tones input signal, 25.875 to 138 kHz, 4.3125 kHz/step, –1 dB.
12. Multitone signal (kHz): 30, 60
13. The analog input test signal is a sine wave with 0 dB = 3 Vpp as the reference level.

power dissipation

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation	Active mode			625		mW
	Power-down mode	Hardware power down		40		
		Software power down (TX+RX+Reference)		45		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

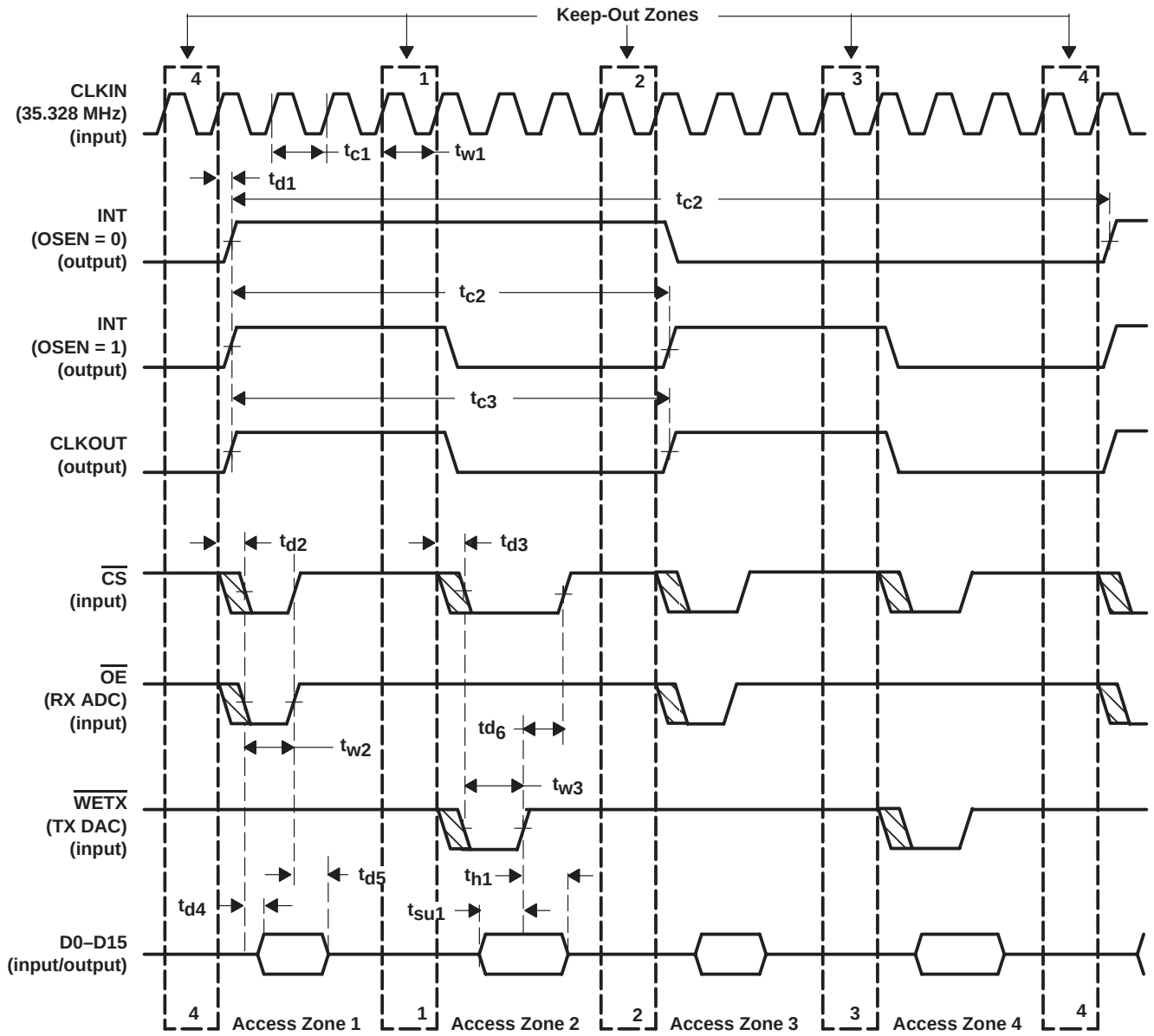
parallel port (see Figures 2 and 3)

PARAMETER			MIN	TYP	MAX	UNIT
t_{c1}	Period, CLKIN			28.3		ns
t_{c2}	Cycle time, INT	OSEN=0		16		CLKIN
		OSEN=1		8		
t_{c3}	Period, CLKOUT			8		
t_{d1}	Delay time, keep-out zone end to INT↑				16	ns
t_{d2}	Delay time, keep-out zone end (CLKIN↑) to $\overline{CS}$↓ (data-read cycle)		0			ns
t_{d3}	Delay time, keep-out zone end (CLKIN↑) to $\overline{CS}$↓ (data-write cycle)		0			ns
t_{d4}	Delay time, data valid after $\overline{OE}$↓				15	ns
t_{d5}	Delay time, data valid (before change to high-Z) after $\overline{OE}$↑				5	ns
t_{d6}	Delay time, time between the rising edge of $\overline{WETX}$ to the rising edge of $\overline{CS}$			5		ns
t_{h1}	Hold time, data valid (before change to high-Z) after $\overline{WETX}$↑		5			ns
t_{h2}	Hold time, SYNC keep high after CLKIN↑		5			ns
t_{su1}	Setup time, data valid before $\overline{WETX}$↑		15			ns
t_{su2}	Setup time, SYNC↑ before CLKIN↑		10			ns
t_{w1}	Pulse width, keep-out zone time			1		CLKIN
t_{w2}	Pulse width, $\overline{OE}$		20			ns
t_{w3}	Pulse width, $\overline{WETX}$		28			ns
t_{w4}	Pulse width, SYNC			28		ns

serial port (see Figure 4)

PARAMETER		MIN	TYP	MAX	UNIT
t_{c4}	Cycle time, SCLK		8		CLKIN
t_{c5}	Cycle time, FS	18			SCLK
t_{d6}	Delay time, SCLK rising edge to SDO valid			15	ns
t_{h3}	Hold time, FS valid after SCLK↓	5			ns
t_{h4}	Hold time, SDI after SCLK↓	5			ns
t_{su3}	Setup time, FS valid before SCLK↓	20			ns
t_{su4}	Setup time, SDI valid before SCLK↓	20			ns
t_{w5}	FS pulse width		28		ns

PARAMETER MEASUREMENT INFORMATION

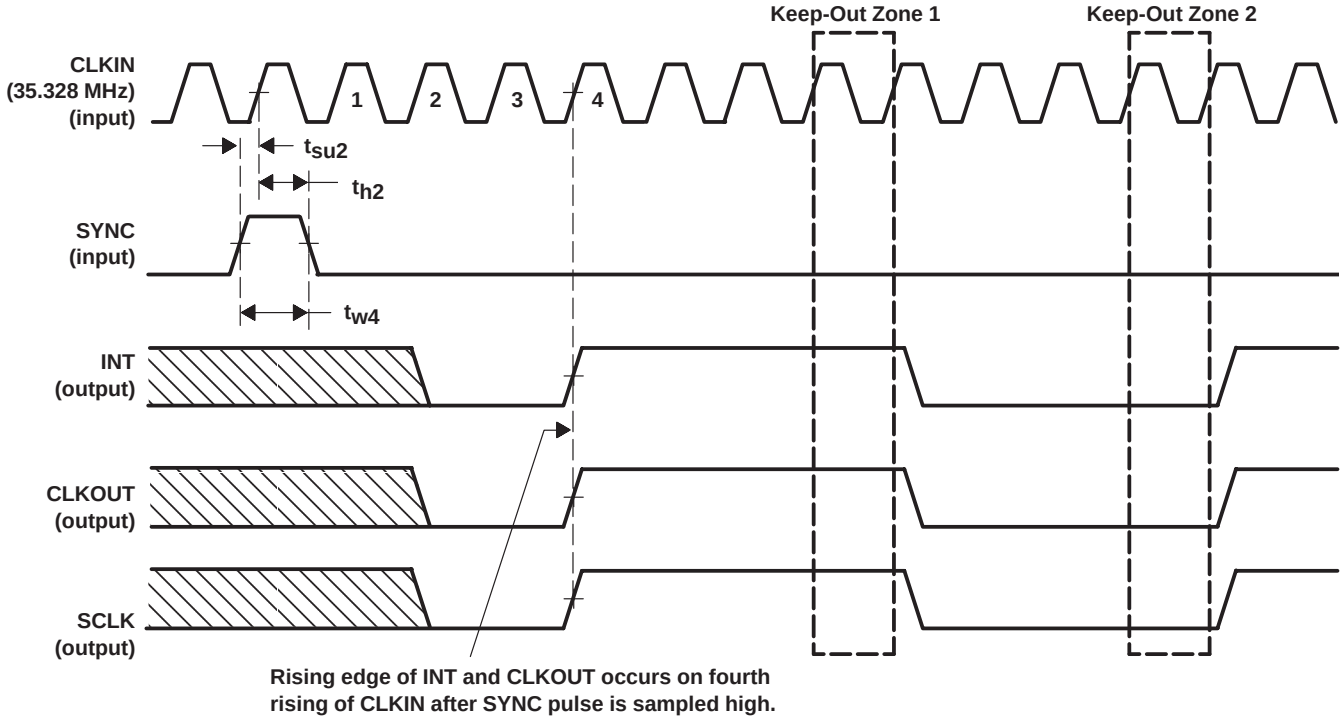


NOTES: A. $\overline{CS}$ AND $\overline{OE}$ may fall/rise together or be skewed from each other. It does not matter which falls/rises first. However, t_{d4} is referenced from whichever falls last, and t_{d5} is referenced from whichever rises first. $\overline{CS}$ can be connected to GND if there is only one codec in the system.

B. $\overline{CS}$ and $\overline{WETX}$ may fall together or be skewed from each other. But the rising edge of $\overline{WETX}$ should occur prior to the rising edge of $\overline{CS}$.

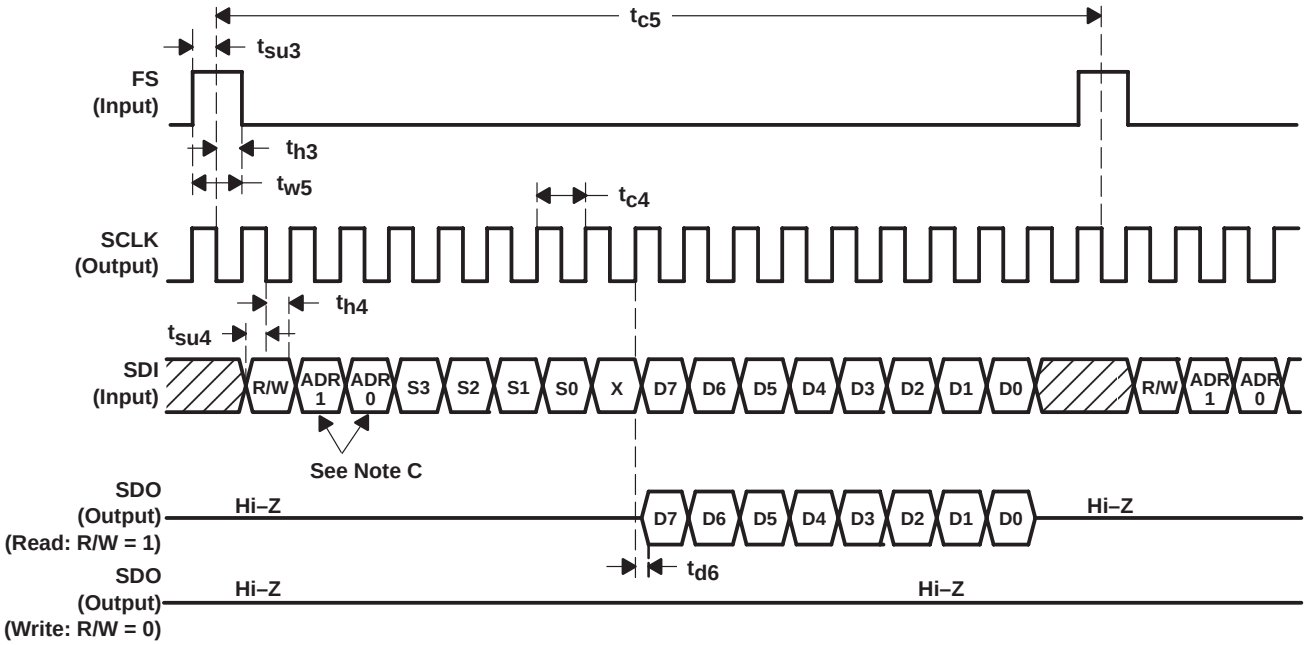
Figure 2. Parallel Port

PARAMETER MEASUREMENT INFORMATION



NOTE A: SYNC is used only during multicodec system-to-synchronous operation. The codec meets KOZ requirements when working alone.

Figure 3. Synchronous Pulse



NOTES: A. Data on SDI is latched at the falling edge of SCLK.
B. Data is sent to SDO at the rising edge of SCLK.
C. ADR0 and ADR1 are the hardware configuration of ADR0 and ADR1 input pins.

Figure 4. Serial Port

APPLICATION INFORMATION

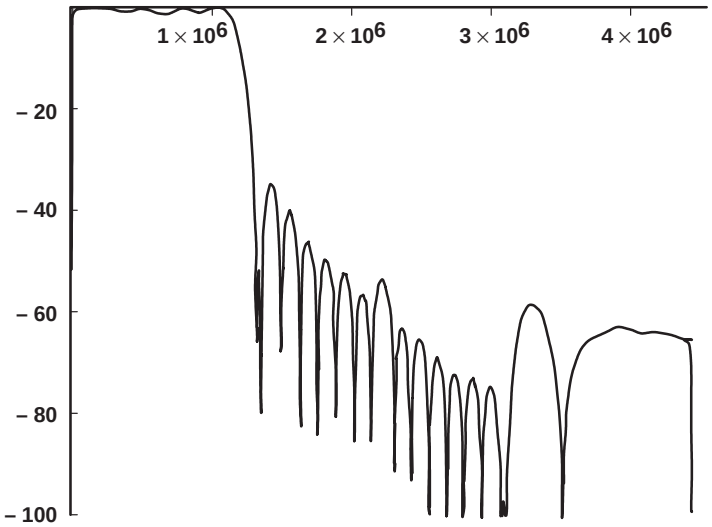


Figure 5. AD12 Transmitter Filter With High-Pass Filter, DC-4.46 MHz Frequency Range

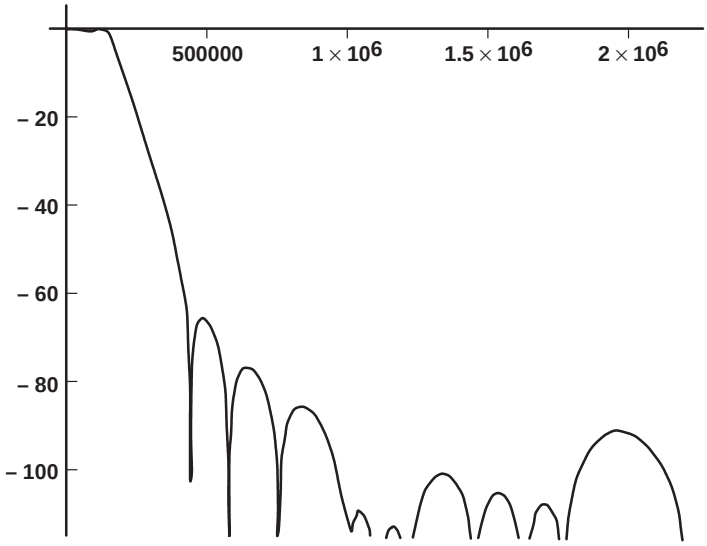


Figure 6. AD12 Receiver Filter, DC-2 MHz Frequency Range

APPLICATION INFORMATION

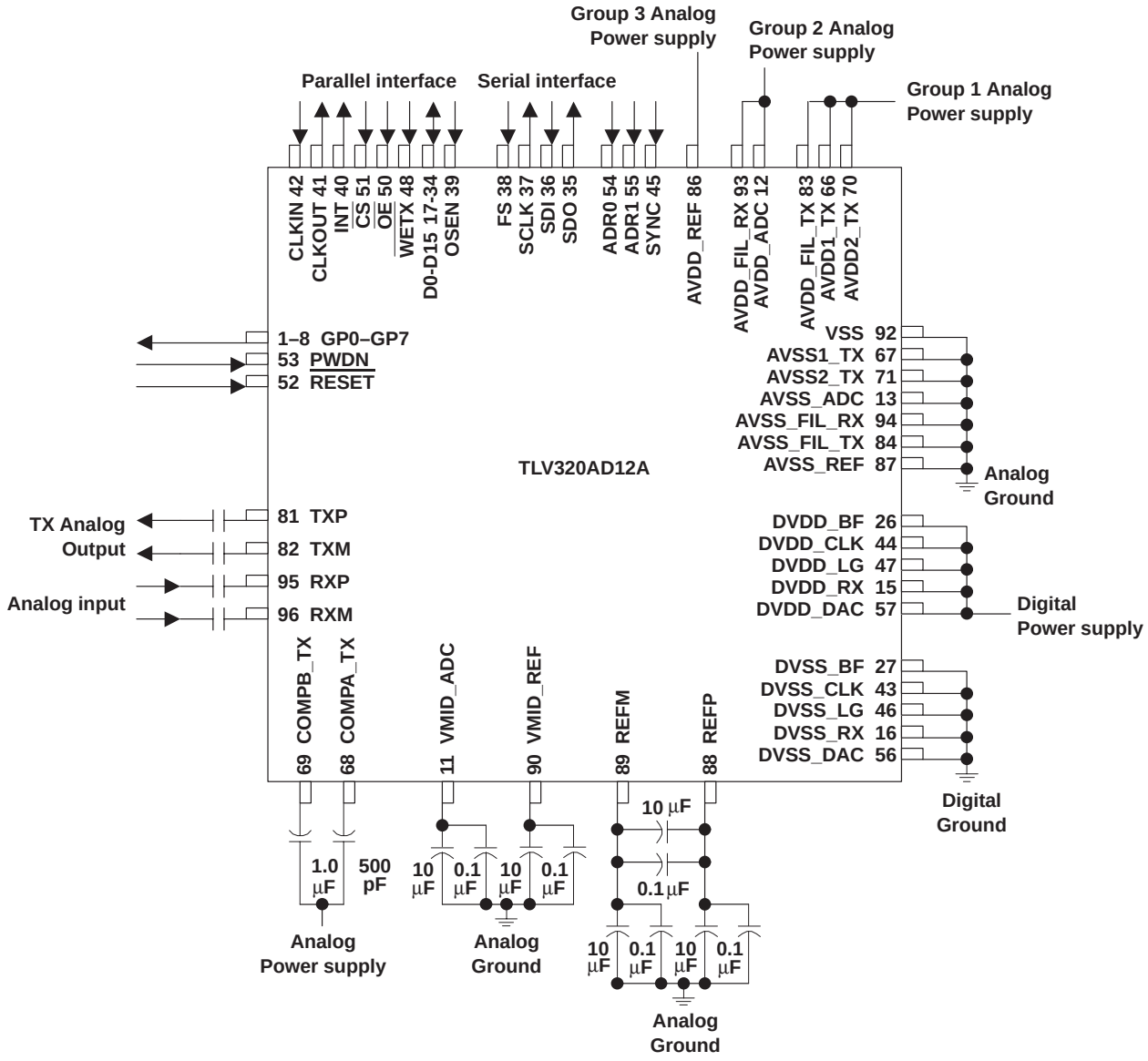
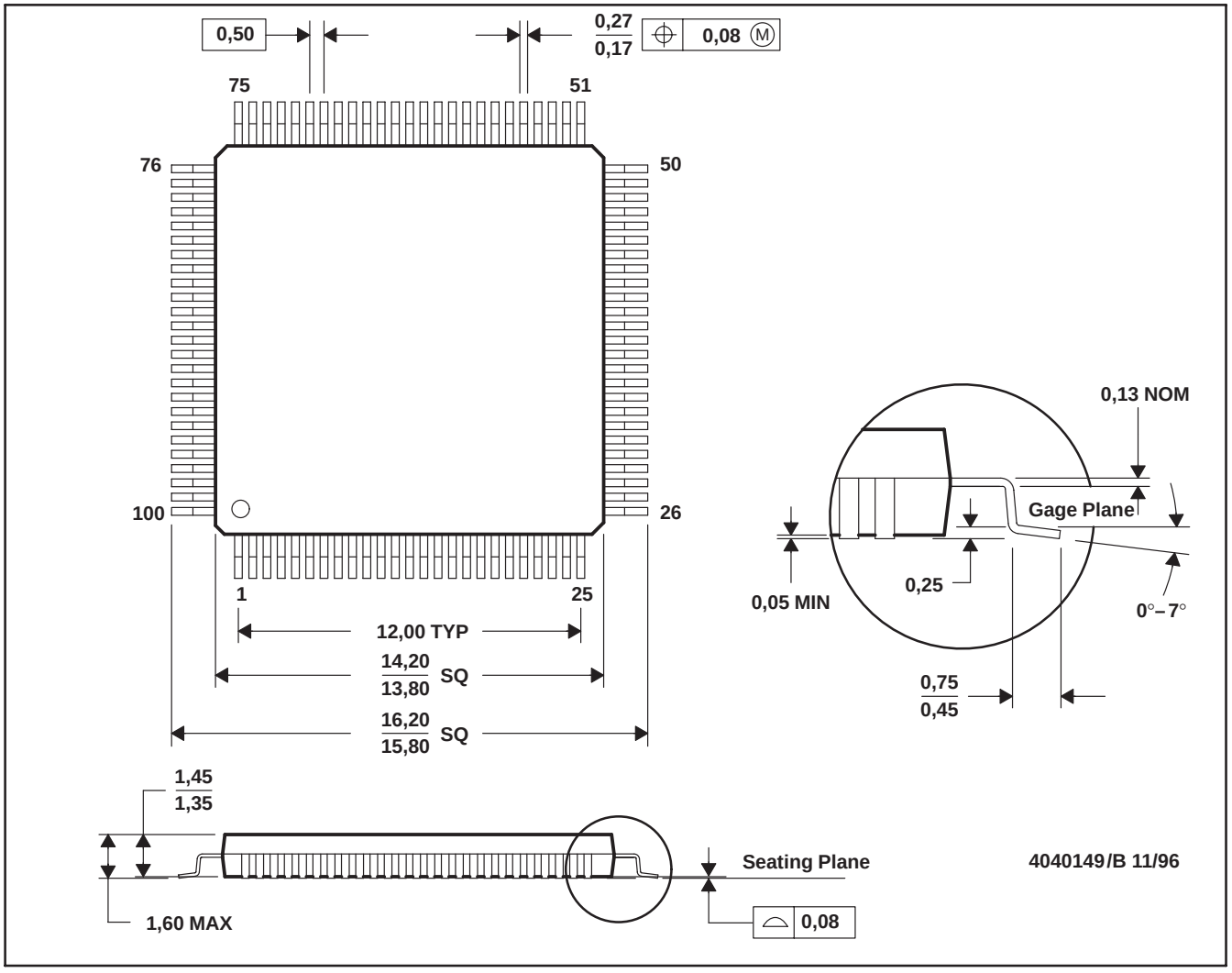


Figure 7. Typical Chip Configuration

MECHANICAL DATA

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

thermal resistance characteristics (S-PQFP package)

NO			°C/W	AIR FLOW LFPM
1	$R1_{JC}$	Junction-to-case	5.40	N/A
2	$R1_{JC}$	Junction-to-free air	30.4	0
3	$R1_{JC}$	Junction-to-free air	24.2	100
4	$R1_{JC}$	Junction-to-free air	22.3	250
5	$R1_{JC}$	Junction-to-free air	20	500

† LFPM - Linear feet per minute

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