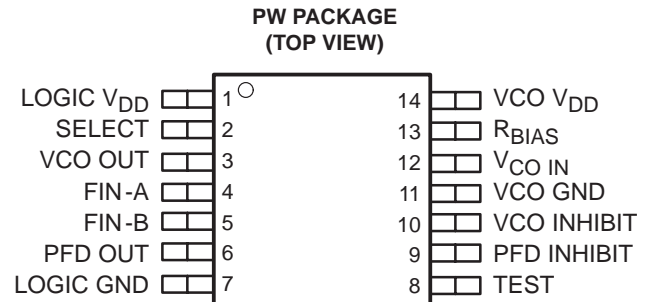


# TLC2934 3.3 V 130 MHz VCO, PHASE FREQUENCY DETECTOR

SLAS306 – NOVEMBER 2000

- **Voltage-Controlled Oscillator (VCO)**
  - Ring Oscillator Using Only One External Biasing Resistor ( $R_{BIAS}$ )
- **Recommended Lock Frequency**
  - 100 MHz to 130 MHz
  - ( $V_{DD} = 3.3\text{ V} + 5\%$ ,  $T_A = -20^\circ\text{C}$  to  $75^\circ\text{C}$ )
- **Phase-Frequency Detector (PFD)**
  - Includes a High-Speed Edge-Triggered Detector With Internal Charge Pump
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 Terminal)**
- **Compatible Pin Assignment to TLC2932, TLC2933**



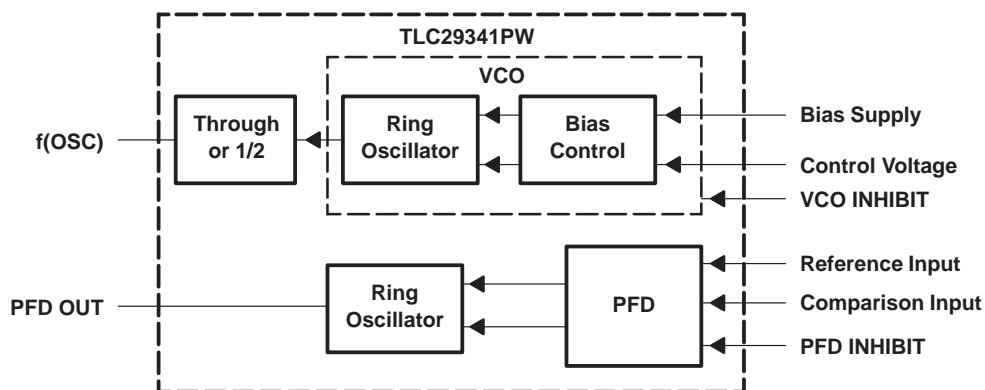
## description

The TLC2934, a mixed signal IC designed for phase-locked-loop (PLL) systems, is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD).

The internal VCO is based on the TLC2932 and TLC2933s ring oscillator. It oscillates in wider frequency with lower supply voltage, and it has stable oscillating performance. The oscillation function, provided by only one external resistor connection, supplies bias to the VCI internal circuit. Oscillator range is covered from 10 MHz to 130 MHz with a 3.3-V supply voltage. The VCO has an inhibit function to stop oscillation and for the power-down mode.

The internal PFD, a high-speed rising edge triggered type, has an internal charge pump with a high-impedance output buffer. The PFD detects phase difference between the reference frequency input and the signal frequency input from the VCO output through an external counter device. This functions the same as TLC2932 and TLC2933. The PFD also has the inhibit function for stop phase comparison and for power-down mode.

## block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

# TLC2934

## 3.3 V 130 MHz VCO, PHASE FREQUENCY DETECTOR

SLAS306 – NOVEMBER 2000

### Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
FIN-A, FIN-B	4 5	I	Frequency signal inputs for PFD. The reference frequency signal ( $f_{REF-IN}$ ) and the VCO output signal through the external counter device are applied to these terminals. When the LPF design is the lag-lead filter (passive filter and noninverting), $f_{REF-IN}$ is input to FIN-A, and the VCO output signal is to FIN-B.
LOGIC GND	7		GND terminal for the internal logic circuit
LOGIC $V_{DD}$	1		Power supply terminal for the internal logic circuit. This power supply terminal separates from VCO $V_{DD}$ to reduce cross-coupling between supplies.
PFD INHIBIT	9	I	PFD INHIBIT (power-down) control signal input terminal
PFD OUT	6	O	PFD output terminal. When PFD INHIBIT is high, PFD OUT is in the high-impedance state.
RBIAS	13	I	Bias resistor ( $R_{BIAS}$ ) terminal. Connect a resistor between VCO GND and this terminal to supply bias to internal VCO circuit. TLC2934 bias resistor connection is different from TLC2932 and TLC2933, where bias resistor $R_{BIAS}$ is connected to VCO $V_{DD}$ .
SELECT	2	I	1/2 divider select terminal. L=through output, H=1/2 output.
TEST	8		Test terminal. Use for production test. Tie to GND when in normal use.
VCO GND	11		GND terminal for internal VCO
VCO OUT	3	O	VCO output terminal. When VCO INHIBIT = high, VCO OUT is low.
VCO INHIBIT	10	I	VCO INHIBIT (power-down) control signal input terminal
VCO IN	12	I	VCO control voltage input terminal. Normally, The external LPF is connected to this terminal.
VCO $V_{DD}$	14		Power supply terminal for the internal VCO circuit. This power supply terminal should be separate from LOGIC $V_{DD}$ to reduce cross-coupling between supplies.

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage (each supply), $V_{DD}$ (see Note 1)	–0.5 V to 4 V
Input voltage range (each input), $V_I$ (see Note 1)	–0.5 V to $V_{DD} + 0.5$ V
Input current (each input), $I_I$	$\pm 20$ mA
Output current (each output), $I_O$	$\pm 20$ mA
Continuous total power dissipation at (or below) $T_A = 25^\circ\text{C}$ (see Note 2), $P_D$	700 mW
Operating free-air temperature range, $T_A$	–20°C to 75°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal.  
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C



# TLC2934

## 3.3 V 130 MHz VCO, PHASE FREQUENCY DETECTOR

SLAS306 – NOVEMBER 2000

### recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage (each supply, $V_{DD}$ (see Notes 3 and 4))		3.15	3.3	3.45	V
Input voltage (each input except for $V_{CO\ IN}$ , $V_I$ )		0		$V_{DD}$	V
Output current (each output), $I_O$		0		$\pm 2$	mA
VCO control voltage, $V_{CO\ IN}$		0.5		$V_{DD}$	V
Lock frequency (through output)	$R_{BIAS} = 1\text{ k}\Omega$	36		130	MHz
	$R_{BIAS} = 1.8\text{ k}\Omega$	28		90	
	$R_{BIAS} = 2.4\text{ k}\Omega$	26		80	
	$R_{BIAS} = 3.3\text{ k}\Omega$	20		60	
Lock frequency (1/2 output)	$R_{BIAS} = 1\text{ k}\Omega$	18		65	MHz
	$R_{BIAS} = 1.8\text{ k}\Omega$	14		45	
	$R_{BIAS} = 2.4\text{ k}\Omega$	13		40	
	$R_{BIAS} = 3.3\text{ k}\Omega$	10		30	
Bias resistor, $R_{BIAS}$		1.0		3.3	$\text{K}\Omega$
Operating temperature range, $T_A$		-20		75	$^{\circ}\text{C}$
$V_{CO\ IN}$ voltage at $V_{CO\ INHIBIT\downarrow}$ , $V_{(CINH)}$ (see Note 5)			0	0.5	V

- NOTES: 3. It is recommended that the logic supply terminal (LOGIC  $V_{DD}$ ) and the VCO supply terminal (VCO  $V_{DD}$ ) be at the same voltage and separated from each other.
4. A bypass capacitor is placed as close as possible to each supply terminal.
5. For stable restart of VCO,  $V_{CO\ IN}$  is 0 V when VCO INHIBIT is pulled down to GND level to disable the VCO INHIBIT function. And also,  $V_{CO\ IN}$  should be 0 V when the operation will be started by supplying the power.

### electrical characteristics over recommended operating free-air temperature range, $V_{DD}=3.3\text{ V}$ (unless otherwise noted)

#### VCO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -2\text{ mA}$	3.1			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
$V_{IH}$	High-level input voltage	Logic signal input	2.3			V
$V_{IL}$	Low-level input voltage	Logic signal input			1.0	V
$I_I$	Input current at TEST, VCO INHIBIT	$V_I = V_{DD}$ or GND			$\pm 1$	$\mu\text{A}$
$Z_{V(CO\ IN)}$	Input impedance at $V_{CO\ IN}$	$V_{CO\ IN} = 1/2 V_{DD}$		10		$\text{M}\Omega$
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 6		0.01	1	$\mu\text{A}$
$I_{DD(VCO)}$	VCO supply current	See Note 7		10	15	mA

- NOTES: 6. Current into VCO  $V_{DD}$ , when VCO INHIBIT =  $V_{DD}$ , PFD is inhibited.
7. Current into VCO  $V_{DD}$ , when  $V_{CO\ IN} = 1/2 V_{DD}$ ,  $R_{BIAS} = 1\text{ k}\Omega$ , VCO INHIBIT = GND, PFD is inhibited.

# TLC2934

## 3.3 V 130 MHz VCO, PHASE FREQUENCY DETECTOR

SLAS306 – NOVEMBER 2000

electrical characteristics over recommended operating free-air temperature range,  $V_{DD}=3.3\text{ V}$  (unless otherwise noted) (continued)

### VCO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -2\text{ mA}$	3.1			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2\text{ mA}$			0.2	V
$I_{OZ}$	High-impedance state output current	PFD INHIBIT = high, $V_O = V_{DD}$ or GND			$\pm 1$	$\mu\text{A}$
$V_{IH}$	High-level input voltage at FIN-A,B		2.3			V
$V_{IL}$	Low-level input voltage at FIN-A,B				1.0	V
$V_{(TO)}$	Positive input threshold voltage at PFD INHIBIT		1.0	1.65	2.3	V
$C_I$	Input capacitance at FIN-A,B			5		pF
$Z_{(IN)}$	Input impedance at FIN-A,B			10		$M\Omega$
$I_{DD(PFD)}$	PFD supply current	See Note 8		1.5	6.0	mA

NOTE 8: Current into LOGIC  $V_{DD}$ , when FIN-A, FIN-B=50 MHz ( $V_{I(pp)} = 3.3\text{V}$ , rectangular wave), Test=GND, no load, and VCO OUT is inhibited.

### VCO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating oscillation frequency	$R_{BIAS} = 1\text{ k}\Omega$	67	90	113	MHz
$t_{(STB)}$	Time to stable oscillation	See Note 9		0.7	10	$\mu\text{s}$
$t_r$	Rise time	$C_L = 15\text{ pF}$ , See Figure 3		1.7	5	ns
$t_f$	Fall time	$C_L = 15\text{ pF}$ , See Figure 3		1.1	4	ns
$f_{(duty)}$	Duty cycle at VCO OUT	$R_{BIAS} = 1.0\text{ k}\Omega$ , $V_{CO\ IN} = 1/2 V_{DD}$	45%	50%	55%	
	Temperature coefficient of oscillation frequency	$R_{BIAS}=1.0\text{k}\Omega$ , $V_{CO\ IN} = 1/2 V_{DD}$ , $T_A = -20^\circ\text{C}$ to $75^\circ\text{C}$		0.03		$\%/^\circ\text{C}$
	Supply voltage coefficient of oscillation frequency	$R_{BIAS} = 1\text{ k}\Omega$ , $V_{CO\ IN} = 1.65\text{ V}$ , $V_{DD} = 3.15\text{ V}$ to $3.45\text{ V}$		0.02		$\%/mV$
	Jitter absolute	$R_{BIAS} = 1\text{ k}\Omega$ , $V_{CO\ IN} = 1/2 V_{DD}$		50		ps

NOTE 9: Current into VCO  $V_{DD}$ , when VCO INHIBIT =  $V_{DD}$ , PFD is inhibited.

### PFD AC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{MAX}$	Maximum operating frequency		50			MHz
$t_{PLZ}$	PFD output disable time from low level	See Figures 4 and 5 and Table 6		15.3	40	ns
$t_{PHZ}$	PFD output disable time from high level			15.5	40	ns
$t_{PZL}$	PFD output enable time from low level			2.4	10	ns
$t_{PZH}$	PFD output enable time from high level			2.5	10	ns
$t_r$	Rise time	$C_L=15\text{ pF}$ (see Figure 3)		1.2	5	ns
$t_f$	Fall time	$C_L=15\text{ pF}$ (see Figure 3)		0.7	5	ns



PARAMETER MEASUREMENT INFORMATION

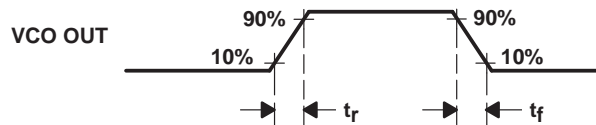
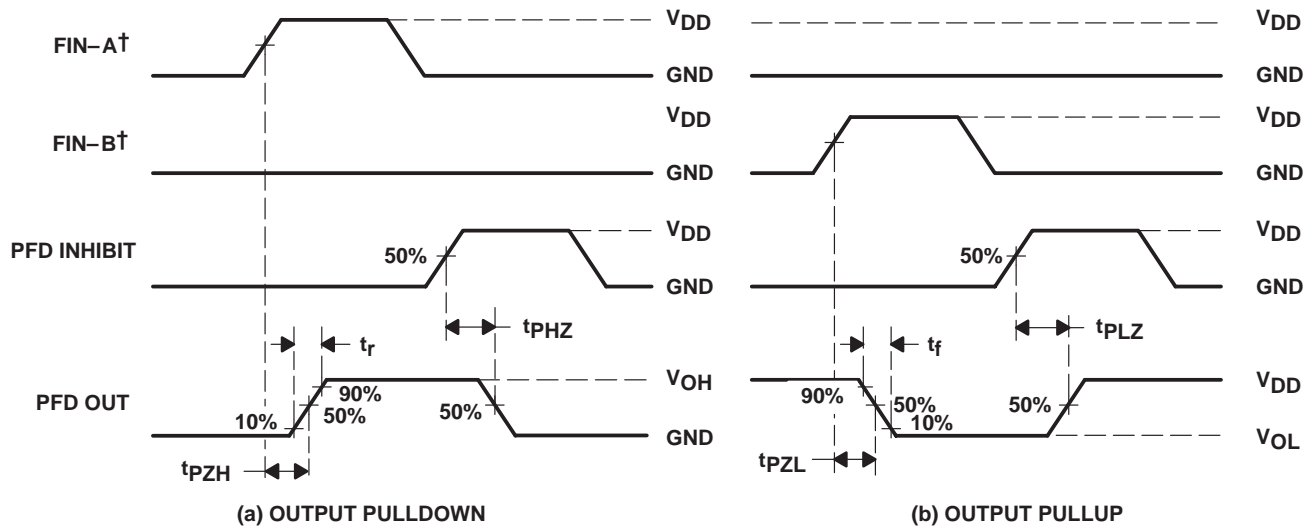


Figure 1. VCO Output Voltage Waveform



(see Figure 3 and PFD Output Test Conditions Table)

† FIN-A and FIN-B are for reference phase only, not for timing.

Figure 2. PFD Output Voltage Waveform

PFD Output Test Conditions

PARAMETER	$R_L$	$C_L$	$S_L$	$S_2$
$t_{PZH}$	1 k $\Omega$	15 pF	Open	Close
$t_{PHZ}$				
$t_r$			Close	Open
$t_{PZL}$				
$t_{PLZ}$				
$t_f$				

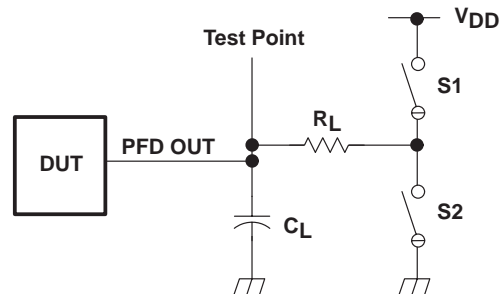


Figure 3. PFD Output Test Condition

# TLC2934

## 3.3 V 130 MHz VCO, PHASE FREQUENCY DETECTOR

SLAS306 – NOVEMBER 2000

### TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY  
vs  
VCO CONTROL VOLTAGE

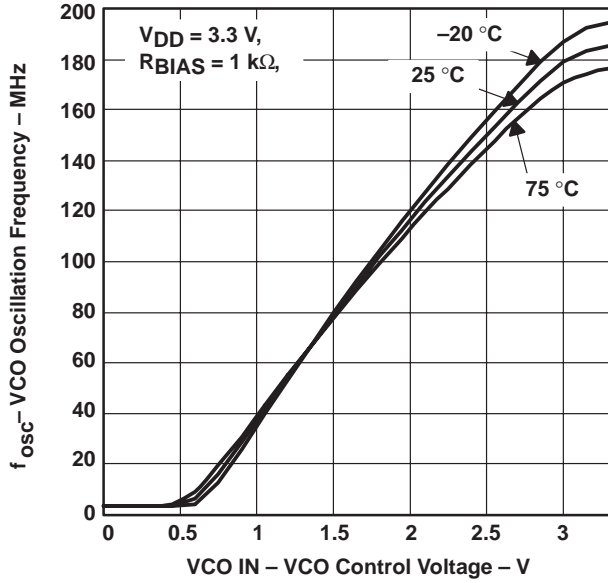


Figure 4

VCO OSCILLATION FREQUENCY  
vs  
VCO CONTROL VOLTAGE

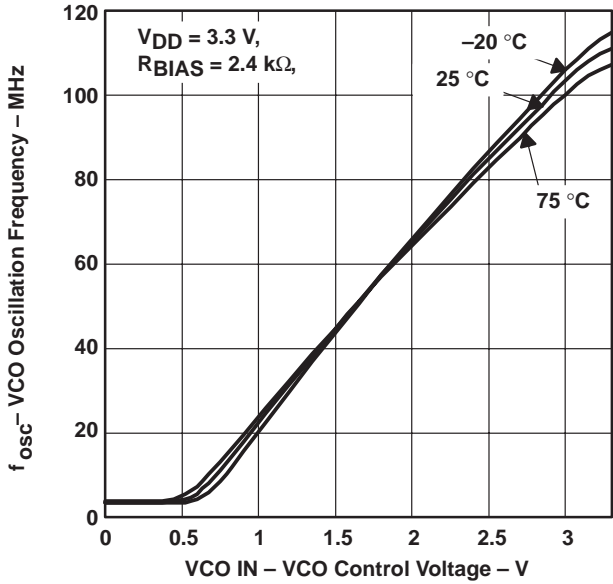


Figure 5

VCO OSCILLATION FREQUENCY  
vs  
VCO CONTROL VOLTAGE

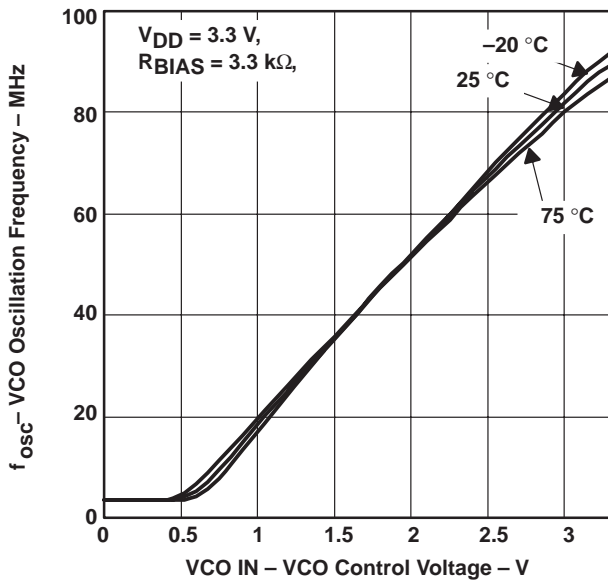


Figure 6

VCO OSCILLATION FREQUENCY  
vs  
VCO SUPPLY VOLTAGE

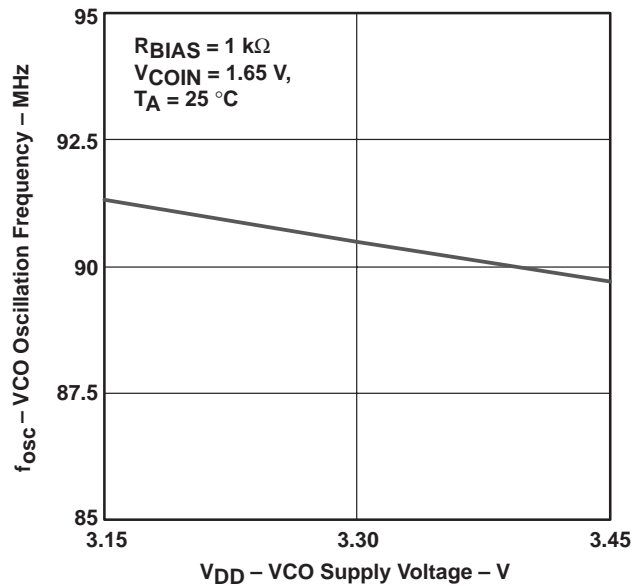


Figure 7



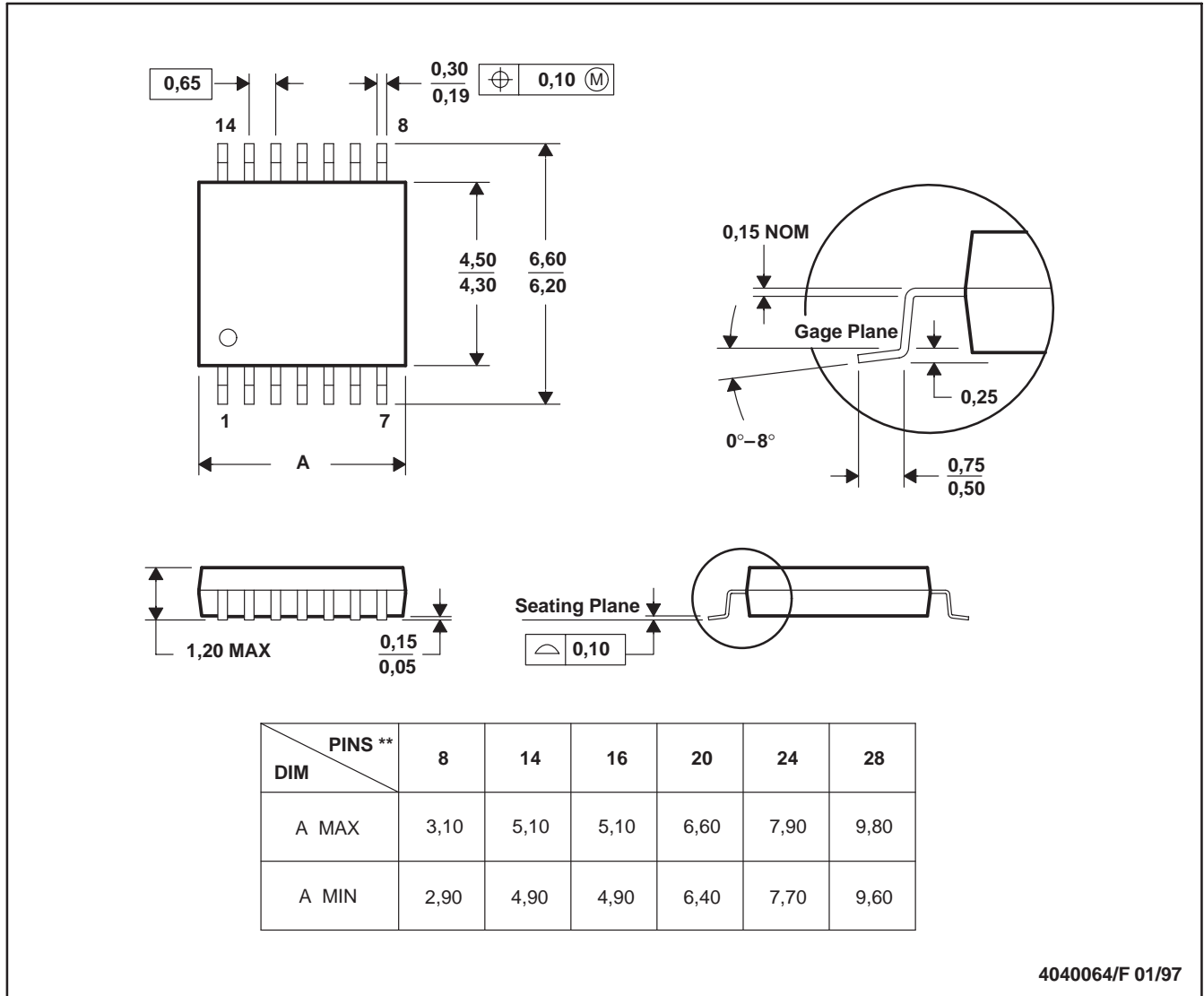
# TLC2934 3.3 V 130 MHz VCO, PHASE FREQUENCY DETECTOR

SLAS306 – NOVEMBER 2000

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.