

TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C
 TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M
 HIGH-PERFORMANCE **IMPACT™** PAL® CIRCUITS

SRPS021 – D2920, JUNE 1986 – REVISED AUGUST 1989

- High-Performance: f_{max} (w/o feedback)
 TIBPAL20R' -15C Series . . . 45 MHz
 TIBPAL20R' -20M Series . . . 41.6 MHz
- High-Performance . . . 45 MHz Min
- Reduced I_{CC} of 180 mA Max
- Functionally Equivalent, but Faster Than
 PAL20L8, PAL20R4, PAL20R6, PAL20R8
- Power-Up Clear on Registered Devices (All
 Register Outputs are Set Low, but Voltage
 Levels at the Output Pins Go High)
- Preload Capability on Output Registers
 Simplifies Testing
- Package Options Include Both Plastic and
 Ceramic Chip Carriers in Addition to Plastic
 and Ceramic DIPs

| DEVICE | I INPUTS | 3-STATE O OUTPUTS | REGISTERED Q OUTPUTS | I/O PORT S |
|---------|-------------|----------------------|-------------------------|------------------|
| PAL20L8 | 14 | 2 | 0 | 6 |
| PAL20R4 | 12 | 0 | 4 (3-state buffers) | 4 |
| PAL20R6 | 12 | 0 | 6 (3-state buffers) | 2 |
| PAL20R8 | 12 | 0 | 8 (3-state buffers) | 0 |

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

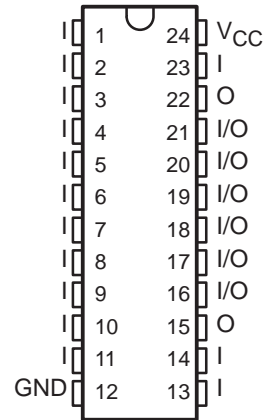
Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C. The TIBPAL20' M series is characterized for operation over the full military temperature range of -55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
 IMPACT is a trademark of Texas Instruments Incorporated.
 PAL is a registered trademark of Advanced Micro Devices Inc.

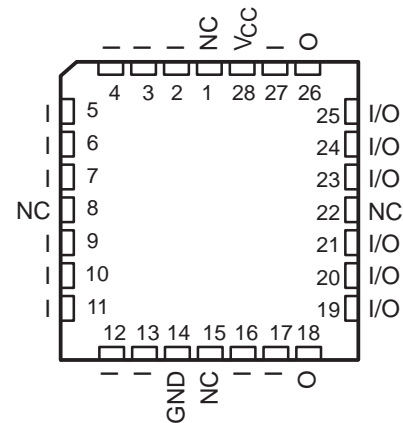
TIBPAL20L8'
 C SUFFIX . . . JT OR NT PACKAGE
 M SUFFIX . . . JT OR W PACKAGE

(TOP VIEW)



TIBPAL20L8'
 C SUFFIX . . . FN PACKAGE
 M SUFFIX . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection
 Pin assignments in operating mode

PRODUCTION DATA information is current as of publication date.
 Products conform to specifications per the terms of Texas Instruments
 standard warranty. Production processing does not necessarily
 include testing of all parameters.

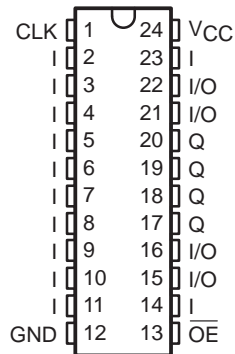


**TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C
TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M
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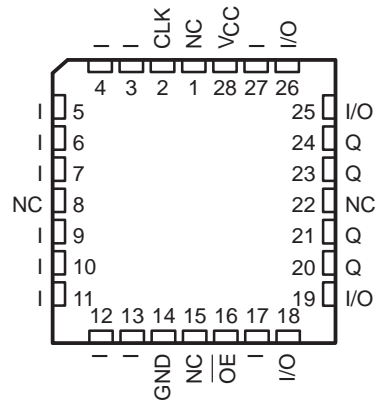
TIBPAL20R4'
C SUFFIX ... JT OR NT PACKAGE
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



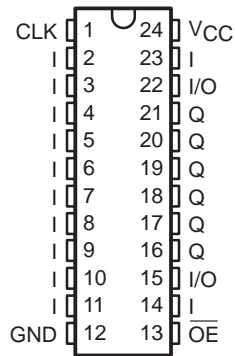
TIBPAL20R4'
C SUFFIX ... FN PACKAGE
M SUFFIX ... FK PACKAGE

(TOP VIEW)



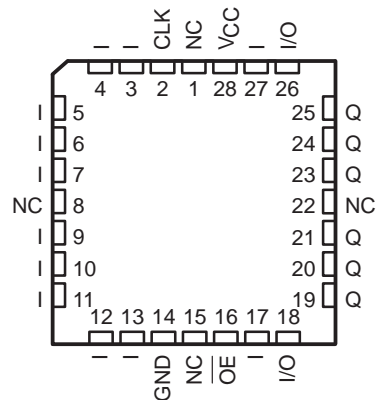
TIBPAL20R6'
C SUFFIX ... JT OR NT PACKAGE
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



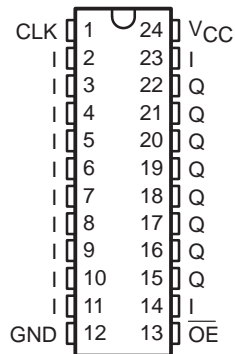
TIBPAL20R6'
C SUFFIX ... FN PACKAGE
M SUFFIX ... FK PACKAGE

(TOP VIEW)



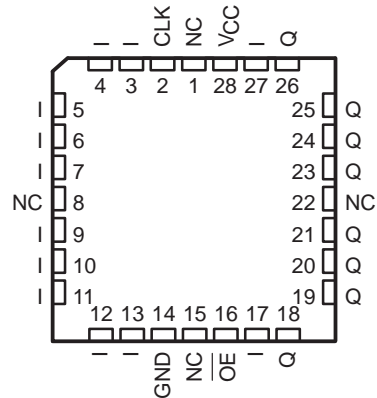
TIBPAL20R8'
C SUFFIX ... JT OR NT PACKAGE
M SUFFIX ... JT OR W PACKAGE

(TOP VIEW)



TIBPAL20R8'
C SUFFIX ... FN PACKAGE
M SUFFIX ... FK PACKAGE

(TOP VIEW)



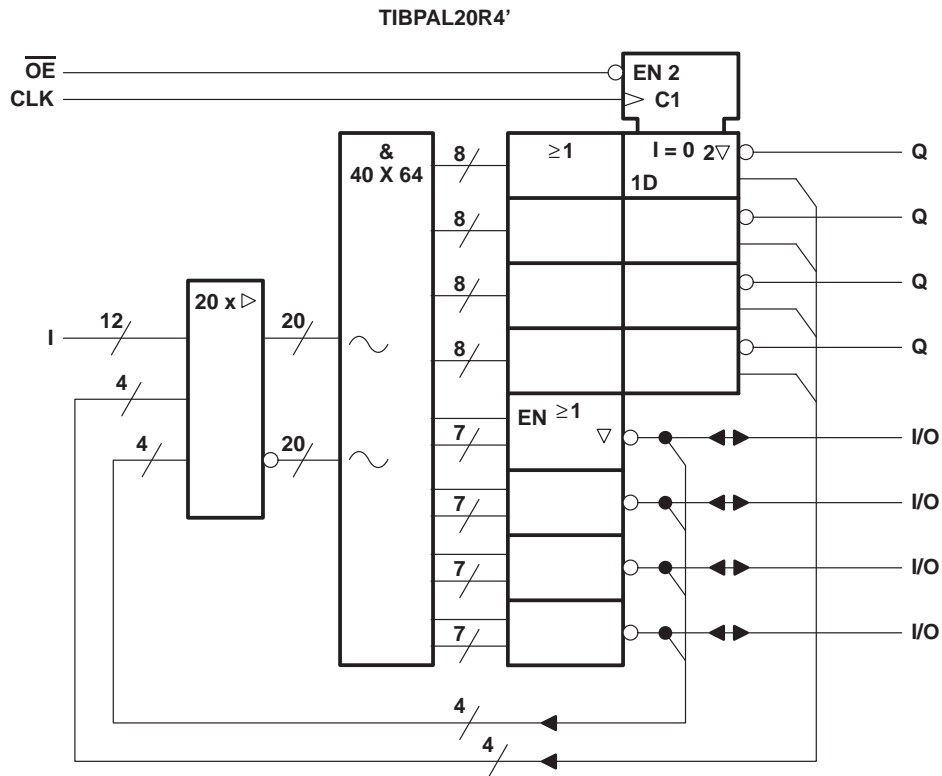
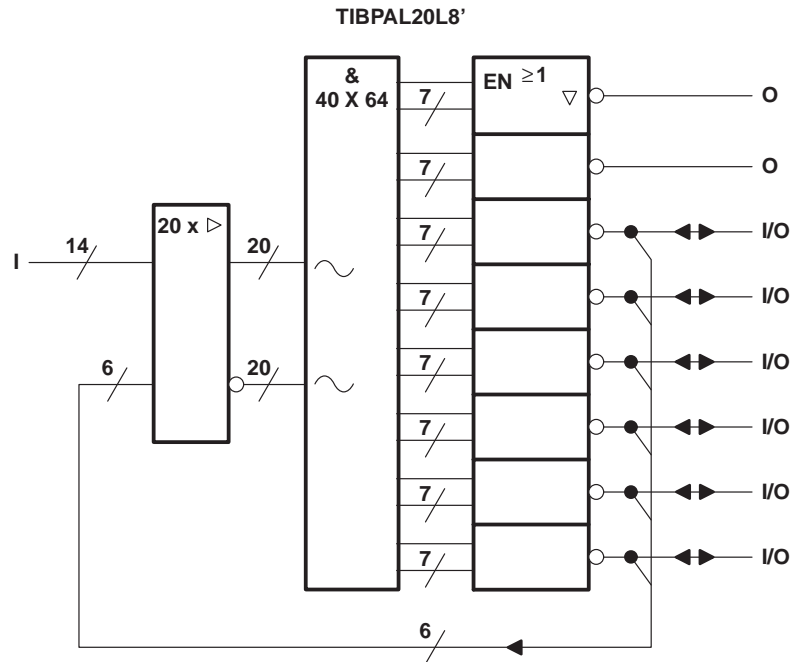
Pin assignments in operating mode

NC – No internal connection



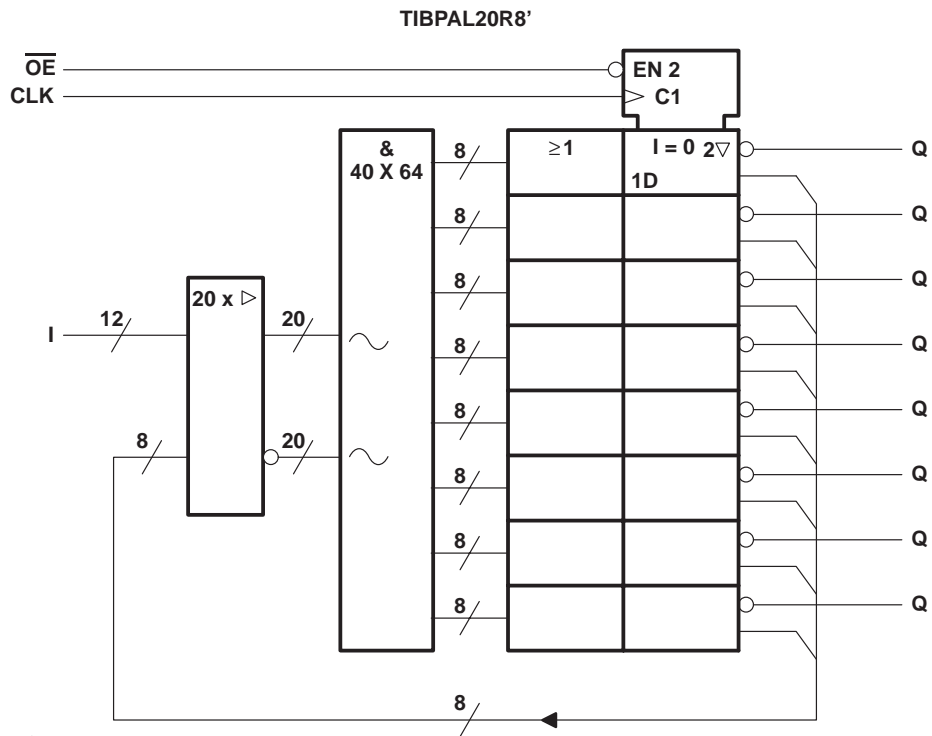
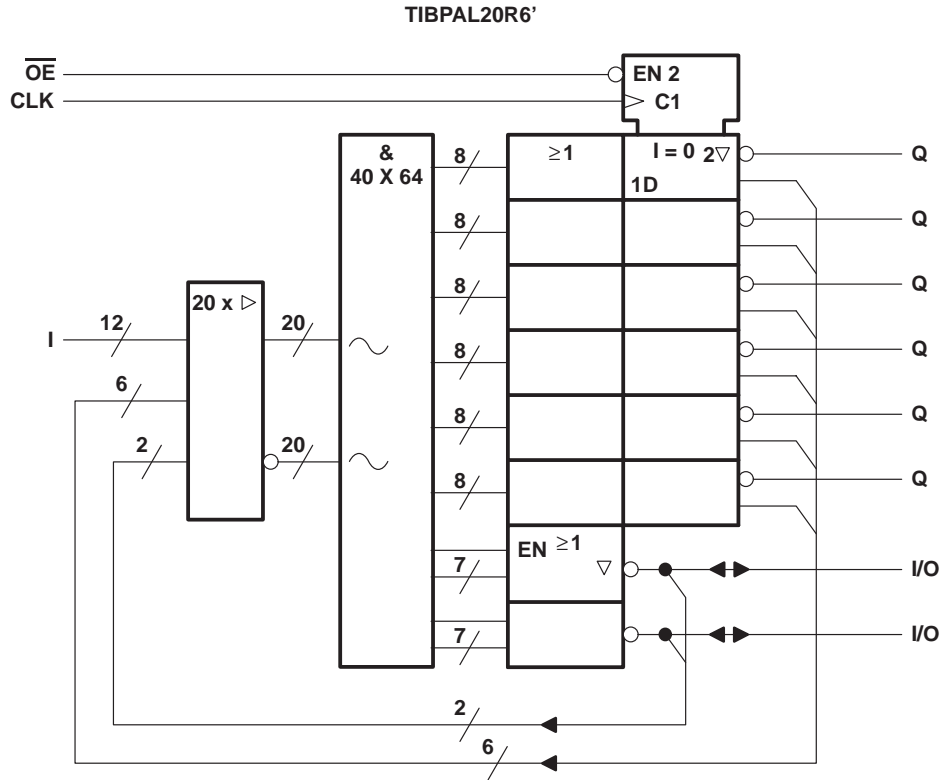
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functional block diagrams (positive logic)



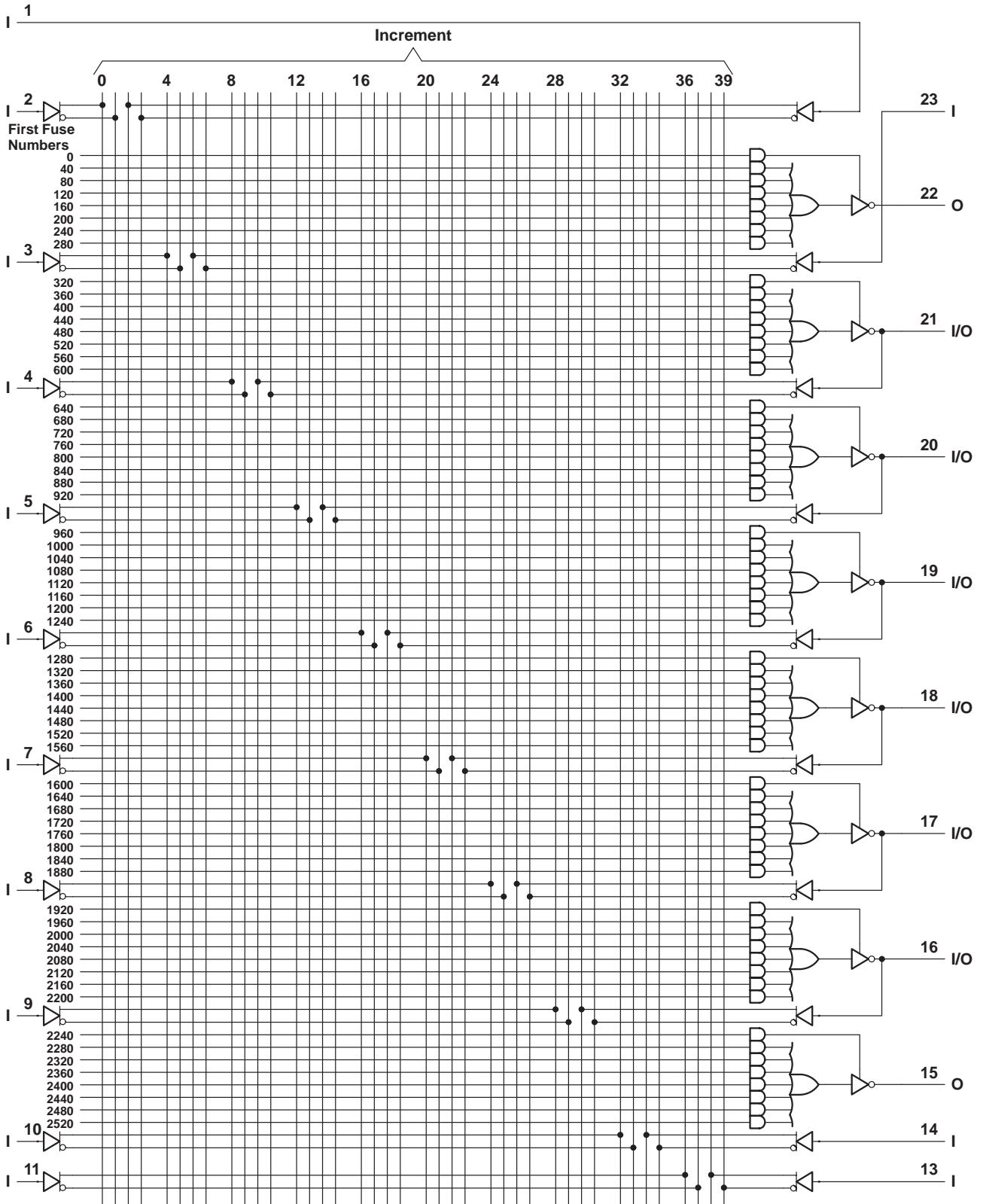
~ denotes fused inputs

functional block diagrams (positive logic)



~ denotes fused inputs

logic diagram (positive logic)

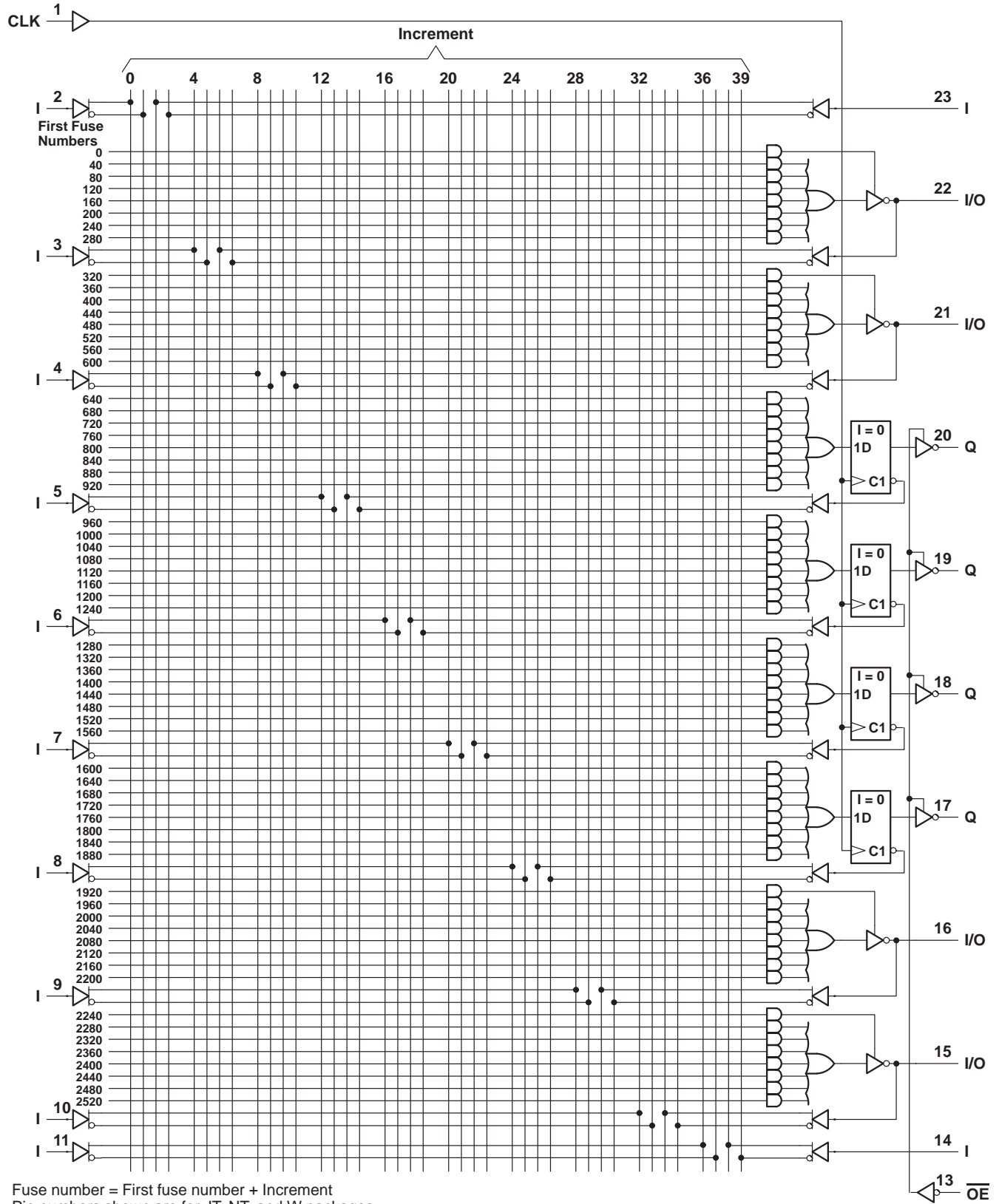


Fuse number = First fuse number + Increment
 Pin numbers shown are for JT, NT, and W packages.

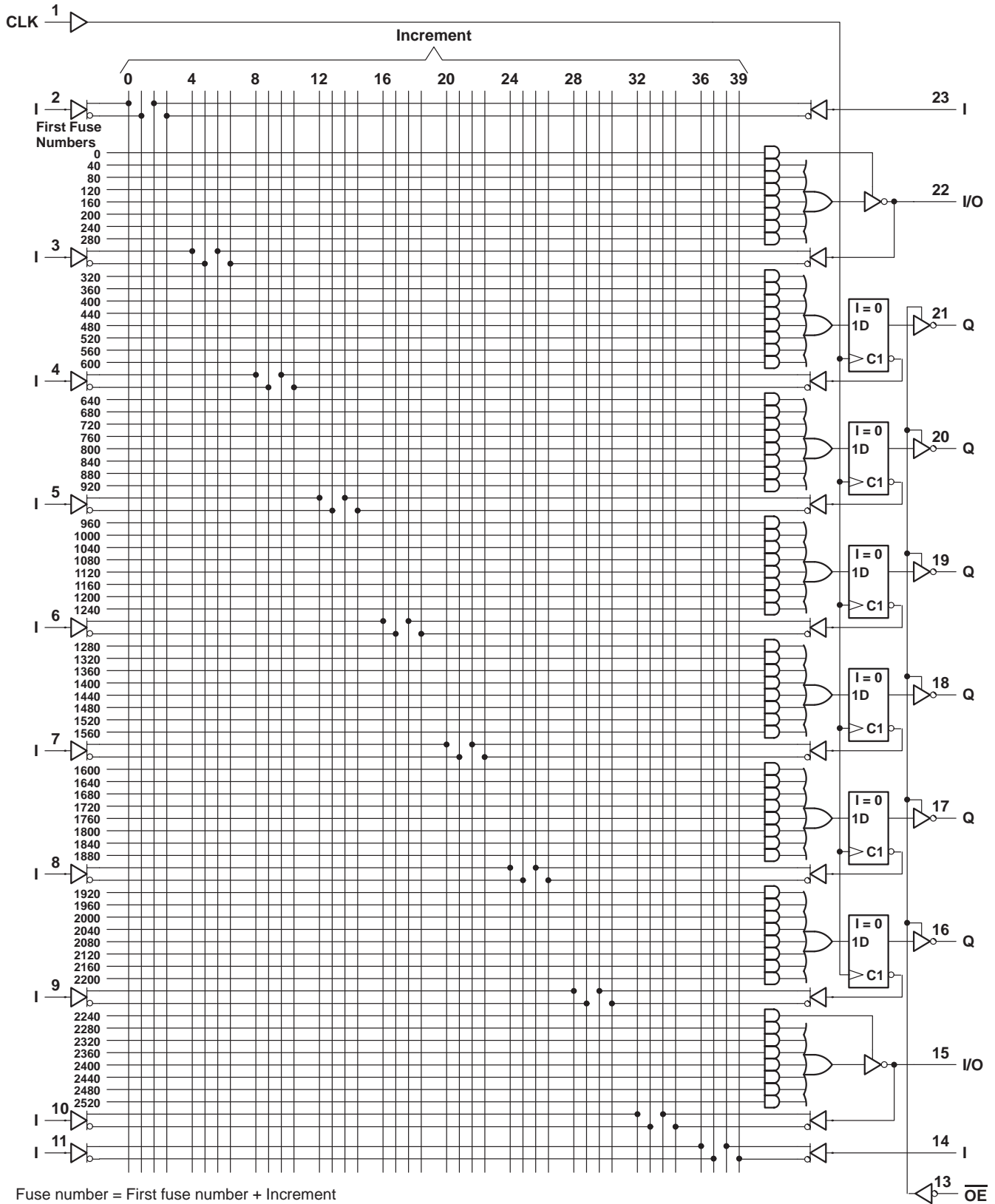


TIBPAL20R4-15C
 TIBPAL20R4-20M
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logic diagram (positive logic)



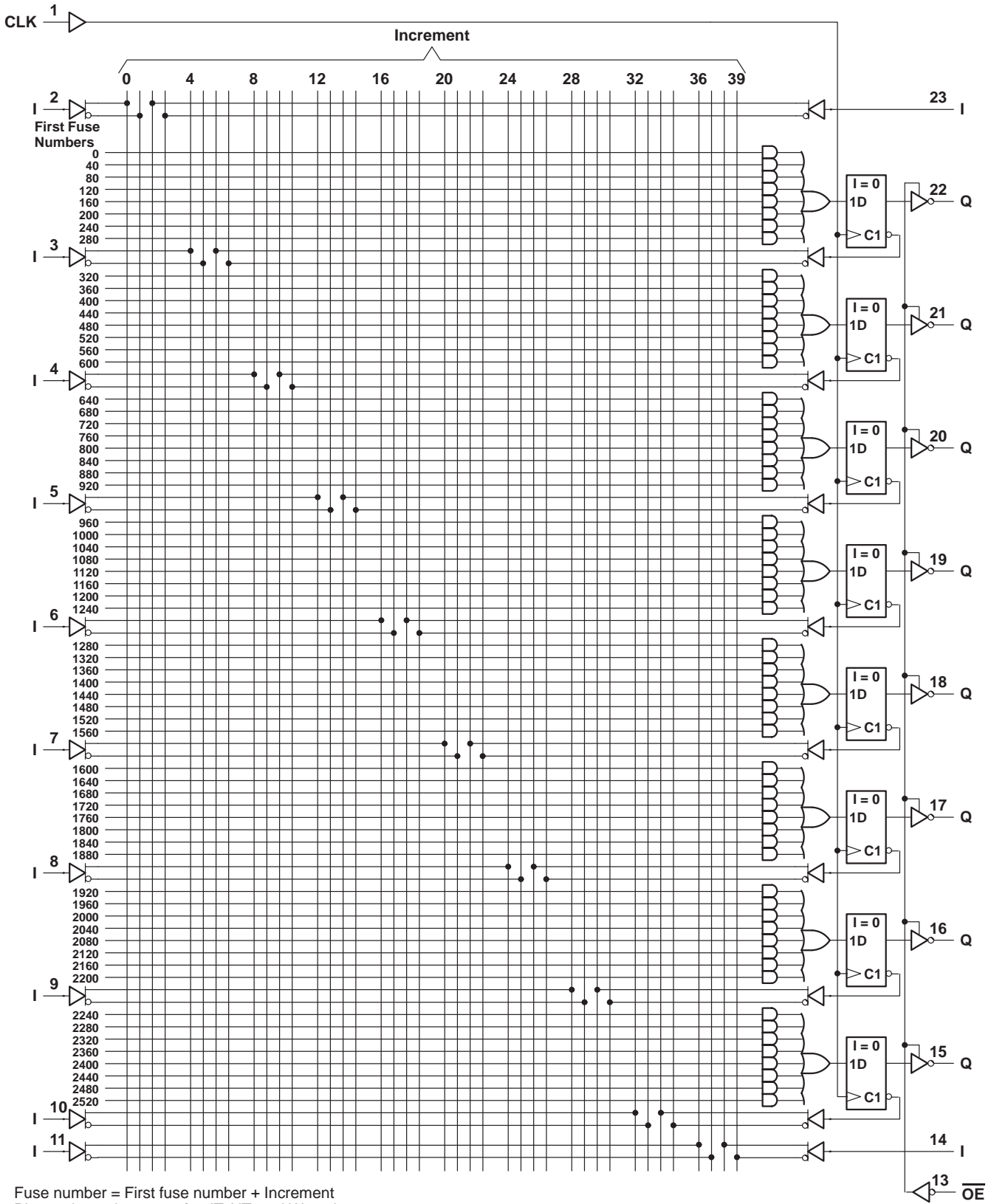
logic diagram (positive logic)



Fuse number = First fuse number + Increment
 Pin numbers shown are for JT, NT, and W packages.

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TIBPAL20R8-20M
HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS
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logic diagram (positive logic)



TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage (see Note 1) | 5.5 V |
| Voltage applied to disabled output (see Note 1) | 5.5 V |
| Operating free-air temperature range | 0°C to 75°C |
| Storage temperature range | –65°C to 150°C |

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------|---|------|-----|------|------|
| V_{CC} | Supply voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | 5.5 | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | –3.2 | mA |
| I_{OL} | Low-level output current | | | 24 | mA |
| f_{clock}^\dagger | Clock frequency | 0 | | 45 | MHz |
| t_w^\dagger | Pulse duration, clock | High | 10 | | ns |
| | | Low | 12 | | |
| t_{su}^\dagger | Setup time, input or feedback before clock \uparrow | 15 | | | ns |
| t_h^\dagger | Hold time, input or feedback after clock \uparrow | 0 | | | ns |
| T_A | Operating free-air temperature | 0 | 25 | 75 | °C |

$^\dagger f_{clock}$, t_w , t_{su} , and t_h do not apply for TIBPAL20L8'.



TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS021 – D2920, JUNE 1986 – REVISED AUGUST 1989

electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-------------------|--------------|--|--|-----|------|-------|------|
| V _{IK} | | V _{CC} = 4.75 V, | I _I = -18 mA | | -0.8 | -1.5 | V |
| V _{OH} | | V _{CC} = 4.75 V, | I _{OH} = -3.2 mA | 2.4 | | | V |
| V _{OL} | | V _{CC} = 4.75 V, | I _{OL} = 24 mA | | 0.3 | 0.5 | V |
| I _{OZH} | O, Q outputs | V _{CC} = 5.25 V, | V _O = 2.7 V | | | 20 | μA |
| | I/O ports | | | | | 100 | |
| I _{OZL} | O, Q outputs | V _{CC} = 5.25 V, | V _O = 0.4 V | | | -20 | μA |
| | I/O ports | | | | | -250 | |
| I _I | | V _{CC} = 5.25 V, | V _I = 5.5 V | | | 0.1 | mA |
| I _{IH} ‡ | | V _{CC} = 5.25 V, | V _I = 2.7 V | | | 25 | μA |
| I _{IL} ‡ | | V _{CC} = 5.25 V, | V _I = 0.4 V | | | -0.25 | mA |
| I _{OS} § | | V _{CC} = 5.25 V, | V _O = 0.5 V | -30 | -70 | -130 | mA |
| I _{CC} | | V _{CC} = 5.25 V, Outputs open, | V _I = 0, OE at V _{IH} | | 120 | 180 | mA |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITION | MIN | TYP† | MAX | UNIT |
|--------------------|------------------|-------------|--|-----|------|-----|------|
| f _{max} ¶ | With feedback | | R1 = 200 Ω, R2 = 390 Ω, See Figure 3 | 37 | 40 | | MHz |
| | Without feedback | | | 45 | 50 | | |
| t _{pd} | I, I/O | O, I/O | | | 12 | 15 | ns |
| t _{pd} | CLK↑ | Q | | | 8 | 12 | ns |
| t _{en} | OE | Q | | | 10 | 15 | ns |
| t _{dis} | OE↑ | Q | | | 8 | 12 | ns |
| t _{en} | I, I/O | O, I/O | | 12 | 18 | ns | |
| t _{dis} | I, I/O | O, I/O | | 12 | 15 | ns | |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

$$¶ f_{\max}(\text{with feedback}) = \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})} \quad f_{\max}(\text{without feedback}) = \frac{1}{t_w \text{ high} + t_w \text{ low}}$$

f_{max} does not apply for TIBPAL20L8.



TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage (see Note 1) | 5.5 V |
| Voltage applied to disabled output (see Note 1) | 5.5 V |
| Operating free-air temperature range | –55°C to 125°C |
| Storage temperature range | –65°C to 150°C |

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---------------------|---|------|-----|------|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 5.5 | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | –2 | mA |
| I_{OL} | Low-level output current | | | 12 | mA |
| f_{clock}^\dagger | Clock frequency | 0 | | 41.6 | MHz |
| t_w^\dagger | Pulse duration, clock | High | | 12 | ns |
| | | Low | | 12 | |
| t_{su}^\dagger | Setup time, input or feedback before clock \uparrow | 20 | | | ns |
| t_h^\dagger | Hold time, input or feedback after clock \uparrow | 0 | | | ns |
| T_A | Operating free-air temperature | –55 | 25 | 125 | °C |

$^\dagger f_{clock}$, t_w , t_{su} , and t_h do not apply for TIBPAL20L8'.



TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------|--------------|---|---|-----|------|-------|------|
| V _{IK} | | V _{CC} = 4.5 V, | I _I = -18 mA | | -0.8 | -1.5 | V |
| V _{OH} | | V _{CC} = 4.5 V, | I _{OH} = -2 mA | 2.4 | 3.2 | | V |
| V _{OL} | | V _{CC} = 4.5 V, | I _{OL} = 12 mA | | 0.3 | 0.5 | V |
| I _{OZH} | | V _{CC} = 5.5 V, | V _O = 2.7 V | | | 100 | μA |
| I _{OZL} ‡ | O, Q outputs | V _{CC} = 5.5 V, | V _O = 0.4 V | | | -20 | μA |
| | I/O ports | | | | | -250 | |
| I _I | | V _{CC} = 5.5 V, | V _I = 5.5 V | | | 1 | mA |
| I _{IH} ‡ | I/O ports | V _{CC} = 5.5 V, | V _I = 2.7 V | | | 100 | μA |
| | All others | | | | | 25 | |
| I _{IL} ‡ | | V _{CC} = 5.5 V, | V _I = 0.4 V | | | -0.25 | mA |
| I _{OS} § | | V _{CC} = 5.5 V, | V _O = 0.5 V | -30 | -70 | -250 | mA |
| I _{CC} | | V _{CC} = 5.5 V, Outputs open, | V _I = 0, OE = V _{IH} | | 120 | 180 | mA |

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITION | MIN | TYP† | MAX | UNIT |
|--------------------|------------------|-------------|--|------|------|-----|------|
| f _{max} ¶ | With feedback | | R1 = 390 Ω, R2 = 750 Ω, See Figure 3 | 28.5 | 40 | | MHz |
| | Without feedback | | | 41.6 | 50 | | |
| t _{pd} | I, I/O | O, I/O | | | 12 | 20 | ns |
| t _{pd} | CLK↑ | Q | | | 8 | 15 | ns |
| t _{en} | OE | Q | | | 10 | 20 | ns |
| t _{dis} | OE↑ | Q | | | 8 | 20 | ns |
| t _{en} | I, I/O | O, I/O | | | 12 | 25 | ns |
| t _{dis} | I, I/O | O, I/O | | | 12 | 20 | ns |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

$$¶ f_{\max(\text{with feedback})} = \frac{1}{t_{\text{su}} + t_{\text{pd}}(\text{CLK to Q})}, \quad f_{\max(\text{without feedback})} = \frac{1}{t_{\text{w high}} + t_{\text{w low}}}$$

f_{max} does not apply for TIBPAL20L8,.



programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL} , raise Pin 13 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 13 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.

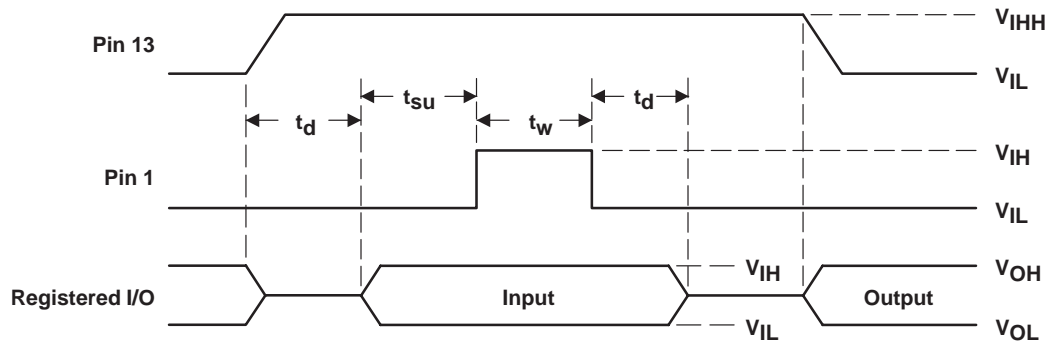


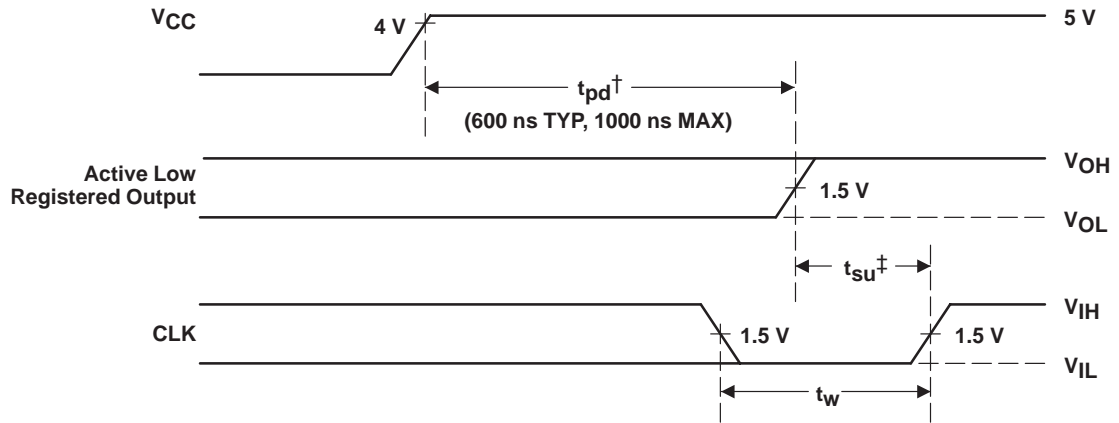
Figure 1. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT, NT, and W packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

3. $t_d = t_{su} = t_h = 100 \text{ ns to } 1000 \text{ ns}$ $V_{IHH} = 10.25 \text{ V to } 10.75 \text{ v}$

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

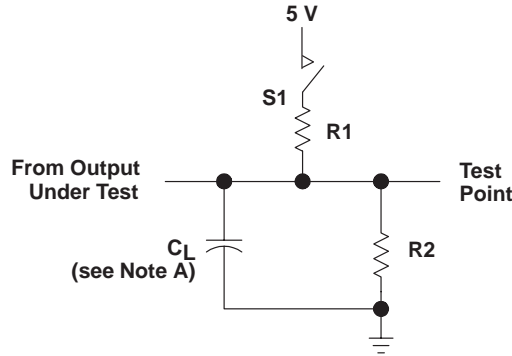


† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

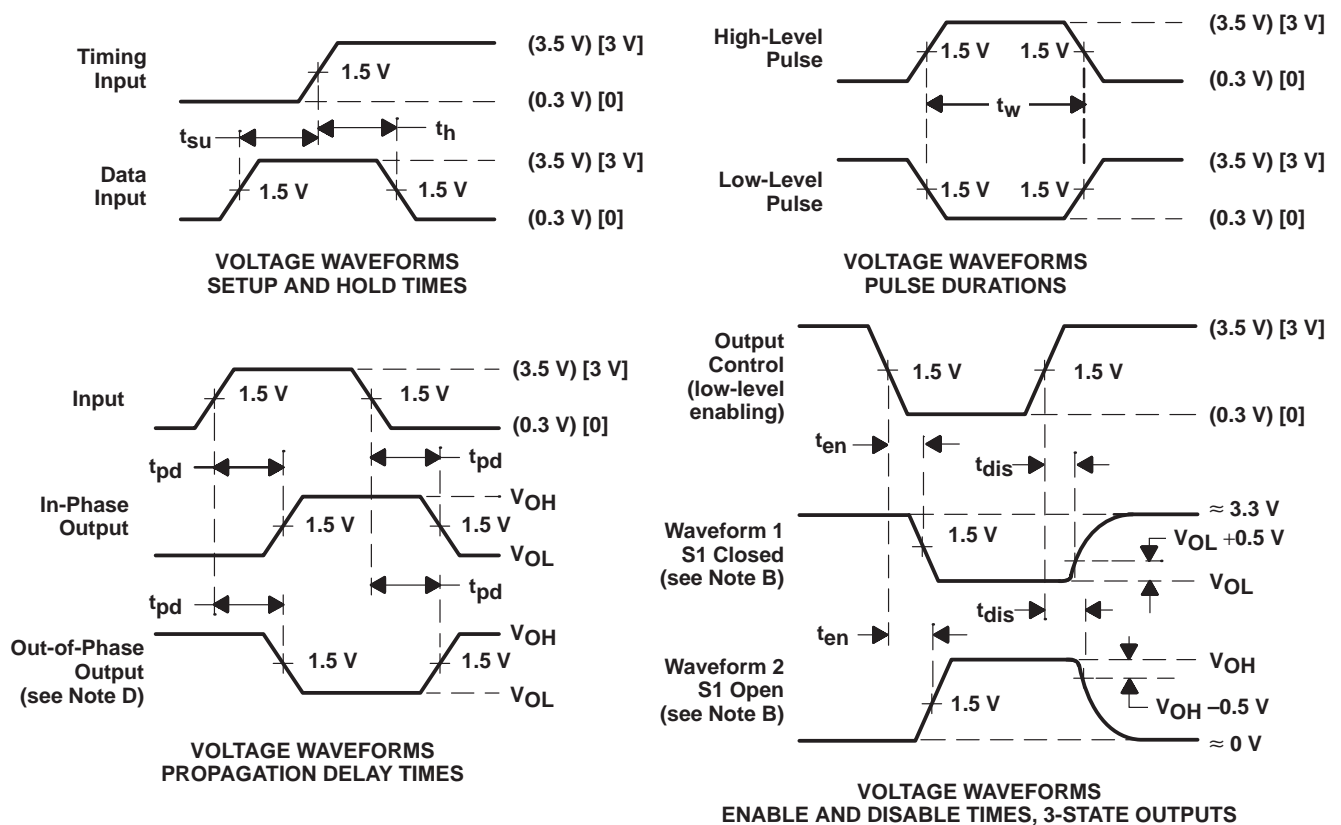
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR 3-STATE OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control.
 C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses (). PRR \leq 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets []. PRR \leq 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

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