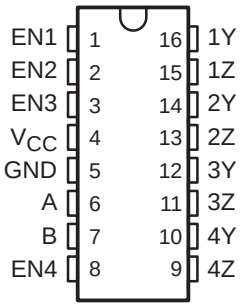
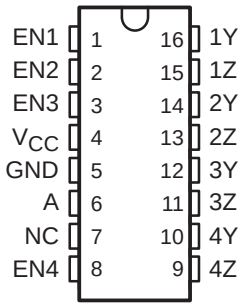
- **Receiver and Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
  - **SN65LVDS105 Receives Low-Voltage TTL (LVTTL) Levels**
  - **SN65LVDS104 Receives Differential Input Levels, ±100 mV**
- **Designed for Signaling Rates up to 630 Mbps**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Propagation Delay Time**
  - **SN65LVDS105 . . . 2.2 ns (Typ)**
  - **SN65LVDS104 . . . 3.1 ns (Typ)**
- **Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Networks**
- **Driver Outputs Are High Impedance When Disabled or With V_{CC} <1.5 V**
- **Bus-Pin ESD Protection Exceeds 16 kV**
- **SOIC and TSSOP Packaging**

SN65LVDS104
D OR PW PACKAGE
(TOP VIEW)

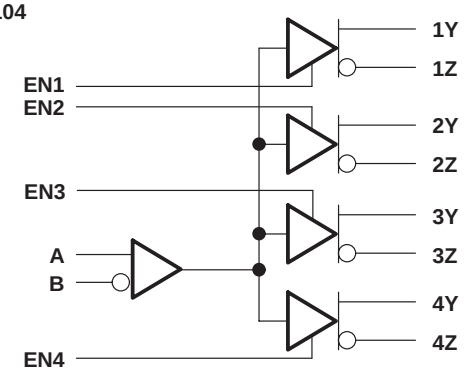


SN65LVDS105
D OR PW PACKAGE
(TOP VIEW)

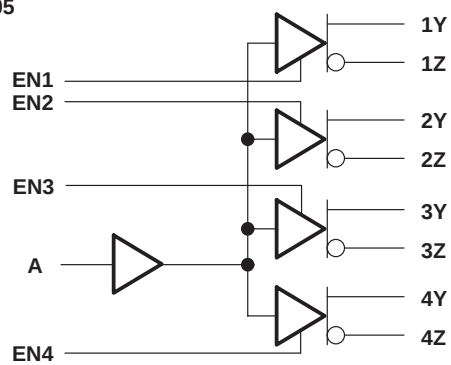


logic diagram (positive logic)

'LVDS104



'LVDS105



description

The SN65LVDS104 and SN65LVDS105 are a differential line receiver and a LVTTL input (respectively) connected to four differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644 is a data signaling technique that offers low-power, low-noise coupling, and switching speeds to transmit data at speeds up to 655 Mbps at relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. Having the drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in distribution or expansion of signals such as clock or serial data stream.

The SN65LVDS104 and SN65LVDS105 are characterized for operation from –40°C to 85°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

The SN65LVDS104 and SN65LVDS105 are members of a family of LVDS repeaters. A brief overview of the family is provided in the table below.

Selection Guide to LVDS Repeaters

DEVICE	NO. INPUTS	NO. OUTPUTS	PACKAGE	COMMENT
SN65LVDS22	2 LVDS	2 LVDS	16-pin D	Dual multiplexed LVDS repeater
SN65LVDS104	1 LVDS	4 LVDS	16-pin D	4-Port LVDS repeater
SN65LVDS105	1 LVTTL	4 LVDS	16-pin D	4-Port TTL-to-LVDS repeater
SN65LVDS108	1 LVDS	8 LVDS	38-pin DBT	8-Port LVDS repeater
SN65LVDS109	2 LVDS	8 LVDS	38-pin DBT	Dual 4-port LVDS repeater
SN65LVDS116	1 LVDS	16 LVDS	64-pin DGG	16-Port LVDS repeater
SN65LVDS117	2 LVDS	16 LVDS	64-pin DGG	Dual 8-port LVDS repeater

Function Tables

SN65LVDS104

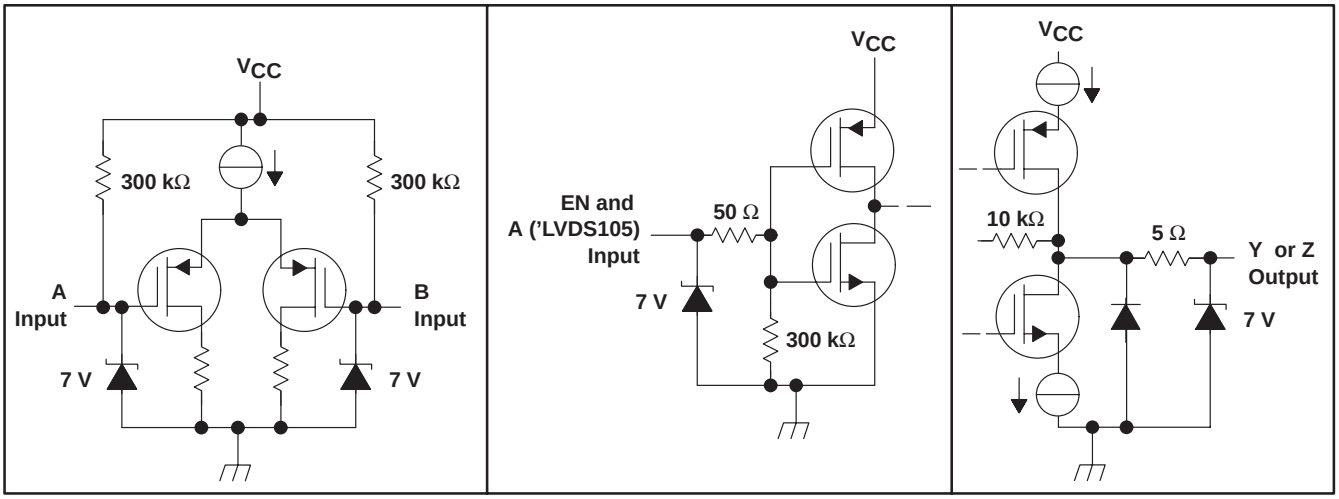
INPUT		OUTPUT	
$V_{ID} = V_A - V_B$	#EN	#Y	#Z
X	X	Z	Z
X	L	Z	Z
$V_{ID} \geq 100$ mV	H	H	L
-100 mV $< V_{ID} < 100$ mV	H	?	?
$V_{ID} \leq -100$ mV	H	L	H

SN65LVDS105

INPUT		OUTPUT	
A	#EN	#Y	#Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Z	Z
X	X	Z	Z

H = high level, L = low level, Z = high impedance, ? = indeterminate, X = don't care

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 to 4 V
Voltage range, Enable inputs . . . . . –0.5 to 6 V
A, B, Y or Z . . . . . –0.5 to 4 V
Electrostatic discharge (see Note 2); Y, Z, and GND . . . . . Class 3, A:16 kV, B: 600 V
All pins . . . . . Class 3, A:7 kV, B: 500 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$	0.1		3.6	V
Common-mode input voltage, V_{IC}	$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	V
			$V_{CC}-0.8$	V
Operating free-air temperature, T_A	–40		85	°C

SN65LVDS104 electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold		–100			
$\|V_{OD}\|$	Differential output voltage magnitude	R_L= 100Ω, V_{ID}= ± 100 mV, See Figure 1 and Figure 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			25	150	mV
I_{CC}	Supply current	Enabled, R_L = 100Ω		23	35	mA
		Disabled		3	8	mA
I_I	Input current (A or B inputs)	V_I = 0 V	–2	–11	–20	µA
		V_I = 2.4 V	–1.2	–3		
$I_{I(OFF)}$	Power-off Input current	V_{CC}= 1.5 V, V_I= 2.4 V			20	µA
I_{IH}	High-level input current (enables)	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±10	mA
		V_{OD} = 0 V			±10	mA
I_{OZ}	High-impedance output current	V_O = 0 V or 2.4 V			±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V			±1	µA
C_{IN}	Input capacitance (A or B inputs)	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
C_O	Output capacitance (Y or Z outputs)	V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled		9.4		pF

† All typical values are at 25°C and with a 3.3 V supply.

SN65LVDS104 switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100Ω, C_L = 10 pF, See Figure 4	2.4	3.2	4.2	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2.2	3.1	4.2	ns
t_r	Differential output signal rise time		0.3	0.8	1.2	ns
t_f	Differential output signal fall time		0.3	0.8	1.2	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)			150	500	ps
$t_{sk(o)}$	Channel-to-channel output skew‡			20	100	ps
$t_{sk(pp)}$	Part-to-part skew§				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		7.2	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			8.4	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.6	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			6	15	ns

† All typical values are at 25°C and with a 3.3 V supply.
‡ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
§ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

SN65LVDS105 electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L= 100Ω, V_{ID}= ± 100 mV, See Figure 6 and Figure 7	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 8	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			25	150	mV
I_{CC}	Supply current	Enabled, R_L = 100Ω		23	35	mA
		Disabled		0.7	6.4	mA
I_{IH}	High-level input current	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±10	mA
		V_{OD} = 0 V			±10	mA
I_{OZ}	High-impedance output current	V_O = 0 V or 2.4 V			±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V		0.3	±1	µA
C_{IN}	Input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		5		pF
C_O	Output capacitance (Y or Z outputs)	V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled		9.4		pF

† All typical values are at 25°C and with a 3.3 V supply.

SN65LVDS105 switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100Ω, C_L = 10 pF, See Figure 9	1.7	2.2	3	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.4	2.3	3.5	ns
t_r	Differential output signal rise time		0.3	0.8	1.2	ns
t_f	Differential output signal fall time		0.3	0.8	1.2	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			150	500	ps
$t_{sk(o)}$	Channel-to-channel output skew‡			20	100	ps
$t_{sk(pp)}$	Part-to-part skew§				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 10		7.2	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			8.4	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.6	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			6	15	ns

† All typical values are at 25°C and with a 3.3 V supply.
‡ $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
§ $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

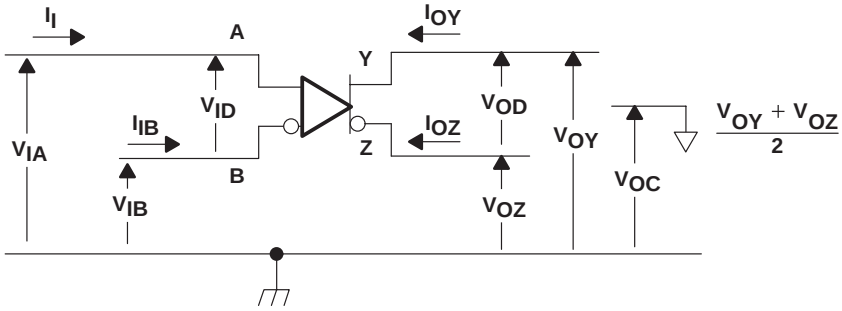


Figure 1. ’LVDS104 Voltage and Current Definitions

Table 1. SN65LVDS104 Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

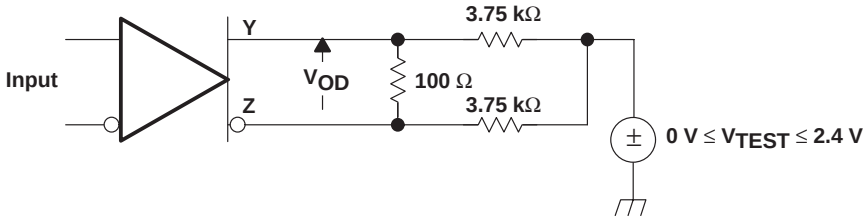
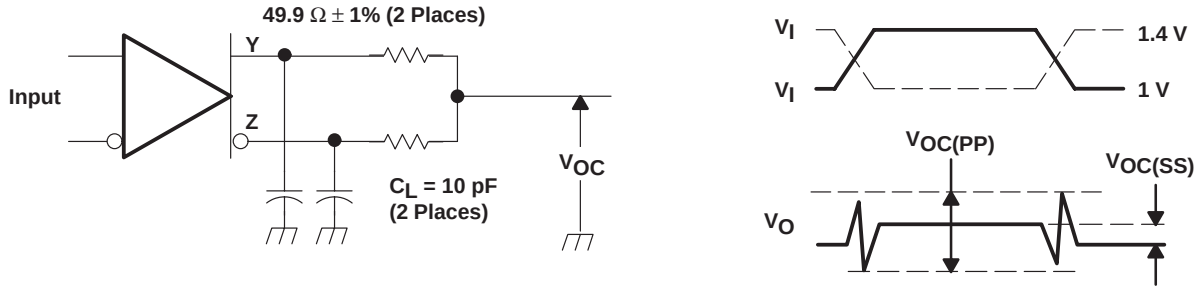


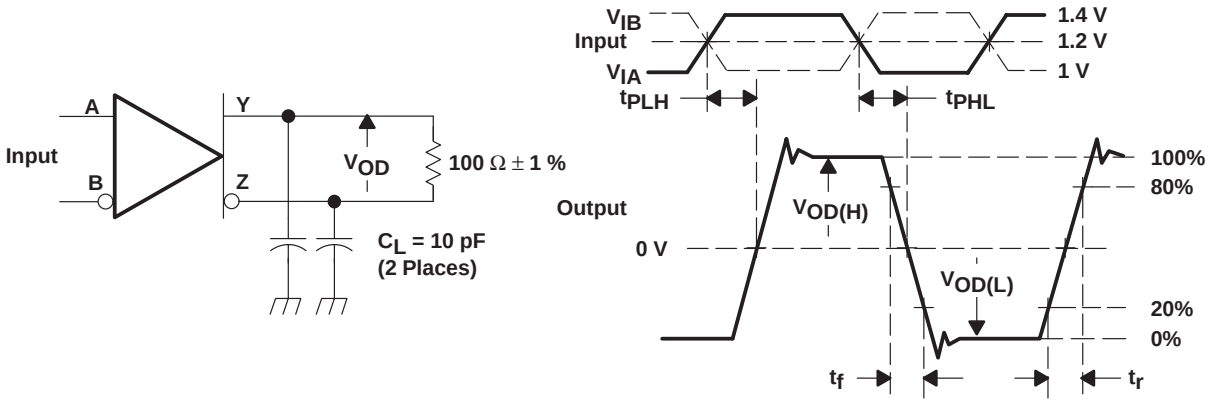
Figure 2. ’LVDS104 VOD Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

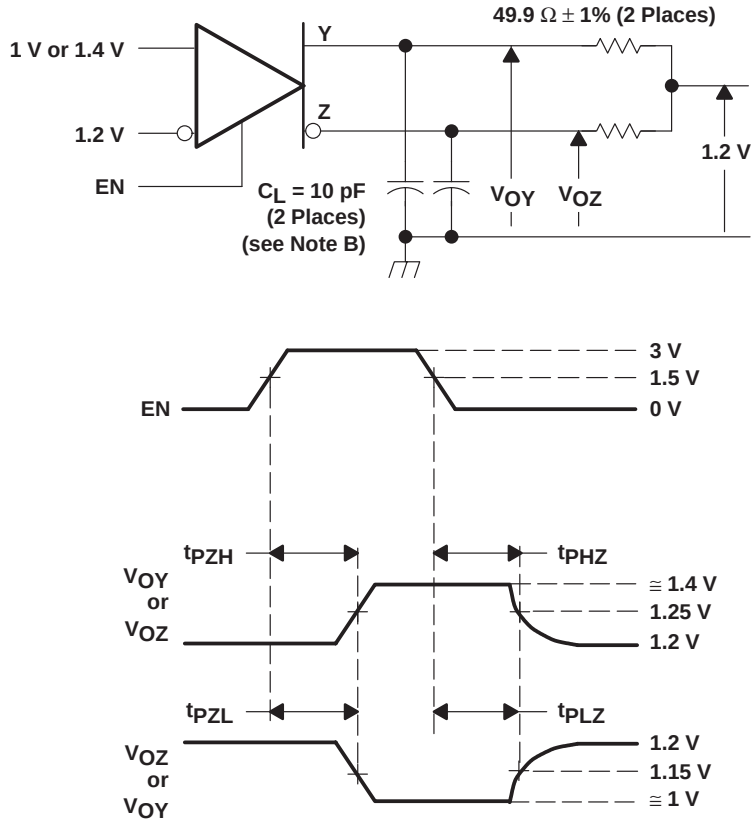
Figure 3. ’LVDS104 Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 4. ’LVDS104 Test Circuit, Timing, and Voltage Definitions for the Differential output Signal

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. ’LVDS104 Enable and Disable Time Circuit and Definitions

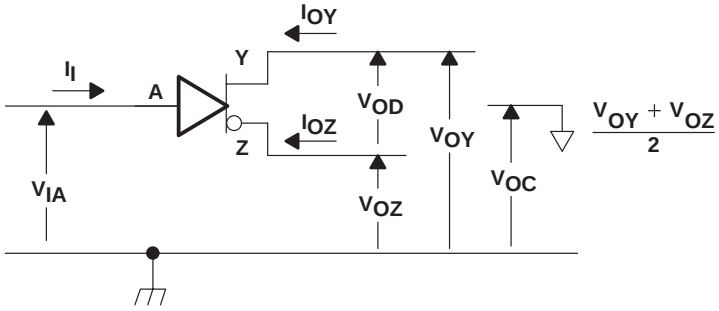


Figure 6. ’LVDS105 Voltage and Current Definitions

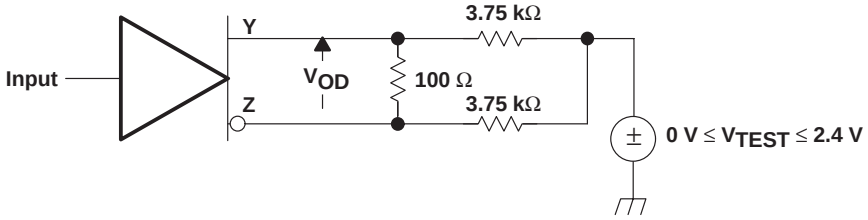
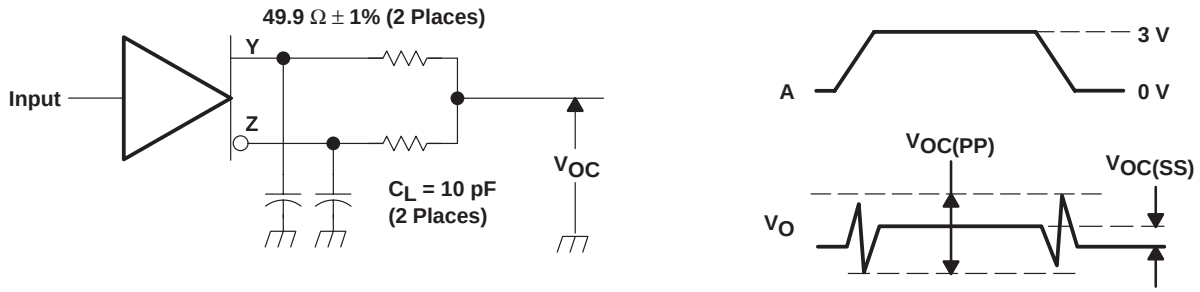


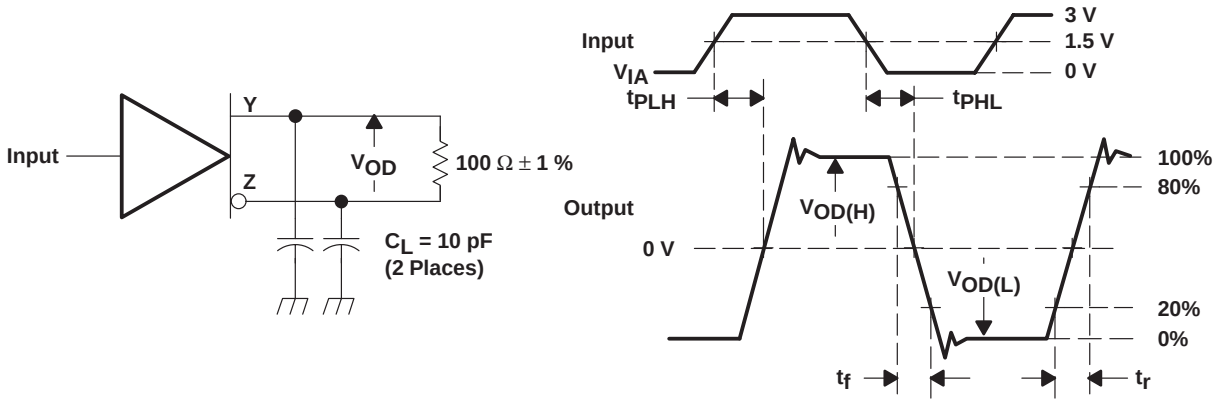
Figure 7. ’LVDS105 VOD Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

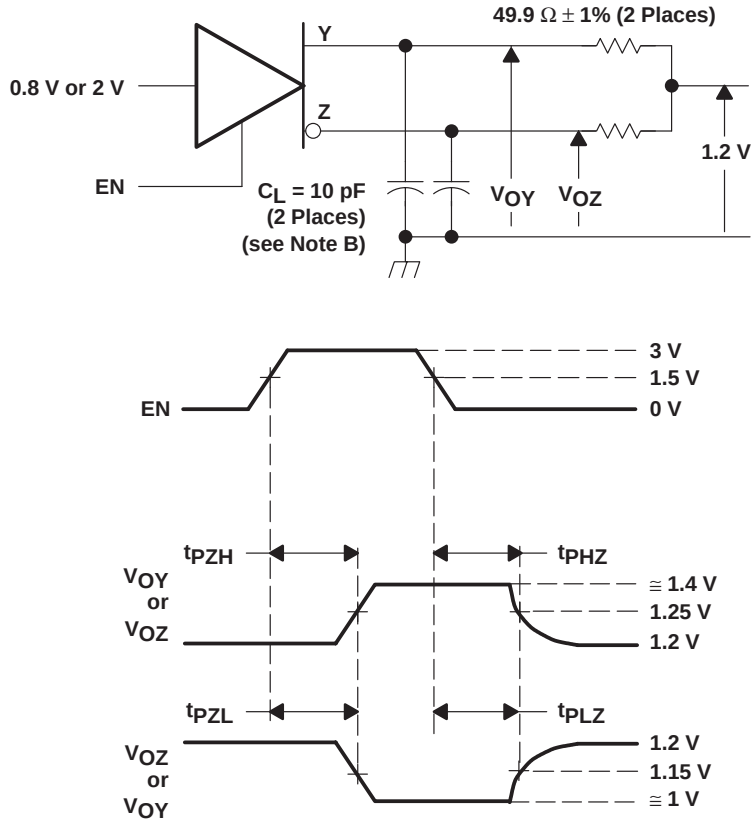
Figure 8. ’LVDS105 Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 9. ’LVDS105 Test Circuit, Timing, and Voltage Definitions for the Differential output Signal

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 10. ’LVDS105 Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTIC

SN65LVDS104
SUPPLY CURRENT
vs
SWITCHING FREQUENCY

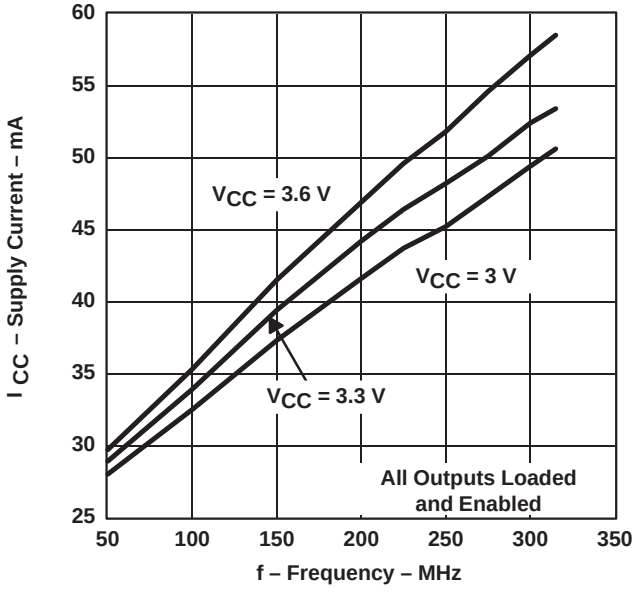


Figure 11

SN65LVDS105
SUPPLY CURRENT
vs
SWITCHING FREQUENCY

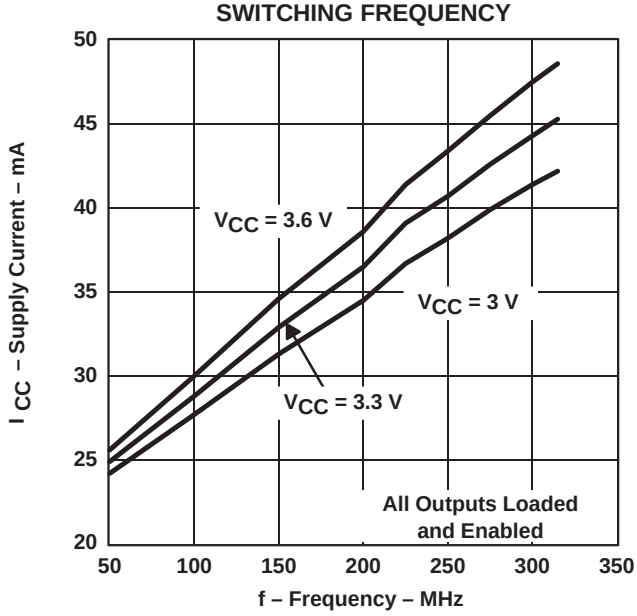


Figure 12

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

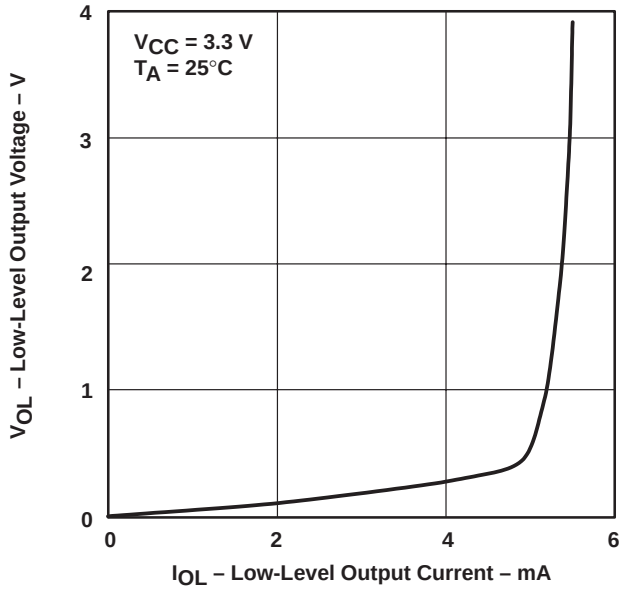


Figure 13

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

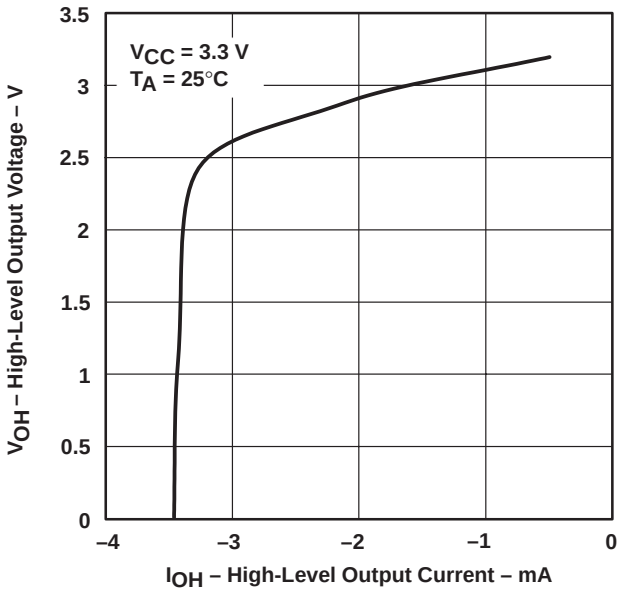


Figure 14

TYPICAL CHARACTERISTIC

SN65LVDS104
LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

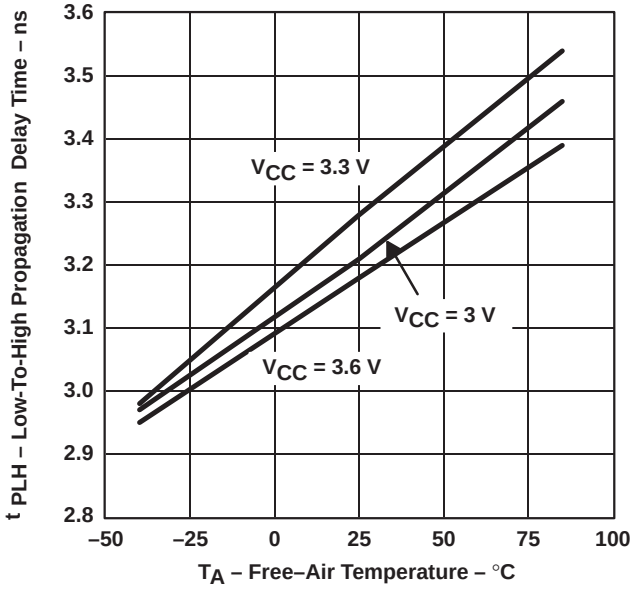


Figure 15

SN65LVDS104
HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

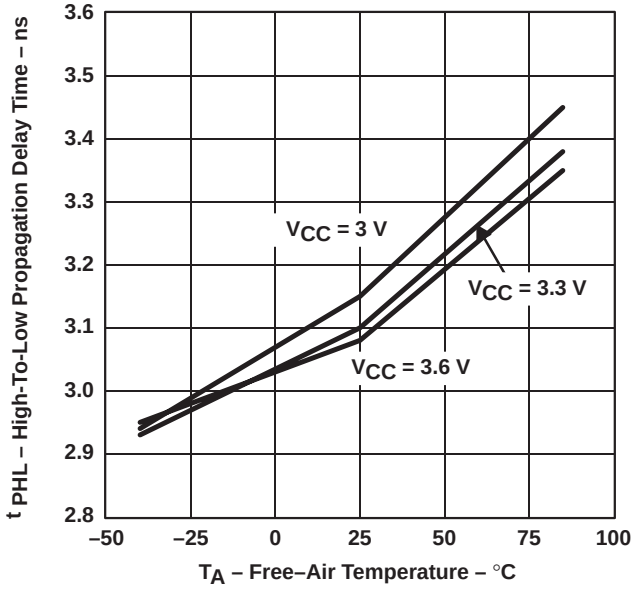


Figure 16

SN65LVDS105
LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

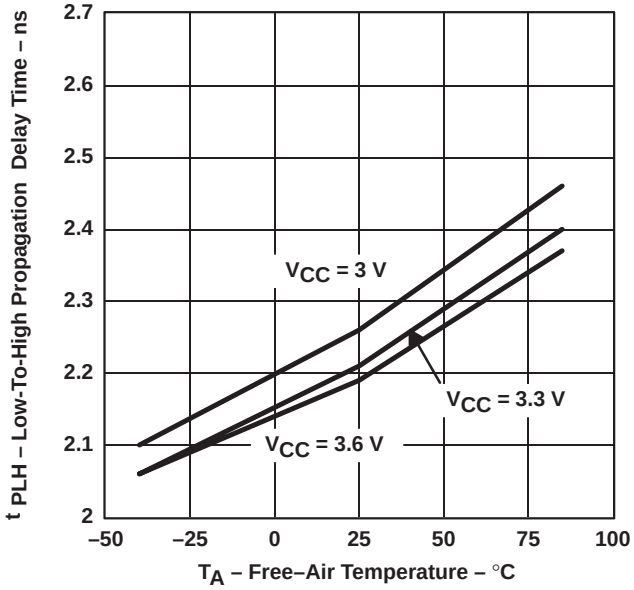


Figure 17

SN65LVDS105
HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

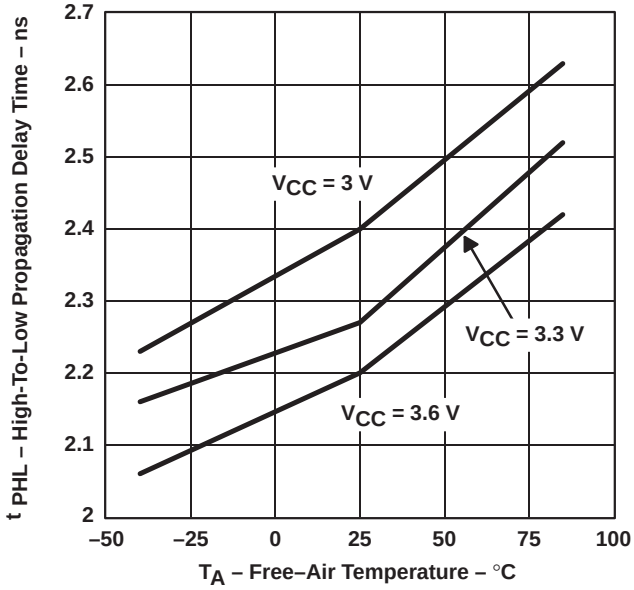


Figure 18

APPLICATION INFORMATION

A LVDS receiver can be used to receive various other types of logic signals. Figure 19 through Figure 28 show the termination circuits for SSTL, HSTL, GTL, BTL, LVPECL, PECL, CMOS, and TTL.

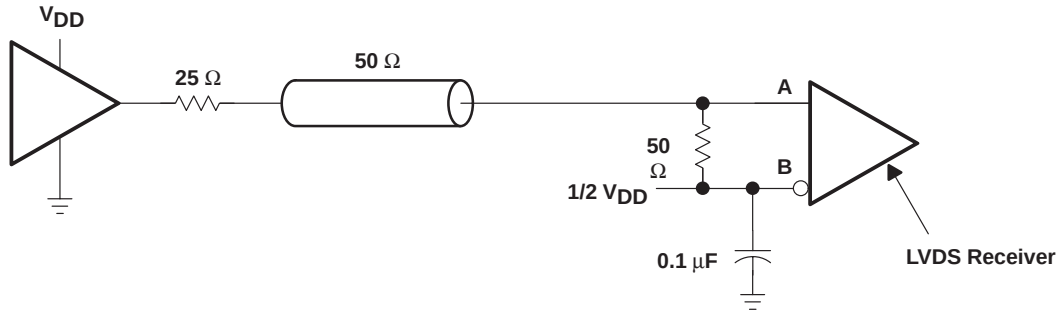


Figure 19. Stub-Series Terminated (SSTL) or High-Speed Transceiver Logic (HSTL)

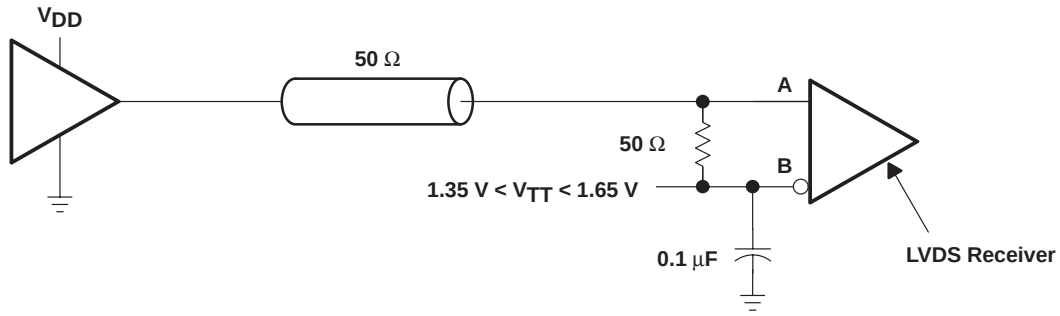


Figure 20. Center-Tap Termination (CTT)

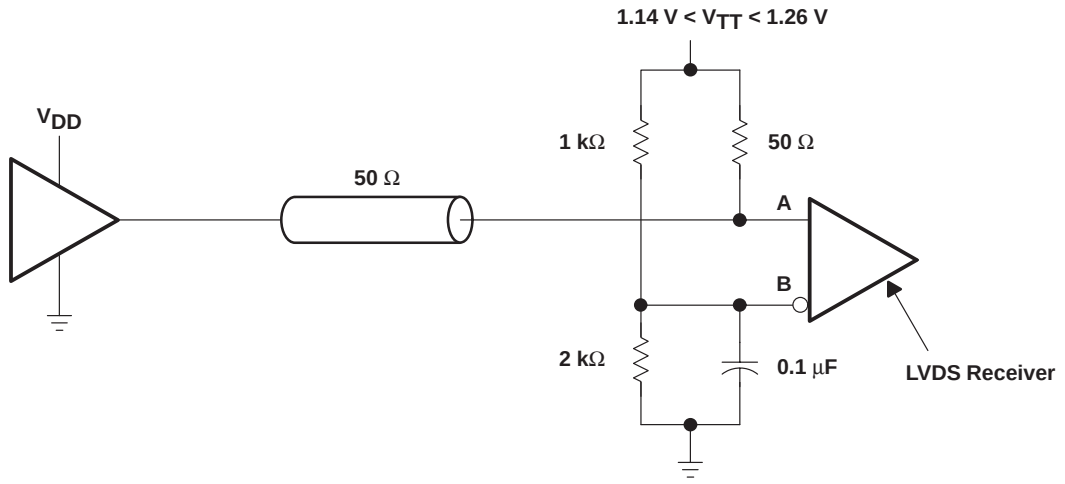


Figure 21. Gunning Transceiver Logic (GTL)

APPLICATION INFORMATION

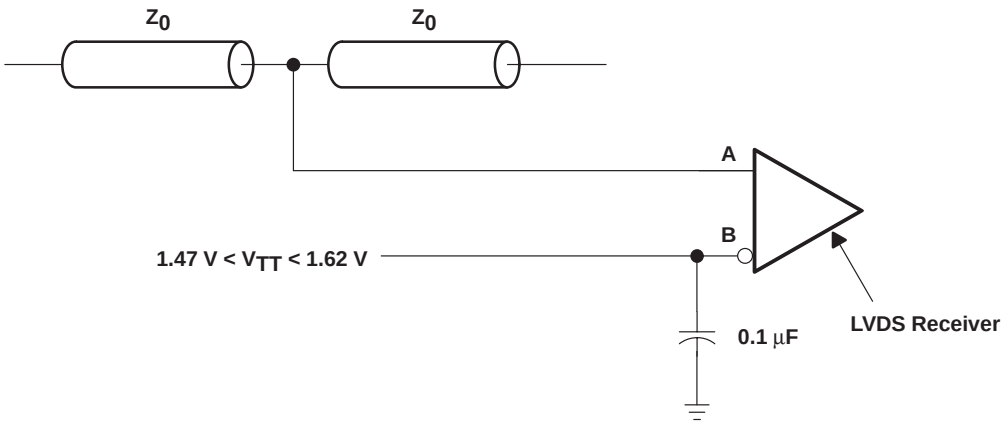


Figure 22. Backplane Transceiver Logic (BTL)

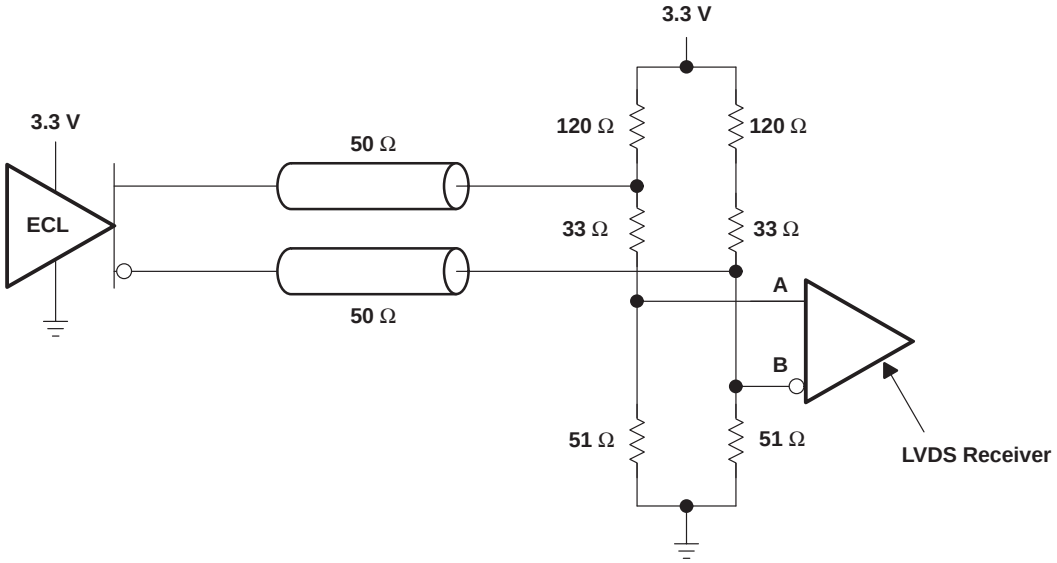


Figure 23. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

APPLICATION INFORMATION

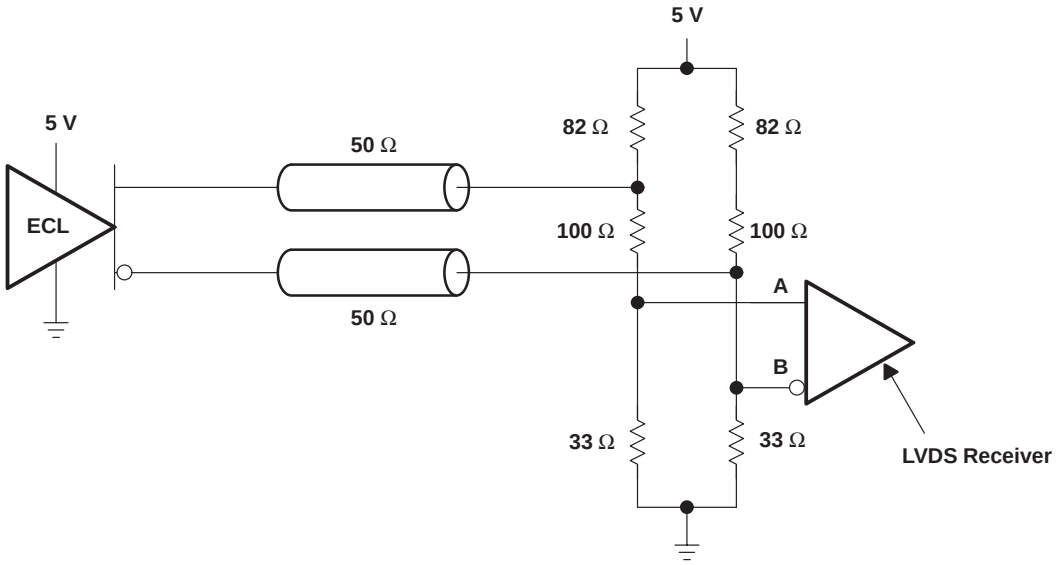


Figure 24. Postive Emitter-Coupled Logic (PECL)

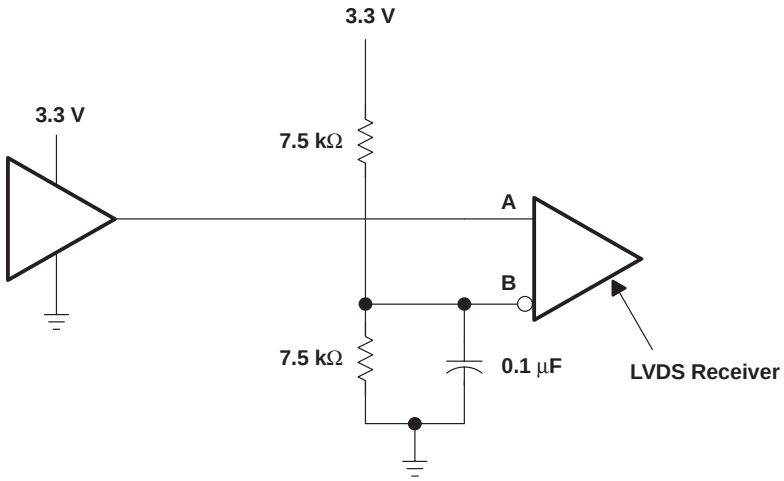


Figure 25. 3.3-V CMOS

APPLICATION INFORMATION

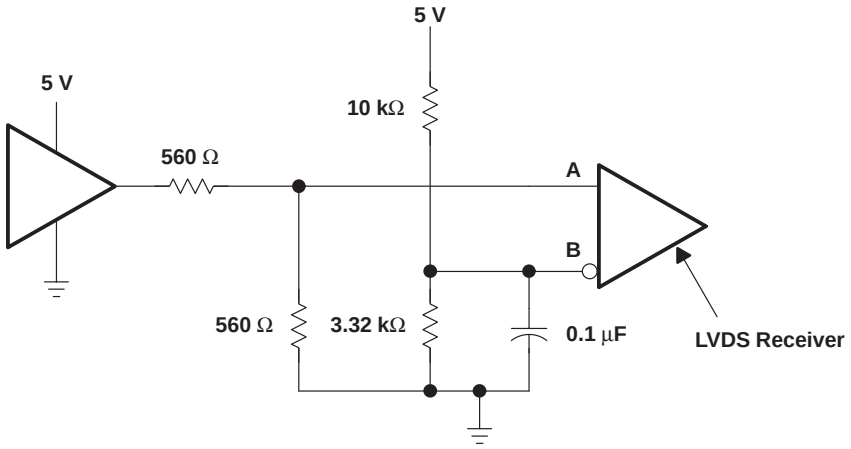


Figure 26. 5-V CMOS

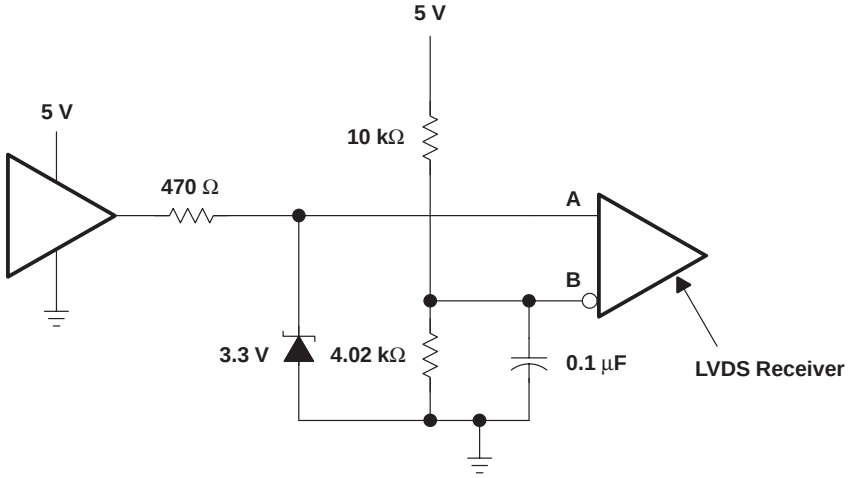


Figure 27. 5-V TTL

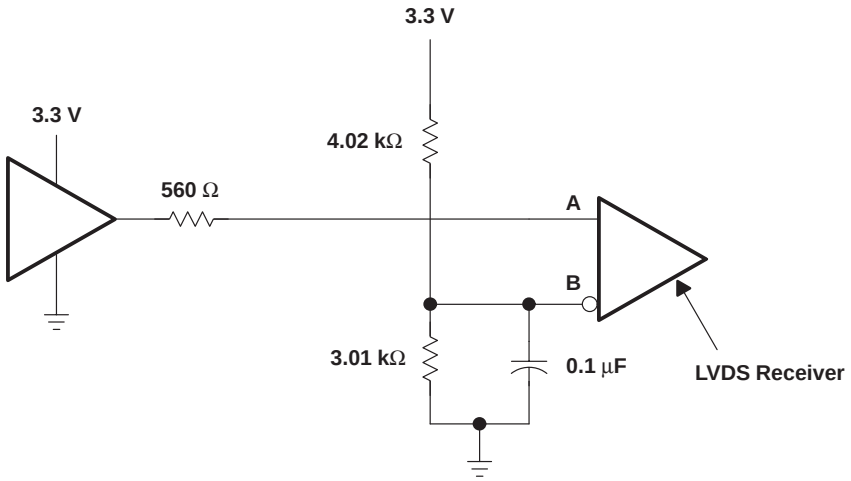


Figure 28. LVTTL

APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 10. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

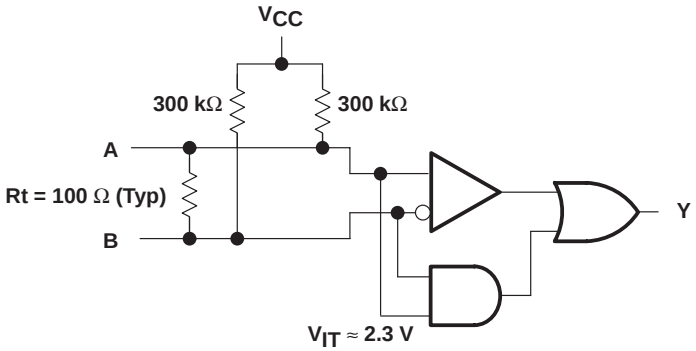


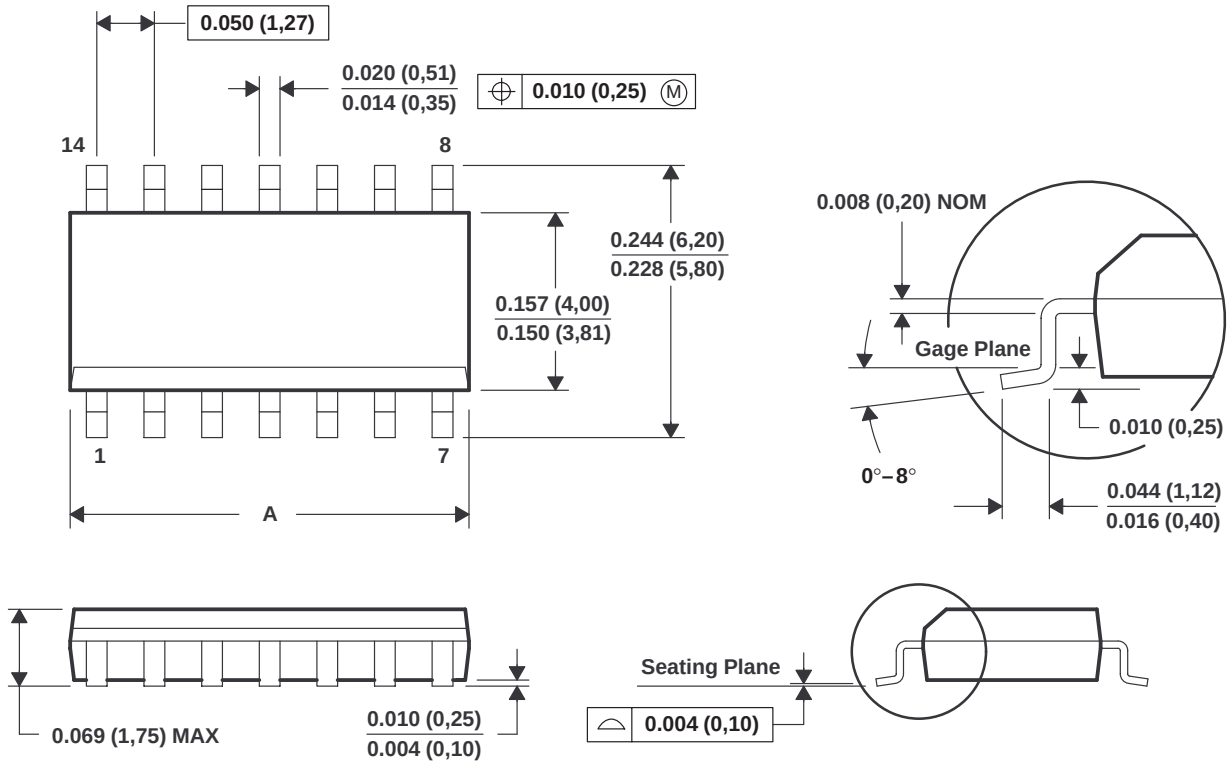
Figure 29. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

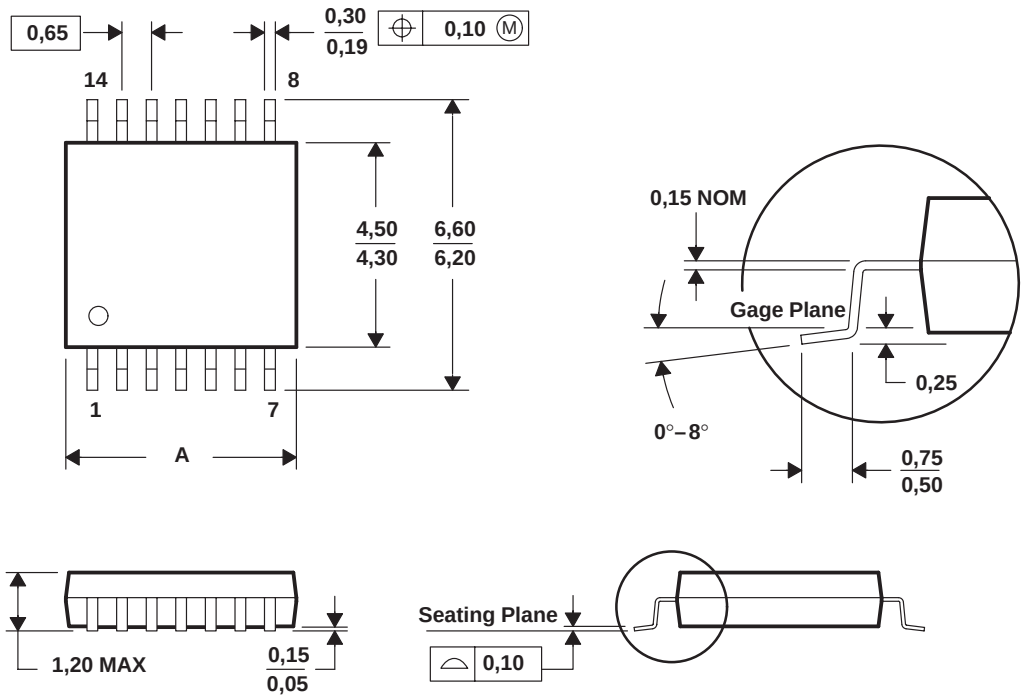
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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