

DUAL LVDS DIFFERENTIAL DRIVERS AND RECEIVERS

FEATURES

- DS90LV049 Compatible
- Up to 400 Mbps Signaling Rates
- Flow-Through Pin-out
- 50 ps Driver Channel-to-Channel Skew (Typ)
- 50 ps Receiver Channel-to-Channel Skew (Typ)
- 3.3-V Power Supply
- High-Impedance Disable for all Outputs
- Internal Failsafe Biasing of Receiver Inputs
- 1.4 ns Driver Propagation Delay (Typ)
- 1.9 ns Receiver Propagation Delay (Typ)
- High Impedance Bus Pins on Power Down
- ANSI TIA/EIA-644-A Compliant
- Receiver Input and Driver Output ESD Exceeds 10 kV
- 16-pin TSSOP Package

APPLICATIONS

- Full-duplex LVDS Communications of Clock and Data
- Printers

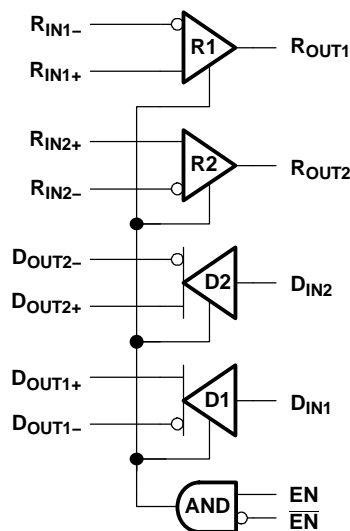
DESCRIPTION

The SN65LVDS049 is a dual flow-through differential line driver-receiver pair that uses low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The TIA/EIA-644-A standard compliant electrical interface provides a minimum differential output voltage magnitude of 250 mV into a 100-Ω load and receipt of signals with up to 1 V of ground potential difference between a transmitter and receiver. The LVDS receivers have internal failsafe biasing that places the outputs into a known high state for unconnected differential inputs.

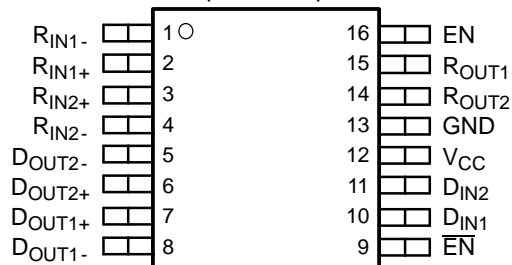
The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics)

The SN65LVDS049 is characterized for operation from -40°C to 85°C

FUNCTIONAL DIAGRAM



PW PACKAGE (Marked as LVDS049) (TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DRIVER TRUTH TABLE

INPUT	ENABLES		OUTPUTS (1)	
DIN	EN	$\overline{\text{EN}}$	D _{OUT+}	D _{OUT-}
L	H	L or OPEN	L	H
H			H	L
X	All other conditions		Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

RECEIVER TRUTH TABLE

DIFFERENTIAL INPUT	ENABLES		OUTPUT (1)
R _{IN-} - R _{IN+}	EN	$\overline{\text{EN}}$	R _{OUT}
V _{ID} ≥ 100 mV	H	L or OPEN	H
V _{ID} ≤ - 100 mV			L
Open/short or terminated			H
X	All other conditions		Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

ENABLE FUNCTION TABLE

ENABLES		OUTPUTS	
EN	EN	LVDS Out	LVCMOS Out
L or Open	L or Open	DISABLED	DISABLED
H	L or Open	ENABLED	ENABLED
L or Open	H	DISABLED	DISABLED
H	H	DISABLED	DISABLED

POWER DISSIPATION RATING

PACKAGE	CIRCUIT BOARD MODEL	T _A ≤ 25°C POWER RATING	DERATING FACTOR (1) ABOVE T _A = 25°C	T _A = 85°C POWER RATING
PW	Low-K (2)	774 mW	6.2 mW/°C	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT	
Supply voltage range (2), V_{CC}		-0.3 V to 4 V	
Voltage range	D_{IN} , R_{OUT} , EN , or \overline{EN}	-0.3 V to ($V_{CC} + 0.3$ V)	
	R_{IN+} or R_{IN-}	-0.3 V to 4 V	
	D_{OUT+} or D_{OUT-}	-0.3 V to 3.9 V	
ESD	Human Body Model (3)	R_{IN+} , R_{IN-} , D_{OUT+} , and D_{OUT-}	± 10 kV
		All pins	± 2 K V
	Charged-Device Model (4)	All pins	± 500 V
LVDS output short circuit duration (D_{OUT+} , D_{OUT-})		Continuous	
Continuous power dissipation		See Dissipation Rating Table	
Storage temperature range		-65°C to 150°C	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	GND			V
Common-mode input voltage, V_{IC}	$\frac{ V_{ID} }{2}$	2.4	$\frac{ V_{ID} }{2}$	V
				$V_{CC} - 0.8$
Operating free-air temperature, T_A	-40		85	°C

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
INPUT DC SPECIFICATIONS (D_{IN}, EN, \overline{EN})						
V_{IH}	Input high voltage		2.0		V_{CC}	V
V_{IL}	Input low voltage		GND		0.8	V
I_{IH}	Input high current	$V_{IN} = V_{CC}$	-10	3	10	μA
I_{IL}	Input low current	$V_{IN} = GND$	-10	1	10	μA
V_{CL}	Input clamp voltage	$I_{CL} = -18 \text{ mA}$	-1.5	-0.8		V
LVDS Output DC Specifications (D_{OUT+}, D_{OUT-})						
$ V_{OD} $	Differential output voltage	$R_L = 100 \Omega$, See Figure 1	250	350	450	V
$\Delta V_{OD} $	Change in magnitude of V_{OD} for complimentary output states		-35	1	35	mV
V_{OS}	Offset voltage		1.125	1.2	1.375	V
ΔV_{OS}	Change in magnitude of V_{OS} for complimentary output states		-25	1	25	mV
I_{OS}	Output short circuit current	Enabled $D_{IN} = V_{CC}$ and $D_{OUT+} = 0 \text{ V}$, or $D_{IN} = GND$ and $D_{OUT-} = 0 \text{ V}$		-4.5	-9	mA
I_{OSD}	Differential output short circuit current (2)	Enabled, $V_{OD} = 0 \text{ V}$		-3.6	-9	mA
I_{OFF}	Power-off leakage	$V_{CC} = 0 \text{ V}$ or Open; $V_O = 0$ or 3.6 V	-20	0	20	μA
I_{OZ}	Output high-impedance current	EN = 0 V and $\overline{EN} = V_{CC}$, $V_O = 0$ or V_{CC}	-10	0	10	μA
LVDS Input DC Specifications (R_{IN+}, R_{IN-})						
V_{IT+}	Differential input high threshold	$V_{CM} = 1.2 \text{ V}, 0.05 \text{ V}, 2.35 \text{ V}$			100	mV
V_{IT-}	Differential input low threshold		-100			mV
V_{CMR}	Common-mode voltage range	$V_{ID} = \pm 100 \text{ mV}$	0.05		2.35	V
I_{IN}	Input current	$V_{CC} = 3.6 \text{ V}, V_{IN} = 0 \text{ V}$ or 2.8 V	-20		20	μA
		$V_{CC} = 0 \text{ V}, V_{IN} = 0 \text{ V}, 2.8 \text{ V},$ or 3.6 V	-20		20	μA
Outputs DC Specifications (R_{OUT})						
V_{OH}	Output high voltage	$I_{OH} = -0.4 \text{ mA}, V_{ID} = 200 \text{ mV}$	2.7	3.3		V
V_{OL}	Output Low voltage	$I_{OL} = 2 \text{ mA}, V_{ID} = -200 \text{ mV}$		0.05	0.25	V
I_{OZ}	Output high-impedance current	Disabled, $V_{OUT} = 0 \text{ V}$ or V_{CC}	-10	0	10	μA
Device DC Specifications						
I_{CC}	Power supply current (LVDS loaded, enabled)	EN = 3.3 V, $D_{IN} = V_{CC}$ or Gnd, 100 $-\Omega$ differential LVDS loads		17	35	mA
I_{CCZ}	High impedance supply current (disabled)	No loads, EN = 0 V		1	25	mA

(1) All typical values are at 25°C and with a 3.3 V supply.

(2) Output short circuit current (IOS) is specified as magnitude only, the minus sign indicates direction only

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
LVDS Outputs (D_{OUT+}, D_{OUT-})					
t _{PLHD}	Differential propagation delay low to high		1.3	2.0	ns
t _{PHL}	Differential propagation delay high to low		1.4	2.0	ns
t _{sk(p)}	Differential pulse skew (t _{PHL} - t _{PLH})	0	0.15	0.4	ns
t _{sk(o)}	Differential channel-to-channel skew (2)	0	0.05	0.5	ns
t _{sk(pp)}	Differential part-to-part skew (3)	0		1	ns
t _r	Differential rise time	0.2	0.5	1	ns
t _f	Differential fall time	0.2	0.5	1	ns
t _{PHZ}	Disable time, high level to high impedance		2.7	4	ns
t _{PLZ}	Disable time, low level to high impedance		2.7	4	ns
t _{PZH}	Enable time, high impedance to high level	1	5	8	ns
t _{PZL}	Enable time, high impedance to low level	1	5	8	ns
f _{MAX}	Maximum operating frequency (4)		250		MHz
LVC MOS Outputs (R_{OUT})					
t _{PLH}	Propagation delay low to high	0.5	1.9	3.5	ns
t _{PHL}	Propagation delay high to low	0.5	1.7	3.5	ns
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})	0	0.2	0.4	ns
t _{sk(o)}	Channel-to-channel skew (5)	0	0.05	0.5	ns
t _{sk(pp)}	Part-to-part skew (6)	0		1	ns
t _r	Rise time	0.3	0.5	1.4	ns
t _f	Fall time	0.3	0.5	1.4	ns
t _{PHZ}	Disable time, high level to high impedance	3	7.2	9	ns
t _{PLZ}	Disable time, low level to high impedance	2.5	4	8	ns
t _{PZH}	Enable time, high impedance to high level	2.5	4.2	7	ns
t _{PZL}	Enable time, high impedance to low level	2	3.3	7	ns
f _{MAX}	Maximum operating frequency (7)	200	250		MHz

(1) All typical values are at 25°C and with a 3.3 V supply.

(2) t_{sk(o)} is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.

(3) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

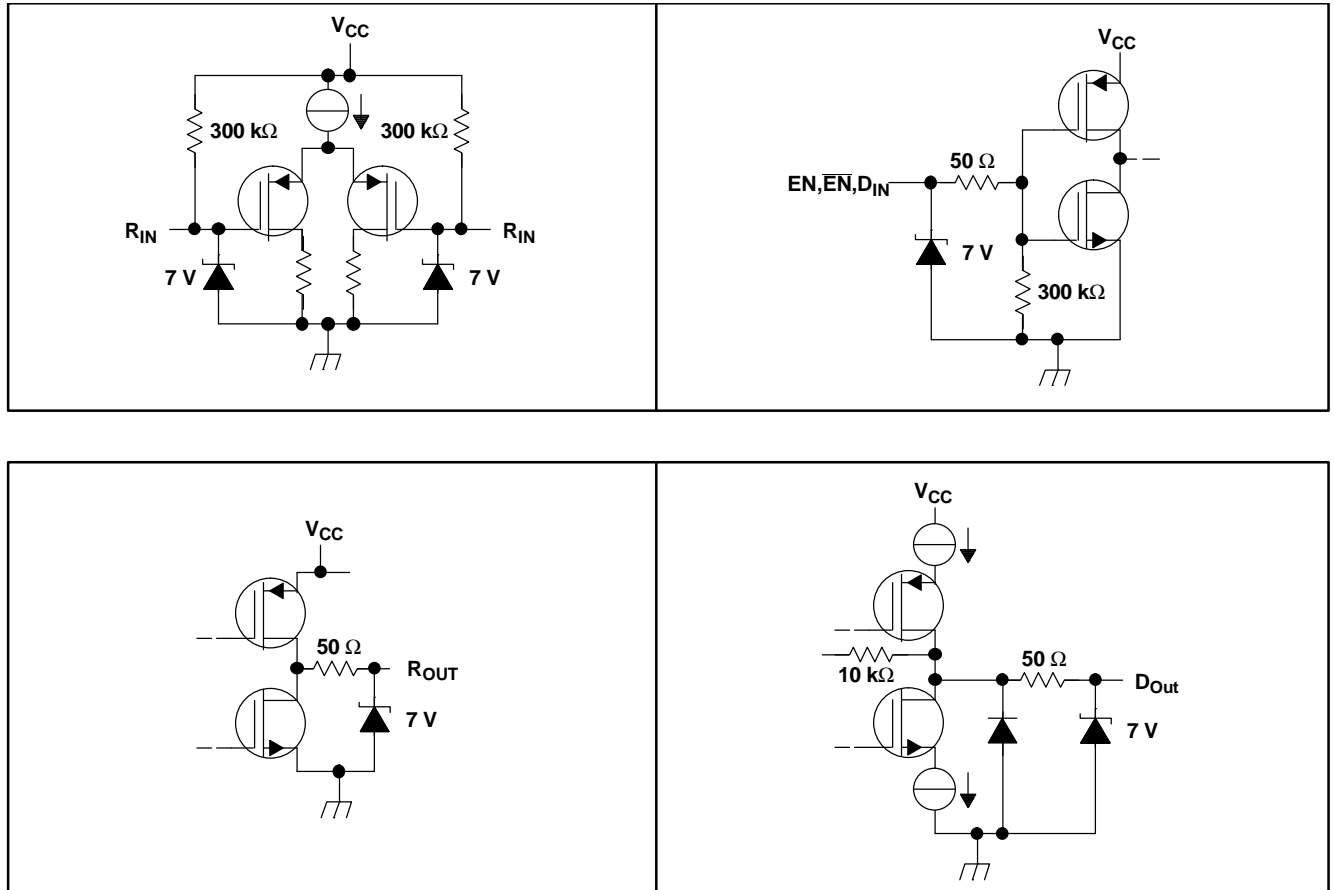
(4) f_(MAX) generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output Criteria: duty cycle = 45% to 55%, V_{OD} > 250 mV, all channels switching.

(5) t_{sk(lim)} is the maximum delay time difference between drivers over temperature, V_{CC}, and process.

(6) tsk(pp) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits

(7) f_(MAX) generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, V_{ID} = 200 mV, V_{CM} = 1.2 V. Output criteria: duty cycle = 45% to 55%, V_{OH} > 2.7 V, V_{OL} < 0.25 V, all channels switching.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



PARAMETER MEASUREMENT INFORMATION

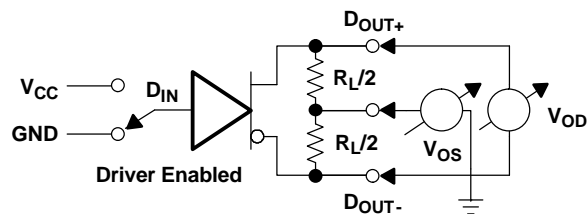


Figure 1. Driver V_{OD} and V_{OS} Test Circuit

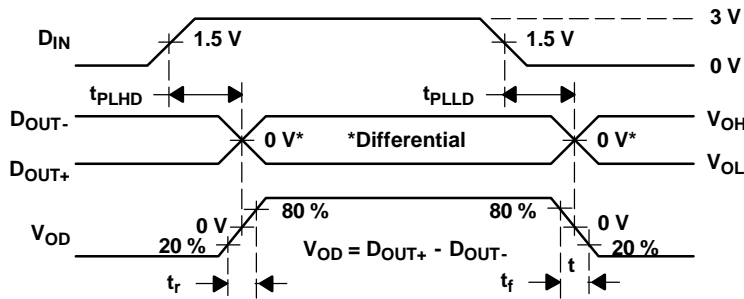
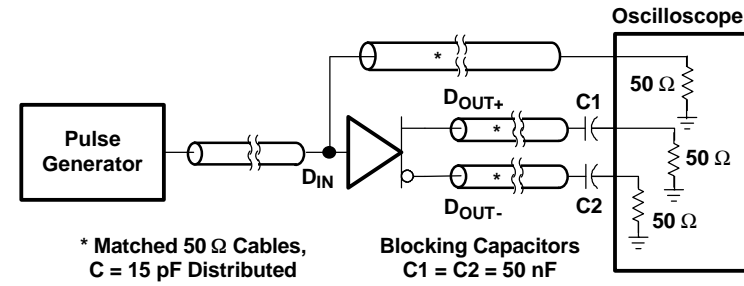


Figure 2. Driver Propagation Delay and Rise/Fall Time Test Circuit and Waveforms

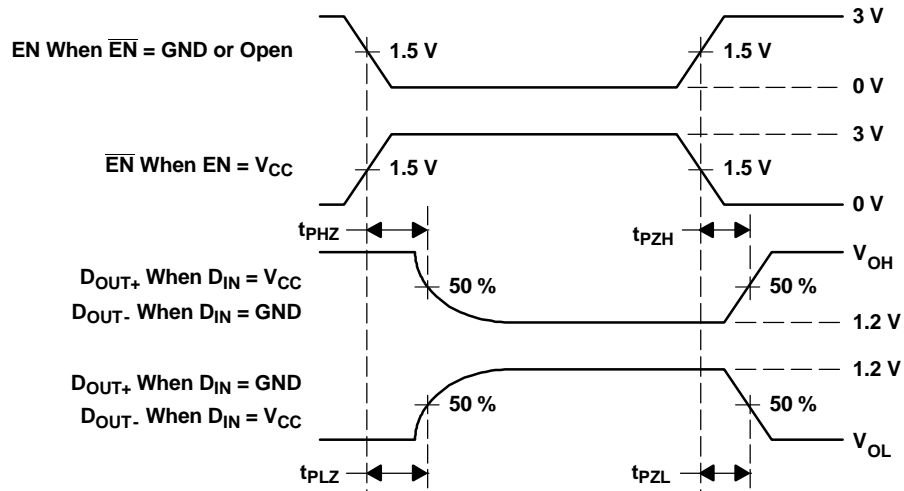
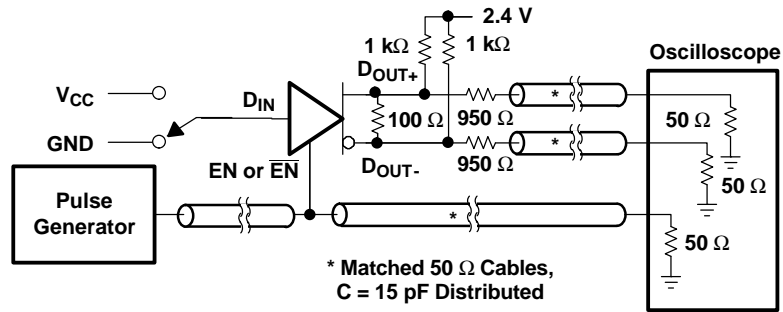


Figure 3. Driver High-Impedance State Delay Test Circuit and Waveforms

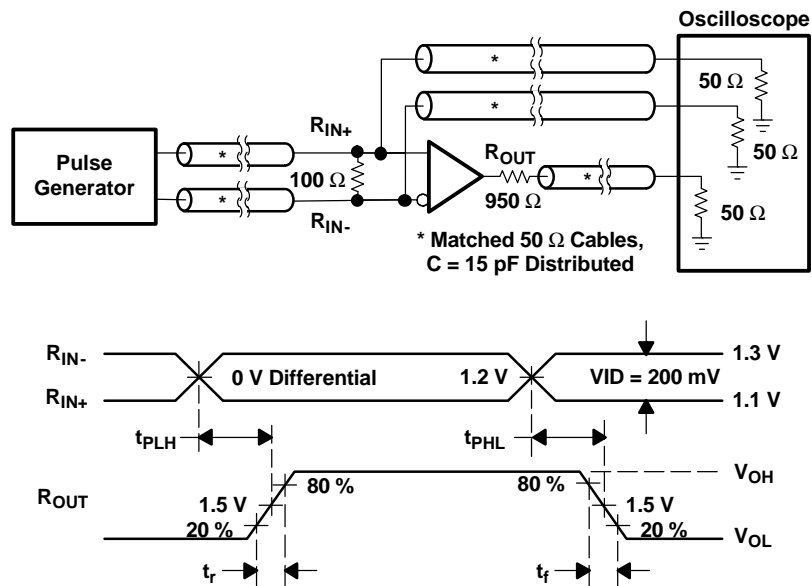


Figure 4. Receiver Propagation Delay and Rise/Fall Test Circuit and Waveforms

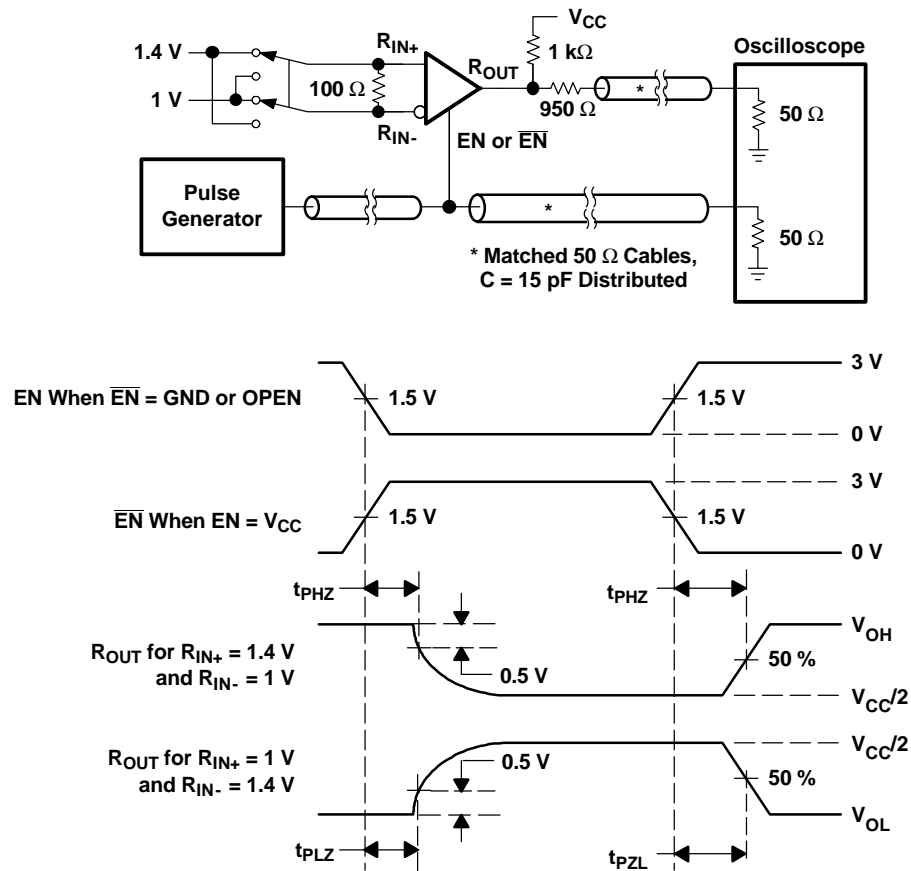


Figure 5. Receiver High-Impedance State Delay Test Circuit and Waveforms
(Note, $V_{CC} = 3.3\text{ V}$)

TYPICAL CHARACTERISTICS

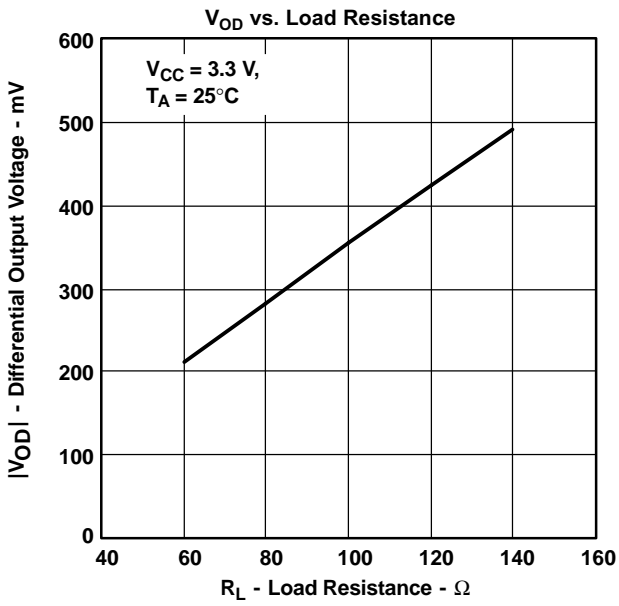


Figure 6.

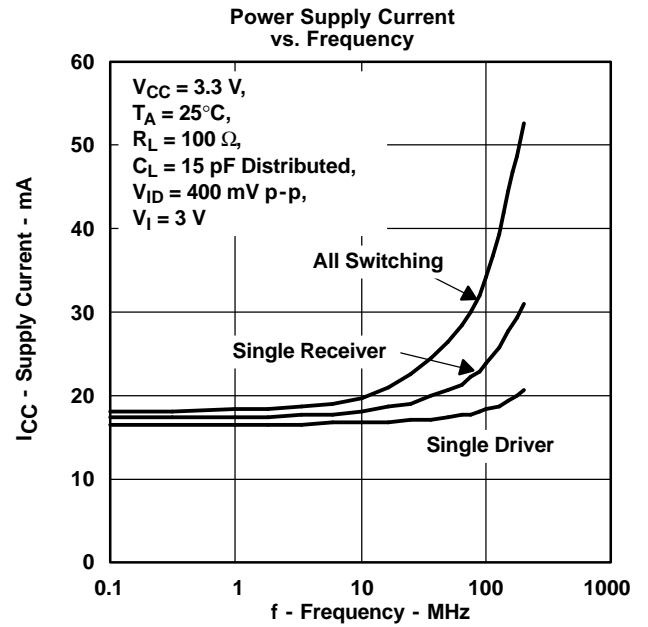


Figure 7.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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