

SN54ABT2245, SN74ABT2245 OCTAL TRANSCEIVERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

SCBS234D – SEPTEMBER 1992 – REVISED MAY 1997

- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

description

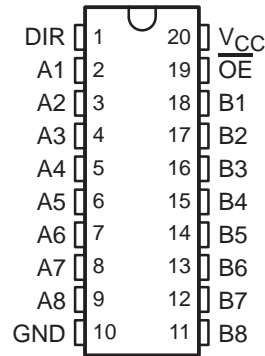
These octal transceivers and line drivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

The B-port outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

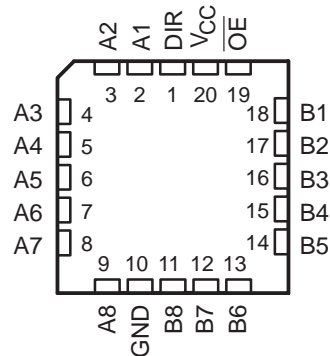
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54ABT2245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT2245 is characterized for operation from -40°C to 85°C .

SN54ABT2245 . . . J OR W PACKAGE
SN74ABT2245 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT2245 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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 **TEXAS
INSTRUMENTS**

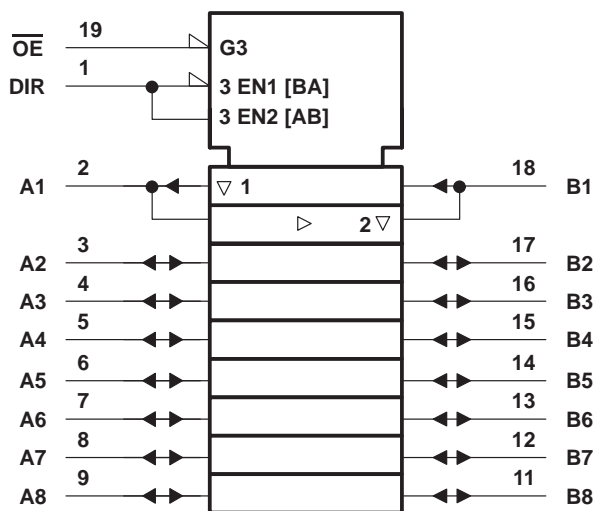
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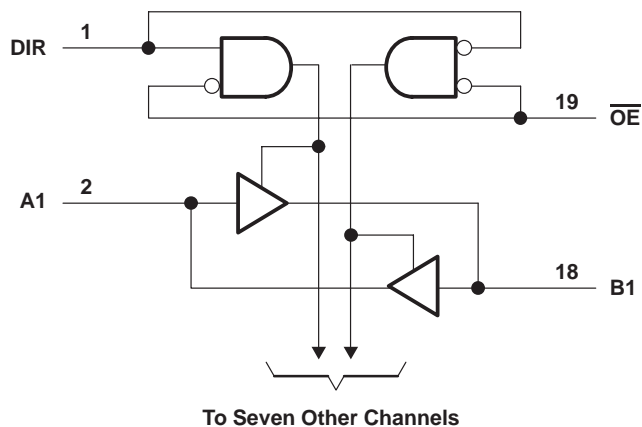
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

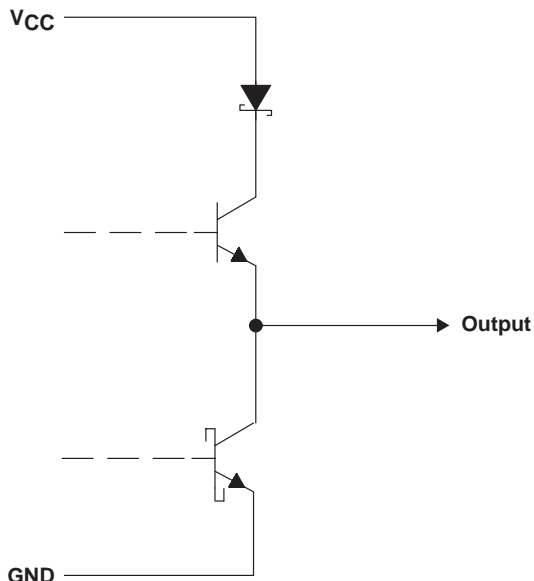
logic diagram (positive logic)



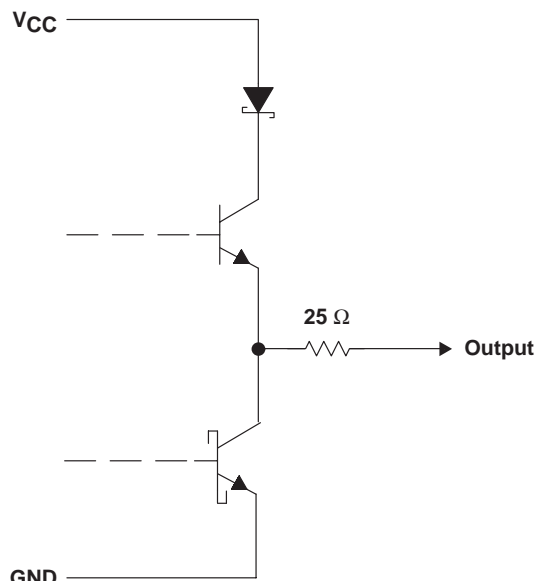
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schematic of A-port outputs



schematic of B-port outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT2245 (except B port)	96 mA
SN74ABT2245 (except B port)	128 mA
B port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

		SN54ABT2245		SN74ABT2245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	A port		-24		mA
		B port		-12		
I_{OL}	Low-level output current	A port		48		mA
		B port		12		
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		5		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABT2245		SN74ABT2245		UNIT		
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2		-1.2		V		
V _{OH}	B port	V _{CC} = 4.5 V, I _{OH} = -1 mA		3.35			3.3		3.35		V		
		V _{CC} = 5 V, I _{OH} = -1 mA		3.85			3.8		3.85				
		V _{CC} = 4.5 V		I _{OH} = -3 mA		2.6			3			3.1	
	V _{CC} = 4.5 V		I _{OH} = -12 mA		2.6			2.6		2.6			
	A port	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5			2.5	
		V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3			3	
V _{CC} = 4.5 V		I _{OH} = -24 mA		2			2		2				
V _{CC} = 4.5 V		I _{OH} = -32 mA		2*			2		2		2		
V _{OL}	B port	V _{CC} = 4.5 V		I _{OL} = 8 mA		0.65			0.8		0.65		
				I _{OL} = 12 mA		0.8			0.8		0.8		
	A port			I _{OL} = 48 mA		0.55			0.55		0.55		
				I _{OL} = 64 mA		0.55*			0.55		0.55		
V _{hys}				100							mV		
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA		
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND		±20			±20		±20				
I _{OZH} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V		10			10		10		μA		
I _{OZL} ‡		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V		-10			-10		-10		μA		
I _{OZPU} §		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$		±50			±50		±50		μA		
I _{OZPD} §		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$		±50			±50		±50		μA		
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100			±100		±100		μA		
I _{CEX}	Outputs high	V _{CC} = 5.5 V, V _O = 5.5 V		50			50		50		μA		
I _O ¶	B port	V _{CC} = 5.5 V, V _O = 2.5 V		-25		-100		-25		-100		mA	
	A port			-50		-100		-180		-50			-180
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		1 250		250		250		μA	
				Outputs low		24 32		32		32		mA	
				Outputs disabled		0.5 250		250		250		μA	
ΔI _{CC} #	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		Outputs enabled		1.5		1.5		1.5		mA	
				Outputs disabled		0.05		0.05		0.05			
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5		1.5		1.5					
C _i	V _I = 2.5 V or 0.5 V		3							pF			
C _{io}	V _O = 2.5 V or 0.5 V		6							pF			

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ This parameter is characterized but not production tested.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

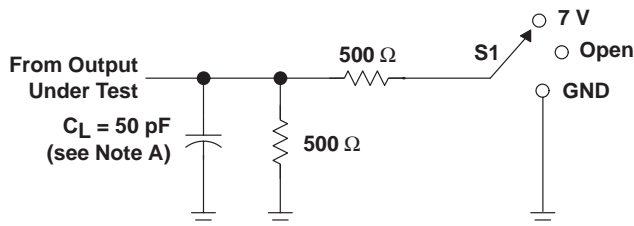
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT2245		SN74ABT2245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	2.5	3.4	1	4	1	3.8	ns
t_{PHL}			1	3.2	4.2	1	4.6	1	4.5	
t_{PLH}	B	A	1	2.2	3.2	1	3.8	1	3.6	ns
t_{PHL}			1	2.7	3.6	1	4.2	1	4	
t_{PZH}	\overline{OE}	A	1	3.3	4.6	1	5.6	1	5.5	ns
t_{PZL}			1	3.2	4.7	1	6	1	5.7	
t_{PHZ}	\overline{OE}	A	2	4	5.1	2	5.7	2	5.6	ns
t_{PLZ}			1	2.9	4	1	4.6	1	4.5	
t_{PZH}	\overline{OE}	B	1.5	3.6	4.9	1.5	6.3	1.5	6.1	ns
t_{PZL}			1.5	3.9	5.3	1.5	6.6	1.5	6.3	
t_{PHZ}	\overline{OE}	B	1.5	3.6	4.7	1.5	5.5	1.5	5.3	ns
t_{PLZ}			1.5	3.3	4.4	1.5	4.9	1.5	4.8	



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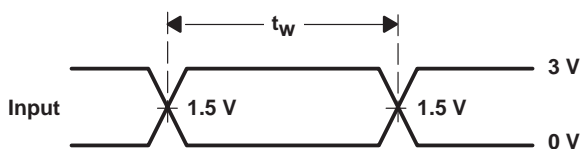
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PARAMETER MEASUREMENT INFORMATION

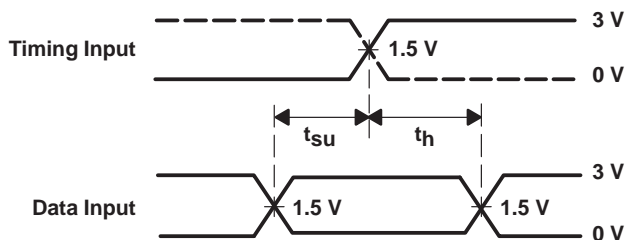


LOAD CIRCUIT

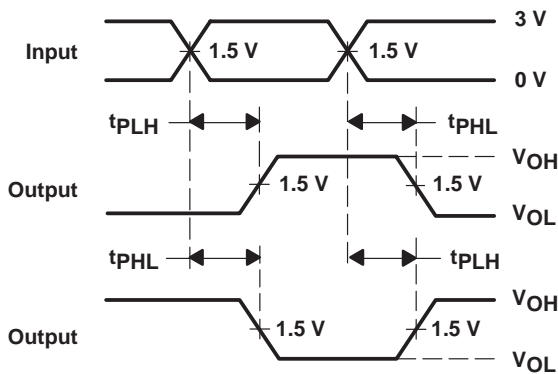
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



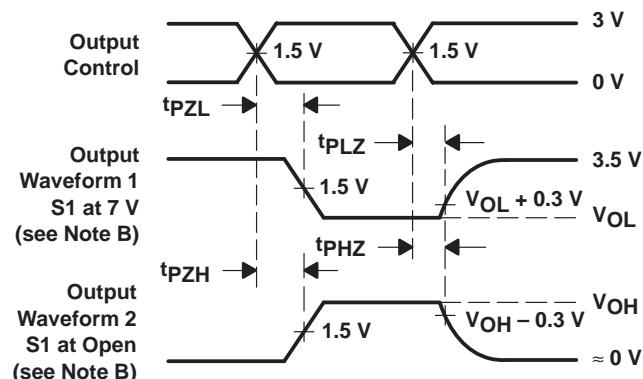
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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