- **3.3-V Core Logic With Universal PCI Interface Compatible With 3.3-V or 5-V PCI Signaling Environments**
- **Supports PCI Local Bus Specification 2.1**
- **Mix-and-Match 3.3-V/5-V PC Card16 Cards and 3.3-V CardBus Cards**
- **Supports Two PC Card™ or CardBus Slots With Hot Insertion and Removal**
- **1995 PC Card-Standard Compliant**
- **Low-Power Advanced Submicron CMOS Technology**
- **Uses Serial Interface to Texas Instruments (TI™) TPS2206 Dual Power Switch**
- **System Interrupts Can Be Programmed as PCI-Style or ISA IRQ-Style Interrupts**
- **ISA IRQ Interrupts Can Be Serialized Onto a Single IRQSER Pin**
- **Programmable Output Select for $\overline{\text{CLKRUN}}$**
- **Supports Burst Transfers to Maximize Data Throughput on the PCI and CardBus Bus**
- **Multifunction PCI Device With Separate Configuration Spaces for Each Socket**
- **Five PCI Memory Windows and Two I/O Windows Available to Each PC Card16 Socket**
- **Two I/O Windows and Two Memory Windows Available to Each CardBus Socket**
- **CardBus Memory Windows Can Be Individually Selected Prefetchable or Nonprefetchable**
- **Exchangeable Card Architecture (ExCA)-Compatible Registers Mapped in Memory or I/O Space**
- **TI Extension Registers Mapped in the PCI Configuration Space**
- **Intel™ 82365SL-DF Register Compatible**
- **Supports 16-Bit Distributed Direct Memory Access (DMA) on Both PC Card Sockets**
- **Supports PC/PCI DMA on Both PC Card Sockets**
- **Supports Zoom Video Mode**
- **Supports Ring Indicate**
- **Packaged in 208-Pin Thin Plastic Quad Flatpack**

Table of Contents

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description

The TI PCI1131 is a high-performance PCI-to-PC Card controller that supports two independent PC Card sockets compliant with the 1995 PC Card standard. The PCI1131 provides a set of features that makes it ideal for bridging between PCI and PC Cards in both notebook and desktop computers. The 1995 PC Card standard retains the 16-bit PC Card specification defined in PCMCIA release 2.1 and defines the new 32-bit PC Card, called CardBus, capable of full 32-bit data transfers at 33 MHz. The PCI1131 supports any combination of 16-bit and CardBus PC Cards in its two sockets, powered at 3.3 V or 5 V, as required.

The PCI1131 is compliant with the PCI local bus specification revision 2.1, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers or CardBus PC Card bus-mastering cycles.

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI1131 is register compatible with the Intel 82365SL-DF ExCA controller. The PCI1131 internal datapath logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent 32-bit write buffers allow fast-posted writes to improve system-bus utilization.

An advanced CMOS process is used to achieve low system-power consumption while operating at PCI clock rates up to 33 MHz. Several low-power modes allow the host power-management system to further reduce power consumption.

All unused PCI1131 inputs should be pulled high through a 43-kΩ resistor.

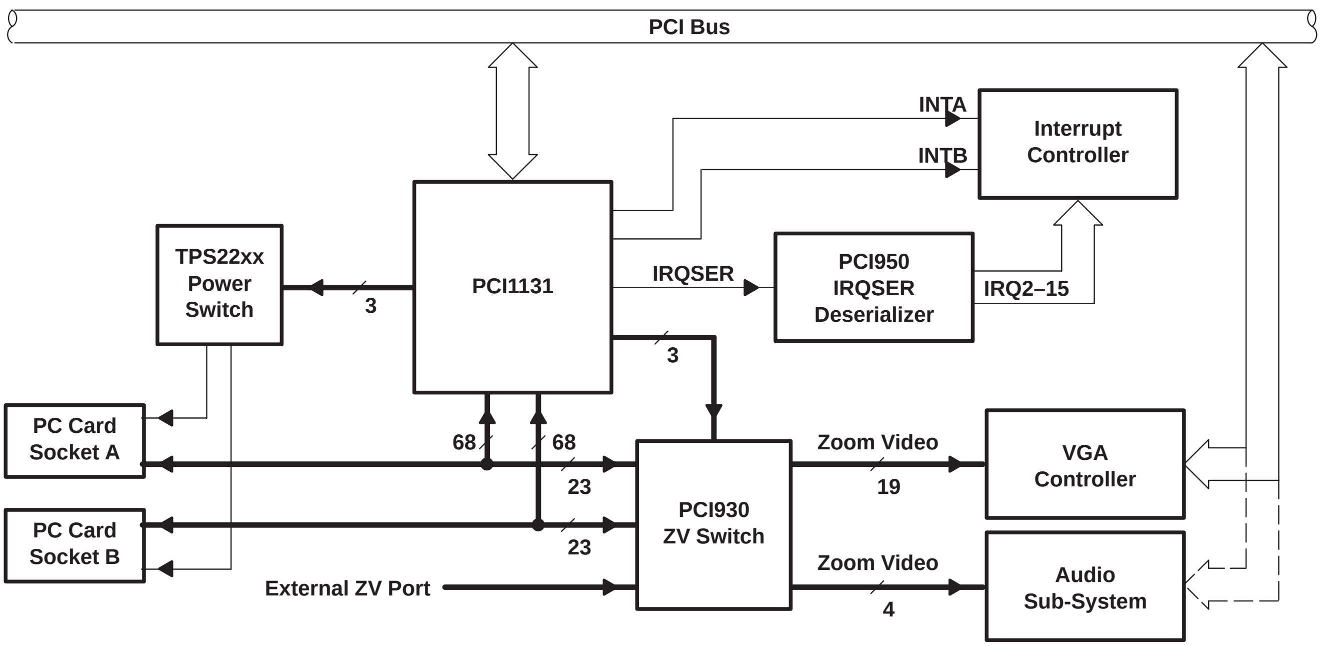
system block diagram

A simplified system block diagram using the PCI1131 is provided below. The PCI950 IRQ deseralizer and the PCI930 zoomed video (ZV) switch are optional functions that can be used when the system requires that capability.

The PCI interface includes all address/data and control signals for PCI protocol. The 68-pin PC Card interface includes all address/data and control signals for CardBus and 16-bit (R2) protocols. When zoomed video (ZV) is enabled (in 16-bit PC Card mode) 23 of the 68 signals are redefined to support the ZV protocol.

The interrupt interface includes terminals for parallel PCI, parallel ISA, and serialized PCI and ISA signaling. Other miscellaneous system interface terminals are available on the PCI1131 that include:

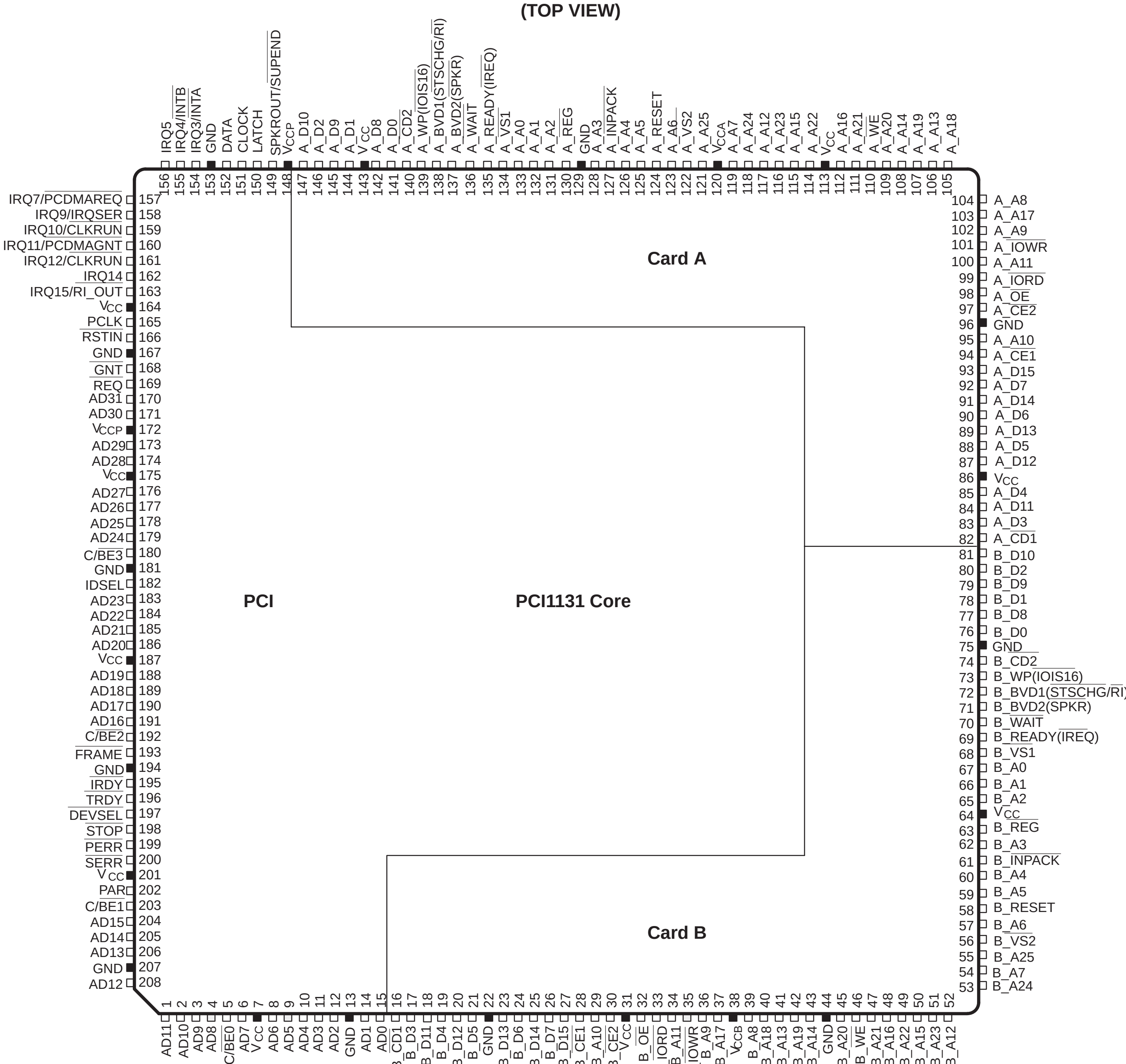
- Multifunction IRQ terminals
- SUSPEND, RI_OUT (power management control signals)
- SPKROUT.



NOTE: The PC Card interface is 68 pins for CardBus and 16-bit PC Cards. In zoomed-video mode 23 pins are used for routing the zoomed video signals too the VGA controller.

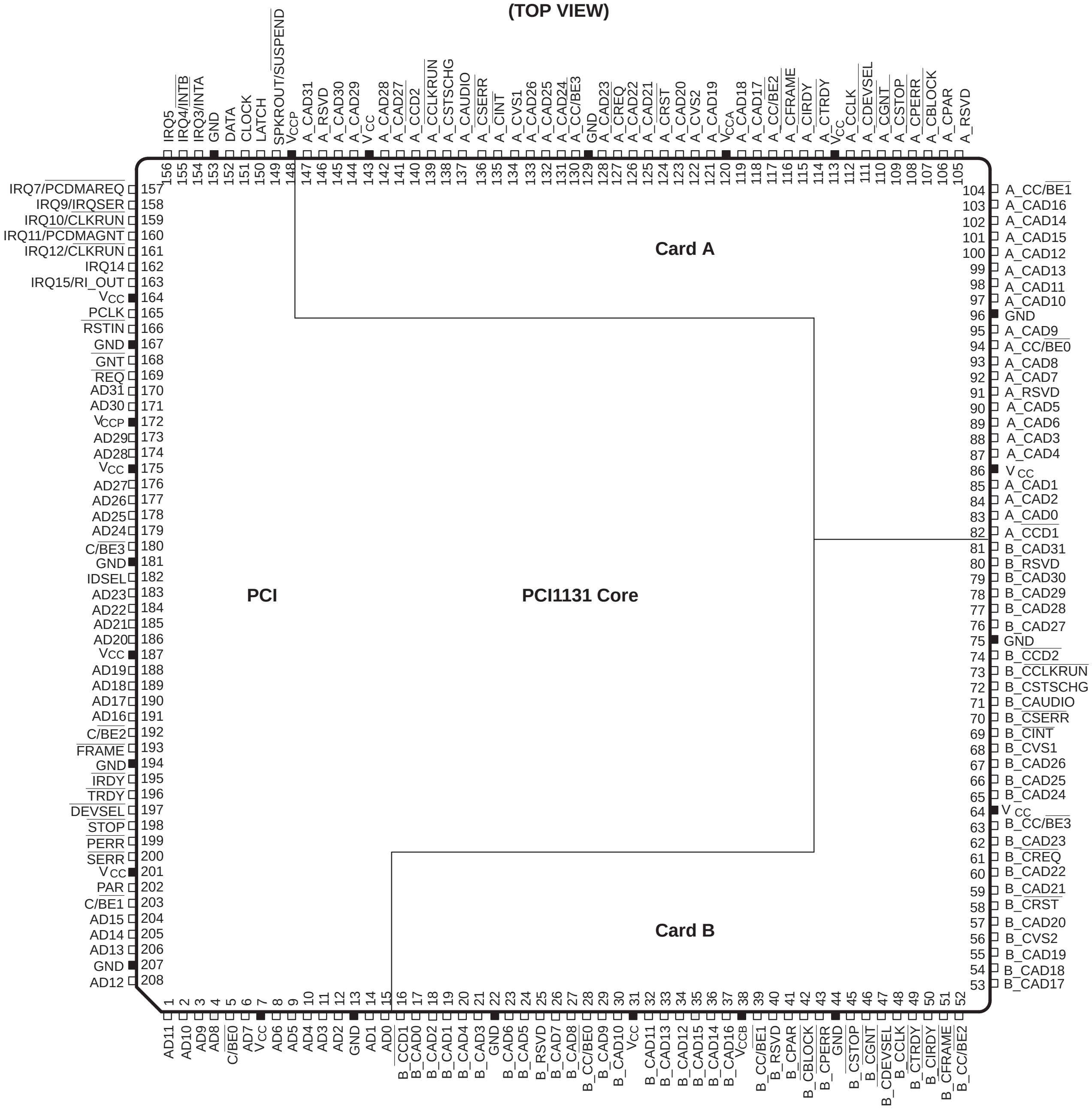
terminal assignments – PCI-to-PC Card (16 bit)

PDV PACKAGE
(TOP VIEW)



terminal assignments – PCI-to-CardBus Card

PDV PACKAGE
(TOP VIEW)



Terminal Functions

PCI system

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
PCLK	165	I	PCI bus clock. PCLK provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCLK.
RSTIN	166	I	PCI reset. When the RSTIN signal is asserted low, the PCI1131 forces all output buffers to the high-impedance state and resets all internal registers. When asserted, the PCI1131 is nonfunctional. After RSTIN is deasserted, the PCI1131 returns to the default state. When the PCI1131 SUSPEND mode is enabled, the device is protected from any RSTIN reset (i.e., the PCI1131 internal register contents are preserved).

PCI address and data

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	170 171 173 174 176 177 178 179 183 184 185 186 188 189 190 191 204 205 206 208 1 2 3 4 6 8 9 10 11 12 14 15	I/O	Address/data bus. AD31–AD0 are the multiplexed PCI address and data bus. During the address phase of a PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
C/BE3 C/BE2 C/BE1 C/BE0	180 192 203 5	I/O	Bus commands and byte enables. C/BE3–C/BE0 are multiplexed on the same PCI terminals. During the address phase, C/BE3–C/BE0 define the bus command. During the data phase, C/BE3–C/BE0 are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C/BE0 applies to byte 0 (AD7–AD0), C/BE1 applies to byte 1 (AD15–AD8), C/BE2 applies to byte 2 (AD23–AD16), and C/BE3 applies to byte 3 (AD31–AD24).
PAR	202	I/O	Parity. As a PCI target during PCI read cycles, or as PCI bus master during PCI write cycles, the PCI1131 calculates even parity across the AD and C/BE buses and outputs the results on PAR, delayed by one clock.

Terminal Functions (Continued)

PCI interface control

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
DEVSEL	197	I/O	Device select. As a PCI target, the PCI1131 asserts DEVSEL to claim the current cycle. As a PCI master, the PCI1131 monitors DEVSEL until a target responds or a time-out occurs.
FRAME	193	I/O	Cycle frame. FRAME is driven by the current master to indicate the beginning and duration of an access, FRAME is low (asserted) to indicate that a bus transaction is beginning. While FRAME is asserted, data transfers continue. When FRAME is sampled high (deasserted), the transaction is in the final data phase.
GNT	168	I	Grant. GNT is driven by the PCI arbiter to grant the PCI1131 access to the PCI bus after the current data transaction is complete.
IDSEL	182	I	Initialization device select. IDSEL selects the PCI1131 during configuration accesses. IDSEL can be connected to one of the upper 24 PCI address lines.
IRDY	195	I/O	Initiator ready. IRDY indicates the bus master's ability to complete the current data phase of the transaction. IRDY is used with TRDY. A data phase is completed on any clock where both IRDY and TRDY are sampled low (asserted). During a write, IRDY indicates that valid data is present on AD31–AD0. During a read, IRDY indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are low (asserted) at the same time. This signal is an output when the PCI1131 is the PCI bus master and an input when the PCI bus is the target.
IRQ10/CLKRUN IRQ12/CLKRUN	159 161	I/O	Interrupt request 10 and 12. IRQ10/CLKRUN and IRQ12/CLKRUN are software configurable and used by the PCI1131 to support the PCI clock run protocol. When configured as CLKRUN by setting bit 0 in the system control register offset 80h, this terminal is an open-drain output. To select between IRQ10 and IRQ12 as the output, use bit 7 of register 80h.
PERR	199	I/O	Parity error. PERR is driven by the PCI target during a write to indicate that a data parity error has been detected.
REQ	169	O	Request. REQ is asserted by the PCI1131 to request access to the PCI bus as a master.
SERR	200	O	System error. SERR pulsed from the PCI1131 indicates an address parity error has occurred.
STOP	198	I/O	Stop. STOP is driven by the current PCI target to request the master to stop the current transaction.
TRDY	196	I/O	Target ready. TRDY indicates the ability of the PCI1131 to complete the current data phase of the transaction. TRDY is used with IRDY. A data phase is completed on any clock where both TRDY and IRDY are sampled asserted. During a read, TRDY indicates that valid data is present on AD31–AD0. During a write, TRDY indicates that the PCI1131 is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together. This signal is an output when the PCI1131 is the PCI target and an input when the PCI1131 is the PCI bus master.

power supply

TERMINAL NAME	TERMINAL NO.	FUNCTION
GND	13, 22, 44, 75, 96, 129, 153, 167, 181, 194, 207	Device ground terminals
V_{CC}	7, 31, 64, 86, 113, 143, 164, 175, 187, 201	Power supply terminal for core logic (3.3 V)
V_{CCA}	120	Power supply terminal for PC Card A (5 V or 3.3 V)
V_{CCB}	38	Power supply terminal for PC Card B (5 V or 3.3 V)
V_{CCP}	148, 172	Power supply terminal for PCI interface (5 V or 3.3 V)

Terminal Functions (Continued)

PC Card power switch

TERMINAL NAME	NO.	I/O TYPE	FUNCTION
CLOCK	151	O	Power switch clock. Information on the DATA line is sampled at the rising edge of CLOCK. The frequency of the clock is derived from dividing PCICLK by 36. The maximum frequency of CLOCK is 2 MHz.
DATA	152	O	Power switch data. DATA is used by the PCI1131 to serially communicate socket power control information.
LATCH	150	O	Power switch latch. LATCH is asserted by the PCI1131 to indicate to the PC Card power switch that the data on the DATA line is valid.

interrupt

TERMINAL NAME	NO.	I/O TYPE	FUNCTION
IRQ3/INTA IRQ4/INTB	154 155	O	Interrupt request 3 and interrupt request 4. IRQ3/INTA–IRQ4/INTB can be connected to either PCI or ISA interrupts. IRQ3/INTA–IRQ4/INTB are software configurable as IRQ3 or INTA and as IRQ4 or INTB. When configured for IRQ3 and IRQ4, IRQ3/INTA–IRQ4/INTB must be connected to the ISA IRQ programmable interrupt controller. When IRQ3/INTA–IRQ4/INTB are configured for INTA and INTB, IRQ3/INTA–IRQ4/INTB must be connected to interrupts on the PCI bus.
IRQ7/PCDMAREQ	157	O	Interrupt request 7. IRQ7/PCDMAREQ is software configurable and is used by the PCI1131 to request PC/PCI DMA transfers from chipsets that support the PC/PCI DMA scheme. When IRQ7/PCDMAREQ is configured for PC/PCI DMA request (IRQ7), it must be connected to the appropriate request (REQ) pin on the Intel Mobile Triton PCI I/O accelerator (MPIIX™).
IRQ9/IRQSER	158	O I/O	Interrupt request 9/serial IRQ. IRQ9/IRQSER is software configurable and indicates an interrupt request from a PC Card to the PCI1131. When IRQ9/IRQSER is configured for IRQ9, it must be connected to the system programmable interrupt controller. IRQSER allows all IRQ signals to be serialized onto one pin. IRQ9/IRQSER is configured via bits 2–1 in the device control register of the TI extension registers.
IRQ10/CLKRUN IRQ12/CLKRUN	159 161	I/O	Interrupt request 10 and 12. IRQ10/CLKRUN and IRQ12/CLKRUN are software configurable and used by the PCI1131 to support the PCI clock run protocol. When configured as CLKRUN by setting bit 0 in the system control register offset 80h, this terminal is an open-drain output. To select between IRQ10 and IRQ12 as the output, use bit 7 of register 80h.
IRQ11/PCDMAGNT	160	I/O	Interrupt request 11. IRQ11/PCDMAGNT is software configurable and is used by the PCI1131 to accept a grant for PC/PCI DMA transfers from chipsets that support the PC/PCI DMA scheme. When IRQ11/PCDMAGNT is configured for PC/PCI DMA grant (IRQ11), it must be connected to the appropriate grant (GNT) pin on the Intel MPIIX controller.
IRQ5 IRQ14	156 162	O	Interrupt request 5 and 14. These signals are ISA interrupts. These terminals indicate an interrupt request from one of the PC Cards. The interrupt mode is selected in the device control register of the TI extension registers.
IRQ15/RI_OUT	163	I/O	Interrupt request 15. IRQ15/RI_OUT indicates an interrupt request from one of the PC Cards. RI_OUT allows the RI input from the 16-bit PC Card to be output to the system. IRQ15/RI_OUT is configured in the card control register of the TI extension registers.

speaker control

TERMINAL NAME	NO.	I/O TYPE	FUNCTION
SPKROUT/ SUSPEND	149	O	Speaker. SPKROUT carries the digital audio signal from the PC Card. SUSPEND places the PCI1131 in suspend mode. SPKROUT/SUSPEND is configured in the card control register of the TI extension registers.

Terminal Functions (Continued)

16-bit PC Card address and data (slots A and B)

TERMINAL NAME	NUMBER SLOT A†	NUMBER SLOT B‡	I/O TYPE	FUNCTION
A25	121	55	O	PC Card address. 16-bit PC Card address lines. A25 is the most-significant bit.
A24	118	53		
A23	116	51		
A22	114	49		
A21	111	47		
A20	109	45		
A19	107	42		
A18	105	40		
A17	103	37		
A16	112	48		
A15	115	50		
A14	108	43		
A13	106	41		
A12	117	52		
A11	100	34		
A10	95	29		
A9	102	36		
A8	104	39		
A7	119	54		
A6	123	57		
A5	125	59		
A4	126	60		
A3	128	62		
A2	131	65		
A1	132	66		
A0	133	67		
D15	93	27	I/O	PC Card data. 16-bit PC Card data lines. D15 is the most-significant bit.
D14	91	25		
D13	89	23		
D12	87	20		
D11	84	18		
D10	147	81		
D9	145	79		
D8	142	77		
D7	92	26		
D6	90	24		
D5	88	21		
D4	85	19		
D3	83	17		
D2	146	80		
D1	144	78		
D0	141	76		

† Terminal name is preceded with A_. For example, the full name for terminal 121 is A_A25.
‡ Terminal name is preceded with B_. For example, the full name for terminal 55 is B_A25.

Terminal Functions (Continued)

16-bit PC Card interface control signals (slots A and B)

TERMINAL NAME	NUMBER SLOT A†	NUMBER SLOT B‡	I/O TYPE	FUNCTION
BVD1 (STSCHG/RI)	138	72	I	Battery voltage detect 1. Generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are kept high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and needs to be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. Status change. STSCHG is used to alert the system to a change in the READY, write protect, or battery voltage dead condition of a 16-bit I/O PC Card. Ring indicate. RI is used by 16-bit modem cards to indicate ring detection.
BVD2(SPKR)	137	71	I	Battery voltage detect 2. Generated by 16-bit memory PC Cards that include batteries. BVD2 is used with BVD1 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and needs to be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. Speaker. SPKR is an optional binary audio signal available only when the card and socket have been configured for the 16-bit I/O interface. The audio signals from cards A and B can be combined by the PCI1131 and output on SPKROUT. DMA request. BVD2 can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, the PC Card asserts BVD2 to request a DMA operation.
CD1 CD2	82 140	16 74	I	PC Card detect 1 and PC Card detect 2. CD1 and CD2 are internally connected to ground on the PC Card. When a PC Card is inserted into a socket, CD1 and CD2 are pulled low.
CE1 CE2	94 97	28 30	O	Card enable 1 and card enable 2. CE1 and CE2 enable even- and odd-numbered address bytes. CE1 enables even-numbered address bytes, and CE2 enables odd-numbered address bytes.
INPACK	127	61	I	Input acknowledge. INPACK is asserted by the PC Card when it can respond to an I/O read cycle at the current address. DMA request. INPACK can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, the PC Card asserts INPACK to indicate a request for a DMA operation.
IORD	99	33	O	I/O read. IORD is asserted by the PCI1131 to enable 16-bit I/O PC Card data output during host I/O read cycles. DMA write. IORD is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1131 asserts IORD during DMA transfers from the PC Card to host memory.
IOWR	101	35	O	I/O write. IOWR is driven low by the PCI1131 to strobe write data into 16-bit I/O PC Cards during host I/O write cycles. DMA read. IOWR is used as the DMA read strobe during DMA operations to a 16-bit PC Card that supports DMA. The PCI1131 asserts IOWR during DMA transfers from host memory to the PC Card.
OE	98	32	O	Output enable. OE is driven low by the PCI1131 to enable 16-bit memory PC Card data output during host memory read cycles. DMA terminal count. OE is used as terminal count (TC) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1131 asserts OE to indicate TC for a DMA write operation.

† Terminal name is preceded with A_. For example, the full name for terminal 138 is A_BVD1.
‡ Terminal name is preceded with B_. For example, the full name for terminal 72 is B_BVD1.

Terminal Functions (Continued)

16-bit PC Card interface control signals (slots A and B) (continued)

TERMINAL			I/O TYPE	FUNCTION
NAME	NUMBER			
	SLOT A†	SLOT B‡		
READY(IREQ)	135	69	I	Ready. The ready function is provided by READY when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit memory PC Card is ready to accept a new data transfer command. Interrupt request. IREQ is asserted by a 16-bit I/O PC Card to indicate to the host that a device on the 16-bit I/O PC Card requires service by the host software. IREQ is high (deasserted) when no interrupt is requested.
REG	130	63	O	Attribute memory select. REG remains high for all common memory accesses. When REG is asserted, access is limited to attribute memory (OE or WE active) and to the I/O space (IORD or IOWR active). Attribute memory is a separately accessed section of card memory and is generally used to record card capacity and other configuration and attribute information. DMA acknowledge. REG is used as a DMA acknowledge (DACK) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1131 asserts REG to indicate a DMA operation. REG is used with the DMA read (IOWR) or DMA write (IORD) strobes to transfer data.
RESET	124	58	O	PC Card reset. RESET forces a hard reset to a 16-bit PC Card.
WAIT	136	70	I	Bus cycle wait. WAIT is driven by a 16-bit PC Card to delay the completion of (i.e., extend) the memory or I/O cycle in progress.
WE	110	46	O	Write enable. WE is used to strobe memory write data into 16-bit memory PC Cards. WE also is used for memory PC Cards that employ programmable memory technologies. DMA terminal count. WE is used as TC during DMA operations to a 16-bit PC Card that supports DMA. The PCI1131 asserts WE to indicate TC for a DMA read operation.
WP(IOIS16)	139	73	I	Write protect. This signal applies to 16-bit memory PC Cards. WP reflects the status of the write-protect switch on 16-bit memory PC Cards. For 16-bit I/O cards, WP is used for the 16-bit port (IOIS16) function. The status of WP can be read from the ExCA interface status register. I/O is 16 bits. WP applies to 16-bit I/O PC Cards. IOIS16 is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds, and the I/O port that is addressed is capable of 16-bit accesses. DMA request. WP can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, the PC Card asserts WP to request a DMA operation.
VS1 VS2	134 122	68 56	I/O	Voltage sense 1 and voltage sense 2. VS1 and VS2, when used together, determine the operating voltage of the 16-bit PC Card.

† Terminal name is preceded with A_. For example, the full name for terminal 98 is A_OE.
‡ Terminal name is preceded with B_. For example, the full name for terminal 32 is B_OE.

Terminal Functions (Continued)

CardBus PC Card address and data signals (slots A and B)

TERMINAL			I/O TYPE	FUNCTION
NAME	NUMBER SLOT A†	NUMBER SLOT B‡		
CAD31	147	81	I/O	CardBus PC Card address and data. CAD31–CAD0 are multiplexed address and data signals. A bus transaction consists of an address phase followed by one or more data phases. The PCI1131 supports both read and write bursts. The address phase is the clock cycle in which CFRAME is asserted. During the address phase, CAD31-CAD0 contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases, CAD7–CAD0 contain the least-significant byte and CAD31–CAD24 contain the most-significant byte. Write data is stable and valid when CIRDY is asserted. Read data is stable and valid when CTRDY is asserted. Data is transferred during those clocks when CIRDY and CTRDY are asserted.
CAD30	145	79		
CAD29	144	78		
CAD28	142	77		
CAD27	141	76		
CAD26	133	67		
CAD25	132	66		
CAD24	131	65		
CAD23	128	62		
CAD22	126	60		
CAD21	125	59		
CAD20	123	57		
CAD19	121	55		
CAD18	119	54		
CAD17	118	53		
CAD16	103	37		
CAD15	101	35		
CAD14	102	36		
CAD13	99	33		
CAD12	100	34		
CAD11	98	32		
CAD10	97	30		
CAD9	95	29		
CAD8	93	27		
CAD7	92	26		
CAD6	89	23		
CAD5	90	24		
CAD4	87	20		
CAD3	88	21		
CAD2	84	18		
CAD1	85	19		
CAD0	83	17		
CC/BE0	94	28	I/O	CardBus PC Card command and byte enables. CC/BE0–CC/BE3 are multiplexed on the same pin. During the address phase of the transaction, CC/BE3–CC/BE0 define the bus command. During the data phase transaction, CC/BE3–CC/BE0 are used as byte enables. Byte enables are valid during the entire data phase and determine the byte lanes that carry the data. CC/BE0 applies to byte 0, CC/BE1 applies to byte 1, CC/BE2 applies to byte 2, and CC/BE3 applies to byte 3.
CC/BE1	104	39		
CC/BE2	117	52		
CC/BE3	130	63		
CPAR	106	41	I/O	CardBus PC Card parity. Even parity across CAD31–CAD0 and CC/BE3–CC/BE0 is calculated and driven by this signal. CPAR is stable and valid for one clock after the address phase. For data phases, CPAR is stable and valid one clock after either CIRDY is asserted on a write transaction or CTRDY is asserted on a read transaction. Once CPAR is valid, it remains valid for one clock after the completion of the current data phase. NOTE: CPAR has the same timing as CAD31–CAD0 but delays by one clock. When the PCI1131 is acting as an initiator, it drives CPAR for address and write data phases; and when acting as a target, the PCI1131 drives CPAR for read data phases.

† Terminal name is preceded with A_. For example, the full name for terminal 147 is A_CAD31.
‡ Terminal name is preceded with B_. For example, the full name for terminal 81 is B_CAD31.

Terminal Functions (Continued)

CardBus PC Card interface system signals (slots A and B)

TERMINAL			I/O TYPE	FUNCTION
NAME	NUMBER SLOT A†	NUMBER SLOT B‡		
CCLK	112	48	O	CardBus PC Card clock. CCLK provides synchronous timing for all transactions on the CardBus PC Card interface. All signals except CRST (upon assertion) CCLKRUN, CINT, CSTSCHG, CAUDIO, CCD2–CCD1, and CVS2–CVS1 are sampled on the rising edge of the clock, and all timing parameters are defined with the rising edge of CCLK. The CardBus clock operates at 33 MHz but can be stopped in the low state.
CCLKRUN	139	73	I/O	CardBus PC Card clock run. CCLKRUN is used by a CardBus PC Card to request an increase in the CCLK frequency. It is used by the PCI1131 to indicate that the CCLK frequency is decreased.
CRST	124	58	O	CardBus PC Card reset. CRST is used to bring CardBus PC Card specific registers, sequencers, and signals to a consistent state. When CRST is asserted, all CardBus PC Card signals must be driven to the high-impedance state. Assertion can be asynchronous to CCLK, but deassertion must be synchronous to CCLK.

CardBus PC Card interface control signals (slots A and B)

TERMINAL			I/O TYPE	FUNCTION
NAME	NUMBER SLOT A†	NUMBER SLOT B‡		
CAUDIO	137	71	I	CardBus audio. CAUDIO is an optional digital output signal from a PC Card to the system speaker. CardBus cards support two types of audio: single amplitude, binary waveform and/or pulsewidth modulation (PWM) encoded signal. The PCI1131 supports the binary audio mode and can output a binary audio signal from the PC Card to SPKROUT.
CBLOCK	107	42	I/O	CardBus lock. CBLOCK is an optional signal used to lock a particular address, ensuring a bus initiator exclusive access. This signal is not supported on the PCI1131.
CCD1 CCD2	82 140	16 74	I	CardBus detect 1 and CardBus detect 2. CCD1 and CCD2 are used with CVS1 and CVS2 to determine the type and voltage of the CardBus PC Card.
CDEVSEL	111	47	I/O	CardBus device select. When actively driven, CDEVSEL indicates that the PCI1131 has decoded its address as the target of the current access. As an input, CDEVSEL indicates whether any device on the bus has been selected.
CFRAME	116	51	I/O	CardBus cycle frame. CFRAME is driven by the PCI1131 or a CardBus card when it is acting as an initiator to indicate the beginning and duration of a transaction. CFRAME is asserted to indicate a bus transaction is beginning, and while it is asserted, data transfer is continuous. When CFRAME is high (deasserted), the transaction is in its final data phase.
CGNT	110	46	O	CardBus grant. CGNT is driven by the PCI1131 to grant a CardBus PC Card access to the CardBus bus after the current data transaction is complete.
CINT	135	69	I	CardBus interrupt. CINT is asserted low by a CardBus PC Card to request interrupt servicing from the host.

† Terminal name is preceded with A_. For example, the full name for terminal 112 is A_CCLK.
‡ Terminal name is preceded with B_. For example, the full name for terminal 48 is B_CCLK.

Terminal Functions (Continued)

CardBus PC Card interface control signals (slots A and B) (continued)

TERMINAL NAME	NUMBER SLOT A†	NUMBER SLOT B‡	I/O TYPE	FUNCTION
CIRDY	115	50	I/O	CardBus initiator ready. CIRDY indicates that the PCI1131 is initiating the ability of the bus initiator to complete a current data phase of the transaction. It is used with CTRDY. When both CIRDY and CTRDY are sampled asserted, a data phase is completed on any clock. During a write, CIRDY indicates that valid data is present on CAD31–CAD0. During a read, CIRDY indicates the PCI1131, as an initiator, is prepared to accept the data. Wait cycles are inserted until CIRDY and CTRDY are both low (asserted).
CPERR	108	43	I/O	CardBus parity error. CPERR reports errors during all CardBus PC Card transactions except during special cycles. CPERR is sustained in the high-impedance state and must be driven active by the agent receiving data, two clocks following the data, when a data parity error is detected. CPERR must be driven active for a minimum duration of one clock for each data phase. CPERR must be driven high for one clock before it is returned to the high-impedance state. An agent cannot report a CPERR until it claims the access by asserting CDEVSEL and completes a data phase.
CREQ	127	61	I	CardBus request. CREQ indicates to the arbiter that the CardBus PC Card requires use of the CardBus bus.
CSERR	136	70	I	CardBus system error. CSERR reports address parity error, data errors on the special cycle command, or any other system error such that the CardBus card can no longer operate correctly. CSERR is open drain and is actively driven for a single CardBus PC Card clock by the agent reporting the error. The assertion of CSERR is synchronous to the clock and meets the setup and hold times of all bused signals. Restoring CSERR to the deasserted state is accomplished by a weak pullup provided by the system designer. This pullup can take two to three clock periods to fully restore CSERR. The PCI1131 reports CSERR to the operating system any time it is sampled low (asserted).
CSTOP	109	45	I/O	CardBus stop. CSTOP indicates the current target is requesting the initiator to stop the current transaction.
CSTSCHG	138	72	I	CardBus status change. CSTSCHG is used to alert the system to a change in the READY, WP, or BVD condition of the I/O CardBus PC Card.
CTRDY	114	49	I/O	CardBus target ready. CTRDY indicates that the PCI1131, as a selected target, can complete a current data phase of the transaction. CTRDY is used with CIRDY. When both of these signals are sampled asserted, a data phase is completed on any clock. During a read, CTRDY indicates that valid data is present on CAD31–CAD0. During a write, CIRDY indicates the PCI1131, as a target, is prepared to accept the data. Wait cycles are inserted until CIRDY and CTRDY are both low (asserted).
CVS1 CVS2	134 122	68 56	I/O	CardBus voltage sense 1 and voltage sense 2. CVS1 and CVS2, together with CCD1 and CCD2, determine the operating voltage of the CardBus PC Card.

† Terminal name is preceded with A_. For example, the full name for terminal 115 is A_CIRDY.
‡ Terminal name is preceded with B_. For example, the full name for terminal 50 is B_CIRDY.

absolute maximum ratings over operating temperature ranges (unless otherwise noted)†

Supply voltage range:	V_{CC}	–0.5 V to 4.6 V
	V_{CCP}	–0.5 V to 6 V
Input voltage range, V_I:	Standard	–0.5 V to V_{CC} + 0.5 V
	Card A	–0.5 to V_{CCA} + 0.5 V
	Card B	–0.5 to V_{CCB} + 0.5 V
	Fail safe	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O:	Standard	–0.5 V to V_{CC} + 0.5 V
	Card A	–0.5 to V_{CCA} + 0.5 V
	Card B	–0.5 to V_{CCB} + 0.5 V
	Fail safe	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)		±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 2)		±20 mA
Storage temperature range, T_{stg}		–65°C to 150°C
Virtual junction temperature, T_J		150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies to external input and bidirectional buffers. $V_I > V_{CC}$ does not apply to fail-safe terminals.
2. Applies to external output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail-safe terminals.

recommended operating conditions

			MIN	NOM	MAX	UNIT
t_t	Input transition (rise and fall) time	CMOS compatible	0		25	ns
T_A	Operating ambient temperature	Commercial	0	25	70	°C
T_J‡	Virtual junction temperature	Commercial	0	25	115	°C

‡ These junction temperatures reflect simulation conditions. The customer is responsible for verifying junction temperature.

recommended operating conditions for PCI interface

			OPERATION	MIN	NOM	MAX	UNIT
V_{CC}	Core voltage	Commercial	3.3 V	3	3.3	3.6	V
V_{CCP}	PCI supply voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
V_I	Input voltage		3.3 V	0		V_{CCP}	V
			5 V	0		V_{CCP}	
V_O§	Output voltage		3.3 V	0		V_{CCP}	V
			5 V	0		V_{CCP}	
V_{IH}¶	High-level input voltage	CMOS compatible	3.3 V	0.5 V_{CCP}			V
			5 V	2			
		Fail safe#	3.3 V	0.5 V_{CC}			
V_{IL}¶	Low-level input voltage	CMOS compatible	3.3 V			0.3 V_{CCP}	V
			5 V			0.8	
		Fail safe#	3.3 V			0.3 V_{CC}	

§ Applies to external output buffers
¶ Applies to external input and bidirectional buffers without hysteresis
# Fail-safe pins are 16, 56, 68, 72, 74, 82, 122, 134, 138, 140, 149, and 152.

recommended operating conditions for PC Cards A and B and miscellaneous inputs and outputs

			OPERATION	MIN	NOM	MAX	UNIT
$V_{CC(A/B)}$	PC Card supply voltage	Commercial	3.3 V	3	3.3	3.6	V
			5 V	4.75	5	5.25	
V_I	Input voltage		3.3 V	0		$V_{CC(A/B)}$	V
			5 V	0		$V_{CC(A/B)}$	
V_O†	Output voltage		3.3 V	0		$V_{CC(A/B)}$	V
			5 V	0		$V_{CC(A/B)}$	
V_{IH}‡	High-level input voltage	CMOS compatible	3.3 V	0.475 $V_{CC(A/B)}$¶			V
			5 V	2.4			
		Fail safe§	3.3 V	0.475 $V_{CC(A/B)}$¶			
V_{IL}‡	Low-level input voltage	CMOS compatible	3.3 V			0.325 $V_{CC(A/B)}$¶	V
			5 V			0.8	
		Fail safe§	3.3 V			0.325 $V_{CC(A/B)}$¶	

† Applies to external output buffers
‡ Applies to external input and bidirectional buffers without hysteresis
§ Fail-safe pins are 16, 56, 68, 72, 74, 82, 122, 134, 138, 140, 149, and 152.
¶ Meets TTL levels, V_{IH} MIN =1.65 V and V_{IL} MAX = 0.99 V

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		SIDE	TEST CONDITIONS	OPERATION	MIN	MAX	UNIT
V_{OH}	High-level output voltage†	PCI	I_{OH} = –0.5 mA	3.3 V	0.9 V_{CC}		V
			I_{OH} = –2 mA	5 V	2.4		
		PC Card	I_{OH} = –0.15 mA	3.3 V	0.9 V_{CC}		
			I_{OH} = –0.15 mA	5 V	2.4		
		Miscellaneous‡	I_{OH} = –4 mA		2.1		
V_{OL}	Low-level output voltage	PCI	I_{OL} = 1.5 mA	3.3 V		0.1 V_{CC}	V
			I_{OL} = 6 mA	5 V		0.55	
		PC Card	I_{OL} = 0.7 mA	3.3 V		0.1 V_{CC}	
			I_{OL} = 0.7 mA	5 V		0.55	
		Miscellaneous‡	I_{OL} = 4 mA			0.5	
		$\overline{SERR}$	I_{OL} = 12 mA			0.5	
I_{IH}	High-level input current§	Input pins	$V_I = V_{CC}$¶	3.6 V		10	µA
			$V_I = V_{CC}$¶	5.25 V		20	
		I/O pins#	$V_I = V_{CC}$¶	3.6 V		10	
			$V_I = V_{CC}$¶	5.25 V		25	
		Fail safe	$V_I = V_{CC}$¶	3.6 V		10	
		DATA	$V_I = V_{CCP}$			290	
I_{IL}	Low-level input current§	Input pins	V_I = GND			–1	µA
		I/O pins	V_I = GND			–10	

† V_{OH} is not tested on $\overline{SERR}$ (pin 200) due to open-drain output.
‡ Miscellaneous pins are 150, 151, 156, 157, 159, 160, 161, 162, 163.
§ I_{IL} is not tested on DATA (pin 152) due to internal pulldown resistor, and I_{IH} is not tested on SPKROUT (pin 149) due to internal pullup resistor.
¶ For PCI and miscellaneous pins, $V_{CC} = V_{CCP}$. For card A/B, $V_{CC} = V_{CCA}/V_{CCB}$, respectively.
# For I/O pins, the input leakage current includes the off-state output current I_{OZ}.

PCI clock/reset timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figure 2 and Figure 3)

		ALTERNATE SYMBOL	MIN	MAX	UNIT
t_c	Cycle time, PCLK	t_{cyc}	30	∞	ns
t_{wH}	Pulse duration, PCLK high	t_{high}	11		ns
t_{wL}	Pulse duration, PCLK low	t_{low}	11		ns
$\Delta v/\Delta t$	Slew rate, PCLK	t_r, t_f	1	4	V/ns
t_w	Pulse duration, RSTIN	t_{rst}	1		ms
t_{su}	Setup time, PCLK active at end of $\overline{\text{RSTIN}}$	$t_{rst\text{-}clk}$	100		μs

PCI timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 3, Figure 1, and Figure 4)

			TEST CONDITIONS	ALTERNATE SYMBOL	MIN	MAX	UNIT
t_{pd}	Propagation delay time	PCLK to shared signal valid delay time	C_L = 50 pF, See Note 4	t_{val}		11	ns
		PCLK to shared signal invalid delay time	C_L = 50 pF, See Note 4	t_{inv}	2		
t_{en}	Enable time, high-impedance-to-active delay time from PCLK			t_{on}	2		ns
t_{dis}	Disable time, active-to-high-impedance delay time from PCLK			t_{off}		28	ns
t_{su}	Setup time before PCLK valid			t_{su}	7		ns
t_h	Hold time after PCLK high			t_h	0		ns

NOTES: 3. This data sheet uses the following conventions to describe time (t) intervals. The format is: t_A, where *subscript A* indicates the type of dynamic parameter being represented. One of the following is used: t_{pd} = propagation delay time, t_d = delay time, t_{su} = setup time, and t_h = hold time.

4. PCI shared signals are AD31–AD0, C/$\overline{\text{BE3}}$–C/$\overline{\text{BE0}}$, $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, $\overline{\text{STOP}}$, IDSEL, $\overline{\text{DEVSEL}}$, and PAR.

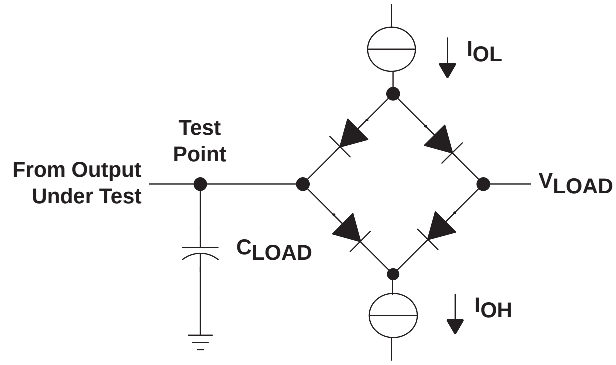
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT PARAMETERS

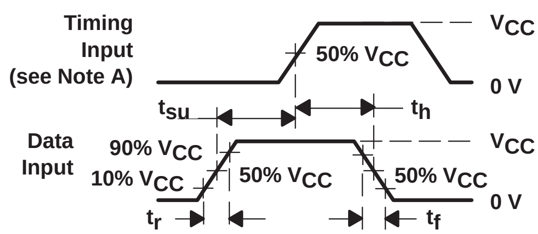
TIMING PARAMETER		C_{LOAD}† (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	50	8	–8	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	50	8	–8	1.5
	t_{PLZ}				
t_{pd}		50	8	–8	‡

† C_{LOAD} includes the typical load-circuit distributed capacitance.

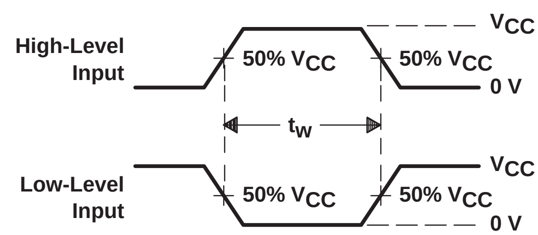
‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}} = 50\ \Omega$, where $V_{OL} = 0.6$ V, $I_{OL} = 8$ mA



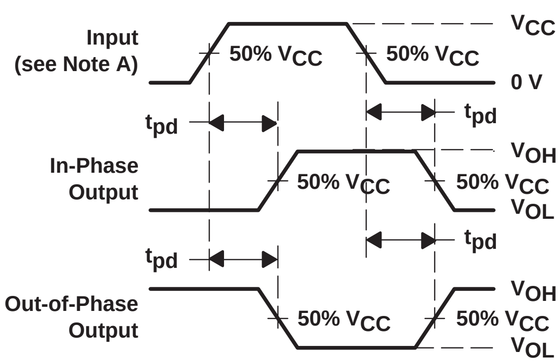
LOAD CIRCUIT



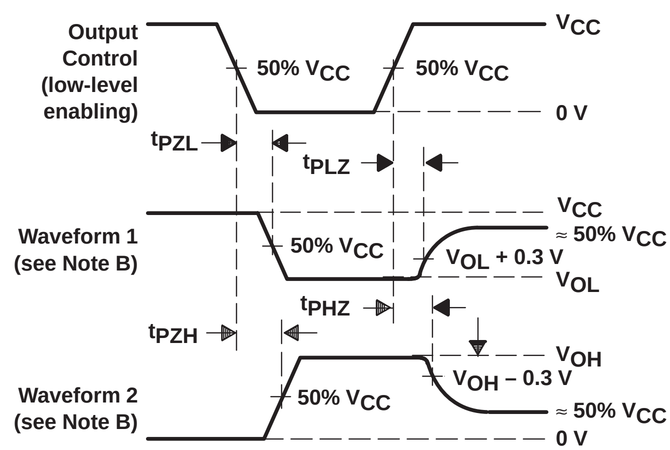
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz, $Z_O = 50\ \Omega$, $t_r \le 6$ ns, $t_f \le 6$ ns.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. For t_{PLZ} and t_{PHZ}, V_{OL} and V_{OH} are measured values.

Figure 1. Load Circuit and Voltage Waveforms

PCI BUS PARAMETER MEASUREMENT INFORMATION

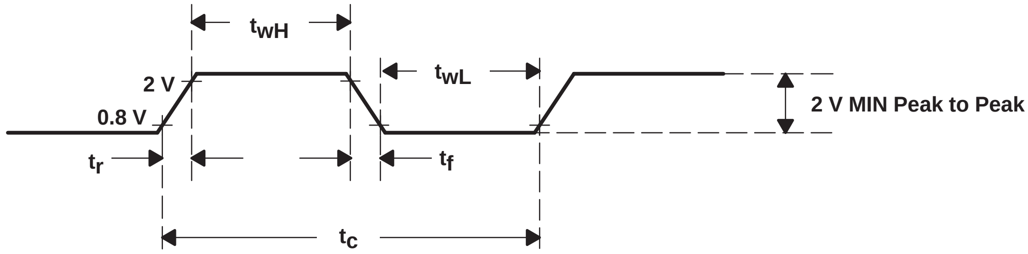


Figure 2. PCLK Timing Waveform

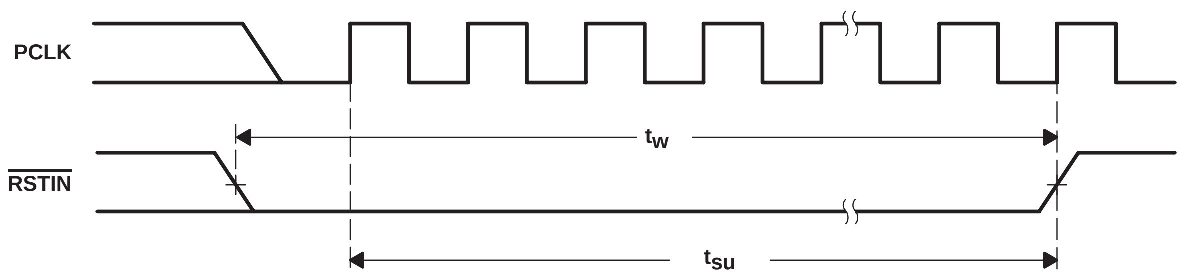


Figure 3. RSTIN Timing Waveforms

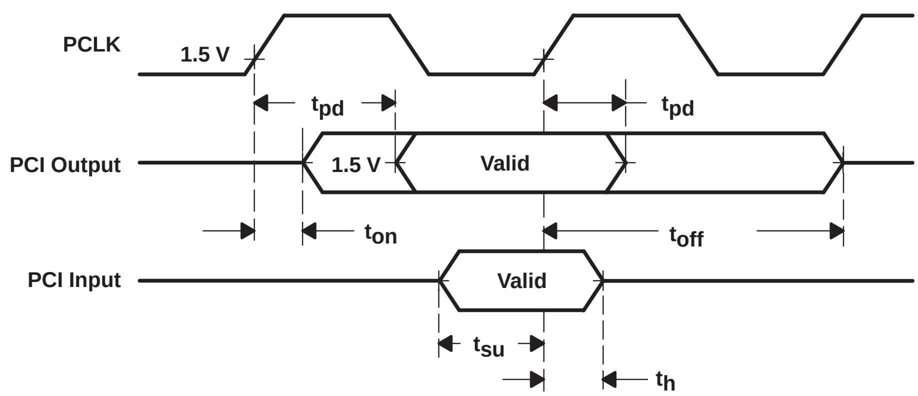


Figure 4. Shared-Signals Timing Waveforms

PC Card cycle timing

The PC Card cycle timing is controlled by the wait-state bits in the Intel 82365SL-DF compatible memory and I/O window registers. The PC Card cycle generator uses the PCI clock to generate the correct card address setup and hold times and the PC Card command active (low) interval. This allows the cycle generator to output PC Card cycles that are as close to the Intel 82365SL-DF timing as possible while always slightly exceeding the Intel 82365SL-DF values. This ensures compatibility with existing software and maximizes throughput.

The PC Card address setup and hold times are a function of the wait-state bits. Table 1 shows address setup time in PCLK cycles and nanoseconds for I/O and memory cycles. Table 2 and Table 3 show command active time in PCLK cycles and nanoseconds for I/O and memory cycles. Table 4 shows address hold time in PCLK cycles and nanoseconds for I/O and memory cycles.

Table 1. PC Card Address Setup Time, $t_{su(A)}$, 8-Bit and 16-Bit PCI Cycles

WAIT-STATE BITS			TS1 – 0 = 01 (PCLK/ns)
I/O			3/90
Memory	WS1	0	2/60
Memory	WS1	1	4/120

Table 2. PC Card Command Active Time, $t_{c(A)}$, 8-Bit PCI Cycles

WAIT-STATE BITS			TS1 – 0 = 01 (PCLK/ns)
	WS	ZWS	
I/O	0	0	19/570
	1	X	23/690
	0	1	7/210
Memory	00	0	19/570
	01	X	23/690
	10	X	23/690
	11	X	23/690
	00	1	7/210

Table 3. PC Card Command Active Time, $t_{c(A)}$, 16-Bit PCI Cycles

WAIT-STATE BITS			TS1 – 0 = 01 (PCLK/ns)
	WS	ZWS	
I/O	0	0	7/210
	1	X	11/330
	0	1	N/A
Memory	00	0	9/270
	01	X	13/390
	10	X	17/510
	11	X	23/630
	00	1	5/150

Table 4. PC Card Address Hold Time, $t_{h(A)}$, 8-Bit and 16-Bit PCI Cycles

WAIT-STATE BITS			TS1 – 0 = 01 (PCLK/ns)
I/O			2/60
Memory	WS1	0	2/60
Memory	WS1	1	3/90

timing requirements over recommended ranges of supply voltage and operating free-air temperature, memory cycles (for 100-ns common memory) (see Note 5 and Figure 5)

		ALTERNATE SYMBOL	MIN	MAX	UNIT
t_{su}	Setup time, $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ before $\overline{\text{WE}}$/$\overline{\text{OE}}$ low	T1	60		ns
t_{su}	Setup time, CA25–CA0 before $\overline{\text{WE}}$/$\overline{\text{OE}}$ low	T2	$t_{su(A)}$+2PCLK		ns
t_{su}	Setup time, $\overline{\text{REG}}$ before $\overline{\text{WE}}$/$\overline{\text{OE}}$ low	T3	90		ns
t_{pd}	Propagation delay time, $\overline{\text{WE}}$/$\overline{\text{OE}}$ low to $\overline{\text{WAIT}}$ low	T4			ns
t_w	Pulse duration, $\overline{\text{WE}}$/$\overline{\text{OE}}$ low	T5	200		ns
t_h	Hold time, $\overline{\text{WE}}$/$\overline{\text{OE}}$ low after $\overline{\text{WAIT}}$ high	T6			ns
t_h	Hold time, $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ after $\overline{\text{WE}}$/$\overline{\text{OE}}$ high	T7	120		ns
t_{su}	Setup time (read), CDATA15–CDATA0 valid before $\overline{\text{OE}}$ high	T8			ns
t_h	Hold time (read), CDATA15–CDATA0 valid after $\overline{\text{OE}}$ high	T9	0		ns
t_h	Hold time, CA25–CA0 and $\overline{\text{REG}}$ after $\overline{\text{WE}}$/$\overline{\text{OE}}$ high	T10	$t_{h(A)}$+1PCLK		ns
t_{su}	Setup time (write), CDATA15–CDATA0 valid before $\overline{\text{WE}}$ low	T11	60		ns
t_h	Hold time (write), CDATA15–CDATA0 valid after $\overline{\text{WE}}$ low	T12	240		ns

NOTE 5: These times are dependent on the register settings associated with ISA wait states and data size. They are also dependent on cycle type (read/write, memory/I/O) and $\overline{\text{WAIT}}$ from PC Card. The times listed here represent absolute minimums (the times that would be observed if programmed for zero wait state, 16-bit cycles) with a 33-MHz PCI clock.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, I/O cycles (see Figure 6)

		ALTERNATE SYMBOL	MIN	MAX	UNIT
t_{su}	Setup time, $\overline{\text{REG}}$ before $\overline{\text{IORD}}$/$\overline{\text{IOWR}}$ low	T13	60		ns
t_{su}	Setup time, $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ before $\overline{\text{IORD}}$/$\overline{\text{IOWR}}$ low	T14	60		ns
t_{su}	Setup time, CA25–CA0 valid before $\overline{\text{IORD}}$/$\overline{\text{IOWR}}$ low	T15	$t_{su(A)}$+2PCLK		ns
t_{pd}	Propagation delay time, $\overline{\text{IOIS16}}$ low after CA25–CA0 valid	T16		35	ns
t_{pd}	Propagation delay time, $\overline{\text{IORD}}$ low to $\overline{\text{WAIT}}$ low	T17	35		ns
t_w	Pulse duration, $\overline{\text{IORD}}$/$\overline{\text{IOWR}}$ low	T18	T_{cA}		ns
t_h	Hold time, $\overline{\text{IORD}}$ low after $\overline{\text{WAIT}}$ high	T19			ns
t_h	Hold time, $\overline{\text{REG}}$ low after $\overline{\text{IORD}}$ high	T20	0		ns
t_h	Hold time, $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ after $\overline{\text{IORD}}$/$\overline{\text{IOWR}}$ high	T21	120		ns
t_h	Hold time, CA25–CA0 after $\overline{\text{IORD}}$/$\overline{\text{IOWR}}$ high	T22	$t_{h(A)}$+1PCLK		ns
t_{su}	Setup time (read), CDATA15–CDATA0 valid before $\overline{\text{IORD}}$ high	T23	10		ns
t_h	Hold time (read), CDATA15–CDATA0 valid after $\overline{\text{IORD}}$ high	T24	0		ns
t_{su}	Setup time (write), CDATA15–CDATA0 valid before $\overline{\text{IOWR}}$ low	T25	90		ns
t_h	Hold time (write), CDATA15–CDATA0 valid after $\overline{\text{IOWR}}$ high	T26	90		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, miscellaneous (see Figure 7)

PARAMETER			ALTERNATE SYMBOL	MIN	MAX	UNIT
t_{pd}	Propagation delay time	BVD2 low to SPKROUT low	T27		30	ns
		BVD2 high to SPKROUT high			30	
		$\overline{IREQ}$ to IRQ15–IRQ3	T28		30	
		$\overline{STSCHG}$ to IRQ15–IRQ3			30	

PC Card PARAMETER MEASUREMENT INFORMATION

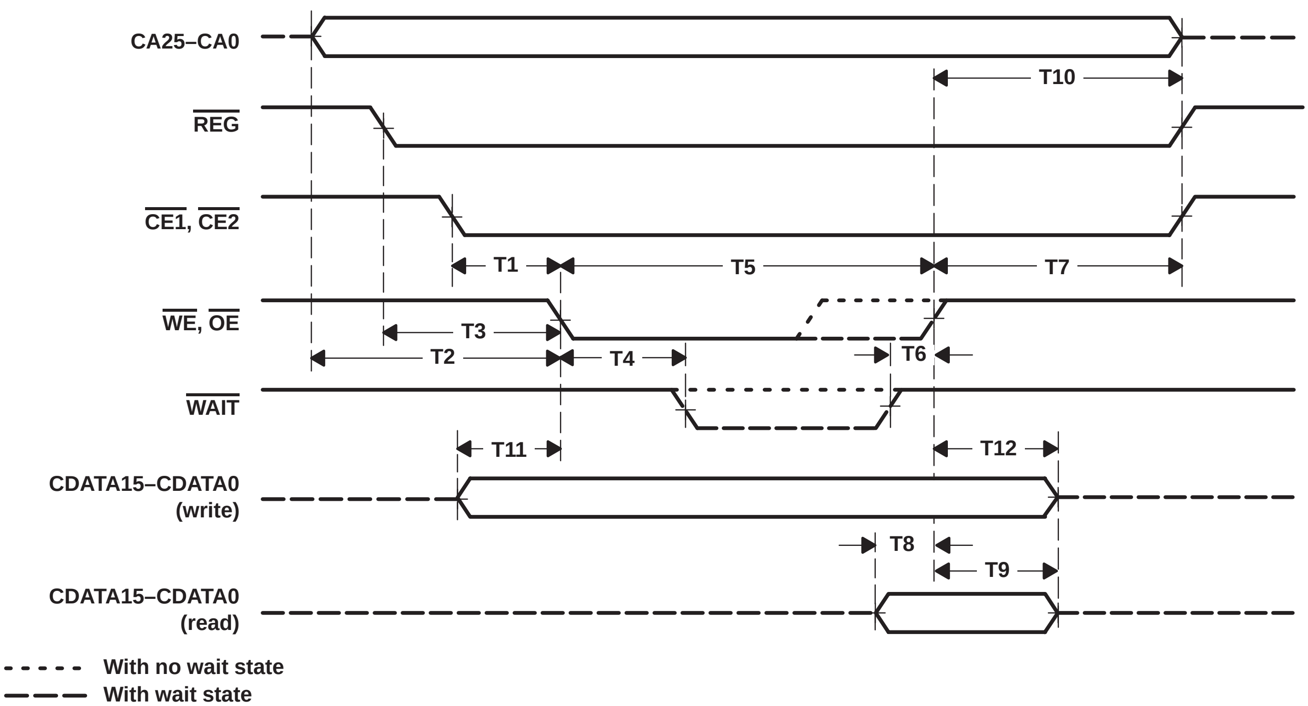


Figure 5. PC Card Memory Cycle

PC Card PARAMETER MEASUREMENT INFORMATION

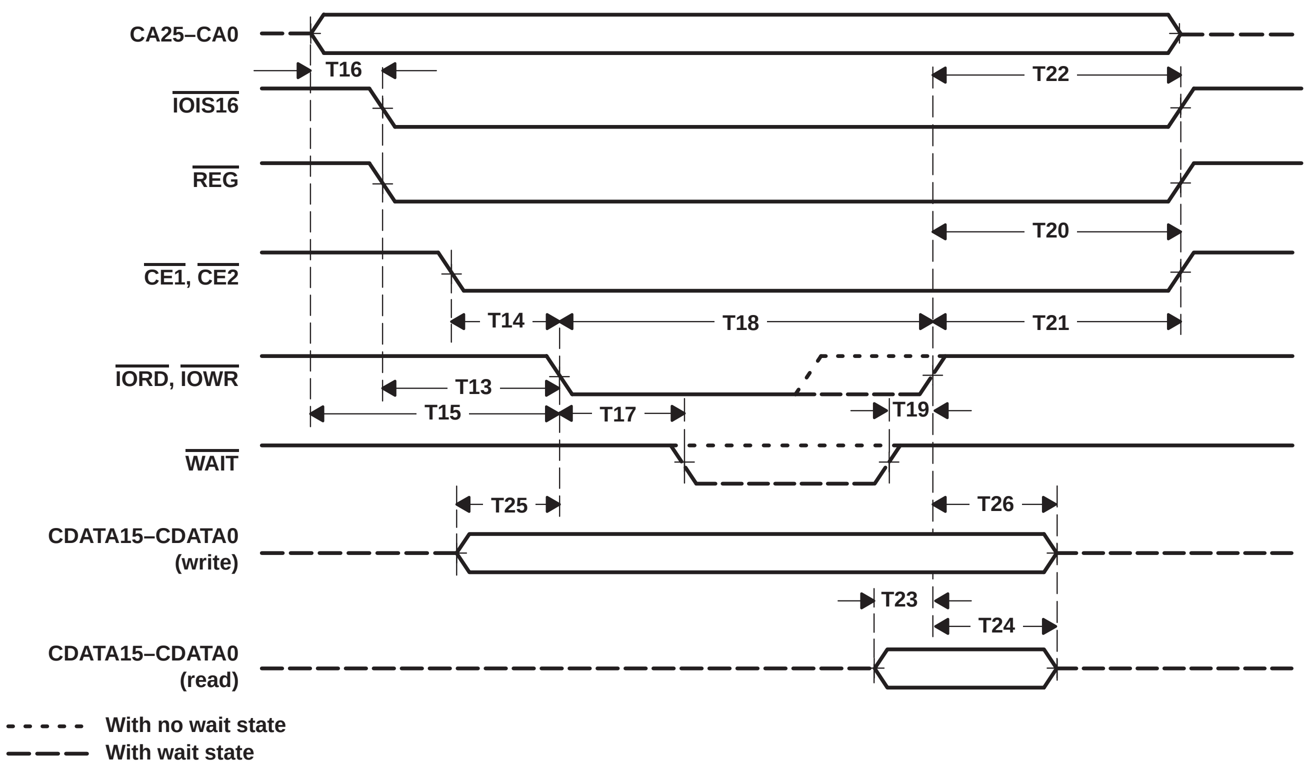


Figure 6. PC Card I/O Cycle

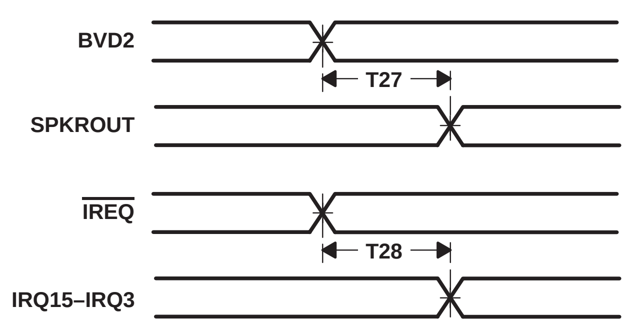
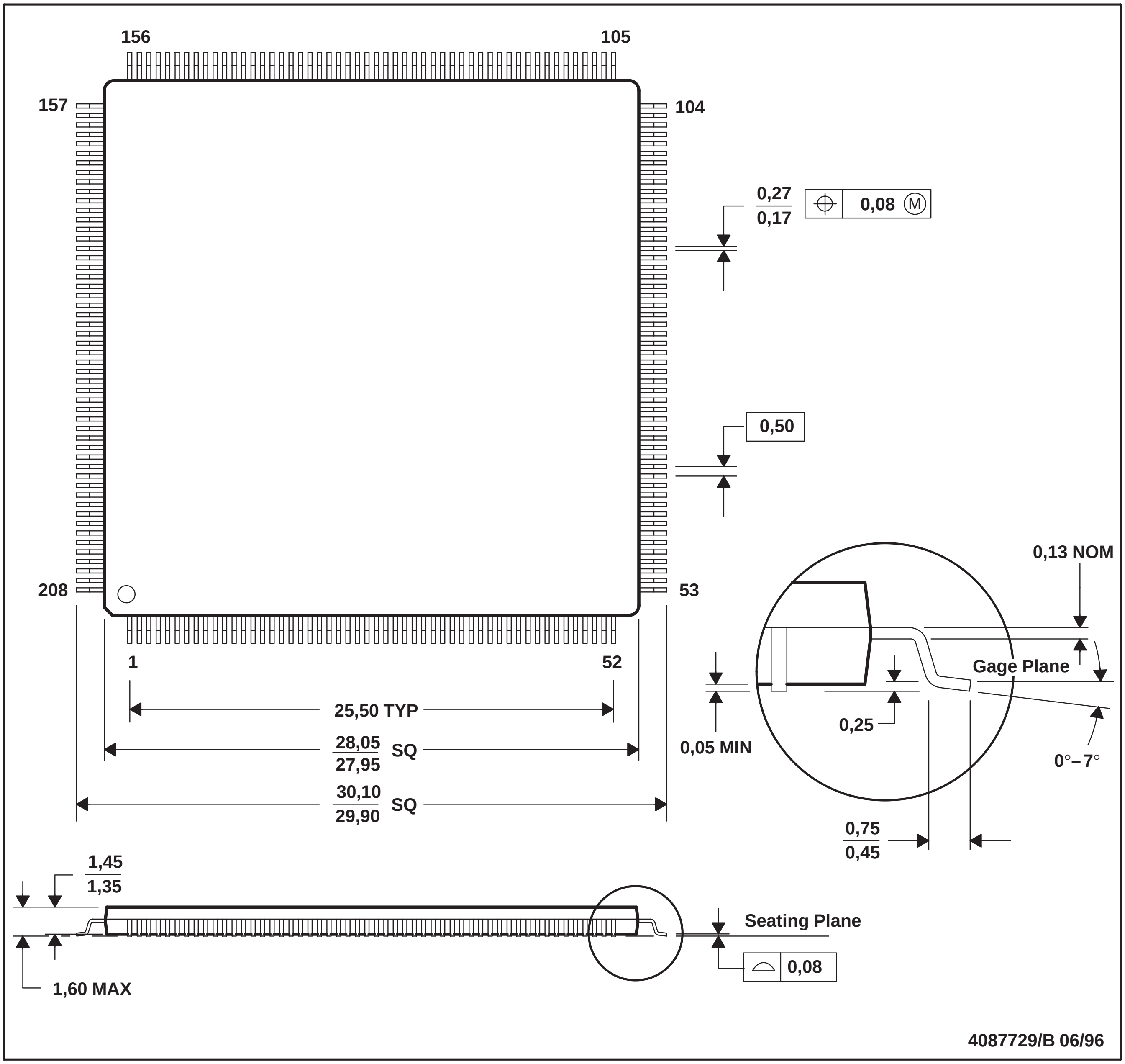


Figure 7. Miscellaneous PC Card Delay Times

MECHANICAL DATA

PDV (S-PQFP-G208) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

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