

# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

- Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 60 MHz to 200 MHz
- Low Jitter (cycle-cycle):  $\pm 50$  ps
- Low Static Phase Offset:  $\pm 50$  ps
- Low Jitter (Period):  $\pm 35$  ps
- Distributes One Differential Clock Input to 10 Differential Outputs
- Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low
- Operates From Dual 2.5-V Supplies
- Available in a 48-Pin TSSOP Package or 56-Ball MicroStar Junior™ BGA Package
- Consumes  $< 100\text{-}\mu\text{A}$  Quiescent Current
- External Feedback Pins (FBIN,  $\overline{\text{FBIN}}$ ) Are Used to Synchronize the Outputs to the Input Clocks
- Meets/Exceeds the Latest DDR JEDEC Spec JESD82-1

### description

The CDCV857B is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK,  $\overline{\text{CLK}}$ ) to 10 differential pairs of clock outputs (Y[0:9],  $\overline{\text{Y}}[0:9]$ ) and one differential pair of feedback clock outputs (FBOU,  $\overline{\text{FBOU}}$ ). The clock outputs are controlled by the clock inputs (CLK,  $\overline{\text{CLK}}$ ), the feedback clocks (FBIN,  $\overline{\text{FBIN}}$ ), and the analog power input (AV<sub>DD</sub>). When  $\overline{\text{PWRDWN}}$  is high, the outputs switch in phase and frequency with CLK. When  $\overline{\text{PWRDWN}}$  is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a  $>20\text{-MHz}$  input signal, this detection circuit turns the PLL on and enables the outputs.

When AV<sub>DD</sub> is strapped low, the PLL is turned off and bypassed for test purposes. The CDCV857B is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV857B is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV857B is characterized for both commercial and industrial temperature ranges.

#### AVAILABLE OPTIONS

T <sub>A</sub>	TSSOP (DGG)	MicroStar Junior™ BGA (GQL)
0°C to 85°C	CDCV857BDGG	CDCV857BGQL
-40°C to 85°C	CDCV857BIGG	—

#### FUNCTION TABLE (Select Functions)

INPUTS				OUTPUTS				PLL
AV <sub>DD</sub>	$\overline{\text{PWRDWN}}$	CLK	$\overline{\text{CLK}}$	Y[0:9]	$\overline{\text{Y}}[0:9]$	FBOU	$\overline{\text{FBOU}}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	$<20$ MHz	$<20$ MHz	Z	Z	Z	Z	Off



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroStar Junior is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



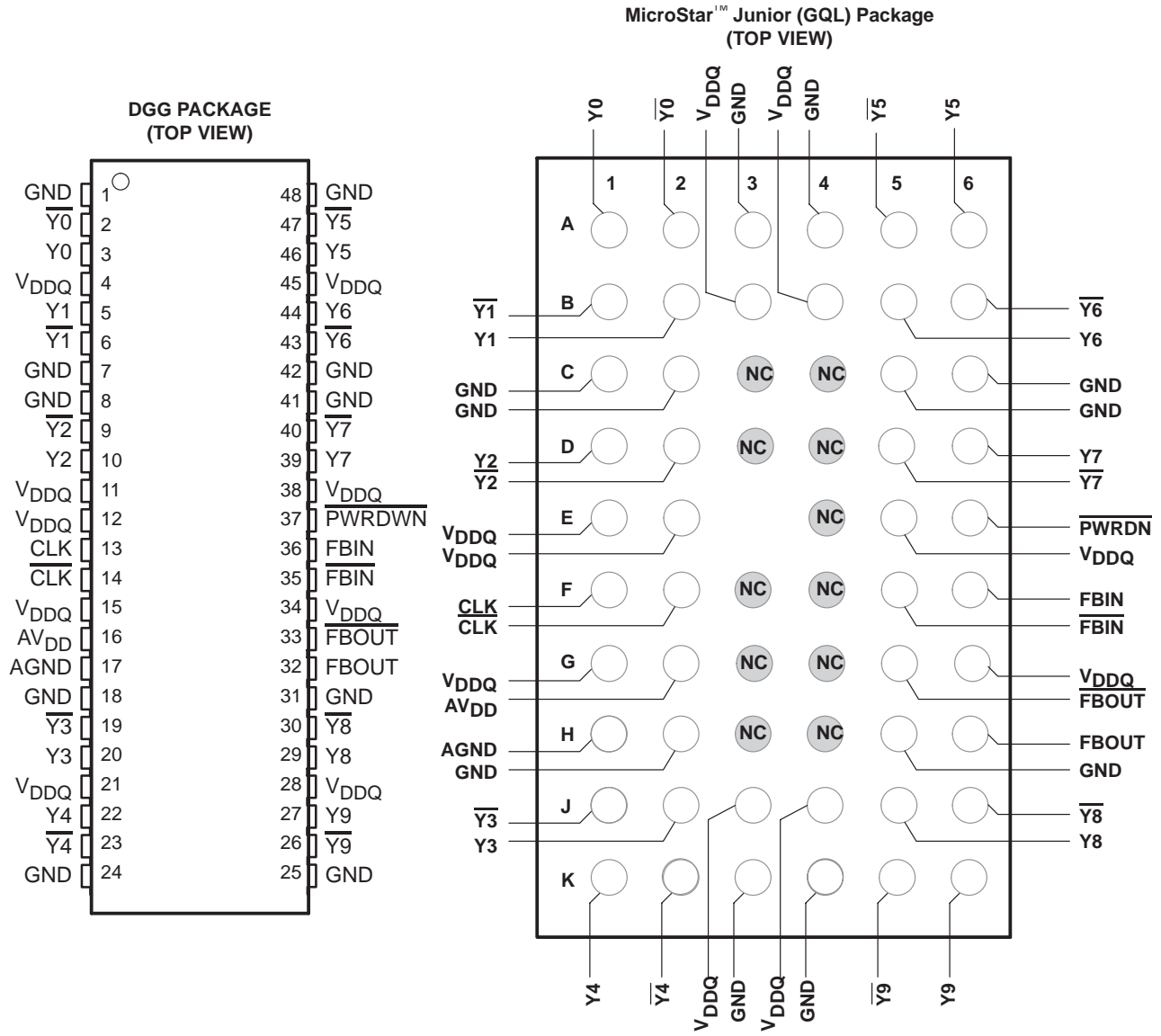
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

# CDCV857B, CDCV857BI

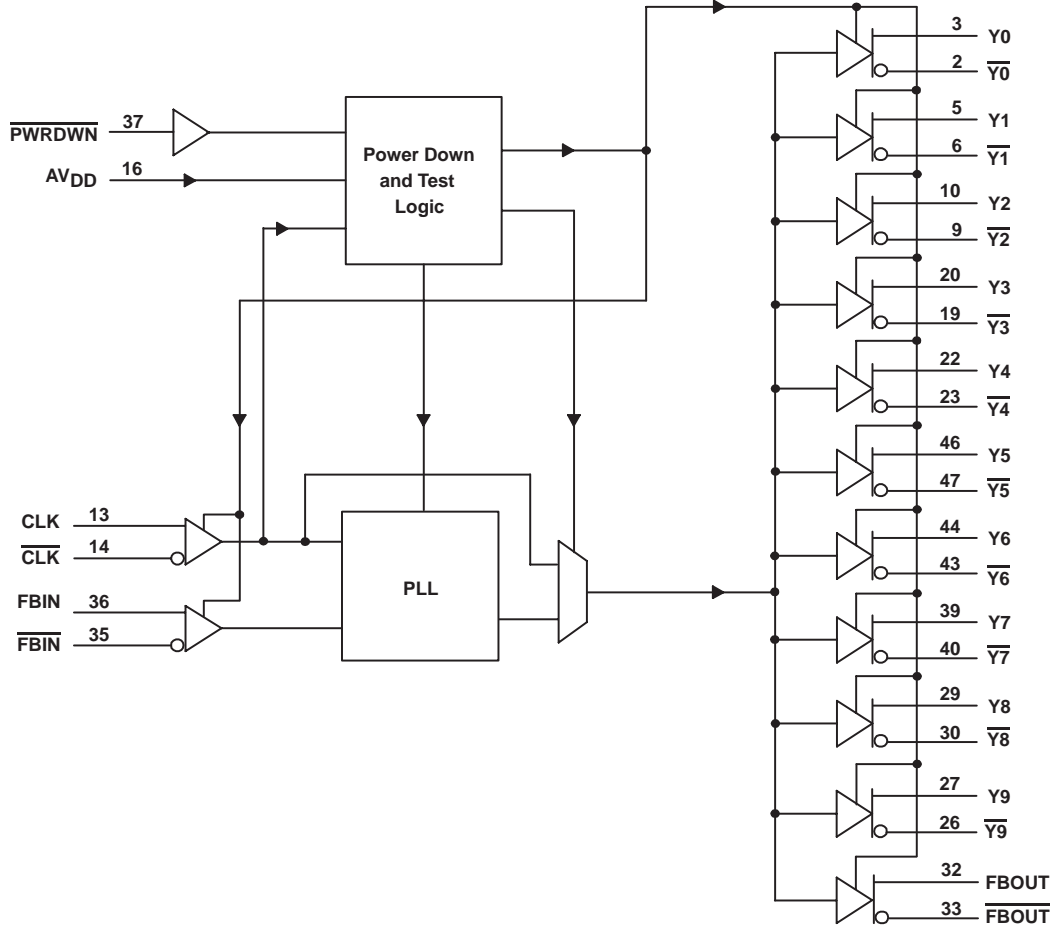
## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

functional block diagram



# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

### Terminal Functions

TERMINAL				DESCRIPTION
NAME	DGG	GQL		
AGND	17	H1		Ground for 2.5-V analog supply
AV <sub>DD</sub>	16	G2		2.5-V Analog supply
CLK, $\overline{\text{CLK}}$	13, 14	F1, F2	I	Differential clock input
$\overline{\text{FBIN}}$ , FBIN	35, 36	F5, F6	I	Feedback differential clock input
$\overline{\text{FBOU}}$ , FBOU	32, 33	H6, G5	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	A3, A4, C1, C2, C5, C6, H2, H5, K3, K4		Ground
$\overline{\text{PWRDWN}}$	37	E6	I	Output enable for Y and $\overline{\text{Y}}$
V <sub>DDQ</sub>	4, 11, 12, 15, 21, 28, 34, 38, 45	B3, B4, E1, E2, E5, G1, G6, J3, J4		2.5-V Supply
Y[0:9]	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	A1, B2, D1, J2, K1, A6, B5, D6, J5, K6	O	Buffered output copies of input clock, CLK
$\overline{\text{Y}}$ [0:9]	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	A2, B1, D2, J1, K2, A5, B6, D5, J6, K5	O	Buffered output copies of input clock, $\overline{\text{CLK}}$

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V <sub>DDQ</sub> , AV <sub>DD</sub>	0.5 V to 3.6 V
Input voltage range, V <sub>I</sub> (see Notes 1 and 2)	-0.5 V to V <sub>DDQ</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	-0.5 V to V <sub>DDQ</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DDQ</sub> )	±50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DDQ</sub> )	±50 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>DDQ</sub> )	±50 mA
Continuous current to GND or V <sub>DDQ</sub>	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): GQL package	137.6°C/W
Storage temperature range T <sub>stg</sub>	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.  
 2. This value is limited to 3.6 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51.



**recommended operating conditions (see Note 4)**

		MIN	TYP	MAX	UNIT
Supply voltage	V <sub>DDQ</sub>	2.3		2.7	V
	AV <sub>DD</sub>	V <sub>DDQ</sub> - 0.12		2.7	V
Low-level input voltage, V <sub>IL</sub>	CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$	V <sub>DDQ</sub> /2 - 0.18			V
	PWRDWN	-0.3		0.7	
High-level input voltage, V <sub>IH</sub>	CLK, $\overline{\text{CLK}}$ , FBIN, $\overline{\text{FBIN}}$	V <sub>DDQ</sub> /2 + 0.18			V
	PWRDWN	1.7		V <sub>DDQ</sub> + 0.3	
DC input signal voltage (see Note 5)		-0.3		V <sub>DDQ</sub> + 0.3	V
Differential input signal voltage, V <sub>ID</sub> (see Note 6)	dc   CLK, FBIN	0.36		V <sub>DDQ</sub> + 0.6	V
	ac   CLK, FBIN	0.7		V <sub>DDQ</sub> + 0.6	
Input differential pair cross voltage, V <sub>IX</sub> (see Note 7)		V <sub>DDQ</sub> /2 - 0.2		V <sub>DDQ</sub> /2 + 0.2	V
High-level output current, I <sub>OH</sub>				-12	mA
Low-level output current, I <sub>OL</sub>				12	mA
Input slew rate, SR		1		4	V/ns
Operating free-air temperature, T <sub>A</sub>	Commercial	0		85	°C
	Industrial	-40		85	

- NOTES: 4. The unused inputs must be held high or low to prevent them from floating.  
 5. The dc input signal voltage specifies the allowable dc execution of the differential input.  
 6. The differential input signal voltage specifies the differential voltage |V<sub>T</sub>R - V<sub>C</sub>P| required for switching, where V<sub>T</sub>R is the true input level and V<sub>C</sub>P is the complementary input level.  
 7. The differential cross-point voltage is expected to track variations of V<sub>CC</sub> and is the voltage at which the differential signals must be crossing.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>	Input voltage	All inputs	V <sub>DDQ</sub> = 2.3 V, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	High-level output voltage		V <sub>DDQ</sub> = min to max, I <sub>OH</sub> = -1 mA	V <sub>DDQ</sub> - 0.1			V
			V <sub>DDQ</sub> = 2.3 V, I <sub>OH</sub> = -12 mA	1.7			
V <sub>OL</sub>	Low-level output voltage		V <sub>DDQ</sub> = min to max, I <sub>OL</sub> = 1 mA			0.1	V
			V <sub>DDQ</sub> = 2.3 V, I <sub>OL</sub> = 12 mA			0.6	
V <sub>OD</sub>	Output voltage swing‡		Differential outputs are terminated with 120 Ω /CL = 14 pF (See Figure 3)	1.1		V <sub>DDQ</sub> - 0.4	V
V <sub>OX</sub>	Output differential cross-voltage§			V <sub>DDQ</sub> /2 - 0.15	V <sub>DDQ</sub> /2	V <sub>DDQ</sub> /2 + 0.15	
I <sub>I</sub>	Input current		V <sub>DDQ</sub> = 2.7 V, V <sub>I</sub> = 0 V to 2.7 V			±10	μA
I <sub>OZ</sub>	High-impedance state output current		V <sub>DDQ</sub> = 2.7 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND			±10	μA
I <sub>DDPD</sub>	Power-down current on V <sub>DDQ</sub> + AV <sub>DD</sub>		CLK and $\overline{\text{CLK}}$ = 0 MHz; PWRDWN = Low; Σ of I <sub>DD</sub> and AI <sub>DD</sub>		20	100	μA
AI <sub>DD</sub>	Supply current on AV <sub>DD</sub>		f <sub>O</sub> = 170 MHz		7	10	mA
			f <sub>O</sub> = 200 MHz		9	12	
C <sub>I</sub>	Input capacitance		V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND	2	2.5	3.5	pF

† All typical values are at a respective nominal V<sub>DDQ</sub>.

‡ The differential output signal voltage specifies the differential voltage |V<sub>T</sub>R - V<sub>C</sub>P|, where V<sub>T</sub>R is the true output level and V<sub>C</sub>P is the complementary output level.

§ The differential cross-point voltage is expected to track variations of V<sub>DDQ</sub> and is the voltage at which the differential signals must be crossing. The frequency range is 100 MHz to 200 MHz.

# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I <sub>DD</sub>	Dynamic current on V <sub>DDQ</sub>	Without load	f <sub>O</sub> = 170 MHz	100	110	mA
			f <sub>O</sub> = 200 MHz	105	120	
		Differential outputs terminated with 120 Ω/CL = 0 pF	f <sub>O</sub> = 170 MHz	200	240	
			f <sub>O</sub> = 200 MHz	210	250	
		Differential outputs terminated with 120 Ω/CL = 14 pF	f <sub>O</sub> = 170 MHz	260	300	
			f <sub>O</sub> = 200 MHz	280	320	
ΔC	Part-to-part input capacitance variation	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND			1	pF
C <sub>I(Δ)</sub>	Input capacitance difference between CLK and CLKB, FBIN, and FBINB	V <sub>DDQ</sub> = 2.5 V, V <sub>I</sub> = V <sub>DDQ</sub> or GND			0.25	pF
C <sub>O</sub>	Output capacitance	V <sub>DDQ</sub> = 2.5 V, V <sub>O</sub> = V <sub>DDQ</sub> or GND	2.5	3	3.5	pF

† All typical values are at a respective nominal V<sub>DDQ</sub>.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f <sub>CLK</sub>	Operating clock frequency	60	200	MHz
	Application clock frequency			
Input clock duty cycle		40%	60%	
Stabilization time† (PLL mode)			10	μs
Stabilization time‡ (Bypass mode)			30	ns

† The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and V<sub>DD</sub> must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

‡ A recovery time is required when the device goes from power-down mode into bypass mode (AVDD at GND).

### switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> §	Low to high level propagation delay time	Test mode/CLK to any output		3.5		ns
t <sub>PHL</sub> §	High-to low level propagation delay time	Test mode/CLK to any output		3.5		ns
t <sub>jit(per)</sub> ¶	Jitter (period), See Figure 7	66 MHz	-60		60	ps
		100/133/167/200 MHz	-35		35	ps
t <sub>jit(cc)</sub> ¶	Jitter (cycle-to-cycle), See Figure 4	66 MHz	-75		75	ps
		100/133/167/200 MHz	-50		50	ps
t <sub>jit(hper)</sub> ¶	Half-period jitter, See Figure 8	66 MHz	-100		100	ps
		100/133/167/200 MHz	-75		75	ps
t <sub>slr(o)</sub>	Output clock slew rate, See Figure 9	Load: 120 Ω/14 pF	1		2	V/ns
t(∅)	Static phase offset, See Figure 5	66 MHz	-100		100	ps
		100/133/167/200 MHz	-50		50	ps
t <sub>sk(o)</sub>	Output skew, See Figure 6	Load: 120 Ω/14 pF		70	100	ps
t <sub>r</sub> , t <sub>f</sub>	Output rise and fall times (20% – 80%)	Load: 120 Ω/14 pF	600		900	ps

§ Refers to the transition of the noninverting output.

¶ This parameter is assured by design but can not be 100% production tested.



PARAMETER MEASUREMENT INFORMATION

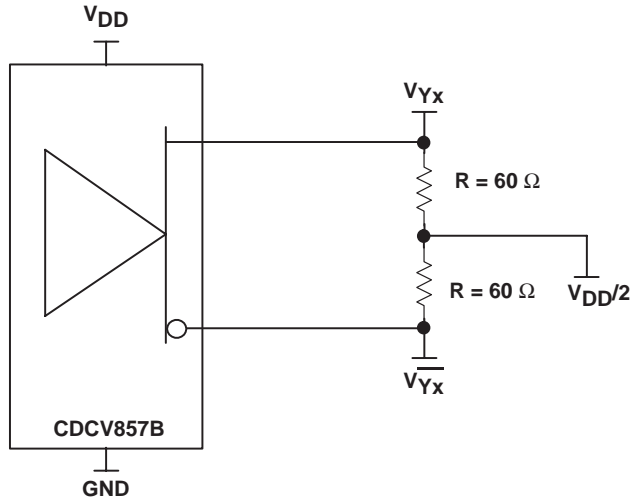


Figure 1. IBIS Model Output Load

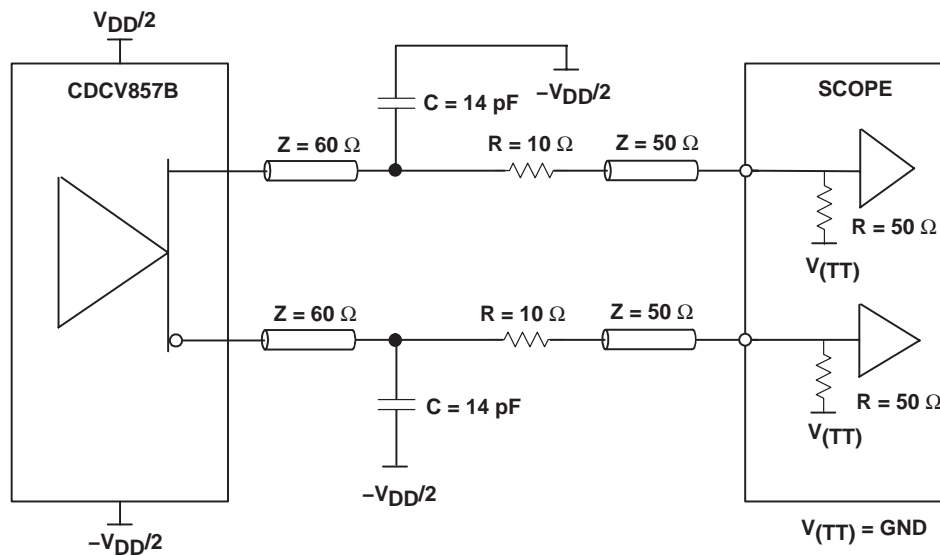


Figure 2. Output Load Test Circuit

# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

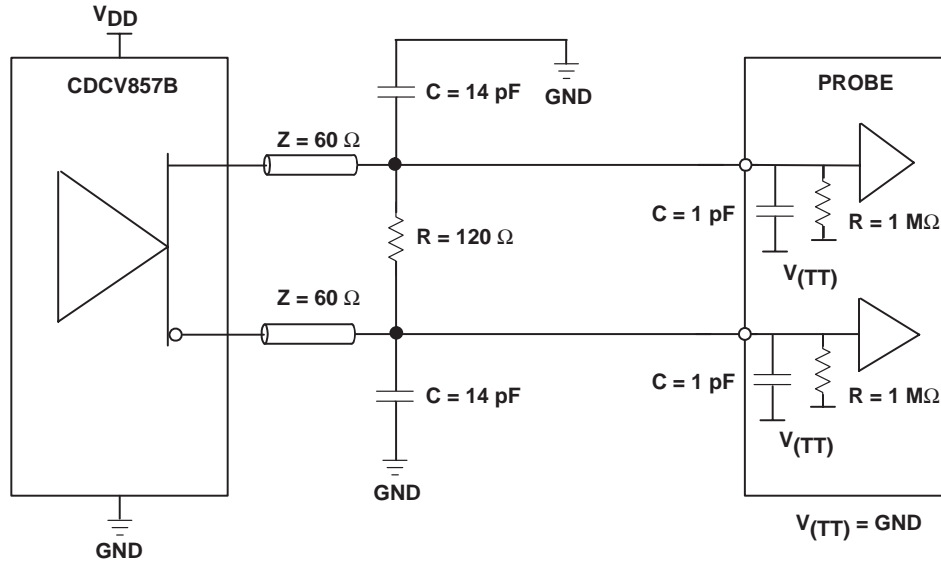


Figure 3. Output Load Test Circuit for Crossing Point

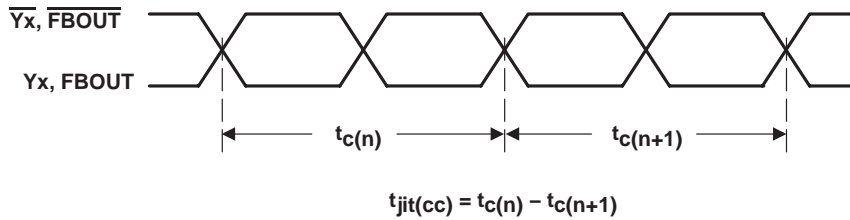


Figure 4. Cycle-to-Cycle Jitter



PARAMETER MEASUREMENT INFORMATION

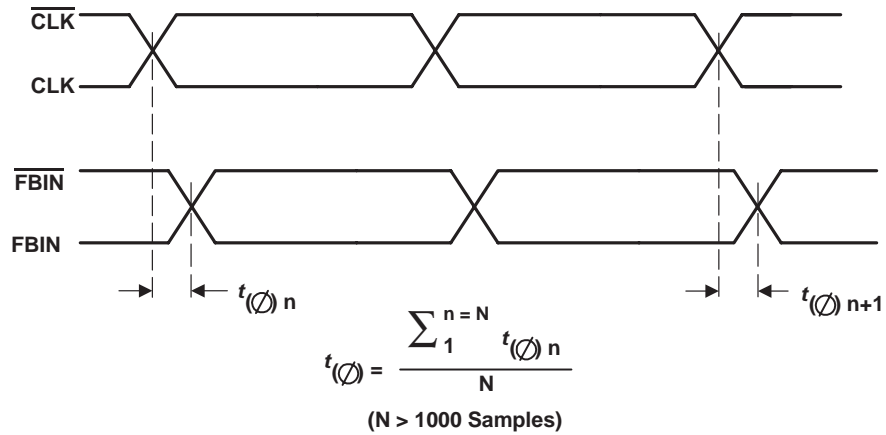


Figure 5. Phase Offset

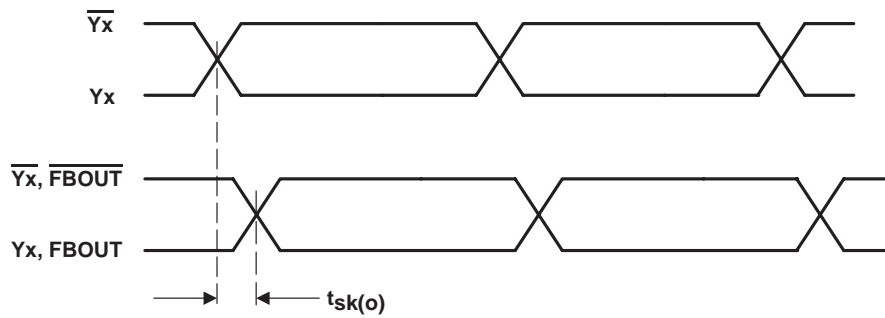


Figure 6. Output Skew

# CDCV857B, CDCV857BI

## 2.5-V PHASE-LOCK LOOP CLOCK DRIVER

SCAS689 – FEBRUARY 2003

### PARAMETER MEASUREMENT INFORMATION

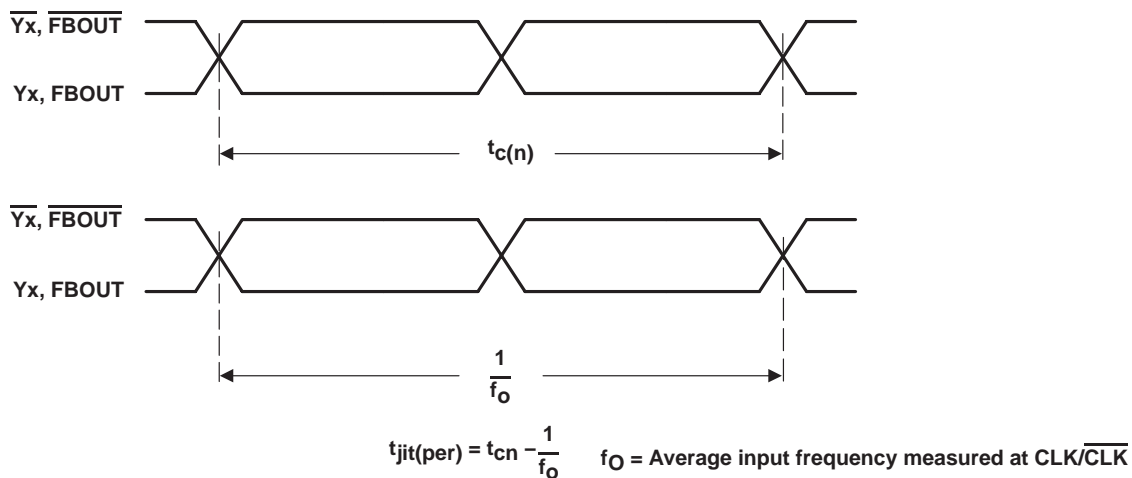


Figure 7. Period Jitter

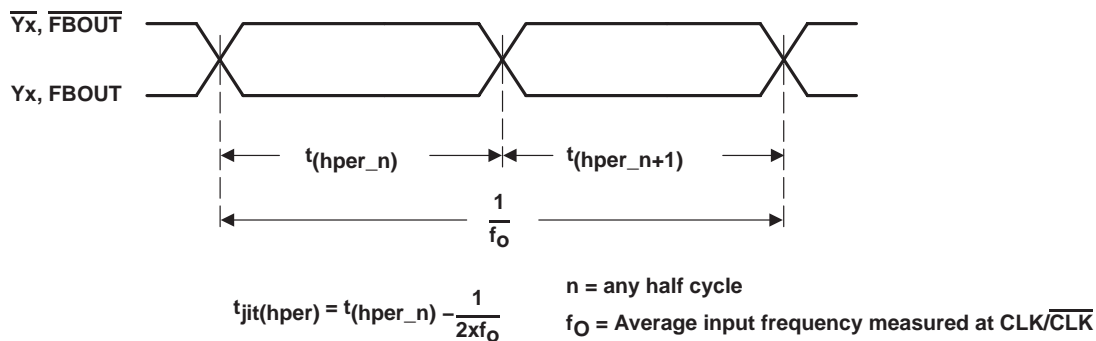


Figure 8. Half-Period Jitter

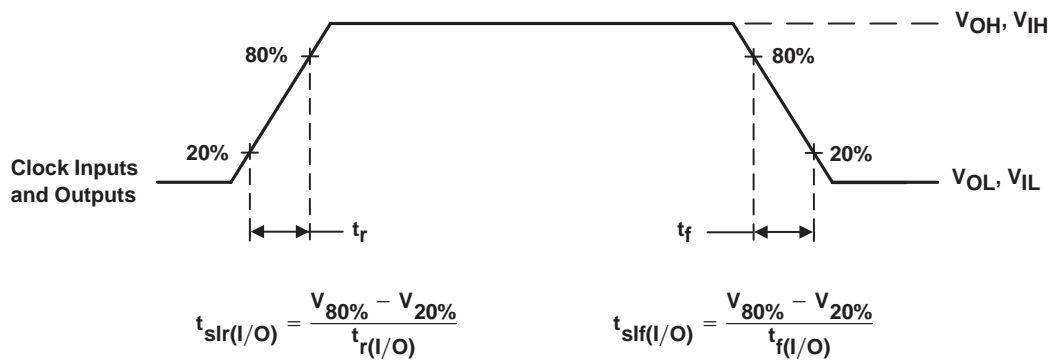


Figure 9. Input and Output Slew Rates

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CDCV857BDGG	ACTIVE	TSSOP	DGG	48	40	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CDCV857BDGGR	ACTIVE	TSSOP	DGG	48	2000	None	Call TI	Call TI
CDCV857BGQLR	ACTIVE	VFBGA	GQL	56	1000	None	Call TI	Level-2A-220C-4 WKS
CDCV857BIDGG	ACTIVE	TSSOP	DGG	48	40	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CDCV857BIDGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

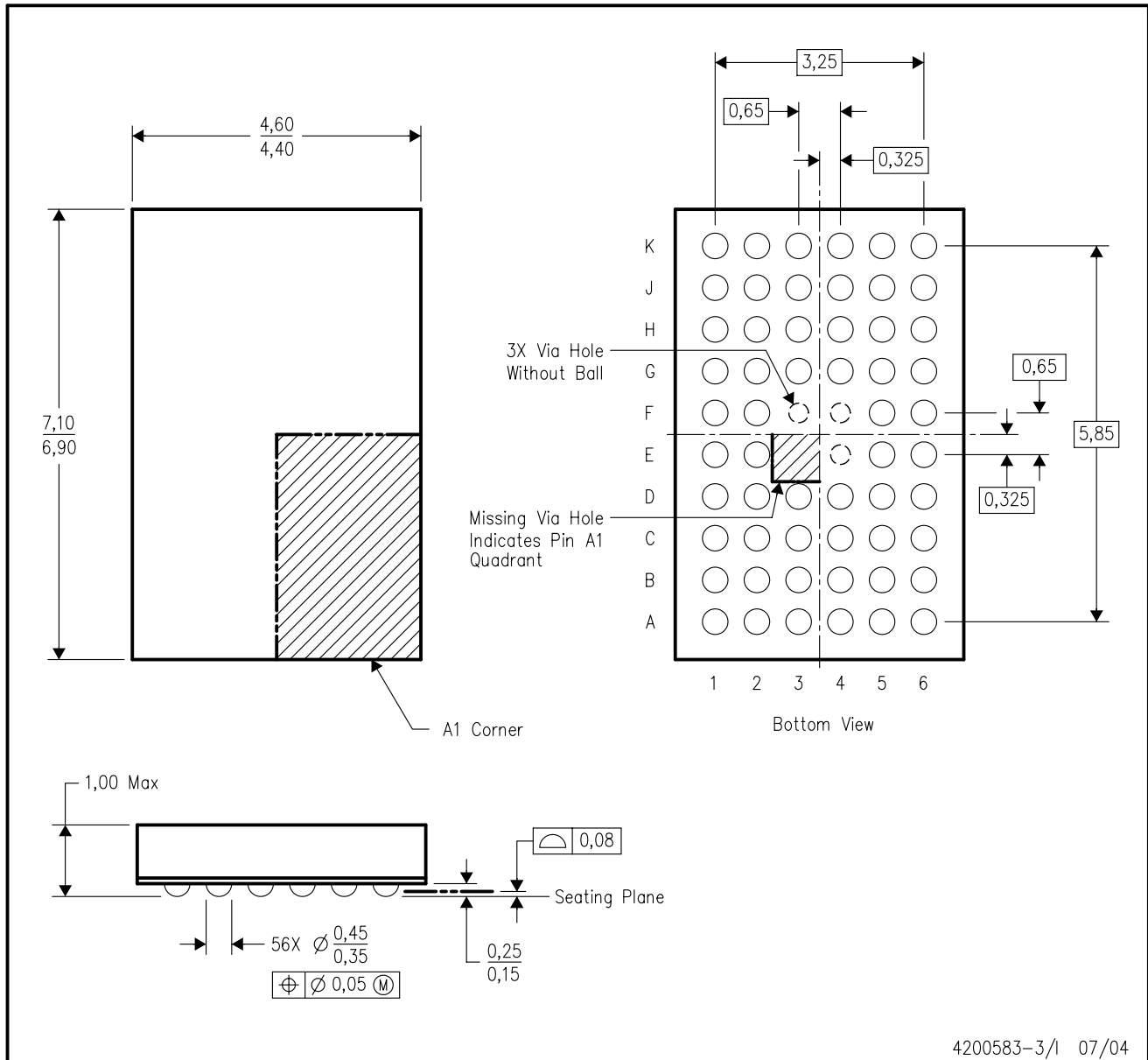
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



4200583-3/1 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BA.
  - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265