SBAS179C – DECEMBER 2000 – REVISED SEPTEMBER 2002

12-Bit, 70MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **DYNAMIC RANGE:**
  SNR: 64dB at 10MHz f_{IN}
  SFDR: 68dB at 10MHz f_{IN}
- **PREMIUM TRACK-AND-HOLD:**
  Low Jitter: 0.25ps rms
  Differential or Single-Ended Inputs
  Selectable Full-Scale Input Range
- **FLEXIBLE CLOCKING:**
  Differential or Single-Ended
  Accepts Sine or Square Wave Clocking Down to 0.5Vp-p
  Variable Threshold Level

APPLICATIONS

- **BASESTATION WIDEBAND RADIOS: CDMA, GSM, TDMA, 3G, AMPS, and NMT**
- **TEST INSTRUMENTATION**
- **CCD IMAGING**

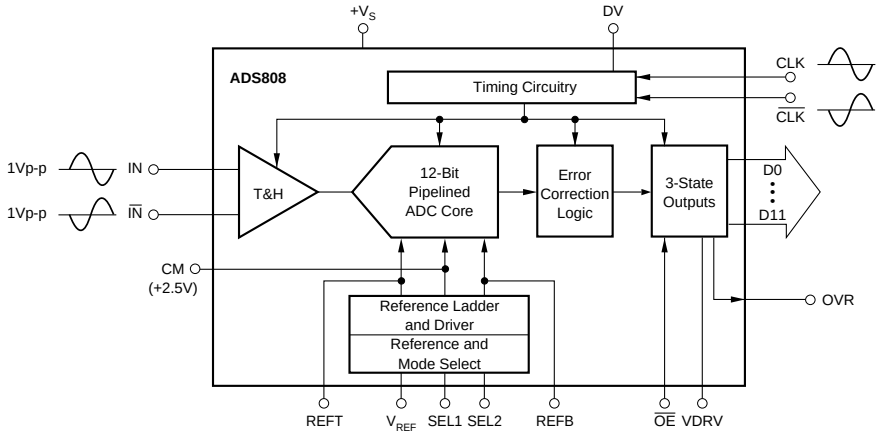
DESCRIPTION

The ADS808 is a high-dynamic range, 12-bit, 70MHz, pipelined Analog-to-Digital Converter (ADC). It includes a high-bandwidth linear track-and-hold that has a low jitter of only 0.25ps rms, leading to excellent SNR performance. The clock input can accept a low-level differential sine wave or square wave signal down to 0.5Vp-p, further improving the SNR performance. It also accepts a single-ended clock signal and has flexible threshold levels.

The ADS808 has a 2Vp-p differential input range (1Vp-p • 2 inputs) for optimum signal-to-noise ratio. The differential operation gives the lowest even-order harmonic components. A lower input voltage of 1.5Vp-p or 1Vp-p can also be selected using the internal references, further optimizing SFDR. Alternatively, a single-ended input range can be used by tying the $\overline{IN}$ input to the common-mode voltage, if desired.

The ADS808 also provides an over-range flag that indicates when the input signal has exceeded the converter's full-scale range. This flag can also be used to reduce the gain of the front-end signal conditioning circuitry. It also employs digital error-correction techniques to provide excellent differential linearity for demanding imaging applications. The ADS808 is available in a small TQFP-48 PowerPAD™ thermally enhanced package.

PowerPAD is a registered trademark of Texas Instruments.



ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6V
Analog Input	(–0.3V) to ($+V_S$ + 0.3V)
Logic Input	(–0.3V) to ($+V_S$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS808Y	TQFP-48	PHP	–40°C to +85°C	ADS808Y	ADS808Y/250	Tape and Reel, 250
"	"	"	"	"	ADS808Y/2K	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, differential input range = 1V to 2V, sampling rate = 70MHz, V_S = +5V, and internal reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS808Y MIN	ADS808Y TYP	ADS808Y MAX	UNITS
RESOLUTION			12 Tested		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85		°C
ANALOG INPUT					
Standard Differential Input Range	(1Vp-p • 2, +10dBm)	1		2	V
Single-Ended Input Voltage	1Vp-p	2		3	V
Common-Mode Voltage			2.5		V
Optional Input Ranges	Selectable		1Vp-p or 1.5Vp-p		V
Analog Input Bias Current			1		µA
Track-Mode Input Bandwidth	–3dBFS		1		GHz
Input Impedance	Static, No Clock		1.25 || 9		MΩ || pF
CONVERSION CHARACTERISTICS					
Sample Rate		1M		70M	Samples/s
Data Latency			5		Clk Cyc
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 1MHz			±0.7	+1.7/–1.0	LSB
No Missing Codes			Tested		
Integral Nonlinearity Error, f = 1MHz			±4.0	±7.0	LSBs
Spurious-Free Dynamic Range[1]					
f = 1MHz			72		dBFS[2]
f = 10MHz		65	68		dBFS
2-Tone Intermodulation Distortion					
f_{IN} = 19.4MHz and 20.4MHz (–7dB each tone)			–77		dBFS
Signal-to-Noise Ratio (SNR)					
f = 1MHz			64.5		dBFS
f = 10MHz			64		dBFS
Signal-to-(Noise + Distortion) (SINAD)					
f = 2.2MHz			64		dBFS
f = 10MHz			63		dBFS
Output Noise	Input AC-Grounded		0.3		LSBs rms
Aperture Delay Time			3		ns
Aperture Jitter			0.25		ps rms
Over-Voltage Recovery Time			2		ns
Full-Scale Step Acquisition Time			5		ns
DIGITAL INPUTS					
Logic Family			+3V/+5V Logic Compatible CMOS		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High-Level Input Current (V_{IN} = 5V)[3]				100	µA
Low-Level Input Current (V_{IN} = 0V)				±10	µA
High-Level Input Voltage		+2.0			V
Low-Level Input Voltage				+1.0	V
Input Capacitance			5		pF

ELECTRICAL CHARACTERISTICS (Cont.)

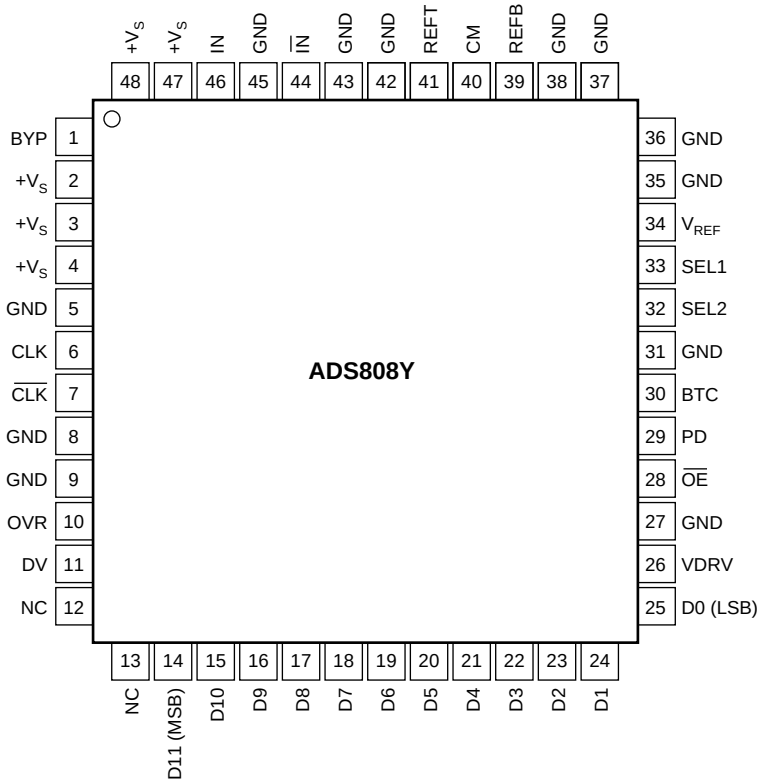
At T_A = full specified temperature range, differential input range = 1V to 2V, sampling rate = 70MHz, V_S = +5V, and internal reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS808Y MIN	ADS808Y TYP	ADS808Y MAX	UNITS
DIGITAL OUTPUTS					
Logic Family			+3V/+5V Compatible CMOS		
Logic Coding			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA to 1.6mA)	VDRV = 3V			+0.2	V
High Output Voltage, (I_{OH} = 50µA to 0.5mA)		+2.5			V
Low Output Voltage, (I_{OL} = 50µA to 1.6mA)	VDRV = 5V			+0.2	V
High Output Voltage, (I_{OH} = 50µA to 1.6mA)		+2.5			V
3-State Enable Time	$\overline{OE}$ = LOW		20	40	ns
3-State Disable Time	$\overline{OE}$ = HIGH		2	10	ns
Output Capacitance			5		pF
ACCURACY (Internal Reference, = 2V, Unless Otherwise Noted)					
Zero Error (Midscale)	at 25°C		0.5		%FS
Zero Error Drift (Midscale)			12		ppm/°C
Gain Error[4]	at 25°C		±1.5		%FS
Gain Error Drift[4]			38		ppm/°C
Gain Error[5]	at 25°C		±0.75		%FS
Gain Error Drift[5]			20		ppm/°C
Power-Supply Rejection of Gain	ΔV_S = ±5%		68		dB
Internal REF Tolerance ($V_{REFP} - V_{REFN}$)	Deviation from Ideal		±10	±40	mV
Reference Input Resistance			660		Ω
POWER-SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating		142		mA
Output Driver Supply Current (VDRV)			10		mA
Power Dissipation: VDRV = 5V	Internal Reference		740		mW
VDRV = 3V	Internal Reference		720	770	mW
VDRV = 5V	External Reference		720		mW
VDRV = 3V	External Reference		700		mW
Power Down	Operating		20		mW
Thermal Resistance, θ_{JA}					
TQFP-48			28.8		°C/W

NOTES: (1) Spurious-Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full-Scale. (3) A 50kΩ pull-down resistor is inserted internally. (4) Includes internal reference. (5) Excludes internal reference.

PIN DIAGRAM

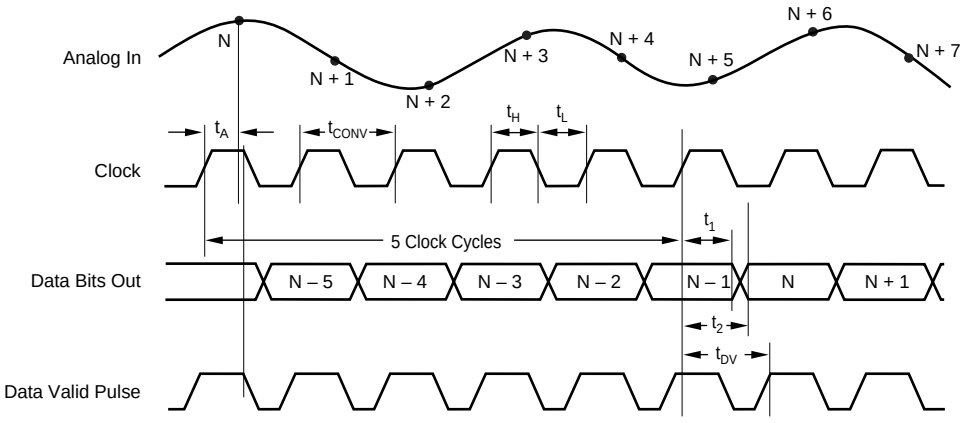
Top View **TQFP**



PIN DESCRIPTIONS

PIN	I/O	DESIGNATOR	DESCRIPTION	PIN	I/O	DESIGNATOR	DESCRIPTION
1		BYP	Bypass Point	26		VDRV	Output Bit Driver Voltage Supply
2		$+V_S$	Supply Voltage	27		GND	Ground
3		$+V_S$	Supply Voltage	28	I	$\overline{OE}$	Output Enable: HI = High Impedance;
4		$+V_S$	Supply Voltage				LO or Floating: Normal Operation
5		GND	Ground	29	I	PD	Power Down: HI = Power Down; LO = Normal
6	I	CLK	Clock Input	30	I	BTC	HI = Binary Two's Complement;
7	I	$\overline{CLK}$	Complementary Clock Input				LO = Straight Binary
8		GND	Ground	31		GND	Ground
9		GND	Ground	32		SEL2	Reference Select 2: See Table on Page 5.
10	O	OVR	Over-Range Indicator	33		SEL1	Reference Select 1: See Table on Page 5.
11	O	DV	Data Valid Pulse: HI = Data Valid	34		V_{REF}	Internal Reference Voltage
12		NC	No Connection	35		GND	Ground
13		NC	No Connection	36		GND	Ground
14	O	D11	Data Bit 11, (MSB)	37		GND	Ground
15	O	D10	Data Bit 10	38		GND	Ground
16	O	D9	Data Bit 9	39		REFB	Bottom Reference Voltage Bypass
17	O	D8	Data Bit 8	40		CM	Common-Mode Voltage (mid-scale)
18	O	D7	Data Bit 7	41		REFT	Top Reference Voltage Bypass
19	O	D6	Data Bit 6	42		GND	Ground
20	O	D5	Data Bit 5	43		GND	Ground
21	O	D4	Data Bit 4	44	I	$\overline{IN}$	Complementary Analog Input
22	O	D3	Data Bit 3	45		GND	Ground
23	O	D2	Data Bit 2	46	I	IN	Analog Input
24	O	D1	Data Bit 1	47		$+V_S$	Supply Voltage
25	O	D0	Data Bit 0, (LSB)	48		$+V_S$	Supply Voltage

TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN(1)	TYP	MAX(1)	UNITS
t_{CONV}	Convert Clock Period	14.3		1µs	ns
t_H	Clock Pulse HIGH	7	$t_{CONV}/2$		ns
t_L	Clock Pulse LOW	7	$t_{CONV}/2$		ns
t_A	Aperture Delay		4.6	6.1	ns
t_{DV}	Data Valid Pulse Delay(2)		11.5	14	ns
t_1	Data Hold Time, C_L = 0pF	4	5		ns
t_2	New Data Delay Time, C_L = 15pF max		9	11	ns

NOTES: (1) Timing values based on simulation at room temperature. Min/Max values provided for design estimation only. (2) Measured from the 50% point of the clock to the time when signals are within valid logic levels.

REFERENCE AND FULL-SCALE RANGE SELECT

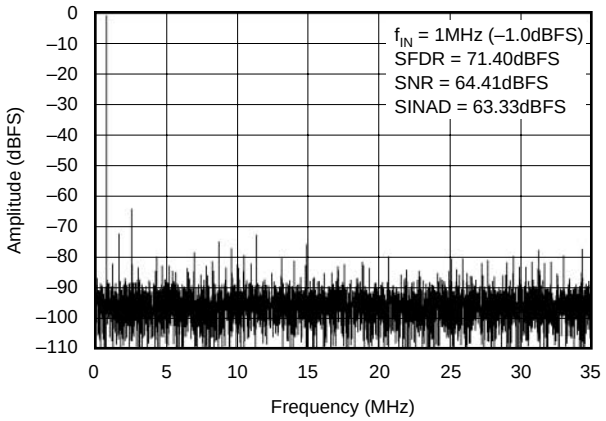
DESIRED FULL-SCALE RANGE	SEL1	SEL2	INTERNAL V_{REF}
1Vp-p	V_{REF}	GND	0.5V
1.5Vp-p	GND	$+V_S$	0.75V
2Vp-p	GND	GND	1.0V

NOTE: For external reference operation, tie V_{REF} to $+V_S$ and apply REFT and REFB externally. Internal voltage buffer of CM is powered up. The full-scale input range is equal to 2x the reference value (REFT – REFB).

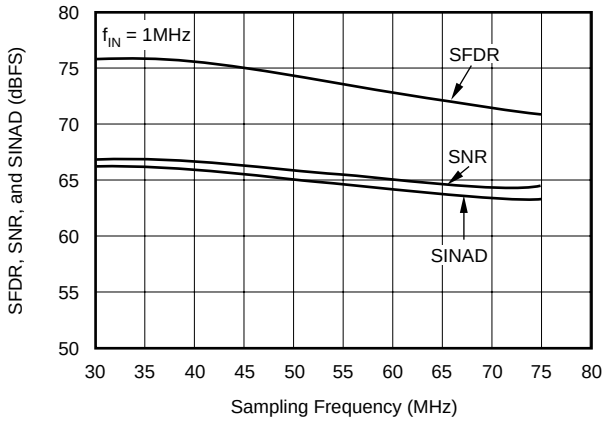
TYPICAL CHARACTERISTICS

At T_A = full specified temperature range, differential input range = 1V to 2V, sampling rate = 70MHz, and internal reference, unless otherwise noted.

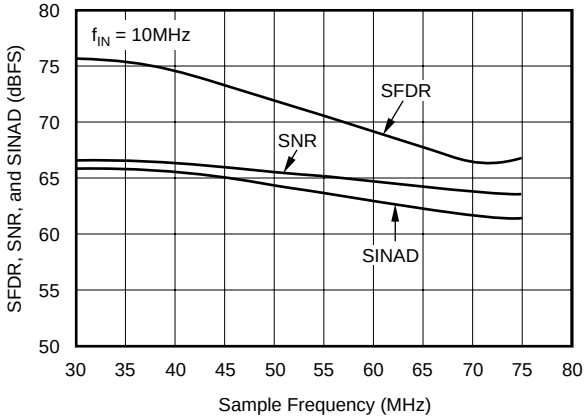
SPECTRAL PERFORMANCE
(Differential, 2Vp-p)



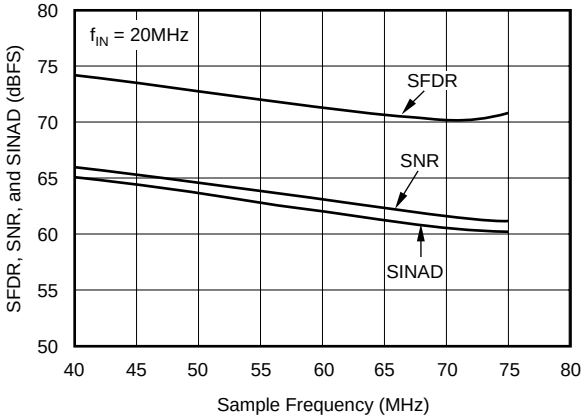
DYNAMIC PERFORMANCE
vs SAMPLING FREQUENCY



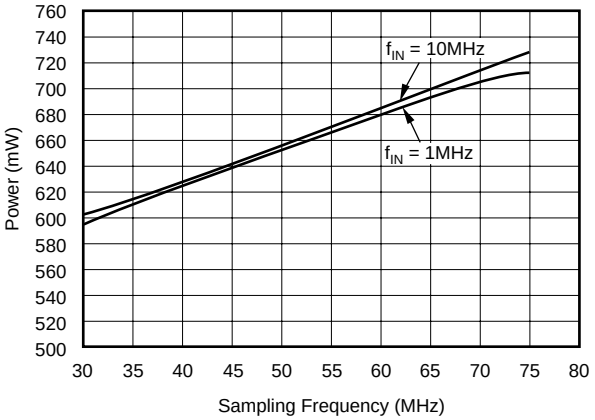
DYNAMIC PERFORMANCE
vs SAMPLING FREQUENCY
(2Vp-p, Differential)



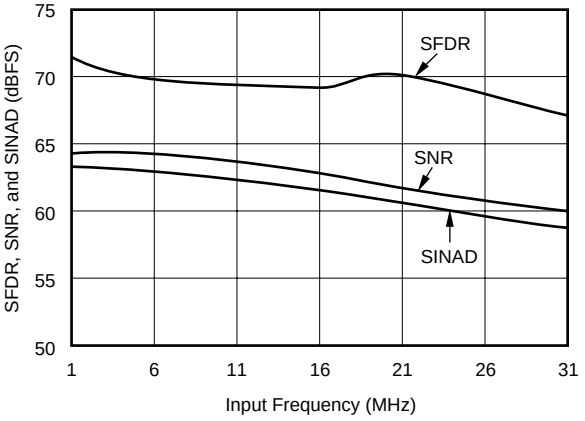
DYNAMIC PERFORMANCE
vs SAMPLING FREQUENCY
(2Vp-p, Differential)



TOTAL POWER vs SAMPLING FREQUENCY



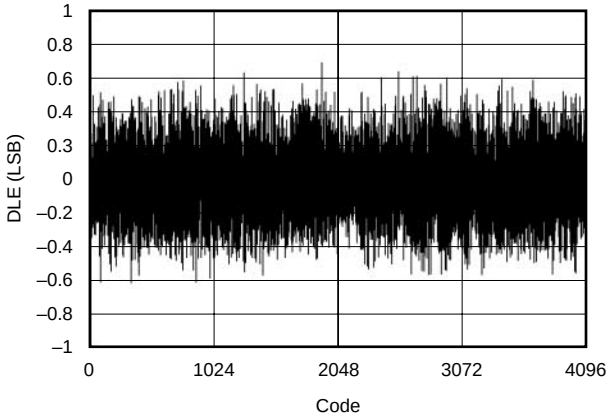
DYNAMIC PERFORMANCE vs INPUT FREQUENCY



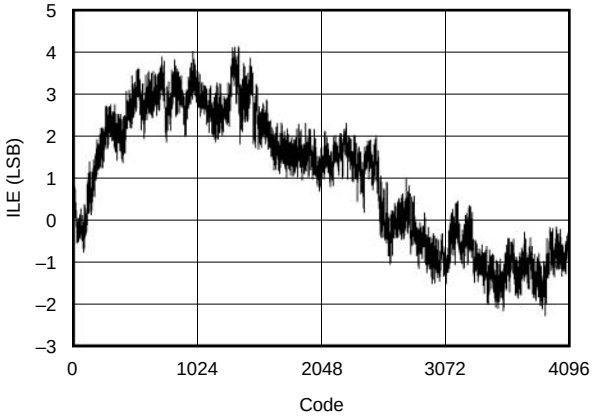
TYPICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, differential input range = 1V to 2V, sampling rate = 70MHz, and internal reference, unless otherwise noted.

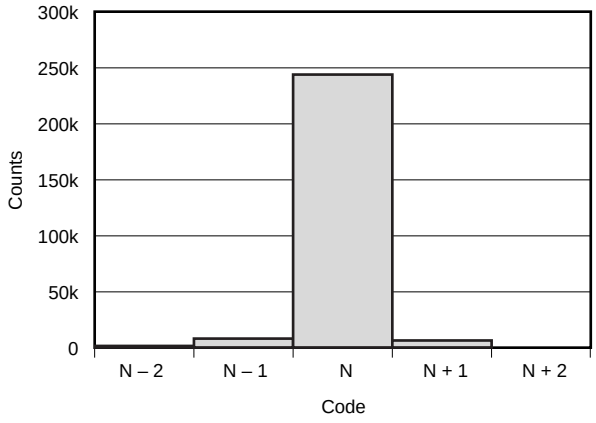
DIFFERENTIAL LINEARITY ERROR



INTEGRAL LINEARITY ERROR



OUTPUT NOISE HISTOGRAM
(2Vp-p, Grounded Input)



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS808 is a high-speed, high-performance, CMOS ADC built with a fully differential, 9-stage pipeline architecture. Each stage contains a low-resolution quantizer and digital error-correction logic, ensuring excellent differential linearity and no missing codes at the 12-bit level. The conversion process is initiated by a rising edge of the external convert clock. Once the signal is captured by the input track-and-hold amplifier, the bits are sequentially encoded starting with the MSB. This process results in a data latency of five clock cycles, after which the output data is available as a 12-bit parallel word either coded in a straight binary or binary two's complement format.

The analog input of the ADS808 consists of a differential track-and-hold circuit, as shown in Figure 1. The differential topology produces a high level of AC-performance at high sampling rates. It also results in a very high usable input bandwidth that is especially important for IF, or undersampling applications. Both inputs (IN, $\overline{IN}$) require external biasing up to a common-mode voltage that is typically at the mid-supply level ($+V_S/2$). This is because the on-resistance of the CMOS switches is lowest at this voltage, minimizing the effects of the signal dependent nonlinearity of R_{ON}. The track-and-hold circuit can also convert a single-ended input signal into a fully differential signal for the quantizer. For ease of use, the ADS808 incorporates a selectable voltage reference, a versatile clock input, and a logic output driver designed to interface to 3V or 5V logic.

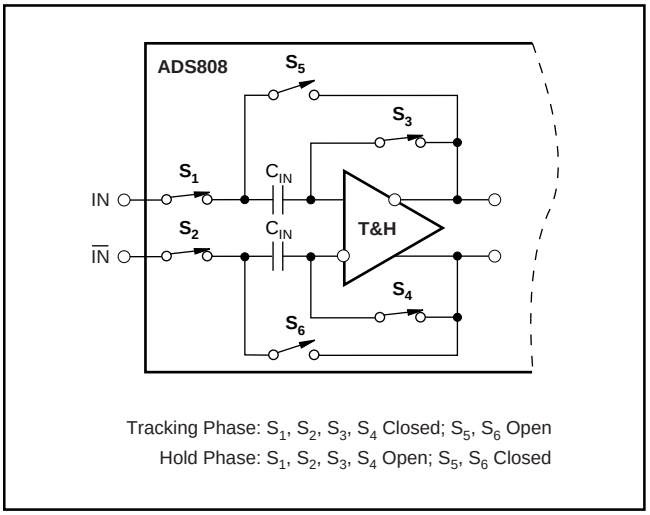


FIGURE 1. Simplified Circuit of Input Track-and-Hold Amplifier.

DRIVING THE ANALOG INPUTS

Types of Applications

The analog input of the ADS808 can be configured in various ways and driven with different circuits, depending on the application and the desired level of performance. Offering a high dynamic range at high input frequencies, the ADS808 is particularly suited for communication systems that digitize wideband signals. Features on the ADS808, like the input range selector or the option of an external reference, provide the needed flexibility to accommodate a wide range of applications. In any case, the analog interface/driver requirements should be carefully examined before selecting the appropriate circuit configuration. The circuit definition should include considerations on the input frequency spectrum and amplitude, single-ended versus differential driver configuration, as well as the available power supplies.

Differential versus Single-Ended

The ADS808 input structure allows it to be driven either single-ended or differentially. Differential operation of the ADS808 requires an input signal that consists of an in-phase and a 180° out-of-phase component simultaneously applied to the inputs (IN, $\overline{IN}$). Differential signals offer a number of advantages that in many applications will be instrumental in achieving the best harmonic performance of the ADS808:

- The signal amplitude is half of that required for the single-ended operation and is, therefore, less demanding to achieve while maintaining good linearity performance from the signal source.
- The reduced signal swing allows for more headroom of the interface circuitry and, therefore, a wider selection of the best suitable driver amplifier.
- Even-order harmonics are minimized.
- Improves the noise immunity based on the converter's common-mode input rejection.

For the single-ended mode, the signal is applied to one of the inputs while the other input is biased with a DC voltage to the required common-mode level. Both inputs are identical in terms of their impedance and performance except that applying the signal to the complementary input ($\overline{IN}$) instead of the IN-input will invert the orientation of the input signal relative to the output code. For example, if the input driver operates in inverting mode using $\overline{IN}$ as the signal input, it will restore the phase of the signal to its original orientation. Time-domain applications may benefit from a single-ended interface configuration and a reduced circuit complexity. Driving the ADS808 with a single-ended signal will result in a trade-off of the excellent distortion performance, while maintaining a good signal-to-noise ratio (SNR). The trade-off of the differential input configuration over the single-ended is its increase in circuit complexity. In either case, the selection of the driver amplifier should be such that the amplifier's performance will not degrade the A/D converter's performance.

Input Full-Scale Range versus Performance

Employing dual-supply amplifiers and AC-coupling will usually yield the best results. DC-coupling and/or single-supply amplifiers impose additional design constrains due to their headroom requirements, especially when selecting the 2Vp-p input range. The full-scale input range of the ADS808 is defined either by the settings of the reference select pins (SEL1, SEL2) or by an external reference voltage (see Table I).

By choosing between the three different signal input ranges, trade-offs can be made between noise and distortion performance. In order to maximize the SNR, which is important for time-domain applications, the 2Vp-p range may be selected. This range may also be used with low-level (–6dBFS to –40dBFS) to high-frequency inputs (multi-tone). The 1.5Vp-p range may be considered for achieving a combination of both low noise and distortion performance. Here the SNR number is typically 3dB down compared to the 2Vp-p range, while an improvement in the distortion performance of the driver amplifier may be realized due to the reduced output power level required. The third option, 1Vp-p FSR, may be considered mainly for applications requiring DC-coupling and/or single-supply operation of the driver and the converter.

Input Biasing (V_{CM})

The ADS808 operates from a single +5V supply, and requires each of the analog inputs to be externally biased to a common-mode voltage of typically +2.5V. This allows a symmetrical signal swing while maintaining sufficient headroom to either supply rail. Communication systems are usually AC-coupled in-between signal processing stages, making it convenient to set individual common-mode voltages and allow optimizing the DC operating point for each stage. Other applications (e.g., imaging) process only unipolar or DC-restored signals. In this case, the common-mode voltage may be shifted such that the full-input range of the converter is utilized.

It should be noted that the CM pin is internally buffered. However, it is recommended to keep the loading of this pin to a minimum to avoid an increase in the converter's nonlinearity. Additionally, the DC voltage at the CM pin is not exactly +2.5V, but is subject to the tolerance of the top and bottom references, as well as the resistor ladder.

Input Impedance

The input of the ADS808 is of a capacitive nature and the driving source needs to provide the slew current to charge or discharge the input sampling capacitor while the track-and-hold amplifier is in track mode (see Figure 1). This effectively results in a dynamic input impedance that is a function of the sampling frequency. Figure 2 depicts the differential input impedance of the ADS808 as a function of the input frequency.

For applications that use op amps to drive the ADC, it is recommended to add a series resistor between the amplifier output and the converter inputs. This will isolate the converter's capacitive input from the driving source and avoid gain peaking, or instability. Furthermore, it will create a 1st-order, low-pass filter in conjunction with the specified input capacitance of the ADS808. Its cutoff frequency can be adjusted even further by adding an external shunt capacitor from each signal input to ground. However, the optimum values of this RC network depend on a variety of factors, including the ADS808's sampling rate, the selected op amp, the interface configuration, and the particular application (time domain versus frequency domain). Generally, increasing the size of the series resistor and/or capacitor will improve the signal-to-noise ratio, however, depending on the signal source, large resistor values may reduce the harmonic distortion performance. In any case, the use of the RC network is optional but optimizing the values to adapt to the specific application is encouraged.

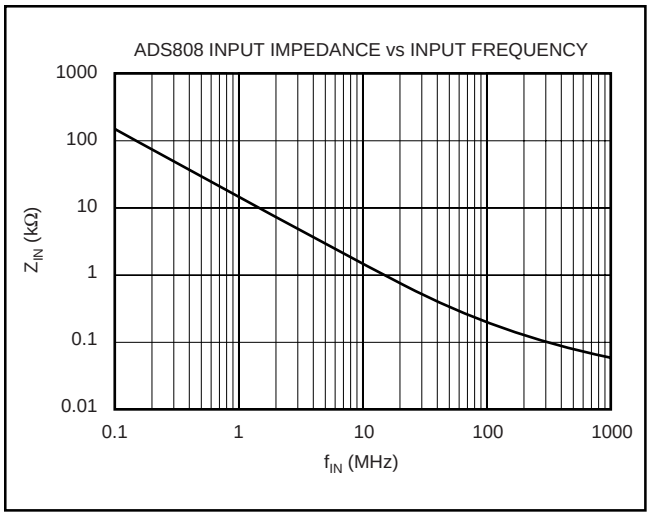


FIGURE 2. Differential Input Impedance versus Input Frequency.

INPUT DRIVER CONFIGURATIONS

The following section provides some principal circuit suggestions on how to interface the analog input signal to the ADS808. A first example of a typical analog interface circuit is shown in Figure 3. Here it is assumed that the input signal is already available in differential form (e.g., coming from a preceding mixer stage). The differential driver performs an impedance transformation as well as amplifying the signal to match the selected full-scale input range of the ADS808 (for example, 2Vp-p). The common-mode voltage (V_{CM}) for the converter input is established by connecting the inputs to the midpoints of the resistor divider. The input signal is AC-coupled through capacitors C_{IN} to the inputs of the converter that are set to a V_{CM} of approximately +2.5V_{DC}.

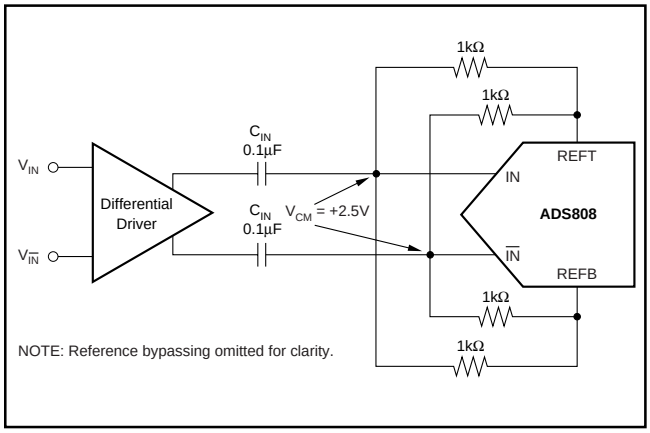


FIGURE 3. AC Coupling Allows for Easy DC Biasing of the ADS808 Inputs While the Input Signal is Applied by the Differential Input Driver.

Some differential driver circuits may allow setting an appropriate common-mode voltage directly at the driver input. This will simplify the interface to the ADS808 and eliminate the external biasing resistors and the coupling capacitors. Texas Instruments offers a line of fully differential high-speed amplifiers (refer to our web site at www.ti.com). The THS4150, for example, may be used for input frequencies from DC to approximately 10MHz, for which the part maintains good distortion performance, providing a 2Vp-p (max) output swing on ±5V supplies. Combining a differential driver circuit with a step-up transformer can lead to significant improvement of the distortion performance (see Figure 6).

Transformer Coupled Interface Circuits

If the application allows for AC-coupling, but requires a signal conversion from a single-ended source to drive the ADS808 differentially, using a transformer offers a number of advantages. As a passive component, it does not add to the total noise; plus by using a step-up transformer, further signal amplification can be realized. As a result, the signal swing out of the amplifier driving the transformer can be reduced, leading to more headroom for the amplifier and improved distortion performance.

One possible interface solution that uses a transformer is given in Figure 4. The input signal is assumed to be an Intermediate Frequency (IF) and bandpass filtered prior to the IF amplifier. Dedicated IF amplifiers, for example the RF2312 or MAR-6, are fixed-gain broadband amplifiers and feature a very high bandwidth, a low-noise figure, and a high intercept point at the expense of high quiescent currents of 50-120mA. The IF amplifier may be AC-coupled or directly connected to the primary side of the transformer.

A variety of miniature RF transformers are readily available from different manufacturers, i.e., Mini-Circuits, Coilcraft, or Trak. When choosing a selection, it is important to carefully examine the application requirements and determine the correct model, the desired impedance ratio, and frequency characteristics. Furthermore, the appropriate model must support the targeted distortion level and should not exhibit any core saturation at full-scale voltage levels. Since the transformer does not appreciably load the ladder, its center tap can be directly tied to the CM pin of the converter, as shown in Figure 4. The value of termination resistor (R_T) should be chosen to satisfy the termination requirements of the source impedance (R_S). It can be calculated using the equation $R_T = n^2 \bullet R_S$ to ensure proper impedance matching.

Transformer Coupled, Single-Ended to Differential Configuration

For applications in which the input frequency is limited to about 40MHz (e.g., baseband), the wideband, current-feedback, operational amplifier OPA685 may be used. As shown in Figure 5, the OPA685 is configured for the noninverting mode, amplifies the single-ended input signal, and drives the primary of an RF transformer. To maintain the very low distortion performance of the OPA685, it may be advantageous to reduce the full-scale input range (FSR) of the ADS808 from 2Vp-p to 1.5Vp-p or 1Vp-p (refer to the “Reference” section for details on selecting the converter’s full-scale range).

The circuit also shows the use of an additional RC low-pass filter placed in series with each converter input. This optional filter can be used to set a defined corner frequency and

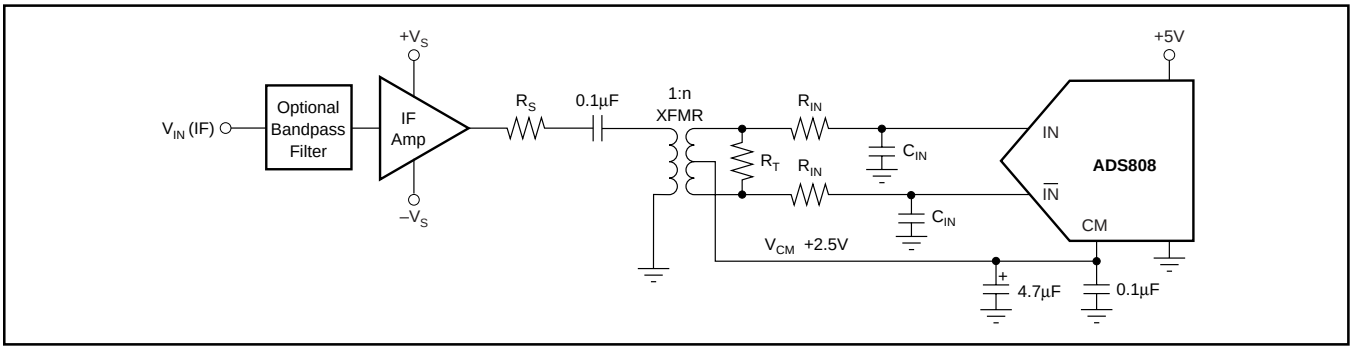


FIGURE 4. Driving the ADS808 with a Low Distortion RF Amplifier and a Transformer Suited for IF Sampling Applications.

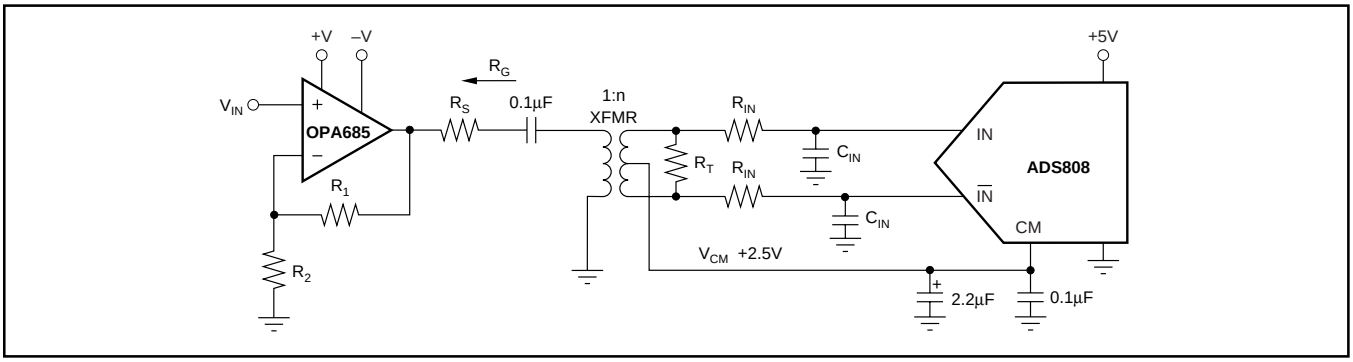


FIGURE 5. Converting a Single-Ended Input Signal into a Differential Signal Using a RF Transformer.

attenuate some of the wideband noise. The actual component values would need to be tuned for the individual application requirements. As a guideline, resistor values are typically in the range of 10Ω to 100Ω, capacitors in the range of 10pF to 200pF. In any case, the R_{IN} and C_{IN} values should have a low tolerance. This will ensure that the ADS808 sees closely matched source impedances.

AC-Coupled, Differential Interface with Gain

The interface circuit example presented in Figure 6 employs two OPA685s, (current-feedback op amps), optimized for gains of 8V/V or higher. The input transformer (T1) converts the single-ended input signal to a differential signal required at the amplifier's inverting inputs, that are tuned to provide a 50Ω impedance match to an assumed 50Ω source. To achieve the 50Ω input match at the primary of the 1:2 transformer, the secondary input must see a 200Ω load impedance. Both amplifiers are configured for the inverting mode resulting in close gain and phase matching of the differential signal. This technique, along with a highly symmetrical layout, is instrumental in achieving a substantial reduction of the 2nd-harmonic, while retaining excellent 3rd-order performance. A common-mode voltage (V_{CM}) is applied to the noninverting inputs of the OPA685. Additional series of 43.2Ω resistors isolate the output of the op amps from the capacitive load presented by the 22pF capacitors and the input capacitance of the ADS808. This 43.2Ω/22pF combination sets a pole at approximately 167MHz and rolls off some of the wideband noise.

REFERENCE

REFERENCE OPERATION

Integrated into the ADS808 is a bandgap reference circuit including some logic that provides a +0.5V, +0.75V, or +1V reference output by selecting the corresponding pin-strap configuration. Table I gives a complete overview of the possible reference options and pin configurations.

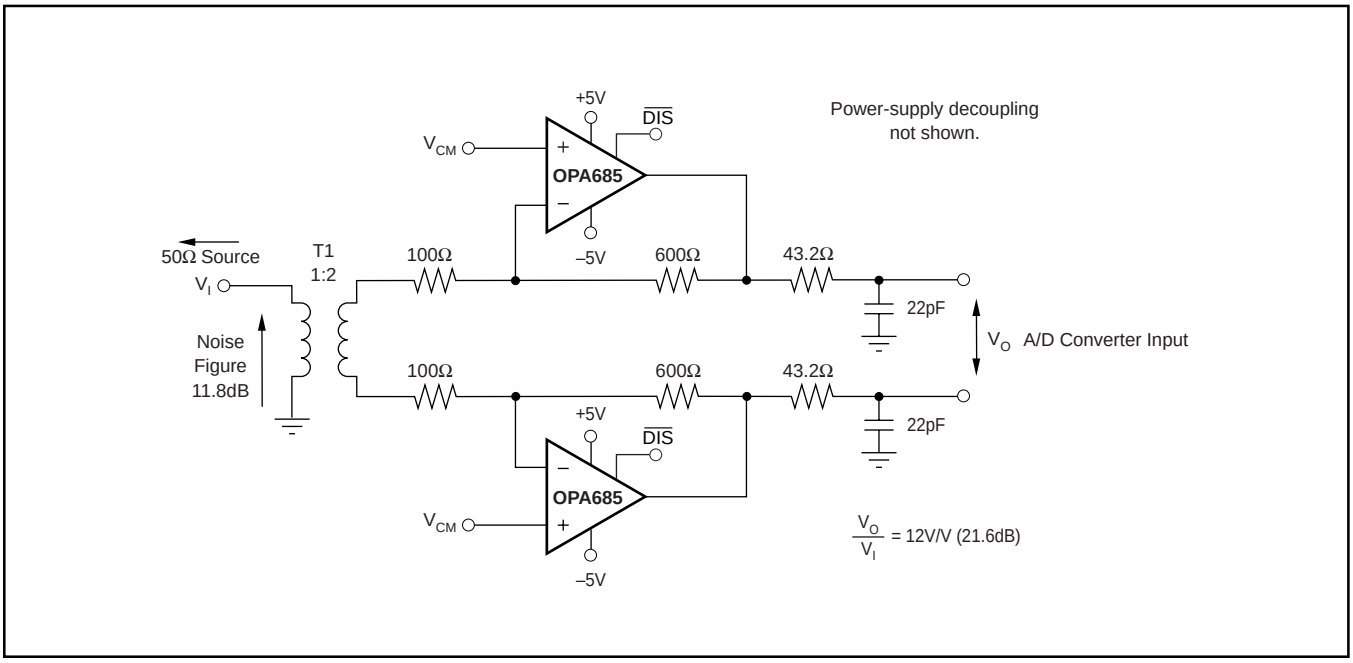


FIGURE 6. Wideband Differential A/D Converter Driver.

DESIRED FULL-SCALE RANGE, FSR (Differential)	CONNECT SEL1 (Pin 33)	CONNECT SEL2 (Pin 32)	VOLTAGE AT V_{REF} (Pin 34)	VOLTAGE AT REFT (Pin 41)	VOLTAGE AT REFB (Pin 39)
2Vp-p (+10dBm)	GND	GND	+1.0V	+3V	+2V
1.5Vp-p (+7.5dBm)	GND	$+V_S$	+0.75V	+2.875V	+2.125V
1Vp-p	V_{REF}	GND	+0.5V	+2.75V	+2.25V
External Reference	—	—	> +3.5V	+2.75V to +4.5V	+0.5V to +2.25V

TABLE I. Reference Pin Configurations and Corresponding Voltage on the Reference Pins.

Figure 7 shows the basic model of the internal reference circuit. The functional blocks are a 1V bandgap voltage reference, a selectable gain amplifier, the drivers for the top and bottom reference (REFT, REFB), and the resistive reference ladder. The ladder resistance measures approximately 660Ω between the REFT and REFB pin. The ladder is split into two equal segments, establishing a common-mode voltage at the ladder midpoint, labeled “CM”. The ADS808 requires solid bypassing for all reference pins to keep the effect of clock feedthrough to a minimum and to achieve the specified level of performance. Figure 7 also demonstrates the recommended decoupling scheme. All 0.1µF capacitors should be located as close to the pins as possible.

When operating the ADS808 from the internal reference, the effective full-scale input span for each of the inputs, IN and $\overline{IN}$, is determined by the voltages at REFT and REFB pins, given as:

Input Span (differential) = 2x (REFT – REFB), in Vp-p = $2 \bullet V_{REF}$

The top and bottom reference outputs may be used to provide up to 1mA (sink or source) of current to external circuits. Degradation of the differential linearity (DNL) and, consequently, of the dynamic performance of the ADS808 may occur if this limit is exceeded.

Using External References

For even more design flexibility, the ADS808 can be operated with an external reference.

The utilization of an external reference voltage may be considered for applications requiring higher accuracy, improved temperature stability, or a continuous adjustment of the converter’s full-scale range. Especially in multichannel applications, the use of a common external reference offers the benefit of improving the gain matching between converters. Selection between internal or external reference operation is controlled through the V_{REF} pin. The internal reference will become disabled if the voltage applied to the V_{REF} pin exceeds $+3.5V_{DC}$. Once selected, the ADS808 requires two reference voltages—a top-reference voltage applied to the REFT pin and a bottom-reference voltage applied to the REFB pin (see Table I). As illustrated in Figure 8, a micropower reference (REF1004) and a dual, single-supply amplifier may be used to generate a precision external reference. Note that the function of the range select pins, SEL1 and SEL2, are disabled while the converter is in external mode.

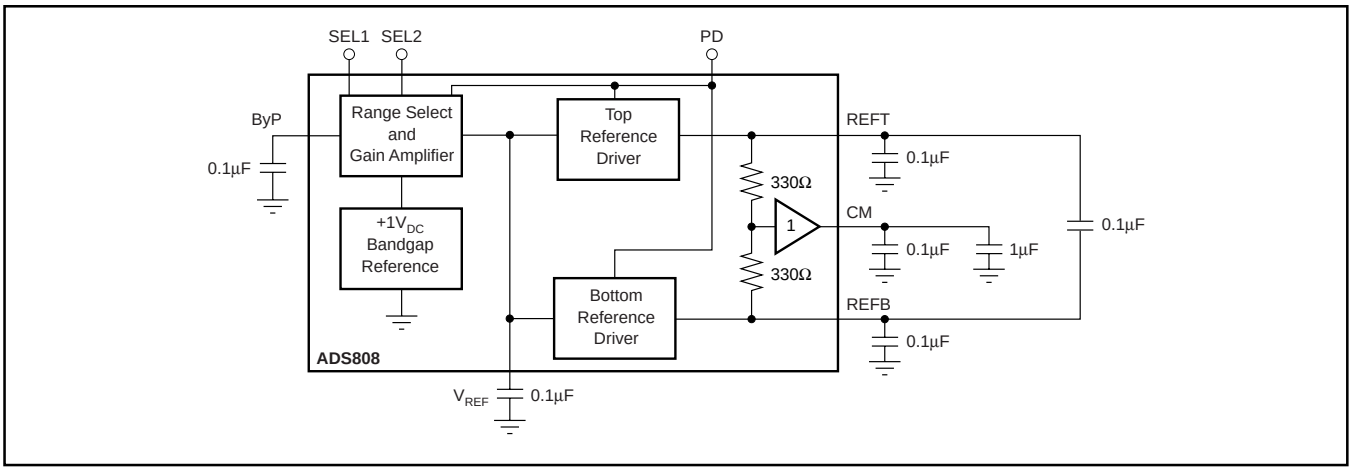


FIGURE 7. Internal Reference Circuit of the ADS808 and Recommended Bypass Scheme.

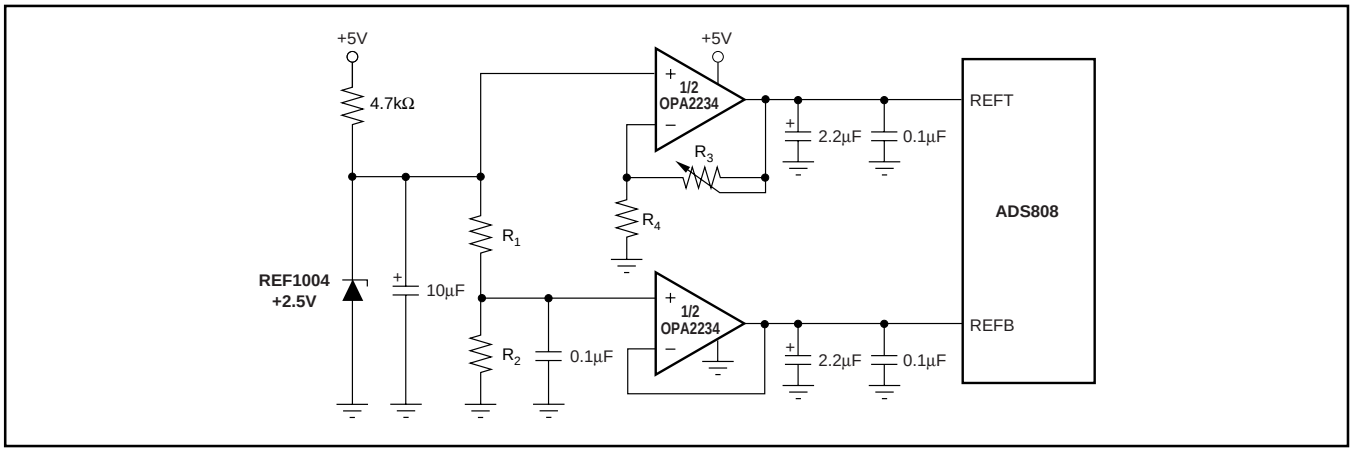


FIGURE 8. Example for an External Reference Circuit Using a Dual, Single-Supply Op Amp.

DIGITAL INPUTS AND OUTPUTS

CLOCK INPUT

Unlike most A/D converters, the ADS808 contains an internal clock conditioning circuitry. This enables the converter to adapt to a variety of application requirements and different clock sources. Some interface examples are given in the following section. With no input signal connected to either clock pin, the threshold level is set to about +1.6V by the on-chip resistive voltage divider, as shown in Figure 9. The parallel combination of R_1 || R_2 and R_3 || R_4 sets the input impedance of the clock inputs (CLK, $\overline{CLK}$) to approximately 2.7kΩ single-ended, or 5.4kΩ differentially. The associated ground-referenced input capacitance is approximately 5pF for each input. If a logic voltage other than the nominal +1.6V is desired, the clock inputs can be externally driven to establish an alternate threshold voltage.

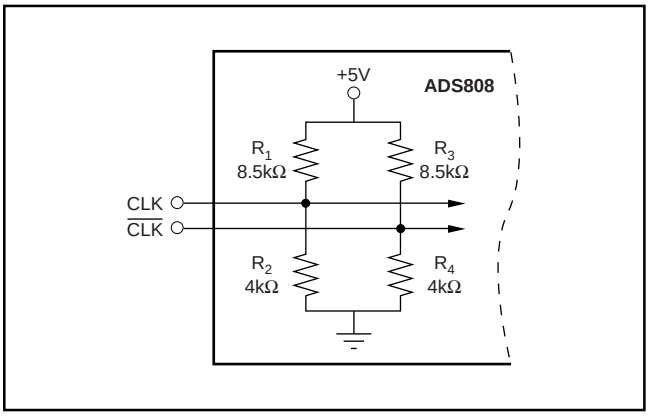


FIGURE 9. The Differential Clock Inputs are Internally Biased.

The ADS808 can be interfaced to standard TTL or CMOS logic and accepts 3V or 5V compliant logic levels. In this case, the clock signal should be applied to the CLK input, while the complementary clock input ($\overline{CLK}$) should be bypassed to ground by a low-inductance ceramic chip capacitor, as shown in Figure 10. Depending on the quality of the signal, inserting a series damping resistor may be beneficial to reduce ringing. When digitizing at high sampling rates (f_S > 50MHz), the clock should have a 50% duty cycle (t_H = t_L) to maintain a good distortion performance.

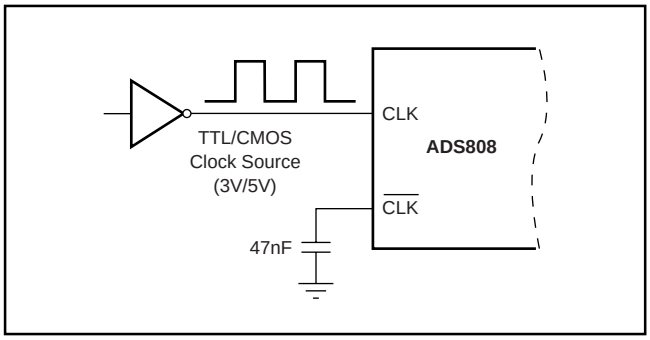


FIGURE 10. Single-Ended TTL/CMOS Clock Source.

Applying a single-ended clock signal will provide satisfactory results in many applications. However, unbalanced high-speed logic signals often introduce a high amount of disturbances, such as ringing or ground bouncing. Also, a high amplitude may cause the clock signal to have unsymmetrical rise and fall times, potentially effecting the converter's distortion performance. Proper termination practice and a clean PCB layout will help to keep those effects to a minimum.

To take full advantage of the excellent distortion performance of the ADS808, it is recommended to drive the clock inputs differentially. A low-level, differential clock improves the digital feedthrough immunity and minimizes the effect of modulation between the signal and the clock. Figure 11 illustrates a simple method of converting a square wave clock from single-ended to differential using a RF transformer. Small surface-mount transformers are readily available from several manufacturers (e.g.: model ADT1-1 by Mini-Circuits). A capacitor in series with the primary side may be inserted to block any DC voltage present in the signal. Since the clock inputs are self-biased, the secondary side connects directly to the two clock inputs of the converter.

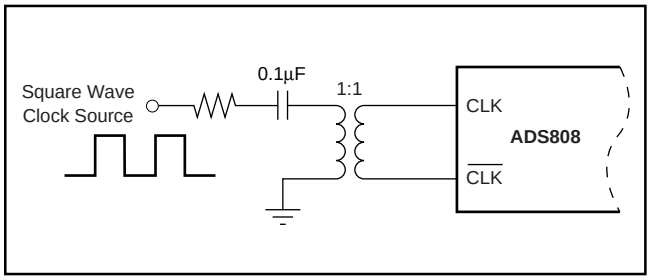


FIGURE 11. Connecting a Ground Referenced Square Wave Clock Source to the ADS808 Using a RF Transformer.

The clock inputs of the ADS808 can be connected in a number of ways. However, the best performance is obtained when the clock input pins are driven differentially. When operating in this mode, the clock inputs accommodate signal swings ranging from 2.5Vp-p down to 0.5Vp-p, differentially. This allows direct interfacing of clock sources, such as voltage-controlled crystal oscillators (VCXO) to the ADS808. The advantage here is the elimination of external logic usually necessary to convert the clock signal into a suitable logic (TTL or CMOS) signal, that otherwise would create an additional source of jitter. In any case, a very low-jitter clock is fundamental to preserving the excellent AC performance of the ADS808. The converter itself is specified for a very low 0.25ps (rms) jitter, characterizing the outstanding capability of the internal clock and track-and-hold circuitry. Generally, as the input frequency increases, the clock jitter becomes more dominant in maintaining a good SNR. This is particularly critical in IF sampling applications where the sampling frequency is lower than the input frequency (or

undersampling). The following equation can be used to calculate the achievable SNR for a given input frequency and clock jitter (t_{JA} in ps rms):

$$SNR = 20\log_{10}\frac{1}{(2\pi f_{IN} t_{JA})}$$

Depending on the nature of the clock source's output impedance, an impedance matching might become necessary. For this, a termination resistor (R_T) may be installed, as shown in Figure 12. To calculate the correct value for this resistor, consider the impedance ratio of the selected transformer and the differential clock input impedance of the ADS808, which is approximately 5.4kΩ.

It is not recommended to employ any type of differential TTL logic that suffers from mismatch in delay time and slew-rate leading to performance degradation. Alternatively, a low jitter ECL or PECL clock may be AC-coupled directly to the clock inputs using small (0.1µF) capacitors.

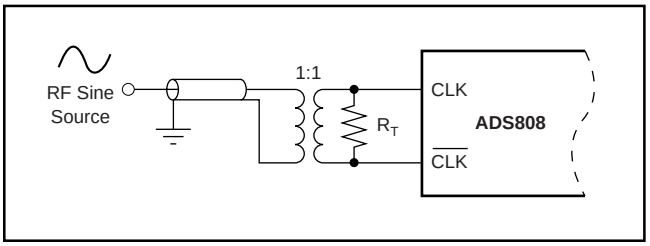


FIGURE 12. Applying a Sinusoidal Clock to the ADS808.

MINIMUM SAMPLING RATE

The pipeline architecture of the ADS808 uses the switched capacitor technique in its internal track-and-hold stages. With each clock cycle charges representing the captured signal level are moved within the ADC pipeline core. The high sampling speed necessitates the use of very small capacitor values. In order to hold the droop errors LOW, the capacitors require a minimum "refresh rate". Therefore, the sampling clock on the ADS808 should not drop below the specified minimum of 1MHz.

DATA OUTPUT FORMAT (BTC)

The ADS808 makes two data output formats available, either the "Straight Offset Binary" code (SOB) or the "Binary Two's Complement" code (BTC). The selection of the output coding is controlled through the BTC pin. Applying a logic HIGH will enable the BTC coding, while a logic LOW will enable the SOB code. The BTC output format is widely used to interface to microprocessors and such. The two code structures are identical with the exception that the MSB is inverted for the BTC format, as shown in Tables II and III.

SINGLE-ENDED INPUT (IN) (IN Biased to V_{CM})	STRAIGHT OFFSET BINARY (SOB)	BINARY TWO'S COMPLEMENT (BTC)
+FS – 1LSB ($\overline{IN}$ = CMV + FSR/2)	1111 1111 1111	0111 1111 1111
+1/2 FS	1100 0000 0000	0100 0000 0000
Bipolar Zero (IN = CMV)	1000 0000 0000	0000 0000 0000
–1/2 FS	0100 0000 0000	1100 0000 0000
–FS (IN = CMV – FSR/2)	0000 0000 0000	1000 0000 0000

TABLE II. Coding Table for Single-Ended Input Configuration with IN Tied to the Common-Mode Voltage (CMV).

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)	BINARY TWO'S COMPLEMENT (BTC)
+FS – 1LSB (IN = +3V, $\overline{IN}$ = +2V)	1111 1111 1111	0111 1111 1111
+1/2 FS	1100 0000 0000	0100 0000 0000
Bipolar Zero (IN = $\overline{IN}$ = CMV)	1000 0000 0000	0000 0000 0000
–1/2 FS	0100 0000 0000	1100 0000 0000
–FS (IN = +2V, $\overline{IN}$ = +3V)	0000 0000 0000	1000 0000 0000

TABLE III. Coding Table for Differential Input Configuration and 2Vp-p Full-Scale Input Range.

Output Enable ($\overline{OE}$)

The digital outputs of the ADS808 can be set to high impedance (tri-state), exercising the output enable pin ($\overline{OE}$). For normal operation, this pin must be at a logic LOW potential, while a logic HIGH voltage disables the outputs. Even though this function effects the output driver stage, the threshold voltages for the $\overline{OE}$ pin do not depend on the output driver supply (VDRV), but are fixed (see the Digital Inputs of the Electrical Characteristics table). Operating the $\overline{OE}$ function dynamically (i.e., high speed multiplexing) should be avoided, as it will corrupt the conversion process.

Power Down (PD)

A power-down of the ADS808 is initiated by taking the PD pin HIGH. This shuts down portions within the converter and reduces the power dissipation to about 20mW. The remaining active blocks include the internal reference, ensuring a fast reactivation time. During power-down, data in the converter pipeline will be lost and new valid data will be subject to the specified pipeline delay. In case the PD pin is not used, it should be tied to ground or a logic LOW level.

Over-Range Indicator (OVR)

If the analog input voltage exceeds the full-scale range set by the reference voltages, an over-range condition exists. The ADS808 incorporates a function, that monitors the input voltage and detects any such out-of-range condition. The current state can be read at the over-range indicator pin (OVR).

This output is LOW when the input voltage is within the defined input range. It will change to HIGH if the applied signal exceeds the full-scale range. It should be noted that the OVR output is updated along with the data output, corresponding to the particular sampled analog input voltage. Therefore, the OVR data is subject to the same pipeline delay as the digital data (5 clock cycles).

Output Loading

It is recommended to keep the capacitive loading on the data output lines as low as possible, preferably below 15pF. Higher capacitive loading will cause larger dynamic currents to flow as the digital outputs are changing. For example, with a typical output slew-rate of 0.8V/ns and a total capacitive loading of 10pF (including 4pF output capacitance, 5pF input capacitance of external logic buffer, and 1pF pc-board parasitics), a bit transition can cause a dynamic current of 10pF • 0.8V/1ns = 8mA. Those high current surges can feed back to the analog portion of the ADS808 and adversely affect the performance. External buffers, or latches, close to the converter's output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS808 from any digital activities on the bus from coupling back high-frequency noise.

POWER SUPPLIES

When defining the power supplies for the ADS808, is it highly recommended to consider linear supplies instead of switching types. Even with good filtering, switching supplies may radiate noise that could interfere with any high-frequency input signal and cause unwanted modulation products. At its full conversion rate of 70MHz, the ADS808 requires typically 170mA of supply current on the +5V supply ($+V_S$). Note that this supply voltage should stay within a 5% tolerance. The ADS808 does not require separate analog and digital supplies, but only one single +5V supply to be connected to all its $+V_S$ pins. This is with the exception of the output driver supply pin, denoted VDRV (see the following section).

Digital Output Driver Supply (VDRV)

A dedicated supply pin, denoted VDRV, provides power to the logic output drivers of the ADS808, and may be operated with a supply voltage in the range of +3.0V to +5.0V. This can simplify interfacing to various logic families, in particular low-voltage CMOS. It is recommended to operate the ADS808 with a +3.0V supply voltage on VDRV. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line that may affect the AC performance of the converter. The analog supply ($+V_S$) and driver supply (VDRV) may be tied together, with a ferrite bead or inductor between the supply pins. Each of the these supply pins must be bypassed separately with at least one 0.1µF ceramic chip capacitor, forming a pi-filter. The recommended operation for the ADS808 is +5V for the $+V_S$ pins and +3.0V on the output driver pin (VDRV).

LAYOUT AND DECOUPLING CONSIDERATIONS

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Achieving optimum performance with a fast sampling converter, like the ADS808, requires careful attention to the pc-board layout to minimize the effect of board parasitics and optimize component placement.

A multilayer board usually ensures best results and allows convenient component placement.

The ADS808 should be treated as an analog component with the $+V_S$ pins connected to clean analog supplies. This will ensure the most consistent results, since digital supplies often carry a high level of switching noise that could couple into the converter and degrade the performance. As mentioned previously, the driver supply pins (VDRV) should also be connected to a low-noise supply. Supplies of adjacent digital circuits may carry substantial current transients. The supply voltage must be thoroughly filtered before connecting to the VDRV supply of the converter. All ground connections on the ADS808 are internally bonded to the metal flag (bottom of package) that forms a large ground plane. All ground pins should directly connect to an analog ground plane that covers the pc-board area under the converter.

Due to its high sampling frequency, the ADS808 generates high-frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. If not sufficiently bypassed, this will add noise to the conversion process. Figure 13 shows the recommended supply decoupling scheme for the ADS808. All $+V_S$ pins may be connected together and bypassed with a combination of 10nF to 0.1µF ceramic chip capacitors (0805, low ESR) and a 10µF tantalum tank capacitor. A similar approach may be used on the driver supply pins, VDRV. In order to minimize the lead and trace inductance, the capacitors should be located as close to the supply pins as possible. Where double-sided component mounting is allowed, they are best placed directly under the package. In addition, larger bipolar decoupling capacitors (2.2µF to 10µF), effective at lower frequencies, should also be used on the main supply pins. They can be placed on the pc-board in proximity (< 0.5") of the ADC.

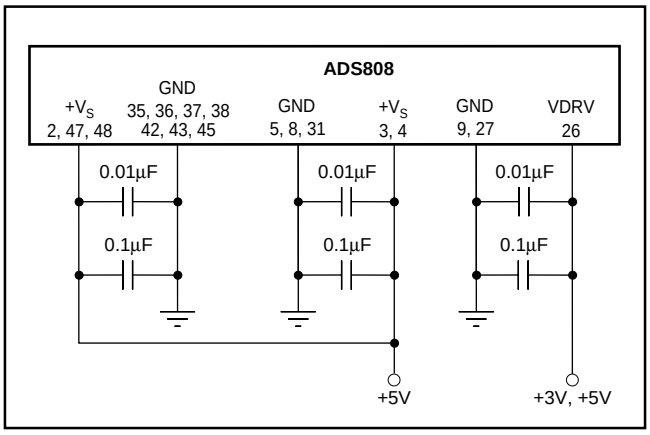


FIGURE 13. Recommended Supply Decoupling Scheme.

If the analog inputs to the ADS808 are driven differentially, it is especially important to optimize towards a highly symmetrical layout. Small trace length differences may create phase shifts compromising a good distortion performance. For this reason, the use of two single op amps (rather than one dual amplifier) enables a more symmetrical layout and a better match of parasitic capacitances. The pin orientation of the ADS808 package follows a “flow-through” design with the analog inputs located on one side of the package while the digital outputs are located on the opposite side of the quad-flat package. This provides a good physical isolation between the analog and digital connections. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog portion.

Also, try to match trace length for the differential clock signal (if used) to avoid mismatches in propagation delays. Single-ended clock lines must be short and should not cross any other signal traces.

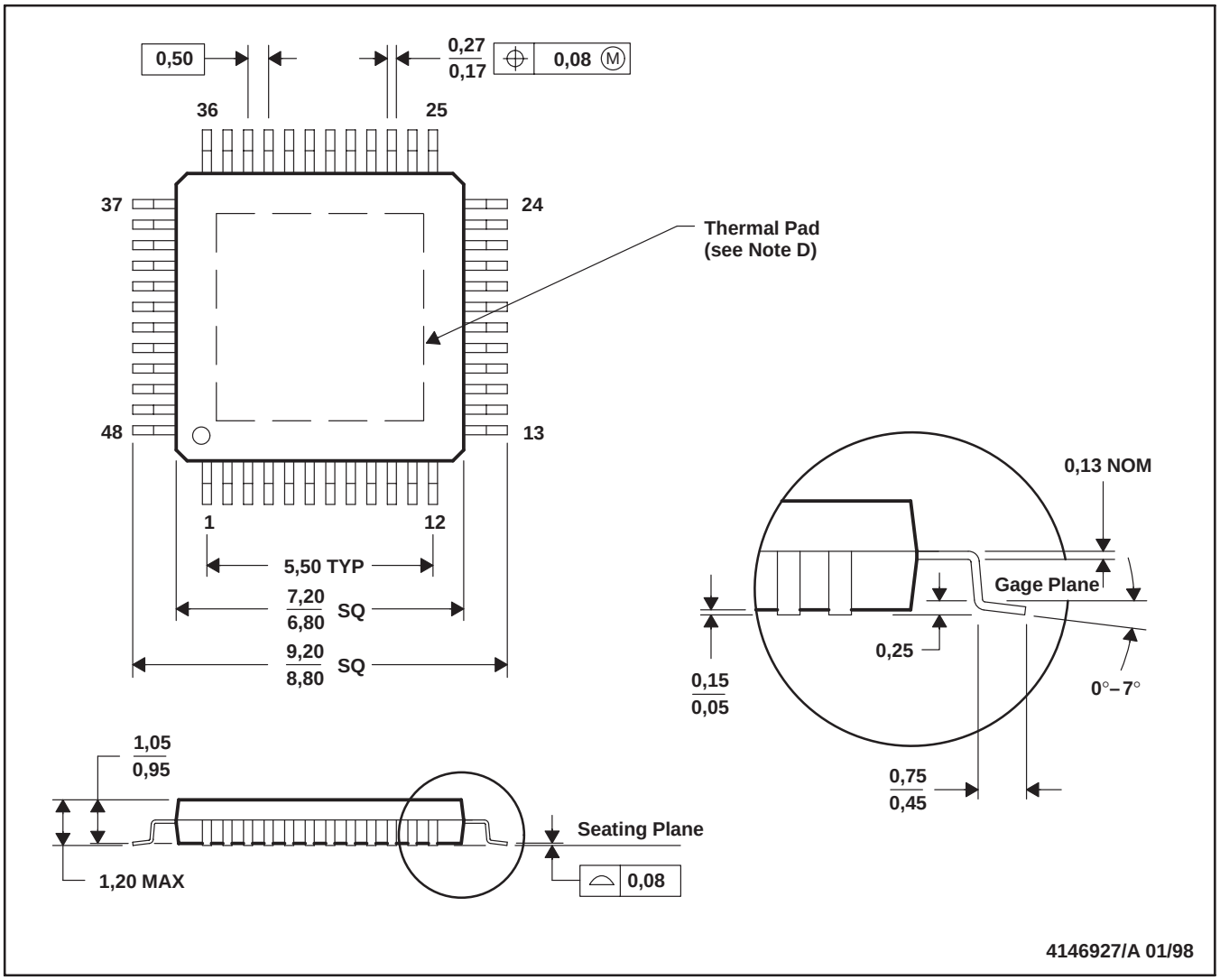
Short-circuit traces on the digital outputs will minimize capacitive loading. Trace length should be kept short to the receiving gate (< 2") with only one CMOS gate connected to one digital output. If possible, the digital data outputs should be buffered (with a 74LCX571, for example). Dynamic performance may also be improved with the insertion of series resistors at each data output line. This sets a defined time constant and reduces the slew rate that would otherwise flow, due to the fast edge rate. The resistor value may be chosen to result in a time constant of 15% to 25% of the used data rate.

LAYOUT OF PCB WITH PowerPAD THERMALLY ENHANCED PACKAGES

The ADS808 is housed in a 48-lead PowerPAD thermally enhanced package. To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. Please refer to SLMA004 PowerPAD brief “PowerPAD Made Easy” on our web site at www.ti.com, which addresses the specific considerations required when integrating a PowerPAD package into the PCB design. For more detailed information, including thermal modeling and repair procedures, please see SLMA002 technical brief “PowerPAD Thermally Enhanced Package” (www.ti.com).

PACKAGE DRAWING

PHP (S-PQFP-G48) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
ADS808Y/250	ACTIVE	HTQFP	PHP	48	250
ADS808Y/2K	ACTIVE	HTQFP	PHP	48	2000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265