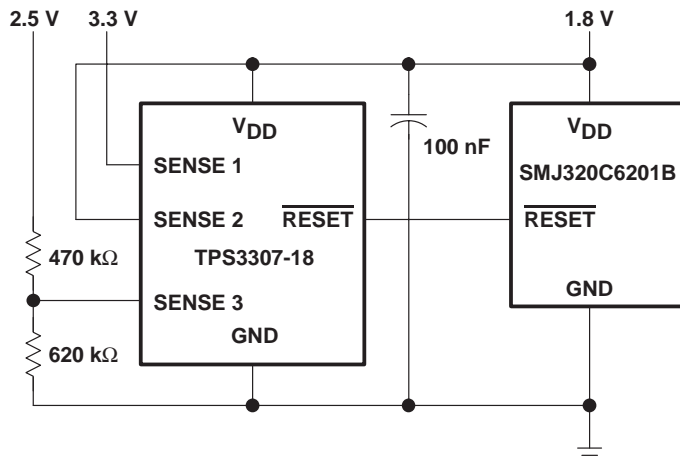


- Qualified for Military Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Triple Supervisory Circuits for DSP and Processor-Based Systems
- Power-On Reset Generator with Fixed Delay Time of 200 ms, No External Capacitor Needed
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40  $\mu$ A
- Supply Voltage Range . . . 2 V to 6 V
- Defined  $\overline{\text{RESET}}$  Output from  $V_{\text{DD}} \geq 1.1$  V
- CDIP-8 and LCCC-20 Packages
- Temperature Range . . .  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$

### typical applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers TPS3307-18 and SMJ320C6201B.



**Figure 1. Applications Using the TPS3307-18**

### description

The TPS3307-18 is a micropower supply voltage supervisor designed for circuit initialization primarily in automotive DSP and processor-based systems, which require more than one supply voltage.

The TPS3307-18 is designed for monitoring three independent supply voltages: 3.3 V/1.8 V/adj,. The adjustable SENSE input allows the monitoring of any supply voltage >1.25 V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

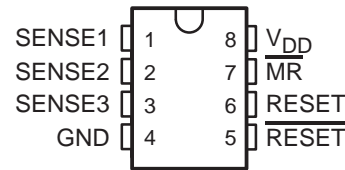
**PRODUCTION DATA** information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



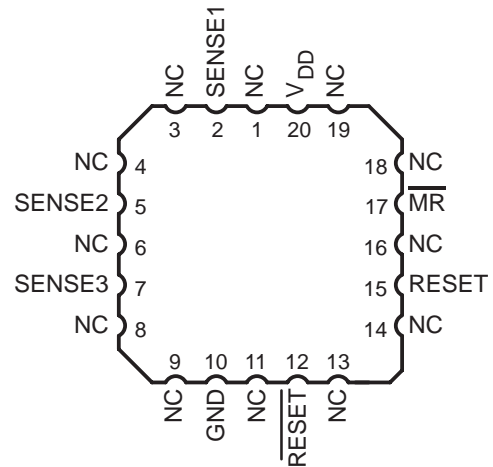
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

#### JG PACKAGE (TOP VIEW)



#### FK PACKAGE (TOP VIEW)



NC – No internal connection

- Military applications using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls

# TPS3307-18M TRIPLE PROCESSOR SUPERVISORS

SGLS133A – JANUARY 2003 – REVISED DECEMBER 2003

## description (continued)

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE			THRESHOLD VOLTAGE (TYP)		
	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3 V	1.8 V	User defined	2.93 V	1.68 V	1.25 V†

† The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{DD}$  becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps  $\overline{\text{RESET}}$  active as long as SENSEn remain below the threshold voltage  $V_{IT+}$ .

An internal timer delays the return of the  $\overline{\text{RESET}}$  output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{d\text{typ}} = 200$  ms, starts after all SENSEn inputs have risen above the threshold voltage  $V_{IT+}$ . When the voltage at any SENSE input drops below the threshold voltage  $V_{IT-}$ , the  $\overline{\text{RESET}}$  output becomes active (low) again.

The TPS3307-18 incorporates a manual reset input,  $\overline{\text{MR}}$ . A low level at  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to become active. In addition to the active-low  $\overline{\text{RESET}}$  output, the TPS3307-18 includes an active-high RESET output.

## ORDERING INFORMATION

TA	PACKAGE‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	Ceramic Dual In Line (JG)	TPS3307-18MJGB	TPS3307-18MJGB
	Leadless Ceramic Chip Carrier (FK)	TPS3307-18MFKB	TPS3307-18MFKB

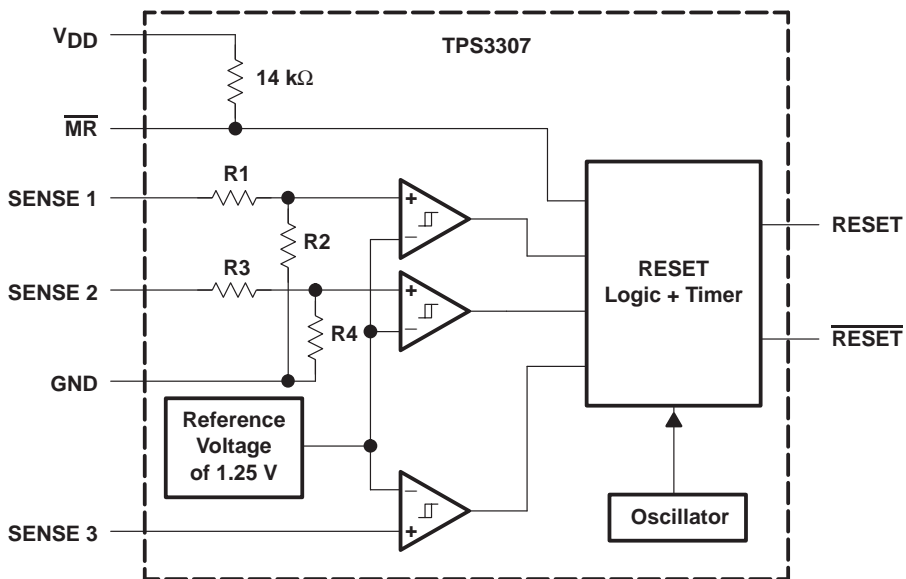
‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION/TRUTH TABLES

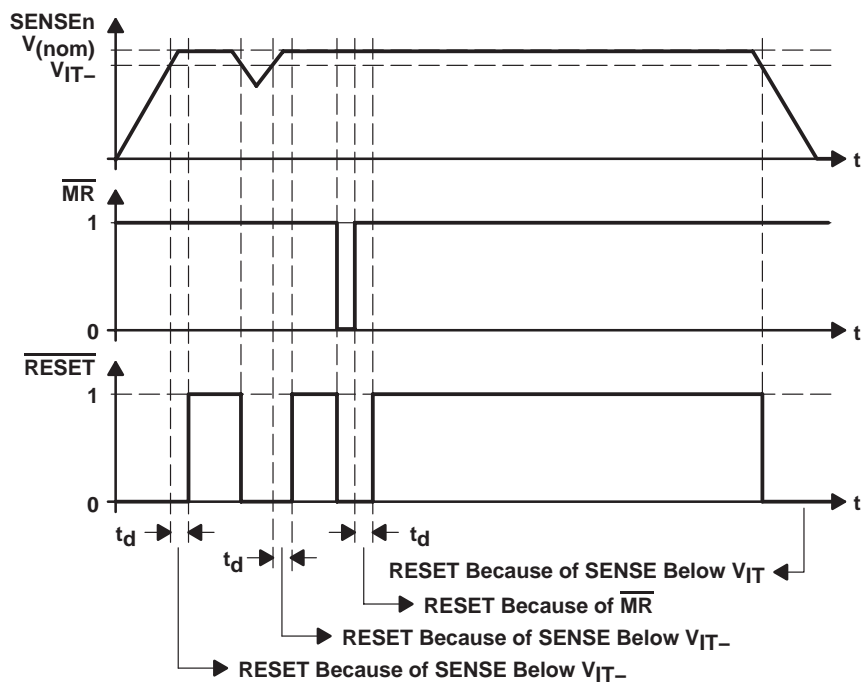
$\overline{\text{MR}}$	SENSE1 > $V_{IT1}$	SENSE2 > $V_{IT2}$	SENSE3 > $V_{IT3}$	$\overline{\text{RESET}}$	RESET
L	X	X	X	L	H
H	0	0	0	L	H
H	0	0	1	L	H
H	0	1	0	L	H
H	0	1	1	L	H
H	1	0	0	L	H
H	1	0	1	L	H
H	1	1	0	L	H
H	1	1	1	H	L

X = Don't care

functional block diagram



timing diagram



# TPS3307-18M

## TRIPLE PROCESSOR SUPERVISORS

SGLS133A – JANUARY 2003 – REVISED DECEMBER 2003

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note1)	7 V
All other pins (see Note 1)	-0.3 V to 7 V
Maximum low output current, $I_{OL}$	5 mA
Maximum high output current, $I_{OH}$	-5 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	$\pm 20$ mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	-55°C to 125°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Soldering temperature	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than  $t = 1000$  h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
JG	1 W	6.25 mW/°C	719 mW	625 mW	375 mW
FK	1.39 W	11.58 mW/°C	869 mW	695 mW	232 mW

### recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$	2	6	V
Input voltage at $\overline{MR}$ and SENSE3, $V_I$	0	$V_{DD}+0.3$	V
Input voltage at SENSE1 and SENSE2, $V_I$	0	$(V_{DD}+0.3)V_{IT}/1.25V$	V
High-level input voltage at $\overline{MR}$ , $V_{IH}$	$0.7 \times V_{DD}$		V
Low-level input voltage at $\overline{MR}$ , $V_{IL}$	$0.3 \times V_{DD}$		V
Input transition rise and fall rate at $\overline{MR}$ , $\Delta t/\Delta V$	50		ns/V
Operating free-air temperature range, $T_A$	-55	125	°C



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 2 V to 6 V, I <sub>OH</sub> = -20 μA	V <sub>DD</sub> - 0.2V			V	
		V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = -2 mA	V <sub>DD</sub> - 0.4V				
		V <sub>DD</sub> = 6 V, I <sub>OH</sub> = -3 mA	V <sub>DD</sub> - 0.4V				
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 2 V to 6 V, I <sub>OL</sub> = 20 μA	0.2			V	
		V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA	0.4				
		V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 3 mA	0.4				
Power-up reset voltage (see Note 2)		V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 20 μA	0.4			V	
V <sub>IT-</sub>	Negative-going input threshold voltage (see Note 3)	VSENSE3	V <sub>DD</sub> = 2 V to 6 V	1.22	1.25	1.29	V
		VSENSE2		1.64	1.68	1.73	V
		VSENSE1		2.86	2.93	3.02	
V <sub>hys</sub>	Hysteresis at VSENSEn input	V <sub>IT-</sub> = 1.25 V	2	10	30	mV	
		V <sub>IT-</sub> = 1.68 V	2	15	40		
		V <sub>IT-</sub> = 2.93 V	3	30	60		
I <sub>H</sub>	High-level input current	$\overline{\text{MR}}$	MR = 0.7 × V <sub>DD</sub> , V <sub>DD</sub> = 6 V		-130	-180	μA
		SENSE1	VSENSE1 = V <sub>DD</sub> = 6 V		5	8	
		SENSE2	VSENSE2 = V <sub>DD</sub> = 6 V		6	9	
		SENSE3	VSENSE3 = V <sub>DD</sub>		-25	25	
I <sub>L</sub>	Low-level input current	$\overline{\text{MR}}$	MR = 0 V, V <sub>DD</sub> = 6 V		-430	-600	μA
		SENSEn	VSENSE1,2,3 = 0 V		-1	1	
I <sub>DD</sub>	Supply current				40	μA	
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = 0 V to V <sub>DD</sub>		10		pF	

NOTES: 2. The lowest supply voltage at which RESET becomes active. t<sub>r</sub>, V<sub>DD</sub> ≥ 15 μs/V  
 3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.

# TPS3307-18M

## TRIPLE PROCESSOR SUPERVISORS

SGLS133A – JANUARY 2003 – REVISED DECEMBER 2003

timing requirements at  $V_{DD} = 2\text{ V to }6\text{ V}$ ,  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_w$	Pulse width	$V_{SENSEnL} = V_{IT-} - 0.2\text{ V}$ , $V_{SENSEnH} = V_{IT+} + 0.2\text{ V}$	6	10		$\mu\text{s}$
		$V_{IH} = 0.7 \times V_{DD}$ , $V_{IL} = 0.3 \times V_{DD}$	100	150		ns

switching characteristics at  $V_{DD} = 2\text{ V to }6\text{ V}$ ,  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d$	Delay time	$V_I(\text{SENSEn}) \geq V_{IT+} + 0.2\text{ V}$ , $\overline{\text{MR}} \geq 0.7 \times V_{DD}$ , See timing diagram	140	200	280	ms
$t_{PHL}$	Propagation (delay) time, high-to-low level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ $\overline{\text{MR}}$ to $\overline{\text{RESET}}$		200	600	ns
$t_{PLH}$	Propagation (delay) time, low-to-high level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ $\overline{\text{MR}}$ to $\overline{\text{RESET}}$				
$t_{PHL}$	Propagation (delay) time, high-to-low level output	$\text{SENSEn}$ to $\overline{\text{RESET}}$		1	5	$\mu\text{s}$
$t_{PLH}$	Propagation (delay) time, low-to-high level output	$\text{SENSEn}$ to $\overline{\text{RESET}}$				



TYPICAL CHARACTERISTICS

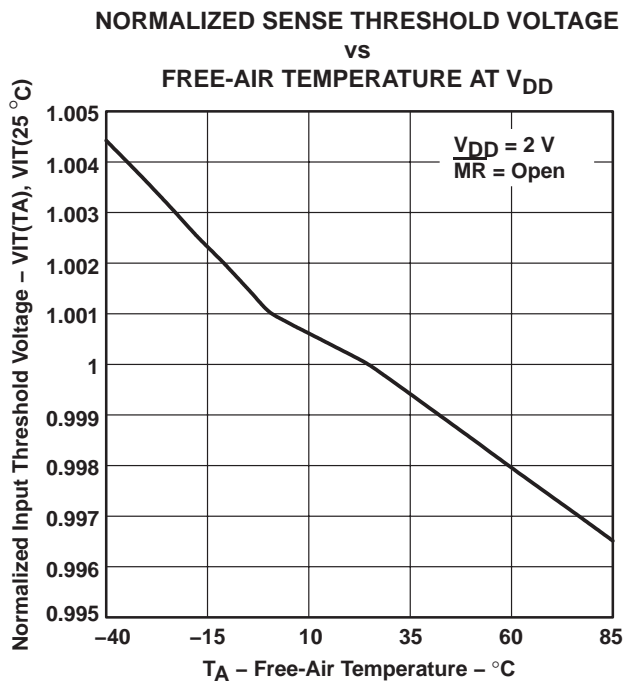


Figure 2

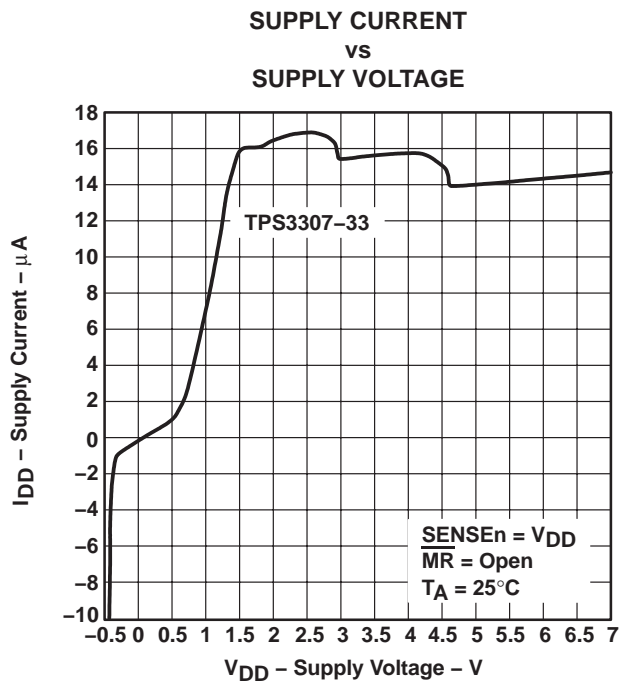


Figure 3

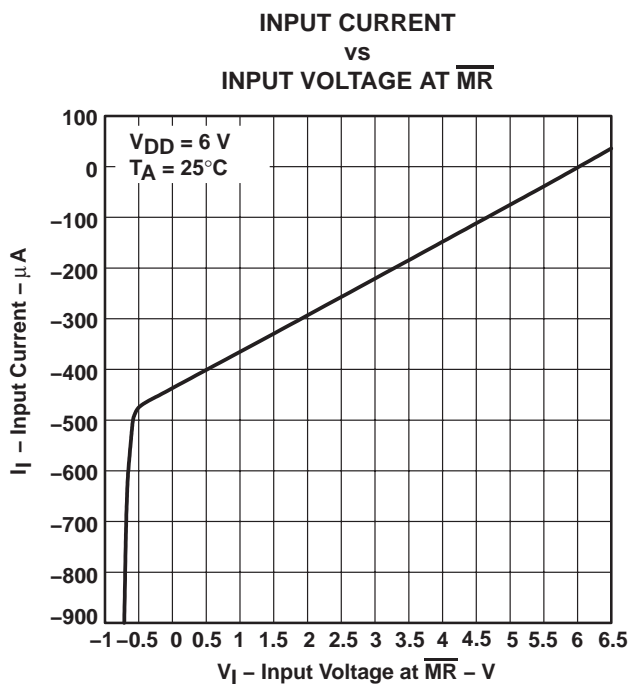


Figure 4

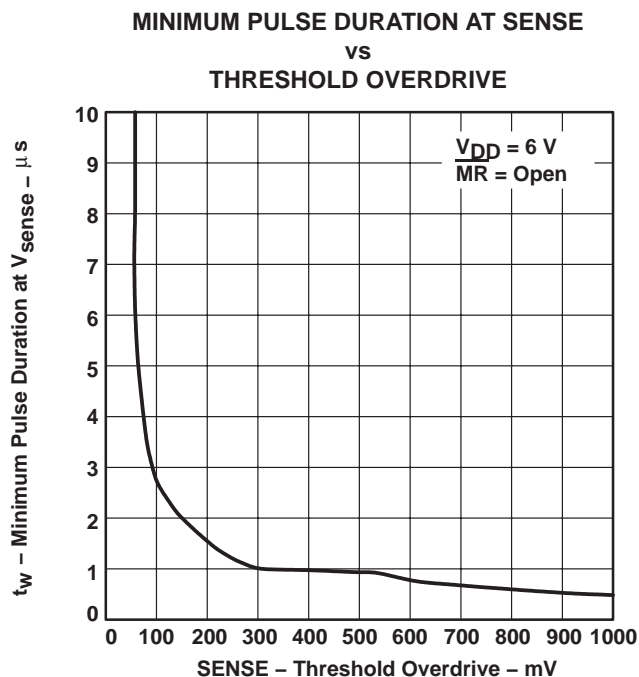
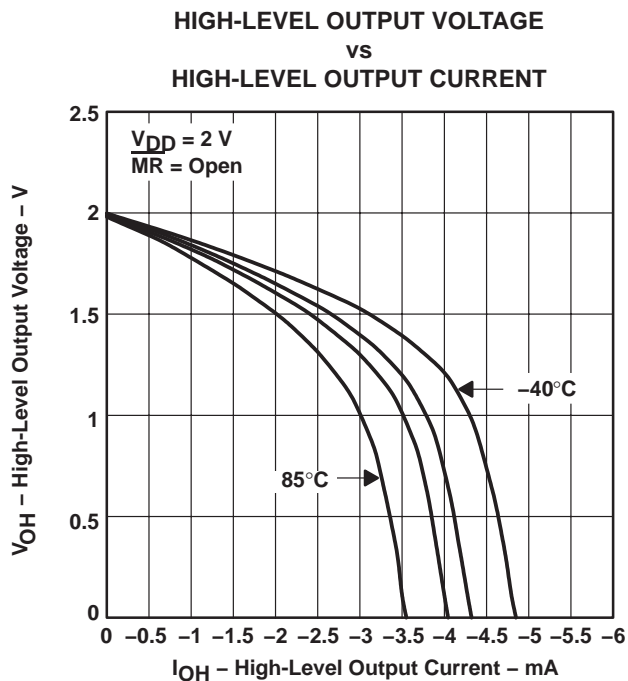
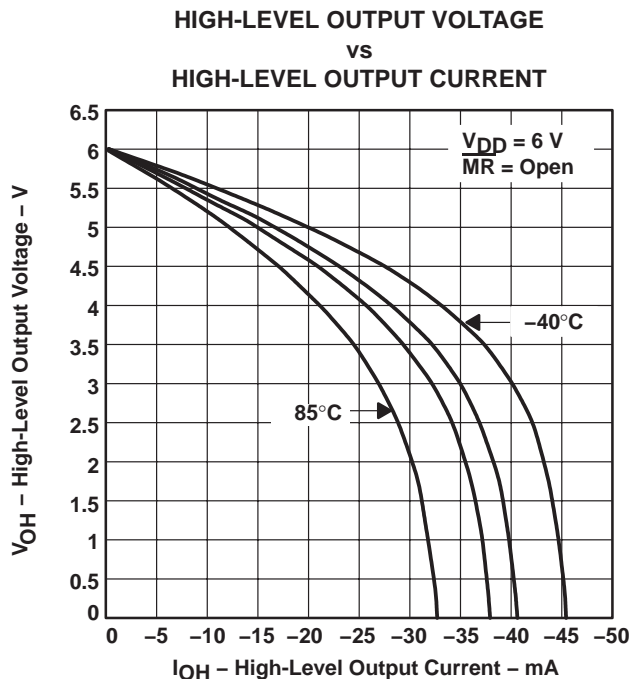


Figure 5

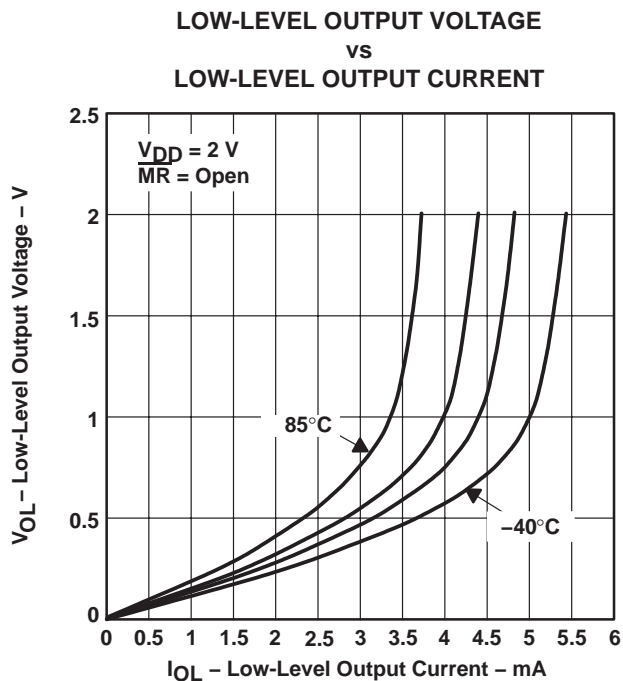
**TYPICAL CHARACTERISTICS**



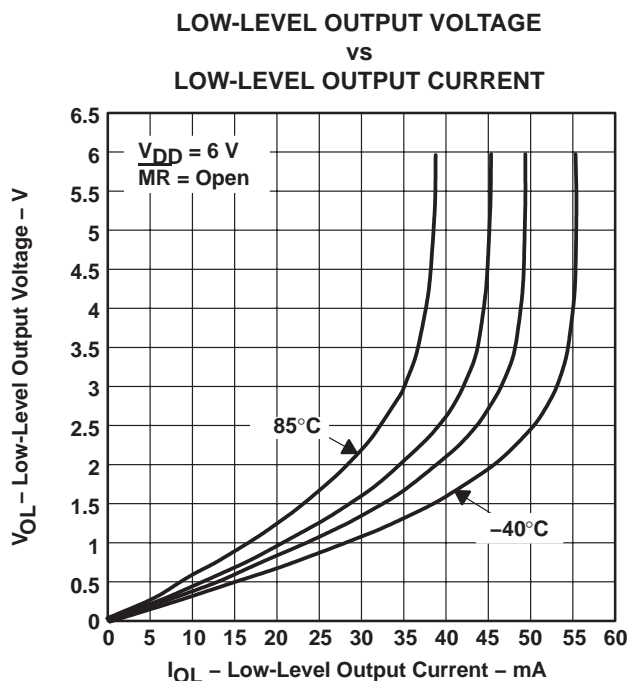
**Figure 6**



**Figure 7**



**Figure 8**



**Figure 9**

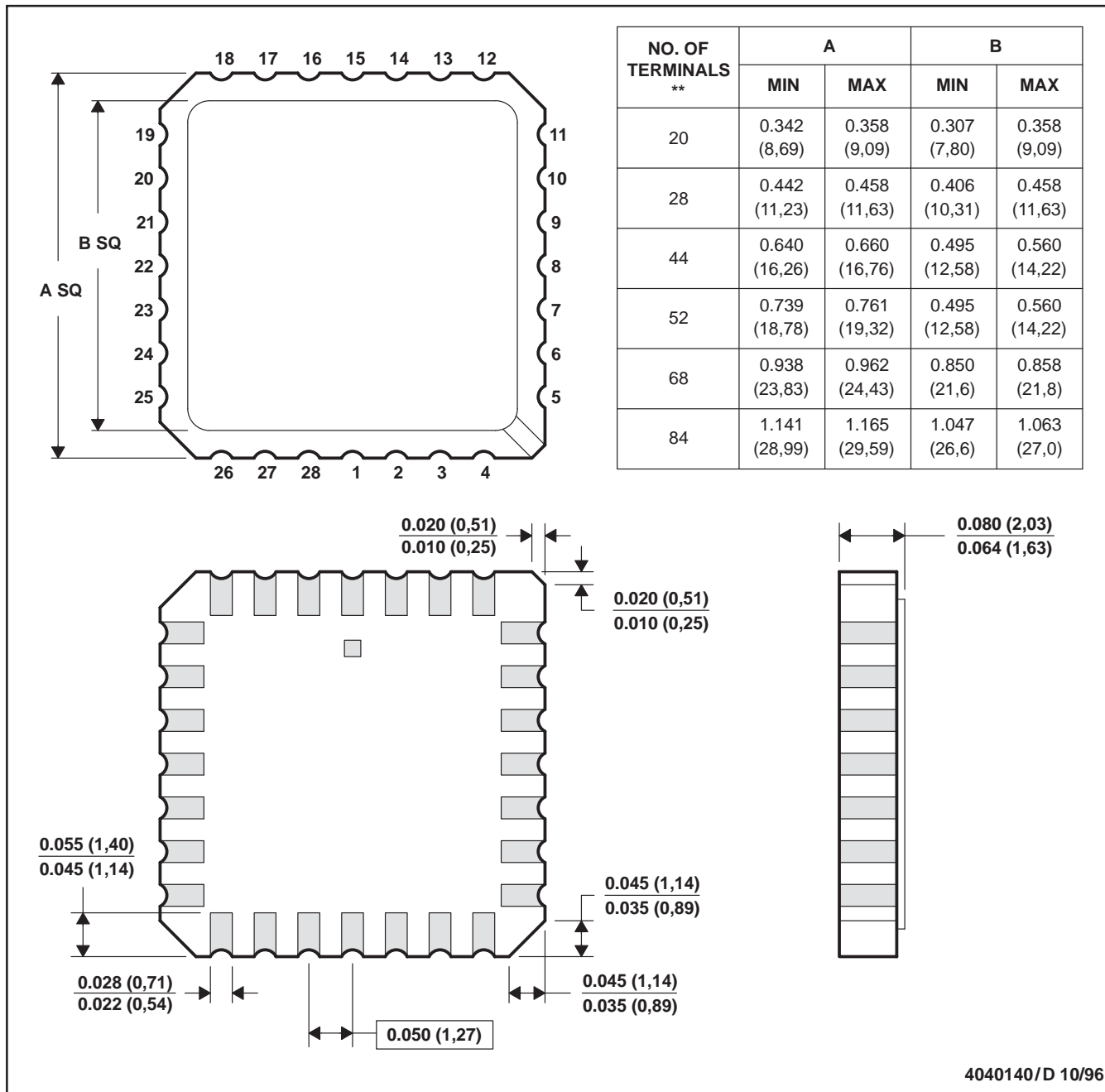


MECHANICAL INFORMATION

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a metal lid.  
 D. The terminals are gold plated.  
 E. Falls within JEDEC MS-004

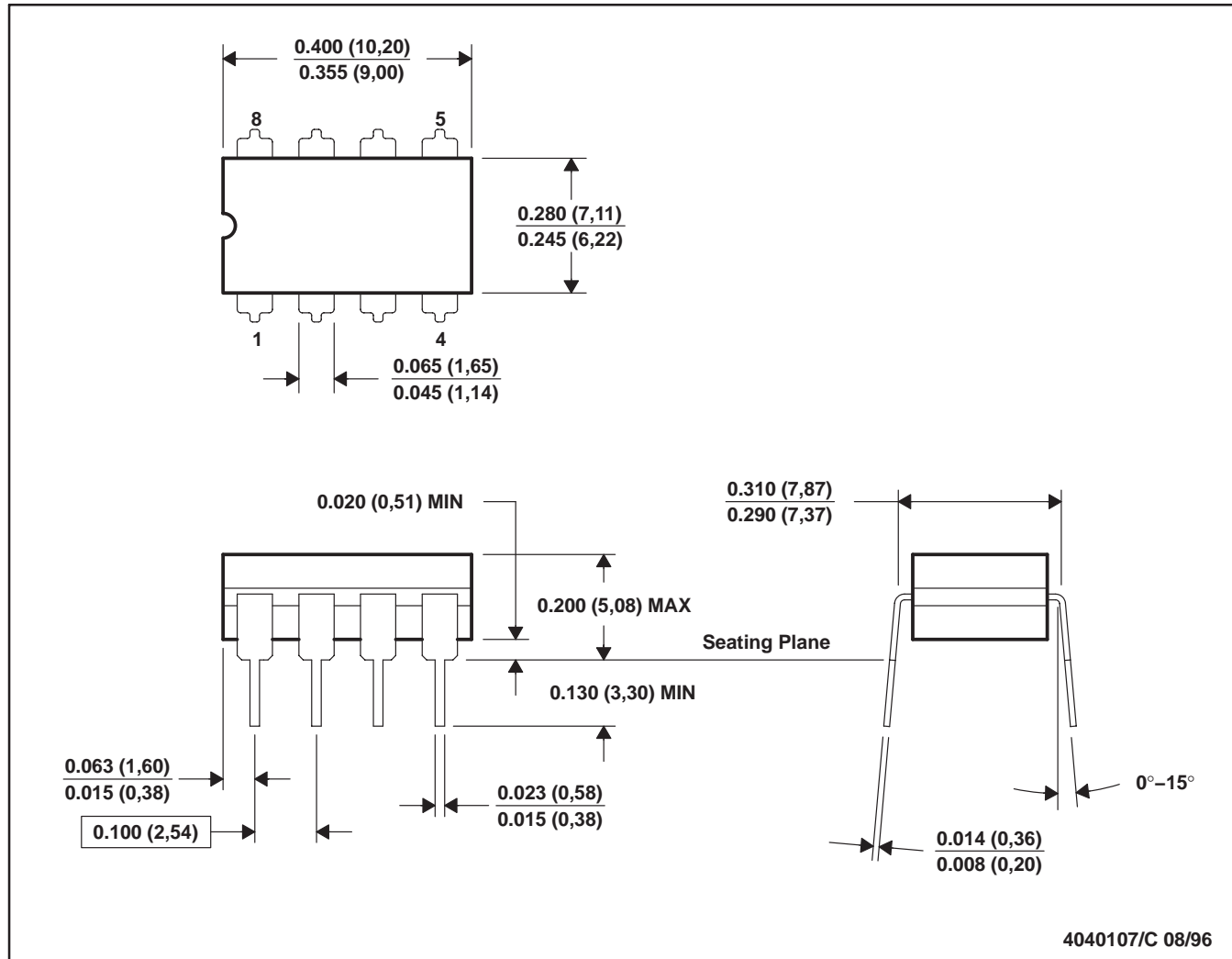
# TPS3307-18M TRIPLE PROCESSOR SUPERVISORS

SGLS133A – JANUARY 2003 – REVISED DECEMBER 2003

## MECHANICAL INFORMATION

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
 E. Falls within MIL-STD-1835 GDIP1-T8

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9959101Q2A	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-9959101QPA	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
TPS3307-18MFKB	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
TPS3307-18MJG	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC
TPS3307-18MJGB	ACTIVE	CDIP	JG	8	1	None	A42 SNPB	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

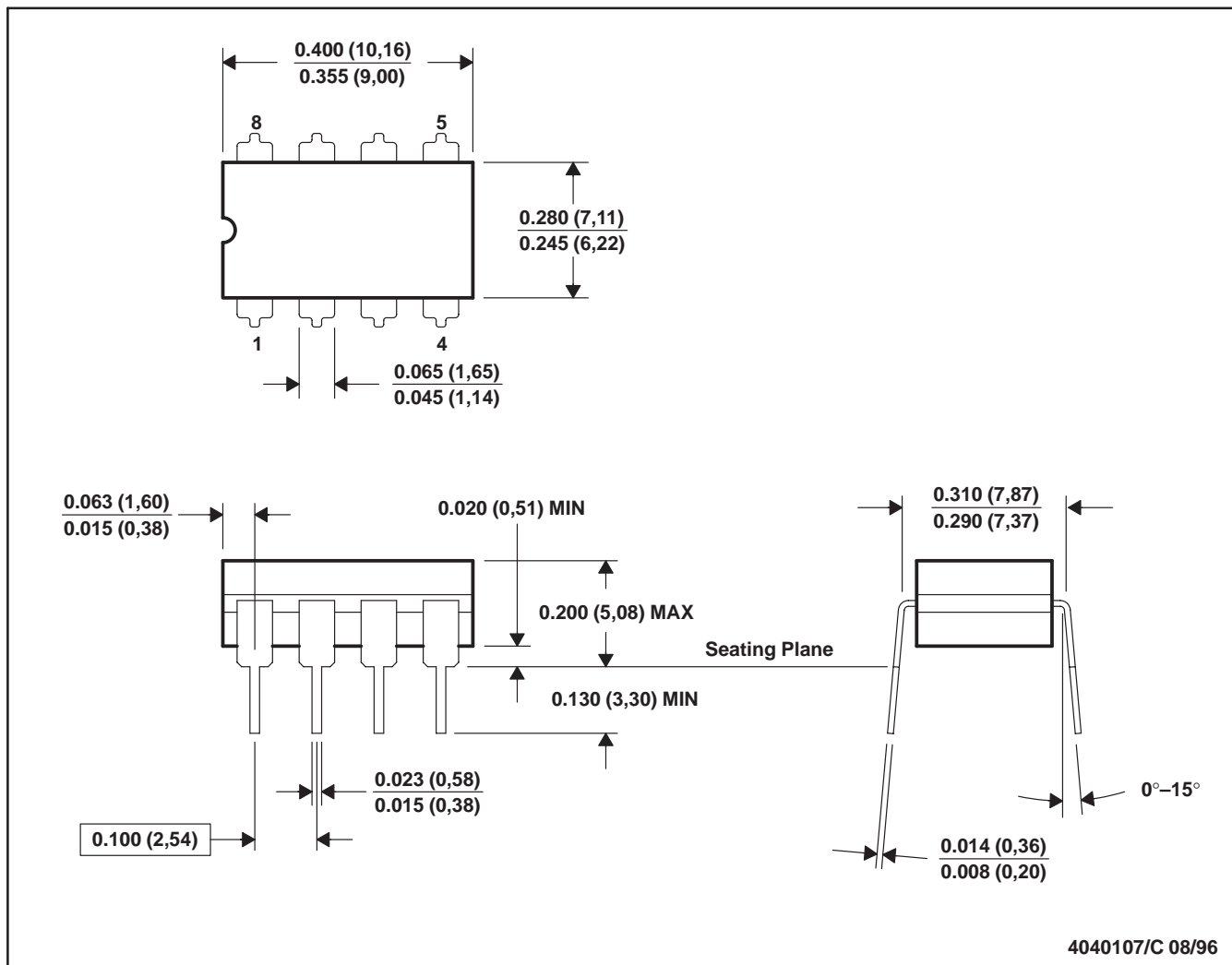
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265