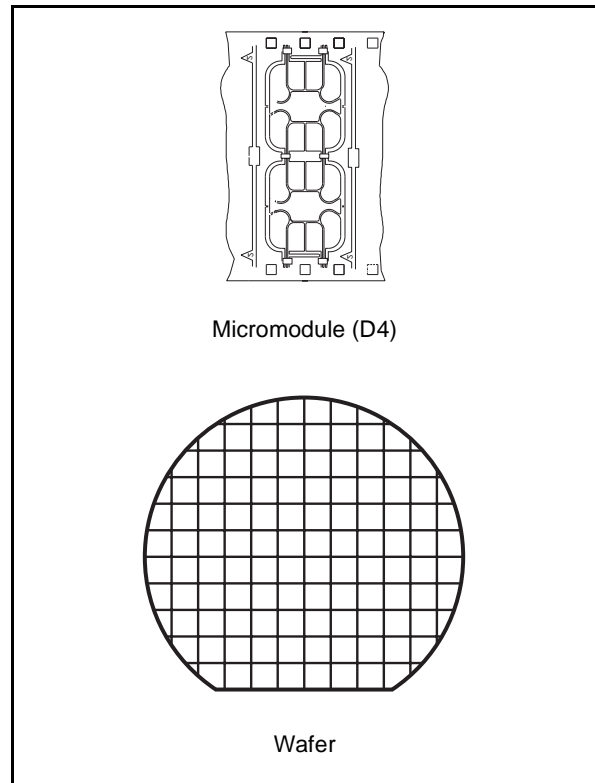# ST16SF4F

Smartcard MCU
With 16352 Bytes EEPROM

DATA BRIEFING

- 8 BIT ARCHITECTURE CPU
- 16 KBytes of USER ROM, SECTOR COMBINATIVE
- 1.5 KByte of SYSTEM ROM
- 384 Bytes of RAM
- 16352 Bytes of EEPROM, SECTOR COMBINATIVE
    - Highly reliable CMOS EEPROM technology
    - 10 year data retention
    - 300,000 Erase/Write cycle endurance
    - Protected One Time Programmable block (32 or 64 bytes)
    - 1 to 32 bytes block either Erase or Write in single cycle programming
- EXTENDED VOLTAGE OPERATION
    - V_{CC} Range: 2.7V to 5.5V
- SERIAL ACCESS, ISO 7816-3 COMPATIBLE
- POWER SAVING STANDBY MODE
- UP TO 5 MHz INTERNAL OPERATING FREQUENCY
- VERY HIGH SECURITY FEATURES INCLUDING EEPROM FLASH ERASE
- CONTACT ASSIGNMENT COMPATIBLE ISO 7816-2
- ESD PROTECTION GREATER THAN 5000V
- MEETS GSM 11.11 AND 11.12 SPECIFICATIONS
- 2 OPERATING CONFIGURATIONS
    - ISSUER
    - USER

Micromodule (D4)

Wafer

DESCRIPTION

The ST16SF4F, a member of the standard ST16 device family, is a serial access microcontroller especially designed for high volume and cost competitive Smartcard applications where firmware security algorithm must be implemented.

The ST16SF4F is based on 8 bit CPU core and includes on chip memories: 384 Bytes of RAM, 16 KBytes of USER ROM, 1.5 KByte of SYSTEM ROM, and 16352 Bytes of EEPROM.

Both ROM and EEPROM memories can be configured into two sectors. Access rules from any memory section or sector to any other are set-up by the User's defined Memory Access Control Matrix (MACM).

Reliability data related to the ST16SF4F product manufactured using STMicroelectronics advanced CMOS EEPROM technology confirm data retention up to 10 years and endurance up to 300,000 Erase/Write cycles.

As all other ST16 family members, the ST16SF4F is fully compatible with the ISO standards for Smartcard applications.

Software development (ROM code, options) can be completed by the ST16-19HDS development system.

The ST16SF4F can be delivered either in unsawn or sawn wafers, 180 or 275 micron thickness as well as in micromodule package.

Figure 1. Block Diagram