



SR176

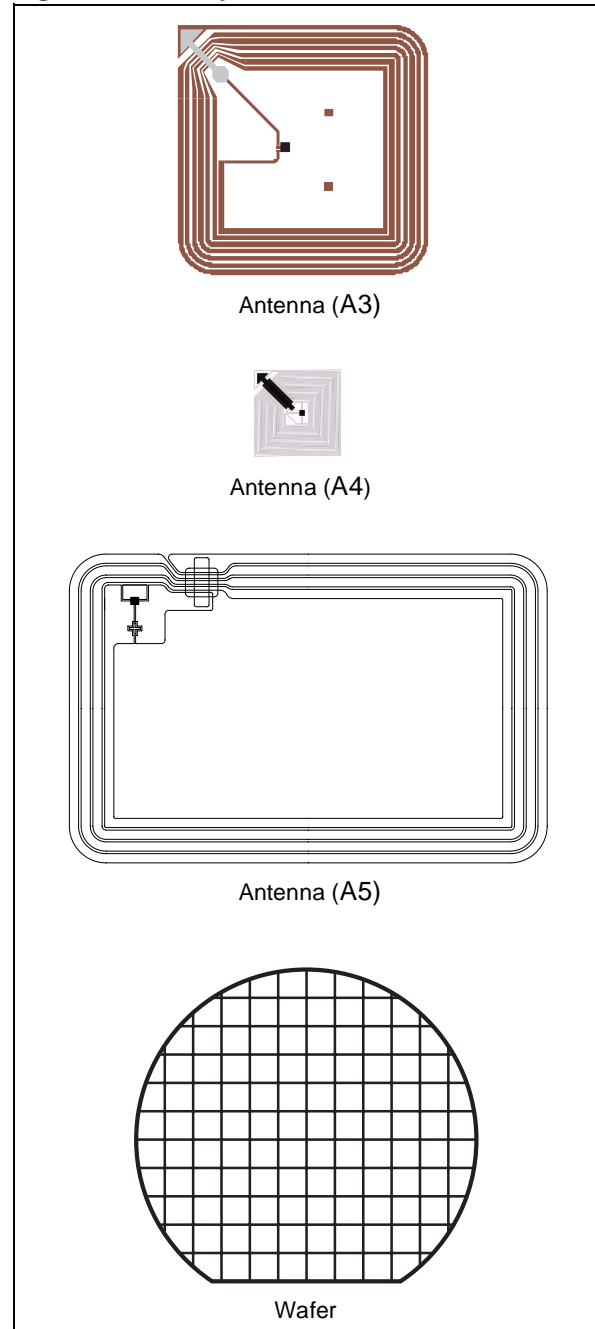
13.56 MHz Short Range Contactless Memory Chip 176 bit USER EEPROM and 64-bit Unique ID

DATA BRIEFING

FEATURES SUMMARY

- ISO 14443 - 2 Type B Air Interface Compliant
- ISO 14443 - 3 Type B Frame Format Compliant
- 13.56MHz Carrier Frequency
- 847kHz Subcarrier Frequency
- 106kbit/s Data Transfer
- Data Transfer
 - ASK Modulation from Reader to Tag
 - BPSK Coding from Tag to Reader
- 176-bit EEPROM with Write Protect Feature
- 64-bit Unique Identifier
- READ BLOCK & WRITE BLOCK (16 Bits)
- Internal Tuning Capacitor
- Self-Timed Programming Cycle
- 5ms Programming Time (typical)
- More than 100,000 Erase/Write Cycles
- More than 10 Year Data Retention

Figure 1. Delivery Forms



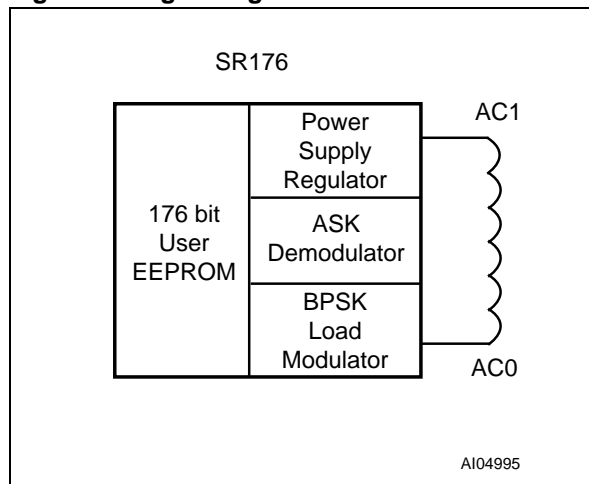
SUMMARY DESCRIPTION

The SR176 is a contactless memory, powered by an externally transmitted radio wave. It contains 176 bits of user EEPROM, fabricated with STMicroelectronics CMOS technology. The memory is organized as 16 blocks of 16 bits, of which 11 blocks are user accessible.

The SR176 is accessed via the 13.56MHz carrier. Incoming data are demodulated and decoded from the received Amplitude Shift Keying modulation signal (ASK). The modulation index of this signal is 10%. Outgoing data are generated by load variation using Bit Phase Shift Keying (BPSK) of a 847kHz subcarrier. The Data transfer rate between the SR176 and the reader is 106kbit/s in both reception and emission modes.

The SR176 follows the ISO 14443 part 2 type B recommendation for radio frequency power and signal interface.

Figure 2. Logic Diagram



The SR176 is principally designed for short range applications, such as in object identification, that

need a low cost and non-reusable product. The SR176 does not include any anti-collision mechanism, but does include a simple selection mechanism to cope with cases where more than one tag is present, within the range of the Reader, at the any one time.

Table 1. Signal Names

AC1	Antenna Coil
AC0	Antenna Coil

The SR176 contactless EEPROM offers read and write random access in block mode. One block is composed by 16 bits. The device has an instruction set containing seven commands:

- READ_BLOCK
- WRITE_BLOCK
- INITIATE
- SELECT
- COMPLETION
- PROTECT_BLOCK
- GET_PROTECTION.

The SR176 is divided into two major areas: the unique identifier (UID) and the User EEPROM. The UID is a 64-bit unique identifier written by ST during product manufacturing. The User EEPROM is divided into areas which can be write-protected so that they behave as ROM. The write protection is activated using an OTP lock bits register. It is possible to program the SR176 4-bit chip_ID used by the SELECT command. Its default value is fixed at the value 0 (0000_b) by ST. When correctly set, up to sixteen SR176s can be selected individually.

MEMORY MAPPING

The SR176 is organized as 16 blocks of 16 bits, as shown in Figure 3.

The first four blocks, from location 0 to 3, are used to store read-only data. They store the 64-bit UID. This value cannot be modified.

Blocks from locations 4 to 14 offer a 176-bit EEPROM user area in which the application can store

its data values. Block 15 contains the OTP LOCK_REG and the programmed Chip_ID.

The PROTECT_BLOCK command is used to lock write access to blocks 4 to 15 by a group of 2 blocks.

The GET_PROTECTION command gives the status of the protection of blocks 4 to 15.

Figure 3. SR176 Memory Mapping

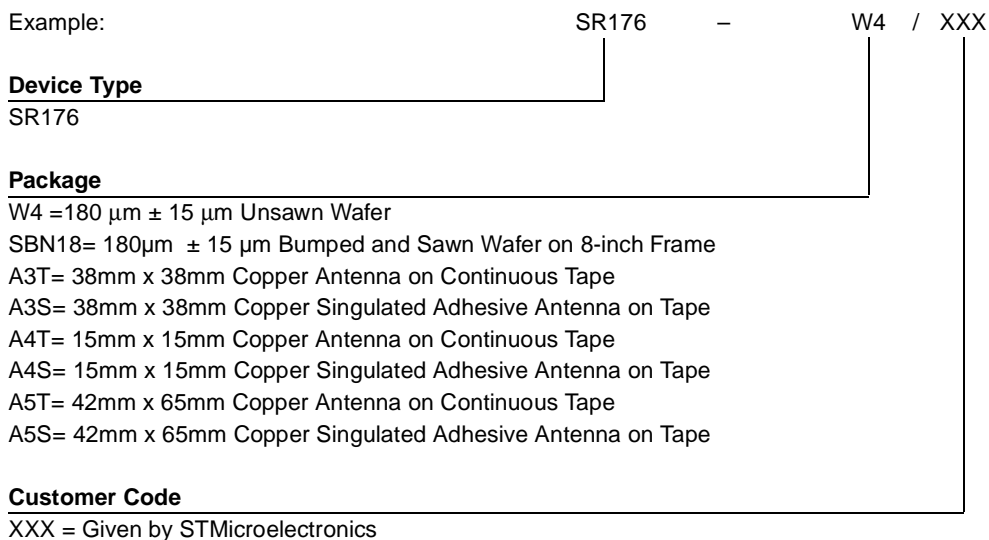
Block Address	MSb b15	16-bit block b8 b7		LSb b0	Description
0		UID0			64-bit UID ROM
1		UID1			
2		UID2			
3		UID3			
4		User Area			Lockable EEPROM
5		User Area			
6		User Area			Lockable EEPROM
7		User Area			
8		User Area			Lockable EEPROM
9		User Area			
10		User Area			Lockable EEPROM
11		User Area			
12		User Area			Lockable EEPROM
13		User Area			
14		User Area			Lockable EEPROM
15		OTP LOCK_REG	Reserved	Chip_ID	

ai07699

PART NUMBERING

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 2. Ordering Information Scheme



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