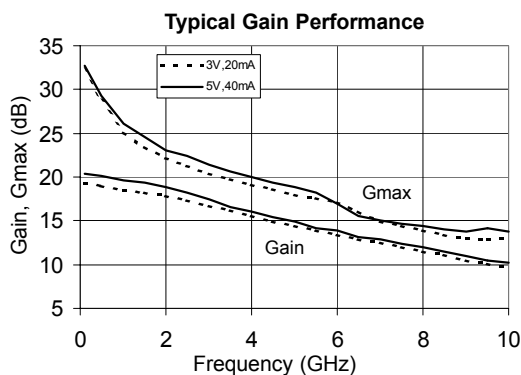


Product Description

Stanford Microdevices' SPF-3043 is a high performance 0.25 μ m pHEMT Gallium Arsenide FET. This 300 μ m device is ideally biased at 3V,20mA for lowest noise performance and battery powered requirements. At 5V,40mA the device delivers excellent OIP3 of 32dBm. It provides ideal performance as a driver stage in many commercial and industrial LNA applications.



SPF-3043

Low Noise pHEMT GaAs FET

Qualification Pending April 2001



Product Features

- DC-10 GHz Operation
- Ultra Low NF:
 - 0.25 dB @ 1 GHz
 - 0.50 dB @ 2 GHz
- High Assoc. Gain:
 - 25 dB @ 1 GHz
 - 22 dB @ 2 GHz
- Low Current Draw for NFopt (3V,20mA)
- +32 dBm OIP3, +20 dBm P1dB (5V,40mA)
- Low Cost High Performance pHEMT

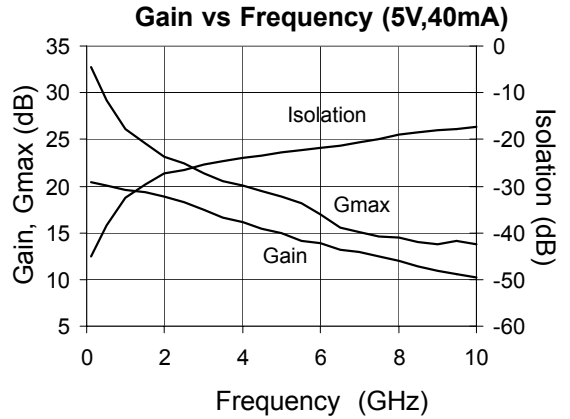
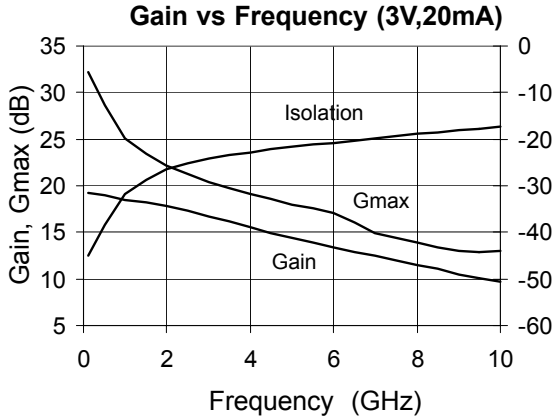
Applications

- LNA for Wireless Infrastructure
- Fixed Wireless Infrastructure
- Wireless Data
- Driver Stage for Low Power Applications

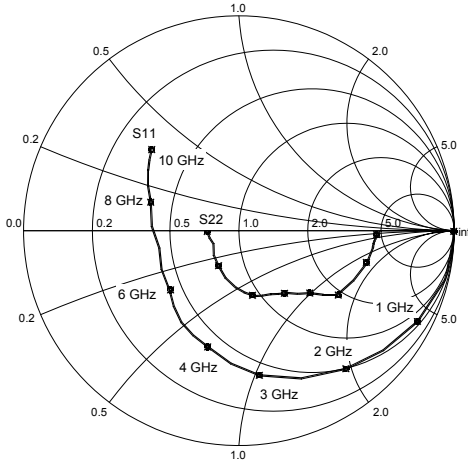
Symbol	Device Characteristics, T = 25°C V _{DS} =3V, I _{DS} =20mA (unless otherwise noted)	Units	Min.	Typ.	Max.
G _{MAX}	Maximum Available Gain Z _S =Z _S [*] , Z _L =Z _L [*]	f = 0.9 GHz f = 1.9 GHz		25.5 22.4	
S ₂₁	Insertion Gain Z _S =Z _L =50Ω	f = 0.9 GHz f = 1.9 GHz		18.5 18.0	
NF _{min}	Minimum Noise Figure Z _S =Γ _{OPT} [*] , Z _L =Z _L [*]	f = 0.9 GHz f = 1.9 GHz		0.25 0.50	
P1dB	Output 1 dB compression point Z _S =Z _{SOPT} [*] , Z _L =Z _L OPT	V _{DS} =3V, I _{DS} =20 mA V _{DS} =5V, I _{DS} =40 mA		15.5 20	
OIP ₃	Output Third Order Intercept Point Z _S =Z _{SOPT} [*] , Z _L =Z _L OPT	V _{DS} =3V, I _{DS} =20 mA V _{DS} =5V, I _{DS} =40 mA		29 32	
V _P	Pinchoff Voltage	V _{DS} = 2V, I _{DS} = 0.1 mA		-1.1	-0.5
I _{BSS}	Saturated Drain Current	V _{DS} = 2V, V _{GS} = 0V		45	100
g _{mp}	Peak Transconductance	V _{DS} = 2V, V _{GS} @ g _{mp}		100	150
BV _{GSO}	Gate-to-Source Breakdown Voltage	I _G = 0.03 mA Drain Open, Source Grounded			-8
BV _{GDO}	Gate-to-Drain Breakdown Voltage	I _G = 0.03 mA Source Open, Drain Grounded			-8
R _{th}	Thermal Resistance (junction to lead)			150	

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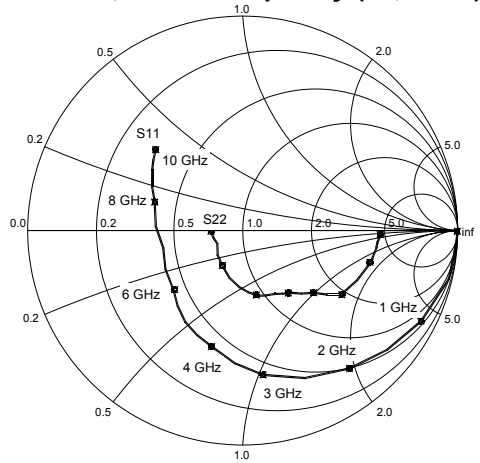
Typical Performance



S11,S22 vs Frequency (3V,20mA)



S11,S22 vs Frequency (5V,40mA)



Note: S-parameters are de-embedded to the device leads with $Z_s = Z_L = 50\Omega$. The data represents typical performance of the device. De-embedded s-parameters can be downloaded from our website (www.stanfordmicro.com).

Typical Performance

Freq (MHz)	V_{DS} (V)	I_{DS} (mA)	Fmin (dB)	Γ_{OPT} Mag \angle Ang	r_N	Gmax (dB)	P1dB (dBm)	OIP3 (dBm)
900	3	20	0.25	0.79 \angle 12	0.22	25.5	15.5	29
	5	40	0.32	0.75 \angle 12	0.25	26.5	20.0	32
1900	3	20	0.50	0.62 \angle 34	0.19	22.4	15.5	29
	5	40	0.54	0.62 \angle 33	0.20	23.3	20.0	32

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Current	I_{DS}	150	mA
Forward Gate Current	I_{GS}	2	mA
Drain-to-Source Voltage	V_{DS}	7	V
Gate-to-Source Voltage	V_{GS}	-3	V
RF Input Power	P_{IN}	15	dBm
Operating Temperature	T_{OP}	-40 to +85	C
Storage Temperature Range	T_{stor}	-40 to +150	C
Power Dissipation	P_{DISS}	430	mW
Operating Junction Temperature	T_J	+150	C



Caution: ESD sensitive

Appropriate precautions in handling, packaging and testing devices must be observed.

Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SPF-3043	7"	3000

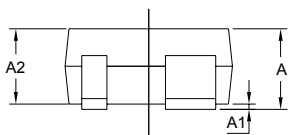
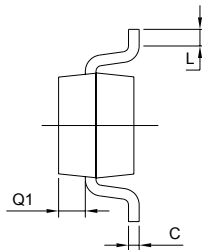
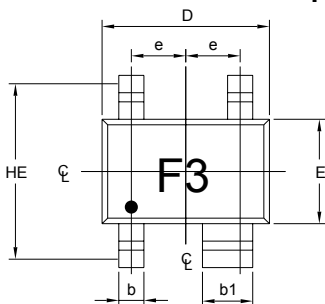
Part Symbolization

The part will be symbolized with an "F3" and a Pin 1 indicator on the top surface of the package.

Pin Description

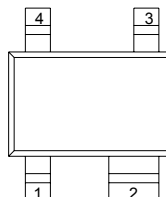
Pin #	Function	Description
1	Gate	RF Input
2	GND & Source	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.
3	Drain	RF Output
4	GND & Source	Same as Pin 2

Package Dimensions



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70.
5. DIE IS FACING UP FOR MOLD AND FACING DOWN FOR TRIM/FORM. ie. REVERSE TRIM/FORM.
6. PACKAGE SURFACE TO BE MIRROR FINISH.



SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
Q1	0.10	0.40
e	0.65 BSC	
b	0.25	0.40
b1	0.55	0.70
c	0.10	0.18
L	0.10	0.30

Use multiple plated-through vias holes located close to the package pins to ensure a good RF ground connection to a continuous groundplane on the backside of the board.