
Description

The CXA3355TQ is an IC developed as a GPS RF down converter. This IC realizes a reduction in the number of external parts by integrating LNA, image rejection mixer, IF filter and PLL/VCO parts, such as inductor and variable capacitors. (Applications: GPS RF down converter IC)

Features

- ◆ Includes all functions required for the GPS down converter
- ◆ Low voltage operation: $V_{CC} = 1.6$ to $2.0V$
- ◆ Low current consumption (active mode): $11mA$ (Typ. at $V_{CC} = 1.8V$, $IF \approx 1MHz$)
- ◆ Low current consumption (power save mode) $< 1\mu A$
- ◆ Total gain $\approx 100dB$
- ◆ Total NF $\approx 4.0dB$
- ◆ On-chip VCO and PLL
- ◆ Selectable TCXO frequency
- ◆ On-chip LNA (NF = $2.0dB$)
- ◆ Image rejection mixer
- ◆ On-chip IF filter, and an external filter can be connected as an option for further band narrowing.
- ◆ 1-bit IF output

Package

48-pin TQFP (Plastic)

Structure

SiGe BiCMOS monolithic IC

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Absolute Maximum Ratings

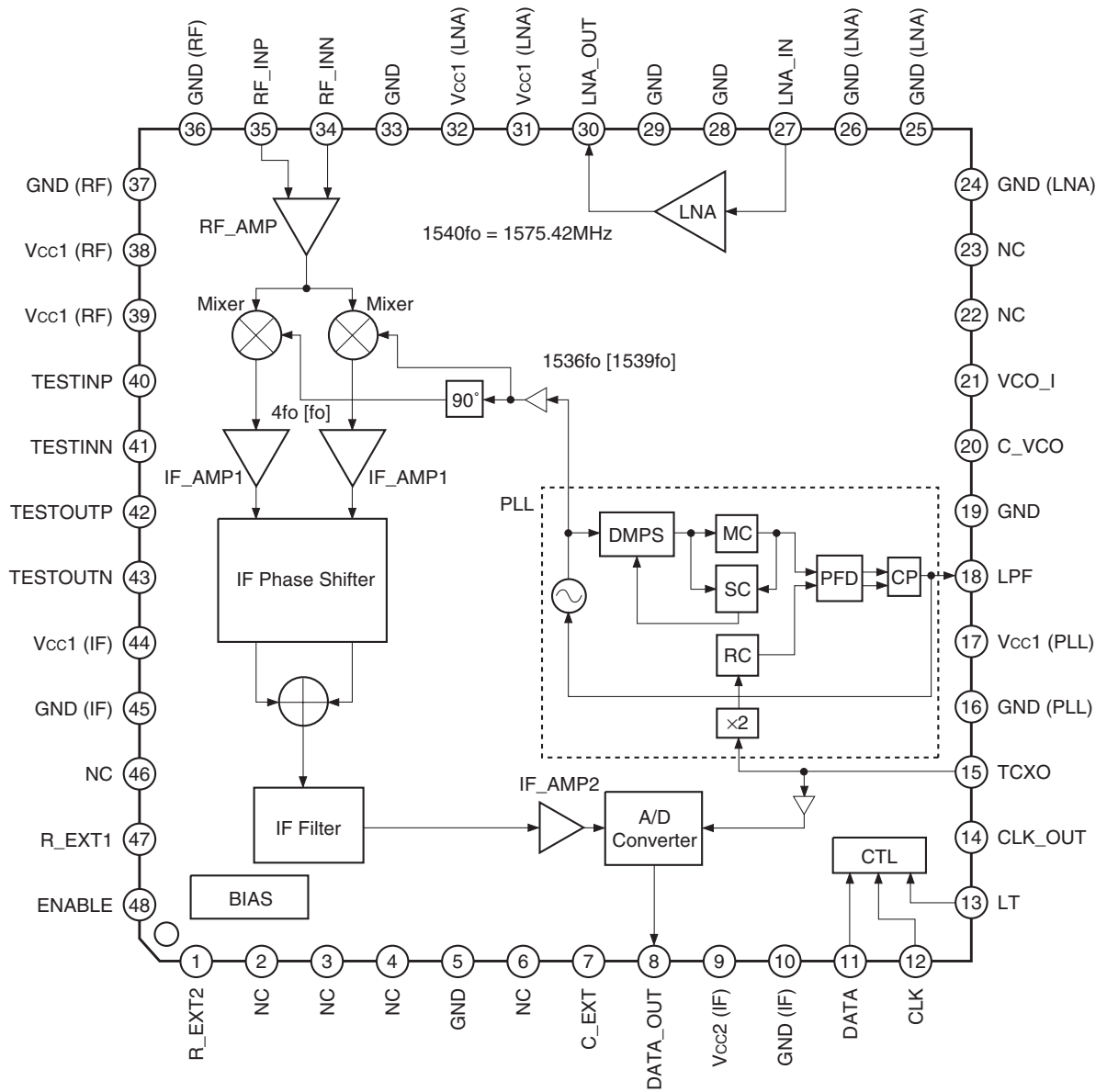
(Ta = 25°C)

◆ Supply voltage	Vcc1	-0.2 to +2.5	V
	Vcc2	-0.2 to +3.6	V
◆ Operating temperature	Topr	-40 to +85	°C
◆ Storage temperature	Tstg	-65 to +150	°C

Recommended Operating Conditions

◆ Supply voltage	Vcc1	1.6 to 2.0	V
	Vcc2	1.6 to 3.3	V

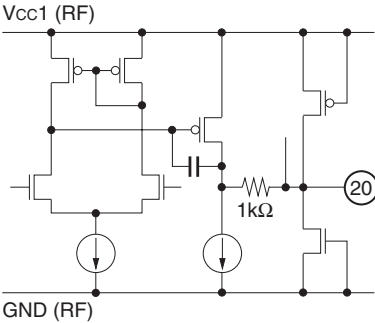
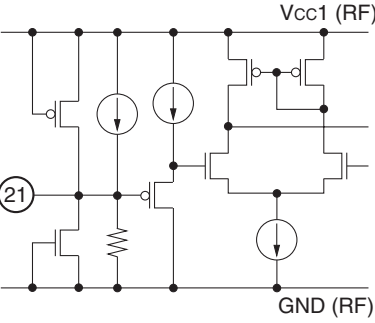
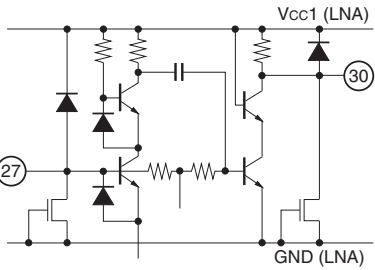
Block Diagram and Pin Configuration

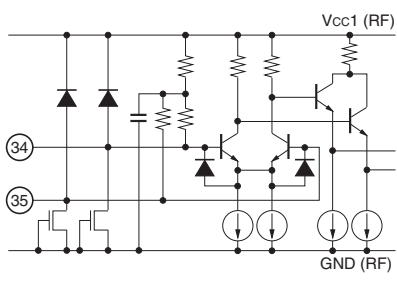
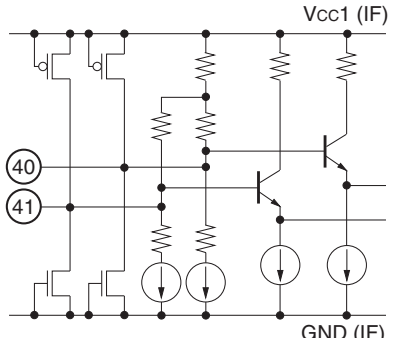
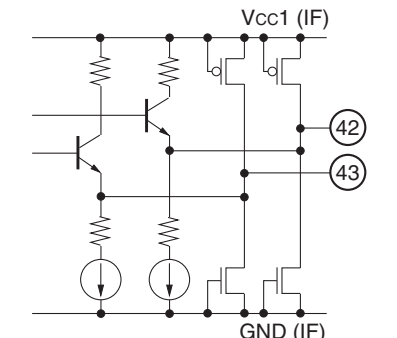


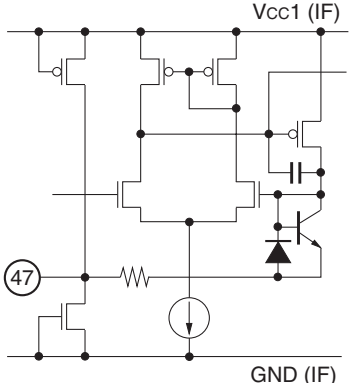
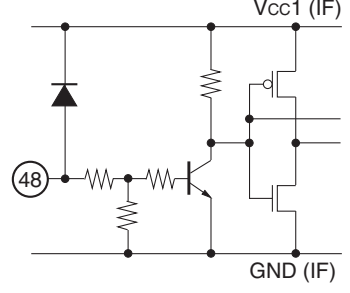
Pin Description

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
1	R_EXT2	1.16	—		External resistor connection. (bias)
2	NC	—	—		Normally leave open.
3	NC	—	—		Normally leave open.
4	NC	—	—		Normally leave open.
5	GND	0	—		GND.
6	NC	—	—		Normally leave open.
7	C_EXT	1.2	—		Capacitor connection for canceling the offset.
8	DATA_OUT	—	1.8 Vp-p		DATA (IF) output.
9	Vcc2 (IF)	1.8	—		IF block Vcc.
10	GND (IF)	0	—		IF block GND.

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
11	DATA	—	—		Serial data input.
12	CLK	—	—		Serial data clock input.
13	LT	—	—		Latch signal input.
14	CLK_OUT	1.2	—		TCXO clock output. Leave open when not using the TCXO clock.
15	TCXO	—	—		Reference frequency input.
16	GND (PLL)	0	—		PLL block GND.
17	Vcc1 (PLL)	1.8	—		PLL block Vcc.
18	LPF	—	—		PLL loop filter connection.
19	GND	0	—		GND.

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
20	C_VCO	—	—		Capacitor connection for decoupling the VCO bias circuit.
21	VCO_I	—	—		Capacitor connection for decoupling the VCO bias circuit.
22	NC	—	—		Normally leave open.
23	NC	—	—		Normally leave open.
24	GND (LNA)	0	—		LNA block GND.
25	GND (LNA)	0	—		LNA block GND.
26	GND (LNA)	0	—		LNA block GND.
27	LNA_IN	0.7	—		LNA input.
30	LNA_OUT	1.8	—		LNA output.
28	GND	0	—		GND.
29	GND	0	—		GND.
31	Vcc1 (LNA)	1.8	—		LNA block Vcc.
32	Vcc1 (LNA)	1.8	—		LNA block Vcc.
33	GND	0	—		GND.

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
34	RF_INN	—	—		RF amplifier input.
35	RF_INP	—	—		
36	GND (RF)	0	—		RF block GND.
37	GND (RF)	0	—		RF block GND.
38	Vcc1 (RF)	1.8	—		RF block Vcc.
39	Vcc1 (RF)	1.8	—		RF block Vcc.
40	TESTINP	1.3	—		IF signal input when using an external filter.
41	TESTINN	1.3	—		IF signal input when using an external filter.
42	TESTOUTP	0.5	—		IF signal output when using an external filter.
43	TESTOUTN	0.5	—		IF signal output when using an external filter.
44	Vcc1 (IF)	1.8	—		IF block Vcc.
45	GND (IF)	0	—		IF block GND.
46	NC	—	—		Normally leave open.

Pin No.	Symbol	Standard pin voltage [V]		Equivalent circuit	Description
		DC	AC		
47	R_EXT1	0.5	—		External resistor connection. (bias)
48	ENABLE	—	—		ENABLE signal input. High (V_{IH} : 1.2V min.): Active mode Low (V_{IL} : 0.2V max.): Power save mode

Electrical Characteristics

DC Characteristics

(Vcc1 = Vcc2 = 1.8V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current 1	Icc1	fo mode	7	11	15	mA
Supply current 2	Icc2	Power save mode	—	0.1	1	μA

Note) fo mode uses the following power-on reset conditions.

fo mode: TCXO = 18.414MHz, f_{LO} = 1574.397MHz, IF = 1.023MHz

AC Characteristics

(Vcc1 = Vcc2 = 1.8V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total voltage gain	G	Excluding the A/D converter	85	100	—	dB
Image rejection ratio	IMRR	Frequency = 1.023MHz	—	-40	-20	dBc
LPF1 (fo mode)	LPF1	@150kHz Normalized at 1.023MHz output level	-5	—	4	dB
LPF2 (fo mode)	LPF2	@2.046kHz Normalized at 1.023MHz output level	-13	—	2	dB
LPF3 (fo mode)	LPF3	@6MHz Normalized at 1.023MHz output level	—	—	-13	dB
C/N 100K	C/N	IF = fo, TCXO = 18.414MHz	—	-70	-55	dBc/Hz

Note) fo mode uses the following power-on reset conditions.

fo mode: TCXO = 18.414MHz, f_{LO} = 1574.397MHz, IF = 1.023MHz

Design Reference Value of Operating Conditions

IF Output (DATA_OUT)

(Vcc1 = Vcc2 = 1.8V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
DATA_OUT rise time	DTr	Pin 8 (DATA_OUT), 10 to 90%, Load = 1MΩ//13pF	—	6	—	ns
DATA_OUT fall time	DTf	Pin 8 (DATA_OUT), 10 to 90%, Load = 1MΩ//13pF	—	4	—	ns

ENABLE

(Vcc1 = 1.8 ± 0.2V, Vcc1 ≤ Vcc2 ≤ 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage High level	EVIH	Pin 48 (ENABLE), input voltage High level threshold voltage	1.2	—	Vcc2 + 0.2	V
Input voltage Low level	EVIL	Pin 48 (ENABLE), input voltage Low level threshold voltage	-0.1	—	0.2	V

Power-on Reset

(Vcc1 = 1.8 ± 0.2V, Vcc1 ≤ Vcc2 ≤ 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Allowable rise time	MTr	ENABLE and power supply (Vcc1, Vcc2) rise time for the power-on reset function to operate. Note) Use an ENABLE and power supply (Vcc1, Vcc2) rise time of 100ms or less.	—	—	100	ms

TCXO

(Vcc1 = Vcc2 = 1.8V, Ta = 25°C)

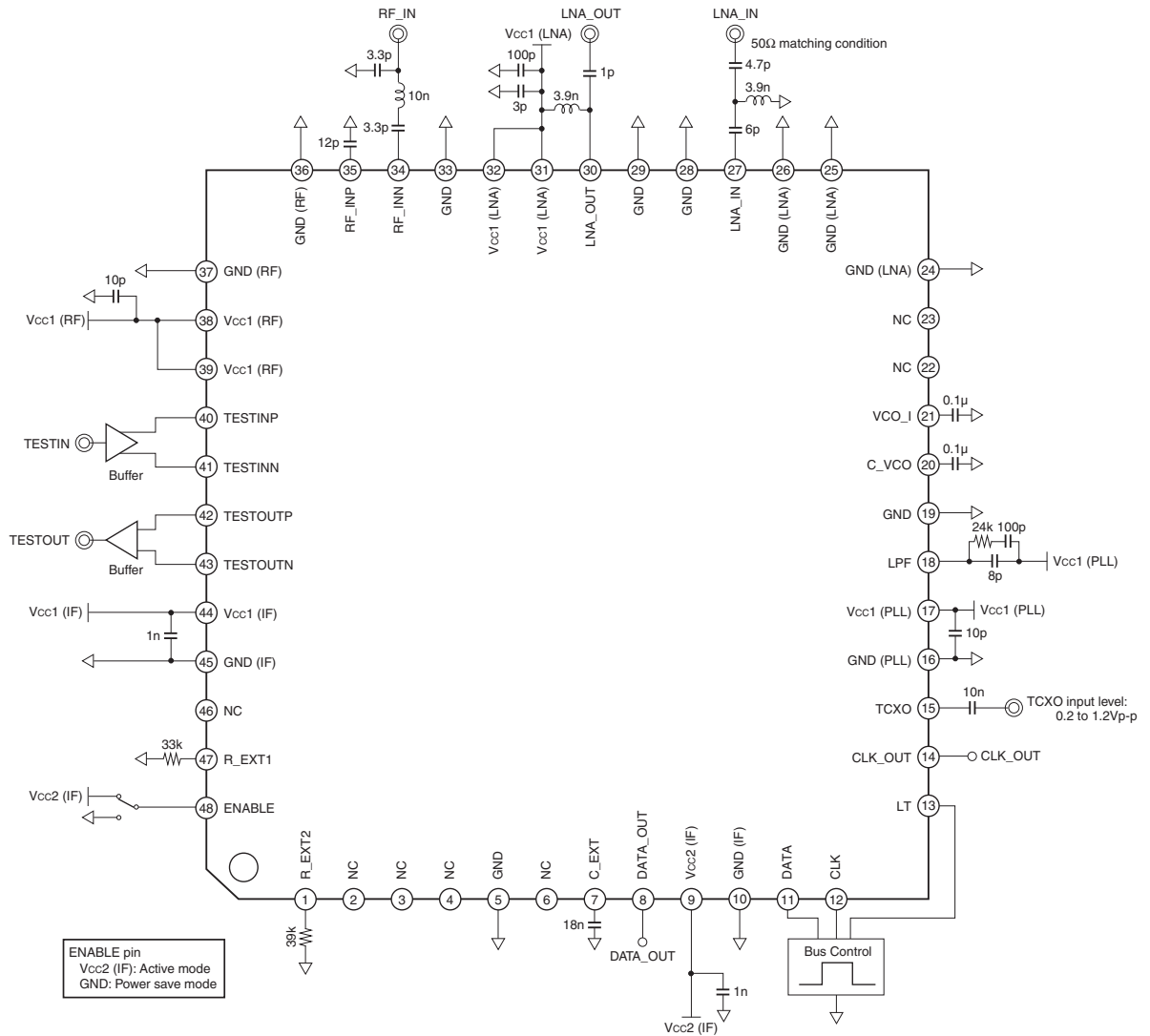
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input level	Vtcxo	Pin 15 (TCXO)	0.2	0.6	1.2	Vp-p
CLK_OUT rise time	CTr	Pin 14 (CLK_OUT), 10 to 90%, Load = 1MΩ//13pF	—	6	—	ns
CLK_OUT fall time	CTf	Pin 14 (CLK_OUT), 10 to 90%, Load = 1MΩ//13pF	—	4	—	ns

Threshold Voltage

(Vcc1 = 1.8 ± 0.2V, Vcc1 ≤ Vcc2 ≤ 3.3V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logic input voltage High level	VIH	Logic input pins = 11 (DATA), 12 (CLK), 13 (LT)	Vcc2 - 0.2	—	Vcc2 + 0.2	V
Logic input voltage Low level	VIL	Logic input pins = 11 (DATA), 12 (CLK), 13 (LT)	-0.1	—	0.2	V
Logic output voltage High level	VOH	Logic output pins = 8 (DATA_OUT), 14 (CLK_OUT)	Vcc2 - 0.2	—	Vcc2	V
Logic output voltage Low level	VOL	Logic output pins = 8 (DATA_OUT), 14 (CLK_OUT)	0	—	0.2	V

Electrical Characteristics Measurement Circuit



- Note) 1. The RF block bypass capacitors should have excellent high frequency characteristics.
 2. Use parts with a tolerance of $\pm 1\%$ for the following resistor elements. Other parts should have a tolerance of $\pm 5\%$.
- Pin 1 (R_EXT2)
 - Pin 18 (LPF)
 - Pin 47 (R_EXT1)

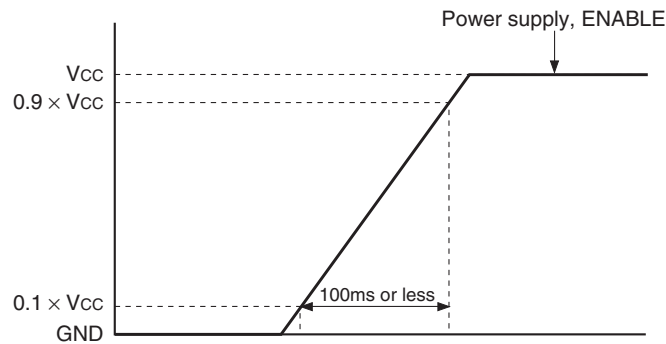
Initial Settings

The CXA3355TQ is initialized by setting the ENABLE signal (Pin 48) from Low level to High level. The timing, etc. should satisfy the conditions below.

In addition, the TCXO frequency and IF frequency combinations in the table below can be obtained by setting Pin 11 (DATA), Pin 12 (CLK) and Pin13 (LT) as shown in the table and then performing initialization. This eliminates the need for serial data setting.

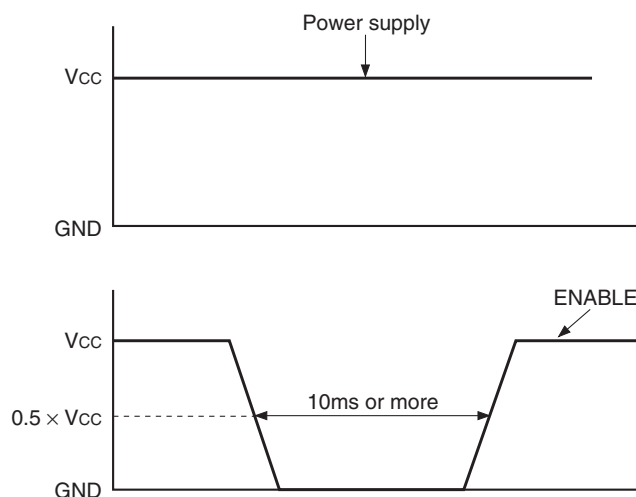
Pin 11 (DATA)	Pin 12 (CLK)	Pin 13 (LT)	TCXO frequency [MHz]	IF frequency [MHz]
GND	GND	GND	Reserved	Reserved
Vcc2	GND	GND	18.414	1.023
Vcc2	Vcc2	GND	13	0.976

1. During Power-on



The CXA3355TQ is initialized by simultaneously rising the power supplies and the ENABLE signal (Pin 48) during power-on. The power supply and ENABLE (Pin 48) rise time should be 100ms or less. In addition, the power supply (Vcc1, Vcc2) should rise simultaneously.

2. Initialization After Power-on



After power-on, the CXA3355TQ is initialized by setting the ENBLE signal (Pin 48) to Low level for 10ms or more and then setting it to High level.

Serial Data Settings

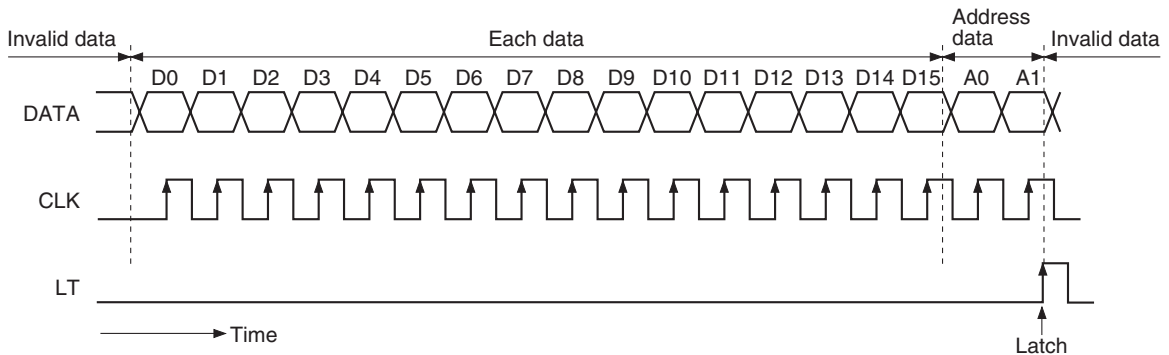
The CXA3355TQ can make the PLL counter settings, perform TCXO_CLK output, select the internal IF Filter, and use the test I/O circuit according to the serial data settings (3-wire bus control). The transfer bit length is 18 bits, and there are four addresses. The address is set by the A1 and A0 bits. The timing, etc. should satisfy the conditions below.

Serial Data Format

(MSB) A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	(LSB) D0
0	0	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0	0	0	0	CLK	0
0	1	SC4	SC3	SC2	SC1	SC0	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	0	TCL
1	0	TI2	TI1	TI0	TO2	TO1	TO0	0	0	0	0	0	0	0	0	FIL	0
1	1	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0	0	0	0	CLK	0

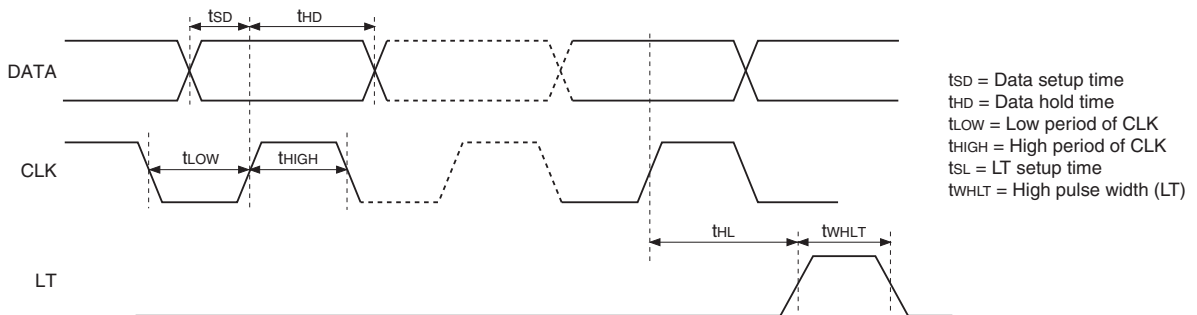
- MC (0 to 10): Main counter frequency division value setting
- SC (0 to 4): Swallow counter frequency division value setting
- RC (0 to 8): Reference counter frequency division value setting
- CLK: TCXO CLK output (0: Not output, 1: Output)
- FIL: Internal filter selection (0: fo mode LPF, 1: Reserved)
- TCL: IF block test I/O control (0: When not using the test I/O circuit, 1: When using the test I/O circuit)
- TI (0 to 2): IF block test input location setting
- TO (0 to 2): IF block test output location setting
- 0: Logic input voltage Low level
- 1: Logic input voltage High level

18-bit Data Format



* Input data to all four addresses.

Serial Data Interface Bus Timing (3-wire Bus Control)

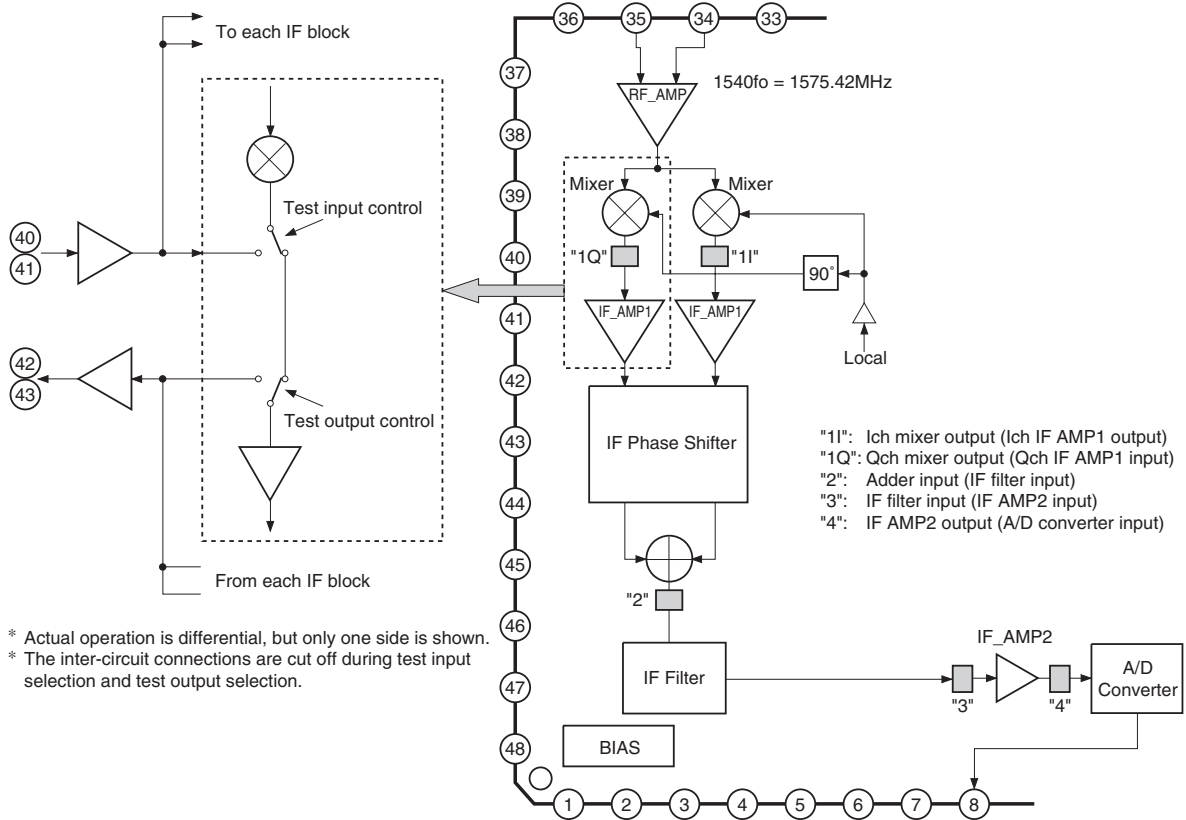


tWHLT ≥ 100ns
tSD, tHD, tLOW, tHIGH, tHL, tWHLT ≥ 50ns

Description of Functions

Test Circuit

The CXA3355TQ has a test circuit for test signal I/O. The test circuit is connected between each IF block, and test I/O control can be performed by the serial data settings. The test circuit location, configuration and the serial data settings are as follows.



* Actual operation is differential, but only one side is shown.
 * The inter-circuit connections are cut off during test input selection and test output selection.

Test Circuit Location and Configuration

Serial Data Settings for Test Input Selection			Serial Data Settings for Test Output Selection			
TI2	TI1	TI0	Test input			Test output
0	0	0	Normal operation			Normal operation
0	0	1	Ich IF AMP1 input			Ich mixer output
0	1	0	Qch IF AMP1 input			Qch mixer output
0	1	1	Not used.			Not used.
1	0	0	Not used.			Not used.
1	0	1	IF filter input			Adder output
1	1	0	IF AMP2 input			IF filter output
1	1	1	A/D converter input			IF AMP2 output

0: Logic input level Low level
 1: Logic input level High level

Note) Set the TCL register to "1" when using or to "0" when not using the test input circuit or the test output circuit. (See page 14.)

Description of Operation

Overview of Operation

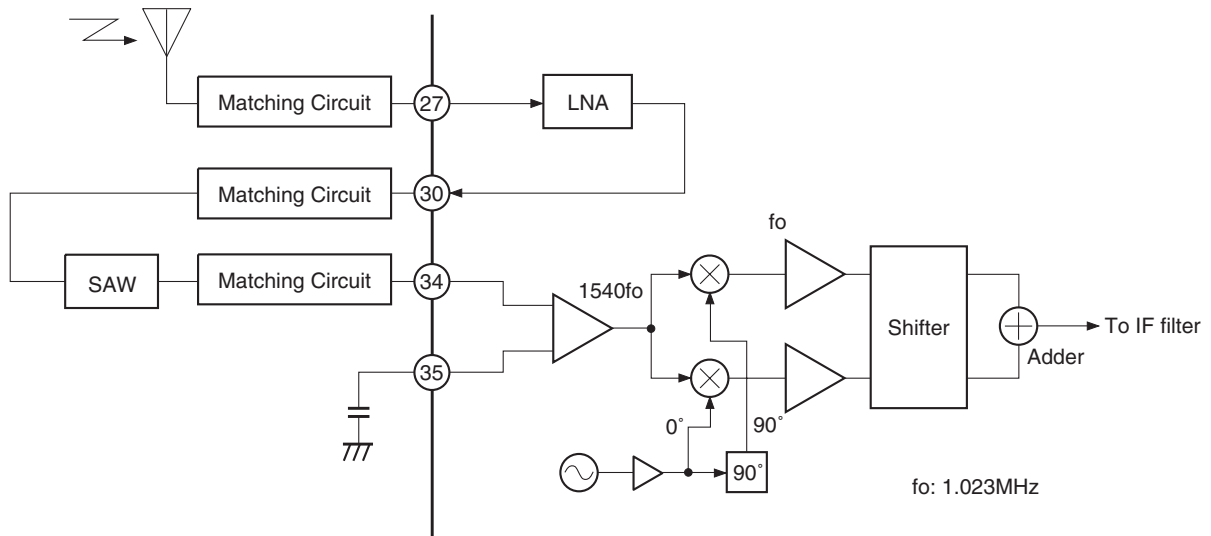
This IC down-converts the GPS (Global Positioning System) frequency of 1.57542GHz to f_o (f_o : 1.023MHz). The internal configuration is divided into the analog block, consisting of the amplifier, mixer and filters, and the digital block (including the comparator block and the control block), which forms PLL. The analog block converts the frequency and amplifies the signal with the amplifier and the mixer, and eliminates undesired components with the filters. The digital block can switch the PLL frequency division ratio in order to down convert the output signal to f_o .

1. LNA

The GPS signal that passes through the antenna is input to Pin 27 via a matching circuit as shown in the figure below. The input signal is amplified by the LNA, and then output from Pin 30. Always use matching circuits for the LNA input pin (Pin 27) and the LNA output pin (Pin 30), and match at 1.57542GHz.

2. RF Amplifier, RF Mixer, IF Phase Shifter and Adder

The signal amplified by the LNA passes through the SAW filter, and is then input to Pin 34 via a matching circuit. The input signal is amplified by the RF amplifier, and then down-converted by the RF mixer to the f_o (1.023MHz) I and Q components. The IF signal down-converted to the I and Q components has the image component eliminated by the phase shifter and the adder, and is then input to the IF filter. Always use a matching circuit for the RF amplifier input pin (Pin 34), and match at 1.57542GHz.



3. IF Filter

The IF signal that passed through the adder has the undesired components outside the band eliminated by the IF Filter. In f_o mode the signal passes through only the LPF and is input to IF AMP2. Set the serial data setting register FIL to "0" for f_o mode (LPF), otherwise IF output level is extremely low. In addition, an external filter can also be connected to this IC using Pins 40 to 43.



4. IF AMP2 and A/D Converter

The signal that passed through the IF filter is amplified by IF AMP2, converted into binary signal by the A/D converter, and then output from the DATA output pin (Pin 8). The A/D converter performs sampling at the TCXO CLK.

In addition, the A/D converter output voltage High level is Vcc2 (1.6 to 3.3V), so a wide range of interfaces can be supported.

5. TCXO (Pin 15)

Input the signal from the external oscillator to Pin 15 via a capacitor as the reference signal. Input frequencies from 10MHz to 26MHz are supported. The input signal level from the external oscillator should be 1.2Vp-p or less (0.6Vp-p typ., 0.2Vp-p min.). This is also the same in power save mode. However, using the typical level of 0.6Vp-p is recommended from the viewpoint of reducing disturbance waves to the receiving system.

6. TCXO CLK Output (Pin 14)

This IC can output TCXO CLK from Pin 14 according to the serial data setting.

The output voltage High level is Vcc2 (1.6 to 3.3V), so a wide range of interface can be supported.

Set the serial data setting register CLK to "0" when not using TCXO CLK, or to "1" when using TCXO CLK. (See page 13.)

7. PLL/VCO

The PLL is comprised by a VCO, frequency divider and phase/frequency detector, as shown in the figure below, and incorporates an inductor, varactor. The loop filter is externally connected. Use components that satisfy the required characteristics.

Serial data setting is unnecessary when this IC is used with the typical TCXO and IF combinations set by the initial settings shown in page 12.

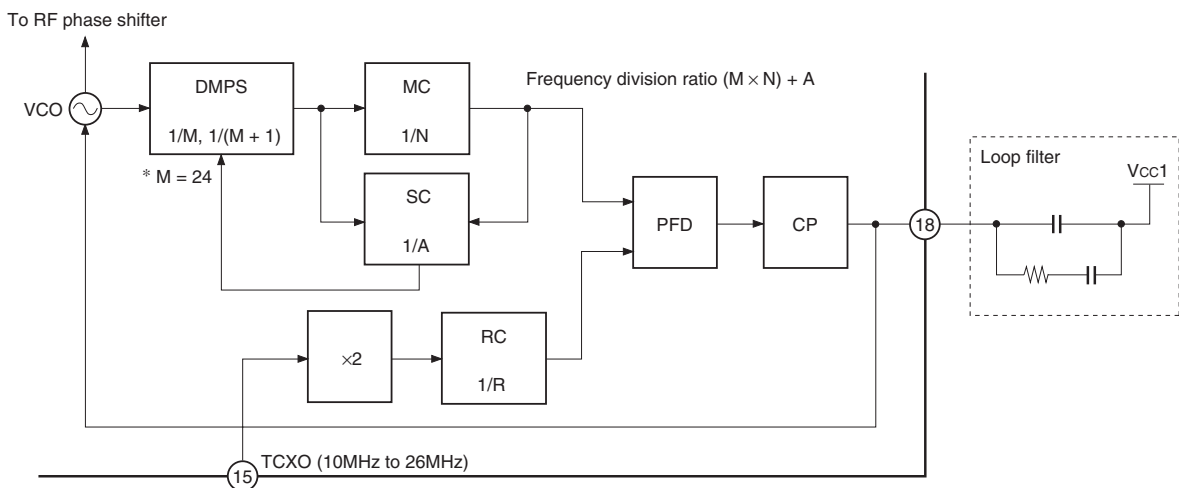
This IC becomes unnecessary in the combination of typical TCXO and IF by serial data initial setting.

When making serial data settings, set counter frequency division values that satisfy the following equations.

- $f_{vco} = (M \times N + A) \times (f_{tcxo} \times 2) \div R$
- $(f_{tcxo} \times 2) \div R > 800\text{kHz}$
- $N \geq 3, R \geq 3$

f_{vco} : VCO oscillation frequency, f_{tcxo} : TCXO frequency

MC data = N, SC data = A, RC data = R, DMPS data = M = 24 (fixed)

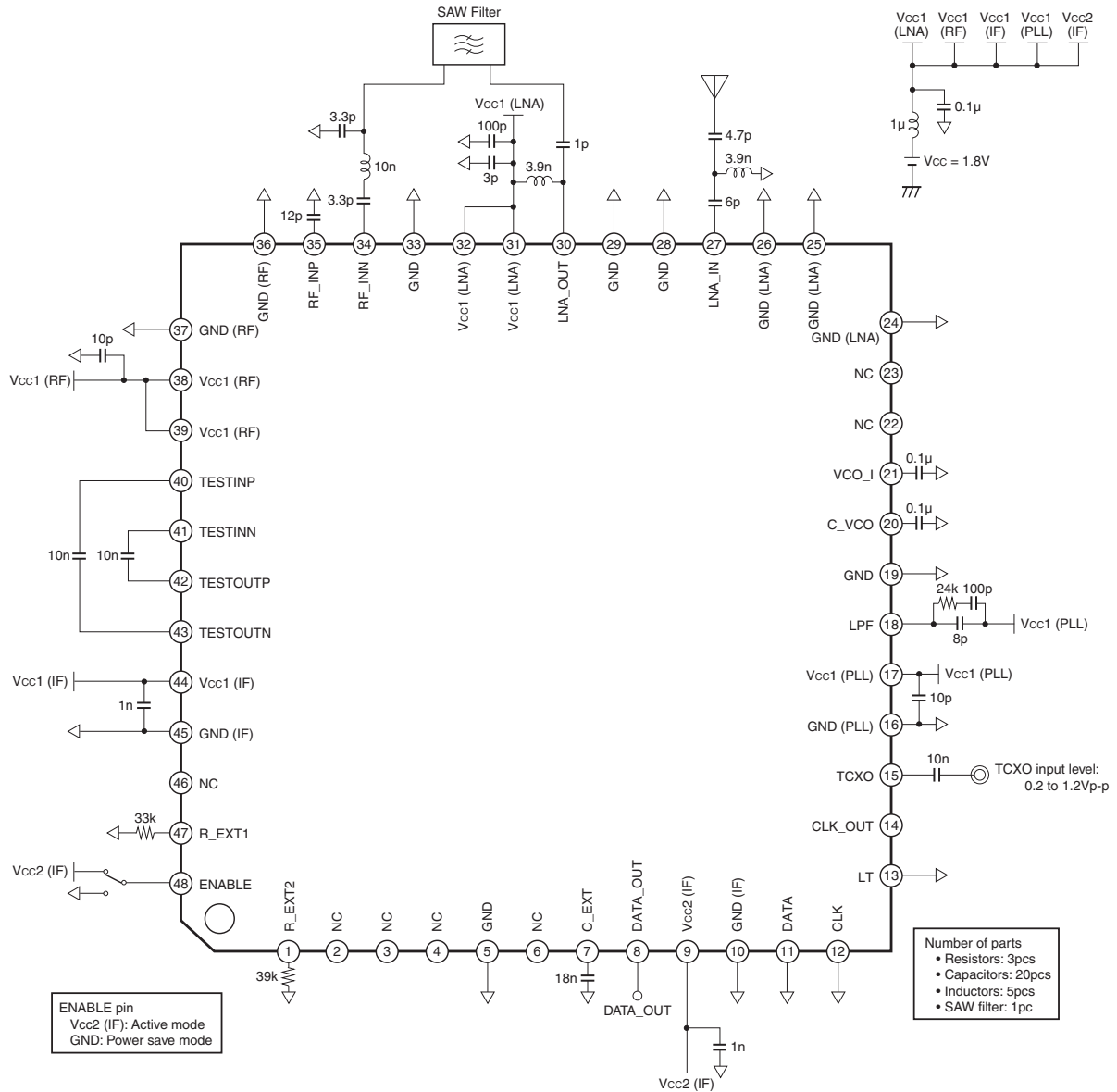


8. ENABLE (Pin 48)

Active mode and power save mode can be switched according to the level.

- High (V_IH: 1.2V min.): Active mode
- Low (V_IH: 0.2V max.): Power save mode

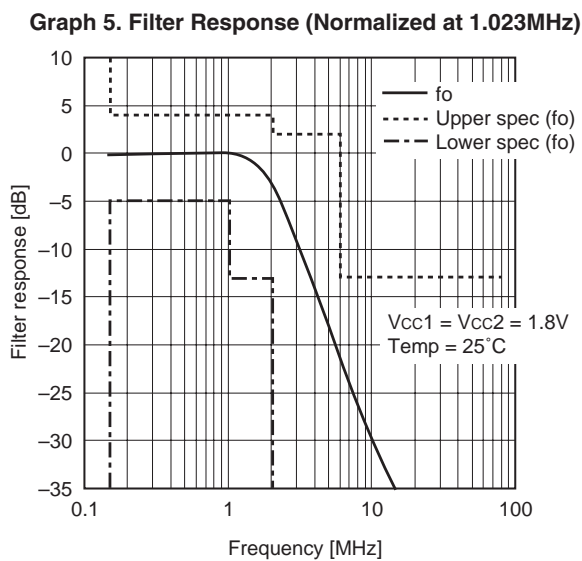
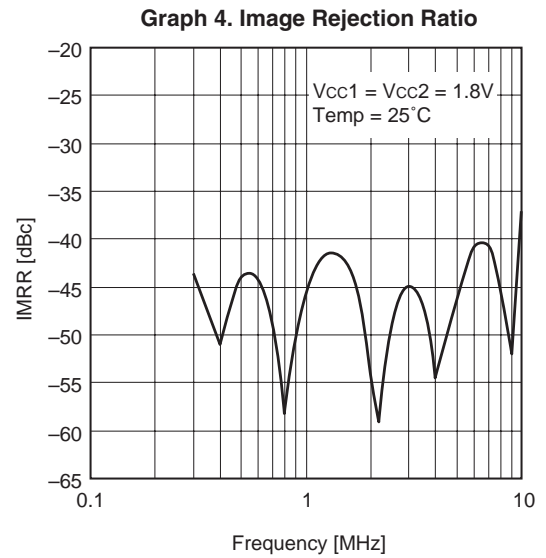
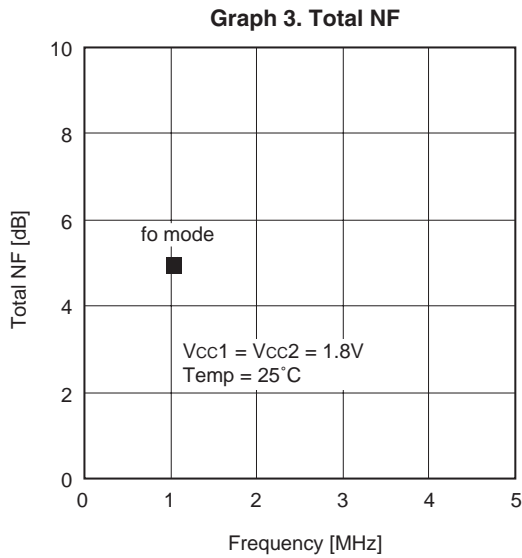
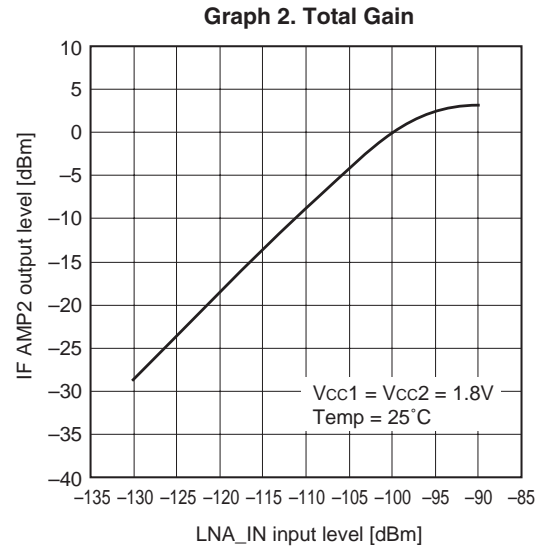
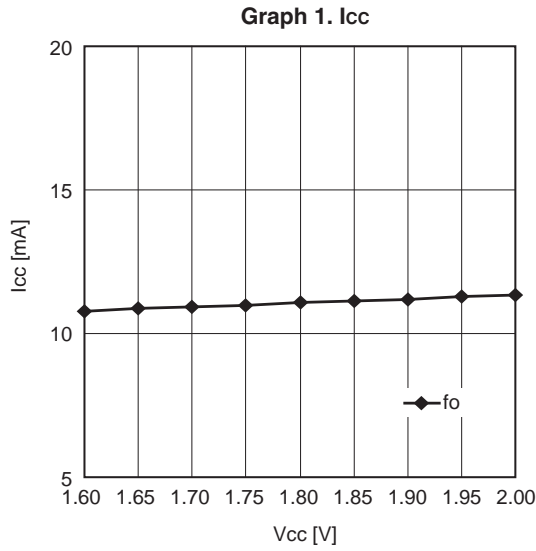
Application Circuit



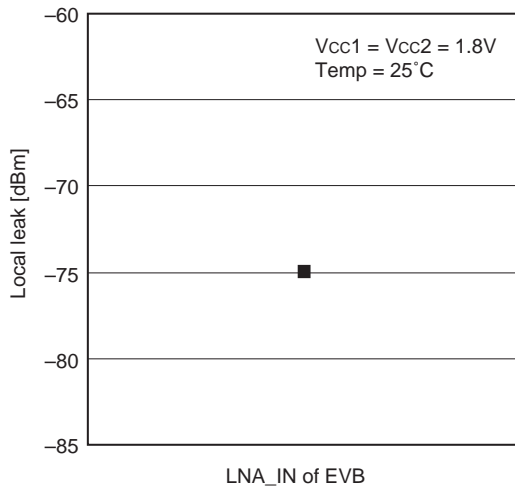
- Note) 1. This diagram shows the application circuit when the initial settings are made for 4fo mode. (See page 13.)
 2. The RF block bypass capacitors should have excellent high frequency characteristics.
 3. Use parts with a tolerance of $\pm 1\%$ for the following resistor elements. Other parts should have a tolerance of $\pm 5\%$.
- Pin 1 (R_EXT2)
 - Pin 18 (LPF)
 - Pin 47 (R_EXT1)

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

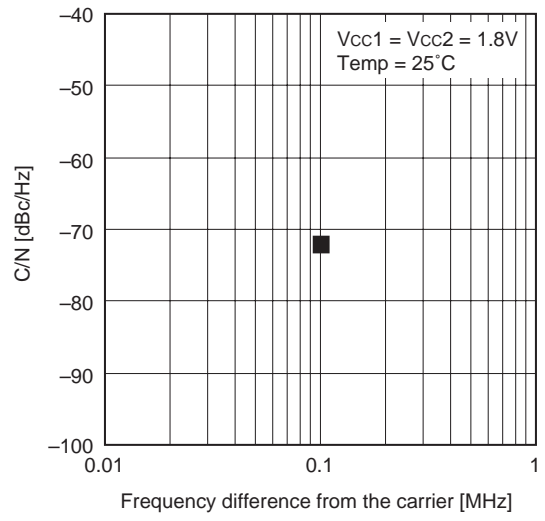
Supplement Materials (Example of representative characteristics)



Graph 6. Local Leak



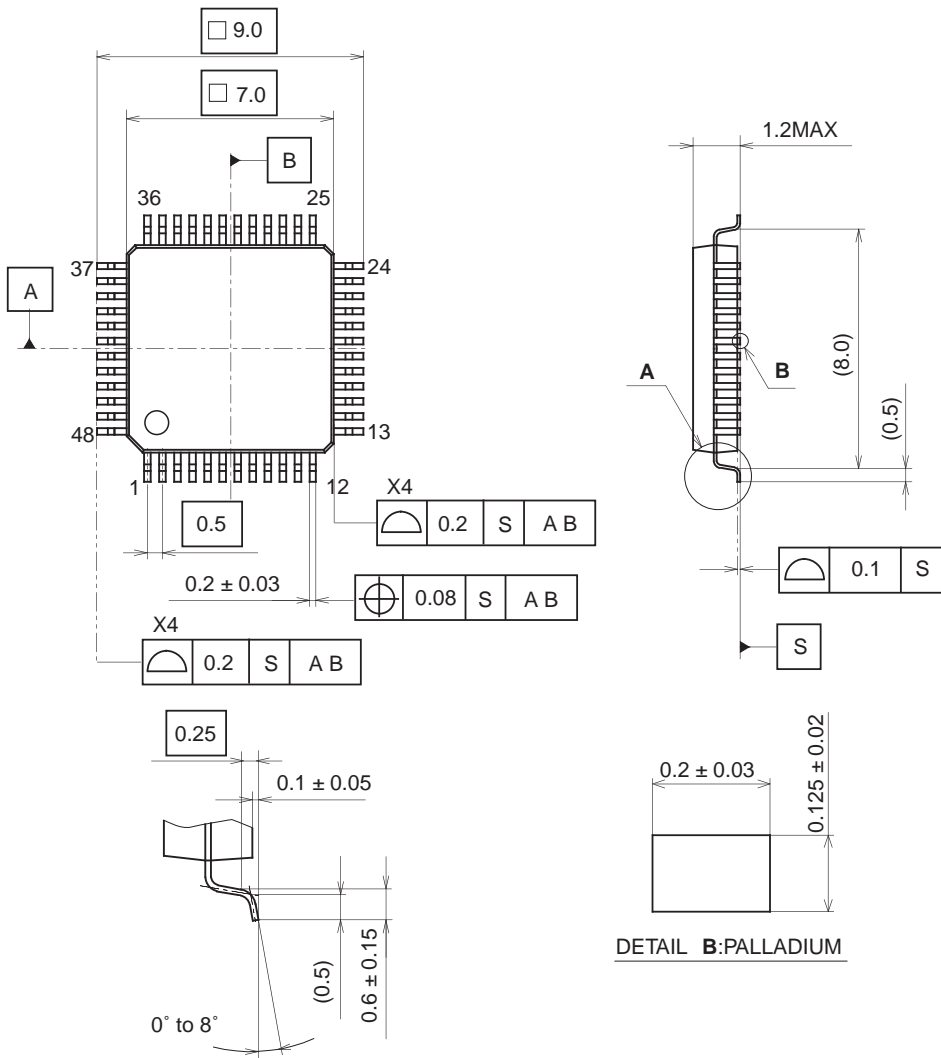
Graph 7. C/N



Package Outline

(Unit: mm)

48PIN TQFP (PLASTIC)



DETAIL A

DETAIL B: PALLADIUM

PACKAGE STRUCTURE

SONY CODE	TQFP-48P-L01
EIAJ CODE	P-TQFP48-7.0X7.0-0.5
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g