SONY

CXA3271AGE

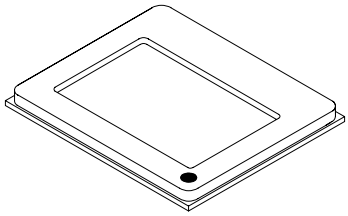
Fingerprint Sensor

Description

The CXA3271AGE is an electrostatic capacitance method fingerprint sensor.

This monolithic IC integrates the sensor block, sense amplifier (3-bit gain adjustment), sample-and-hold, output amplifier and output buffer needed to acquire fingerprint images, as well as the timing generator for determining the operation of these functions onto a single chip.

30 pin LLGA (Plastic)



Features

- Electrostatic capacitance type sensor (charge transfer method)
- Number of pixels: 192 × 128
- 317 DPI
- Low power consumption (50mW or less)
- Single 3.3V power supply
- Sensor gain control: 3 bits
- S/N ratio improved by on-chip sensor block parasitic capacitance cancel function

Applications

Fingerprint verification units

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{DD}, DV_{DD}	V_{SS} – 0.5 to +7.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–25 to +125	°C
• Allowable power dissipation	P_D	1100	mW

Recommended Operating Conditions

• Supply voltage	AV_{DD}, DV_{DD}	3.15 to 3.45	V
• Ambient operating temperature	Ta	0 to +50	°C

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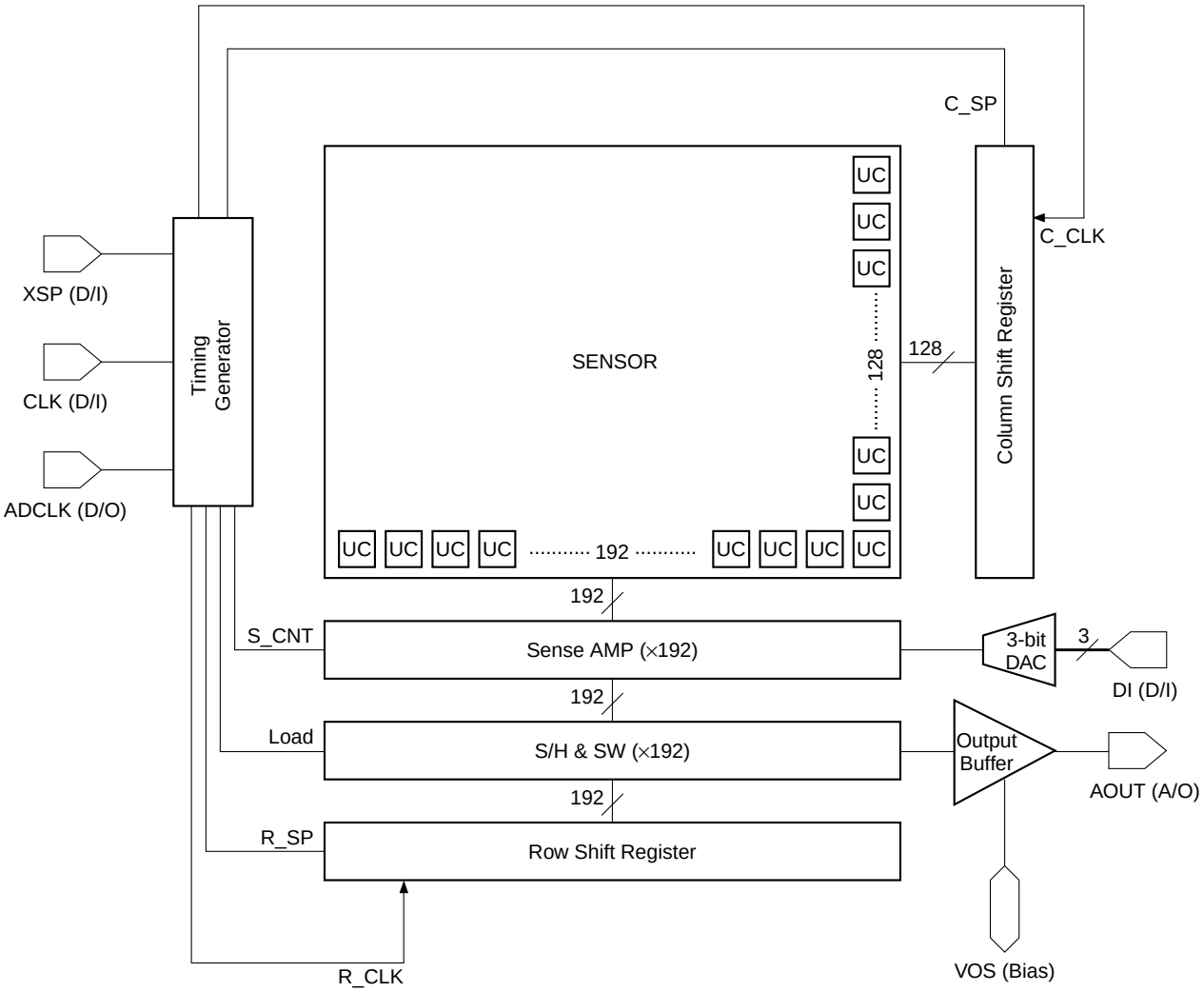
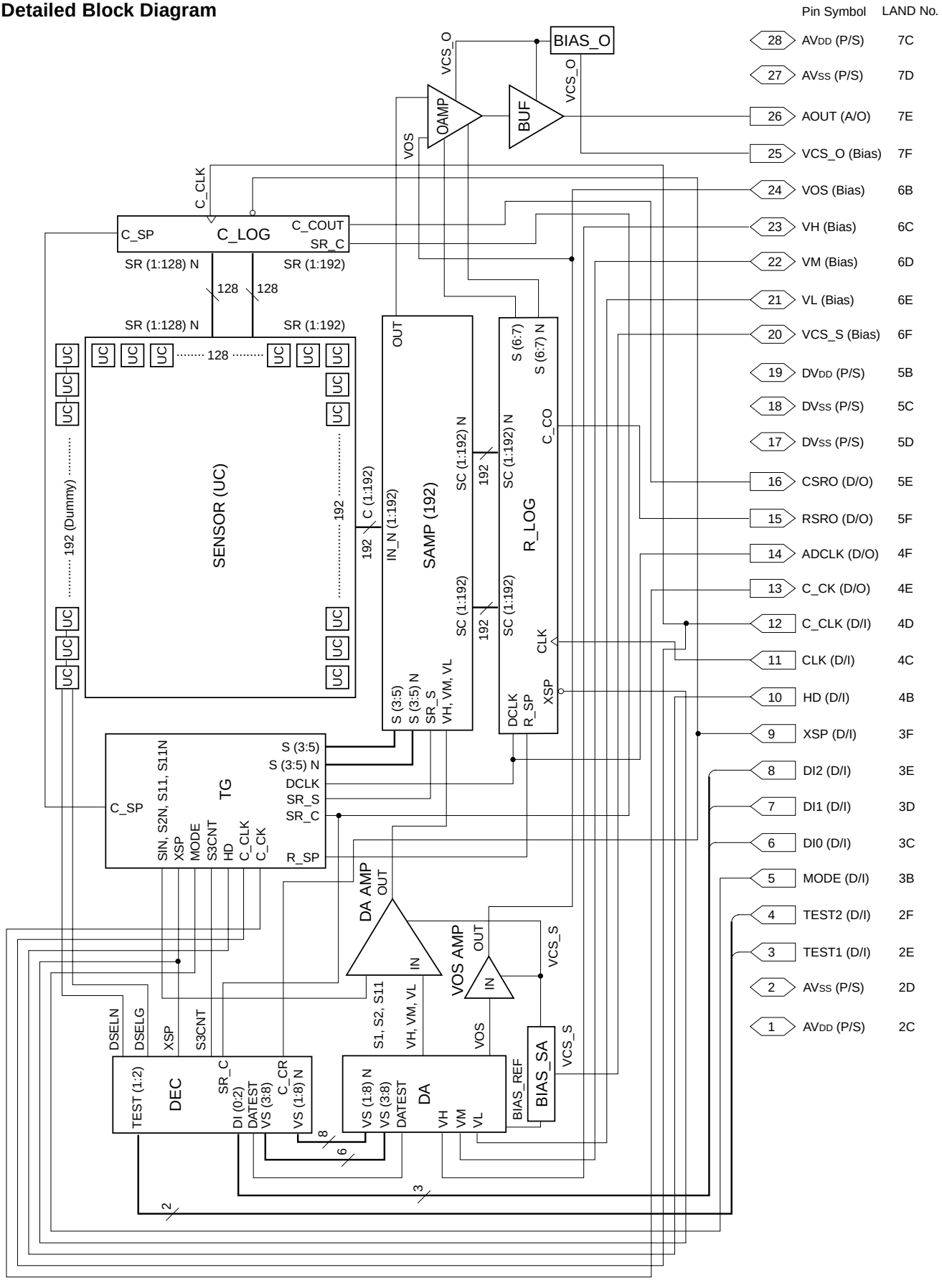
E00Y20-PS

Block Diagram



Detailed Block Diagram



Pin Description

Serial No.	Land No.	Symbol	I/O	Description
	2B	SUB	Power	Substrate electrode (chip rear surface electrode) 3.3V.
1	2C	AV_{DD}	Power	Analog power supply 3.3V.
2	2D	AV_{SS}	Power	Analog GND.
3	2E	TEST1	D/I	Test mode selection. Connect to GND.
4	2F	TEST2	D/I	Test mode selection. Connect to GND.
5	3B	MODE	D/I	Connect to GND.
6	3C	DI0	D/I	Gain setting input. (LSB)
7	3D	DI1	D/I	Gain setting input.
8	3E	DI2	D/I	Gain setting input. (MSB)
9	3F	XSP	D/I	Sense start pulse input (negative pulse). The column and row shift registers and the timing generator are cleared by this signal.
10	4B	HD	D/I	Connect to GND.
11	4C	CLK	D/I	Main clock. (1 to 2MHz)
12	4D	C_CLK	D/I	Column shift register clock. Connect to C_CK (4E).
13	4E	C_CK	D/O	Column shift register clock output. Connect to C_CLK (4D).
14	4F	ADCLK	D/O	Outputs the internally delayed input clock.
19	5B	DV_{DD}	Power	Digital power supply 3.3V.
18	5C	DV_{SS}	Power	Digital GND.
17	5D	DV_{SS}	Power	Digital GND.
16	5E	CSRO	D/O	Column shift register final output. (Connection is not required.)
15	5F	RSRO	D/O	Row shift register final output. (Connection is not required.)
24	6B	VOS	A/O	Output amplifier reference voltage monitor. (1.65V)
23	6C	VH	A/O	Sensor charge voltage monitor. (1 LSB = 80mV) Adjustable within the range of 1.92 to 2.48V by the three bits DI[0:2].
22	6D	VM	A/O	Sense amplifier reference voltage monitor. (1.85V)
21	6E	VL	A/O	Dummy cell charge voltage monitor for canceling parasitic capacitance. VL = 2VM – VH
20	6F	VCS_S	A/O	Sense amplifier current source bias monitor. (Do not connect.)
	7B	SUB	Power	Substrate electrode (chip rear surface electrode) 3.3V.
28	7C	AV_{DD}	Power	Analog power supply 3.3V.
27	7D	AV_{SS}	Power	Analog GND.
26	7E	AOUT	A/O	Sensor output.
25	7F	VCS_O	A/O	Output amplifier and output buffer current source bias monitor. (Do not connect.)

Electrical Characteristics

1. DC Characteristics

(Vss = 0V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Analog supply voltage	AV_{DD}		3.15	3.3	3.45	V
Digital supply voltage	DV_{DD}		3.15	3.3	3.45	V
Input voltage (High)	V_{IH}	CMOS input cell	0.7V_{DD}		V_{DD}	V
Input voltage (Low)	V_{IL}	CMOS input cell	Vss		0.3V_{DD}	V
Output voltage (High) CMOS	V_{IH}	V_{DD} = 3.3V, I_{OH} = –800µA	2.8		3.3	V
Output voltage (Low) CMOS	V_{IL}	V_{DD} = 3.3V, I_{OL} = 2.4mA	0		0.4	V
Input leak current	I_L	V_{DD} = 3.3V, CMOS input pin (3.3V/0V)	–5		5	µA
Output voltage	VH	V_{DD} = 3.3V (D0 D1 D2) = (L L L)		1.92		V
Output voltage	VH	V_{DD} = 3.3V (D0 D1 D2) = (H H H)		2.48		V
Output voltage	VL	V_{DD} = 3.3V (D0 D1 D2) = (L L L)		1.76		V
Output voltage	VL	V_{DD} = 3.3V (D0 D1 D2) = (H H H)		1.2		V
Output voltage	VM	V_{DD} = 3.3V (D0 D1 D2) = (∗ ∗ ∗)	1.75	1.84	1.92	V
Output voltage	VOS	V_{DD} = 3.3V (D0 D1 D2) = (∗ ∗ ∗)	1.55	1.65	1.75	V
Current consumption	I_{DD}	V_{DD} = 3.3V	5	7.5	11	mA

2. AC Characteristics

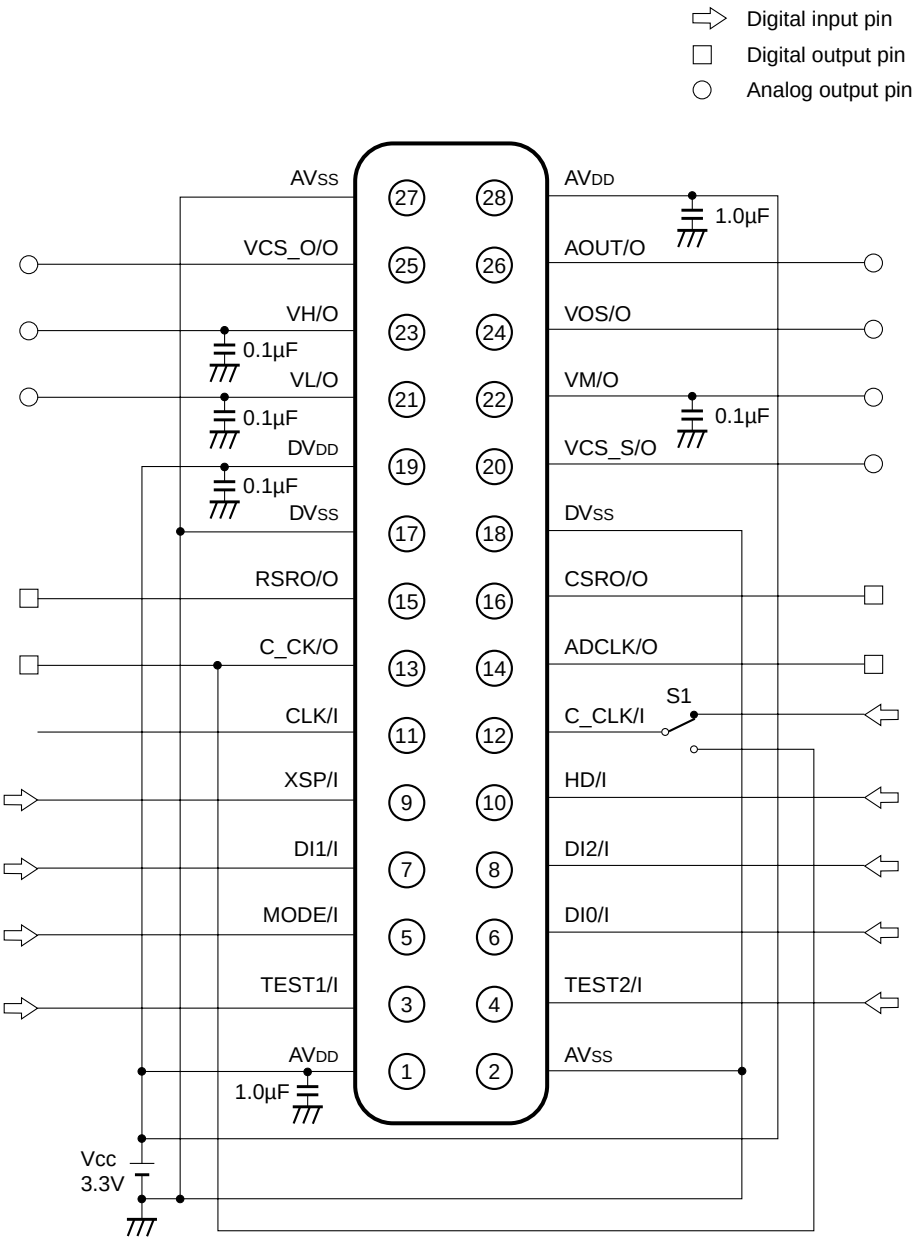
(V_{DD} = 3.3V, V_{SS} = 0V, Ta = 25°C)

Item	Applicable pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock input period	CLK			400			ns
Number of sensor defects						5	Defects
Output voltage Air Level	AOUT		∗1	1000		1550	mV
Output voltage Water Level	AOUT		∗2	250		450	mV

∗1 Output voltage Air Level means the output level in the condition where nothing is placed against the sensor surface (in other words, in air). This rating value is obtained by measuring 32 points within one line of the sensor output and then taking the average.
The gain setting for this measurement is (011).

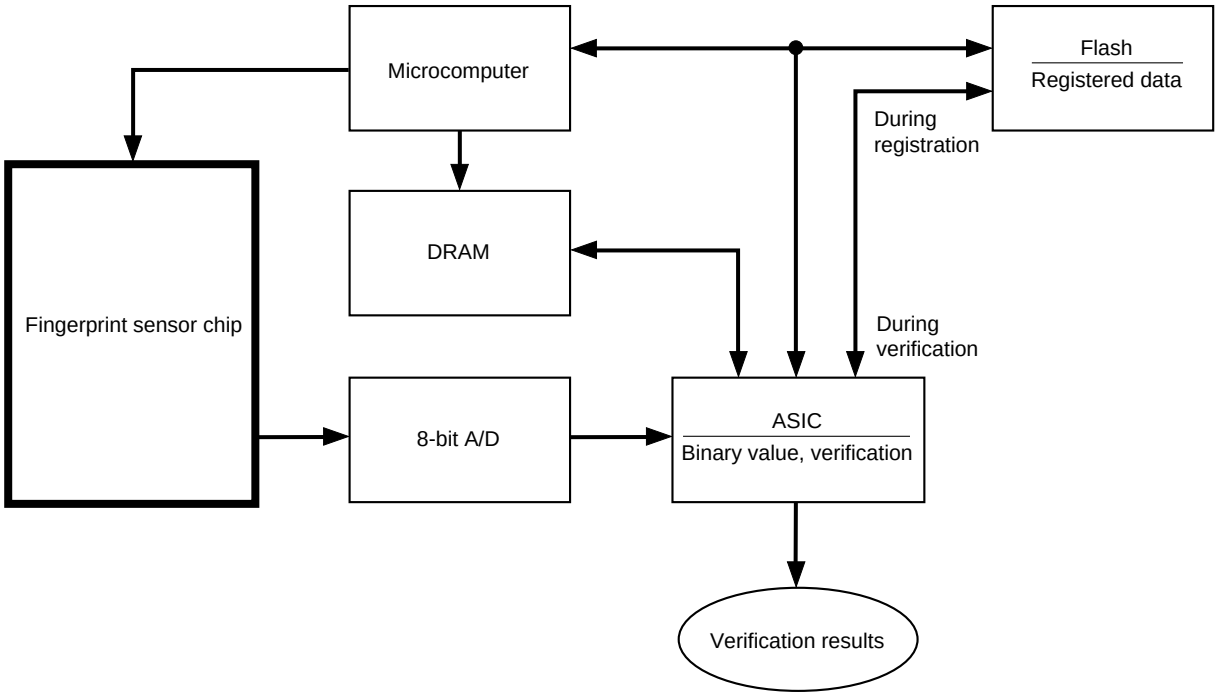
∗2 Output voltage Water Level specifies the degree to which the output level changes from the Air Level when a drop of water is placed on the sensor surface. However, it is unrealistic to place a drop of water on each sensor surface when sorting products, so 32 virtual capacitors (parasitic capacitance equal to the level when a drop of water is placed on the surface) are built into the sensor chip, and the average of these output values is calculated. The difference from the Air Level noted above becomes the Water Level.
The gain setting for this measurement is (011).

Electrical Characteristics Measurement Circuit



30pF or more is added to each pin.

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

• Fingerprint sensor principle

The principle of this newly developed fingerprint sensor is described below (Fig. 1). The sensor block contains an array of metal electrodes which are covered on top by an insulating film (overcoat). When a finger (which is conductive matter) is placed directly against this surface, the three elements of the metal electrode, the insulating film and the finger form a capacitor.

The difference between the fingerprint ridges and valleys is the difference in distance to the metal electrodes, and becomes the difference in the capacitance values of the individually formed capacitors. (The ridge capacitance values are determined by the dielectric constant of the insulating film, but the valleys contain air in addition to this, making the difference between the ridge and valley capacitance values even greater than the difference in distance.)

Using this principle, by applying a constant voltage to all metal electrodes, the charge level accumulated in each electrode differs, making it possible to output the unevenness of the fingerprint as an electric signal by transferring and converting these charges to voltages.

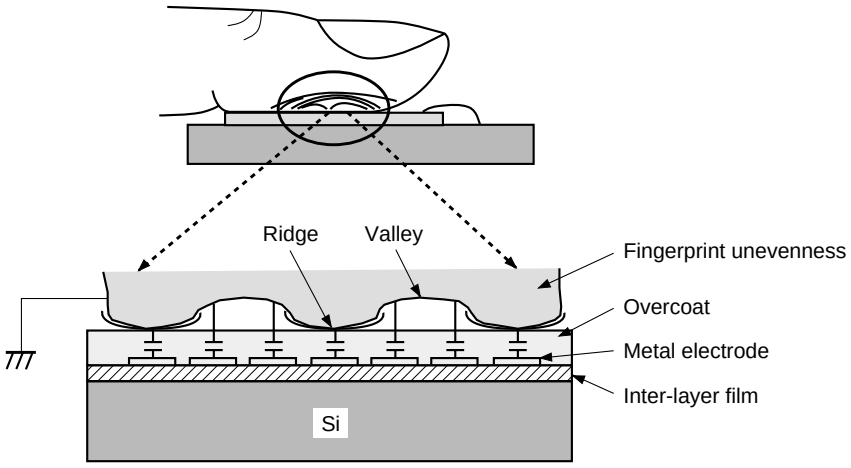


Fig. 1

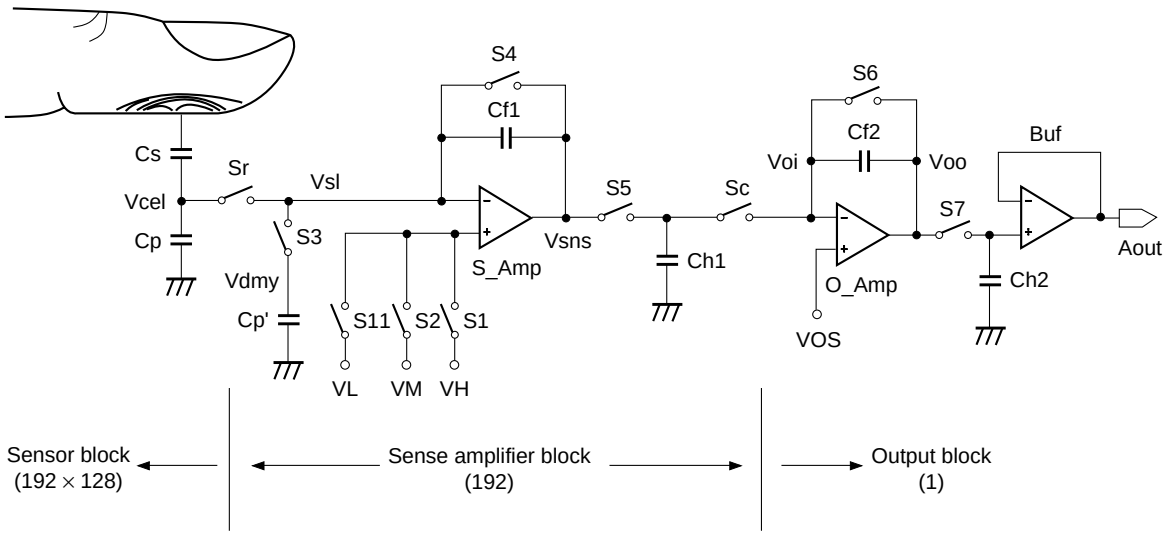


Fig. 2

• Fingerprint sensor operation (Fig. 2)

Description of characters

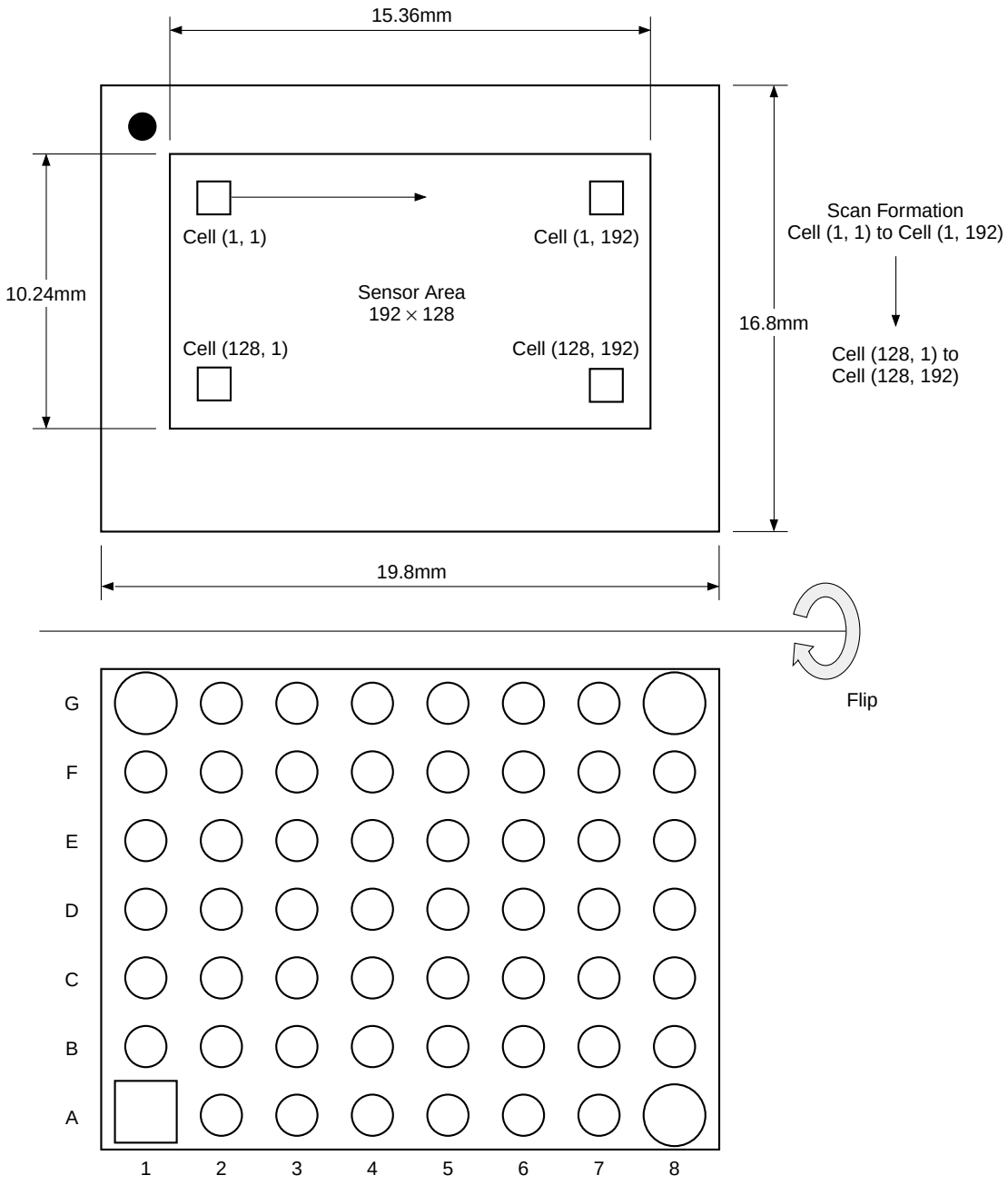
Cs: Capacitance formed between the finger and the metal electrode
Cp: Parasitic capacitance formed between the metal electrode and the silicon substrate
Cp': Capacitance for canceling Cp (Cp ≈ Cp')
Ch∗: Hold capacitance
Cf∗: Feedback capacitance for determining the gain
S∗: Switch
V∗: Node voltage
VH – VM ≈ VM – VL

• Detailed description of operation

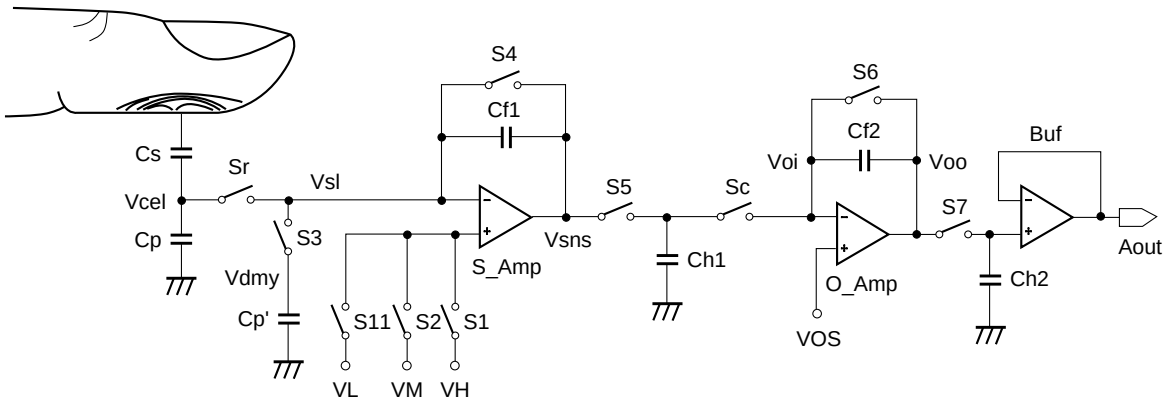
(All switches are off in the default status.)

1. S1, S4 and Sr are turned on, and Vcel is set to voltage VH.
   Vcel accumulated charge (Cs + Cp) VH
2. S1 and Sr are turned off.
3. S11 and S3 are turned on, and Vdmy is set to voltage VL.
   Vdmy accumulated charge Cp'VL
4. S3 and S11 are set to off.
5. S2 is turned on and Vsl is set to VM.
6. S4 is turned off.
7. Sr, S3 and S5 are turned on.
   At this time, the charge level that moves from Vcel and Vdmy to Vsl (actually between capacitances) is:
   (Cs + Cp) (VH – VM) – Cp' (VM – VL) ≈ Cs (VH – VM)
   This means that the sense amplifier gain is determined independently of the parasitic capacitance, making it possible to obtain the required large signal dynamic range.
   Vsns = VM – Cs (VH – VM)/Cf1
   The voltage Vsns determined as shown above is accumulated in Ch1.
8. S5 is turned off.
9. S6 is turned on and the Voi voltage is set to VOS.
10. S6 is turned off.
11. Sc and S7 are turned on.
    At this time, the charge level that moves from Ch1 to Cf2 is:
    (VOS – Vsns) Ch1
    This determines the Voo voltage which is accumulated in Ch2 and output to Aout via the buffer.

Appearance and Readout Order



Notes on Operation



• Aout output variance

Aout output variance can be broadly classified into two types. The first is variance intrinsic to the IC, and the second is variance caused by the influence of external noise due to the extremely high sensitivity.

• Variance intrinsic to the IC

1. The Aout output DC level fluctuates widely due to the IC.
   This is caused by the Cp and Cp' capacitance values, the VM voltage level, the voltage differences VH – VM and VM – VL, and the VOS voltage level in the figure above.
   VOS, VH, VM and VL appear externally as pins. The Aout output level can be set to the desired potential by applying the VOS voltage from an external source.
   The Aout dynamic range is approximately 0.6 to 2.1V, so checking this output level and externally applying the VOS voltage to set the optimum level is recommended.
2. 192 variances within one line
   One line is comprised of 192 sensors. Each sensor is connected to a separate S_Amp, so the S_Amp offset appears in the output. (approximately 100 to 200mV)
3. The DC level of a line changes with a certain regularity for some ICs. This is also caused by the S_Amp DC offset.

• Variance due to the influence of external noise

1. Output fluctuation due to cross talk from the power supply
   Power supply fluctuation has a large influence on the Aout output of this IC.
   In addition to the capacitances between the power supply and GND (approximately 1µF, both sides if possible), attaching capacitances of approximately 0.1µF to VOS, VH, VM and VL is recommended.
2. Finger stabilization
   The human body acts as an antenna, so the finger potential changes during the sensing period, producing noise in the Aout output. To prevent this, the potential of the area around the finger being sensed must be equalized with the sensor GND. Measures such as placing a metal plate connected to GND around the sensor so that the finger touches this place during sensing are recommended.

Fingerprint sensors have the silicon chip directly exposed, so care should be taken for the following points. In addition, a cover should be attached to protect the sensor surface during operation.

Sensor surface electrostatic strength

Contact discharge (150pF, 330Ω): ±1.25kV or more
Body charge (when the charge accumulated in the body is discharged over the sensor surface): ±4kV or more
Body charge differs between individuals.

Sensor surface strength

The sensor surface is covered with only a thin coating in order to acquire fingerprint information.
Therefore, care should be taken when handling the sensor.

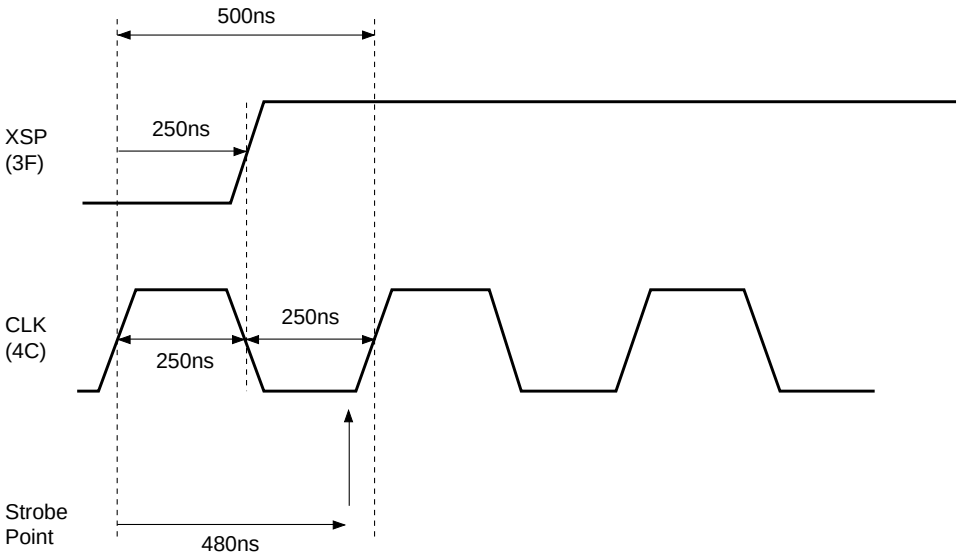
Problems have been confirmed not to occur during the following tests.

- Pressing 10,000 times with a finger (Pressing time: 2s/time)
- Rubbing 10,000 times with a finger (Back and forth, 2s/time)
- Scratching with a fingernail (20 times back and forth)
- Rubbing strongly with a pencil (6H hardness) (20 times back and forth)
- Rubbing with a tissue (1,000 times back and forth)

Note that problems also occurred with the sensor surface during the following tests.

- Pressing strongly with a needle (normal sewing needle)
- Rubbing with an eraser
- Rubbing with the tip of a ball point pen
- Rubbing with steel wool

Timing Chart



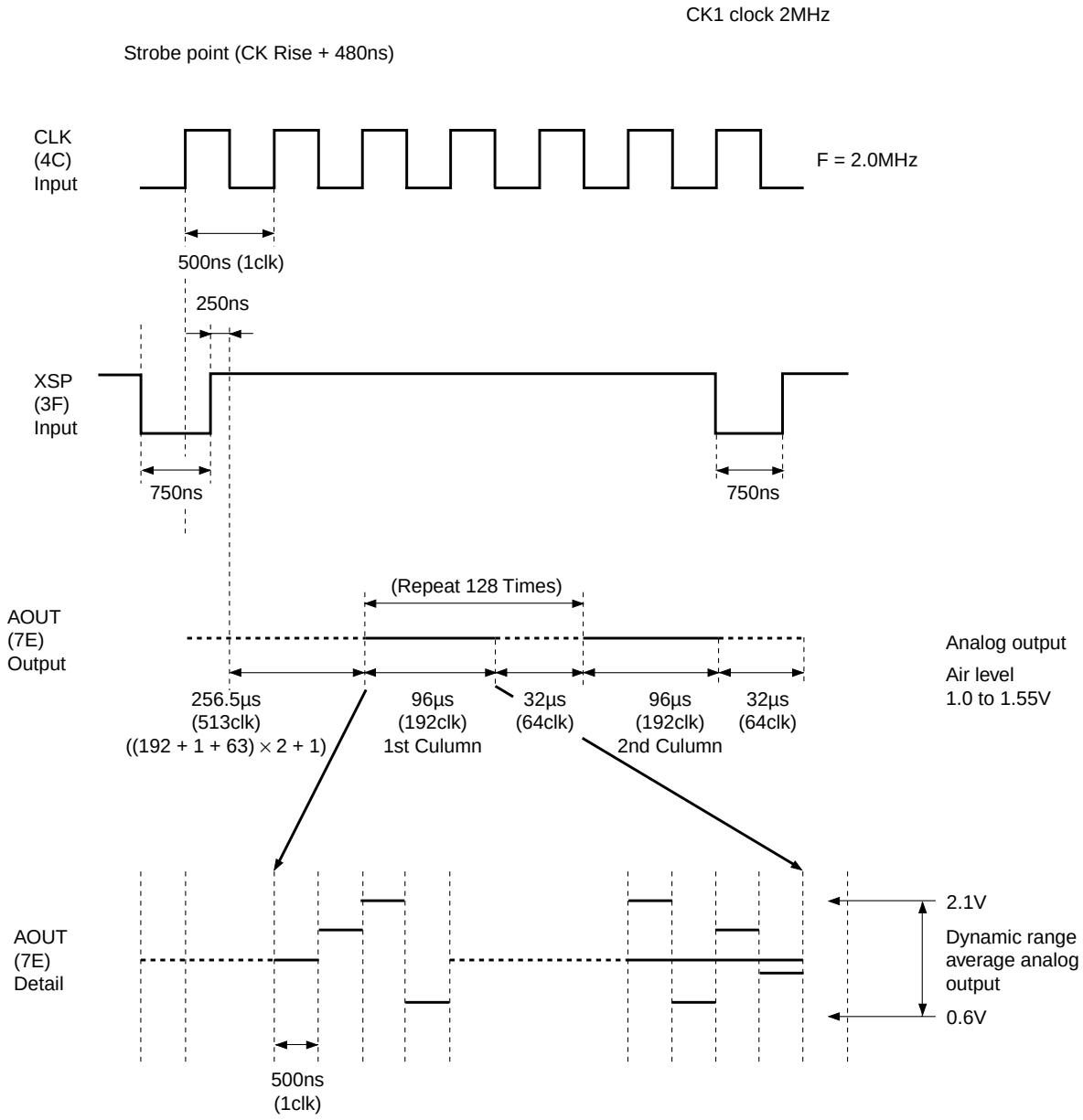
Input level

$V_{IH} = 0.7V_{DD}$
$V_{IL} = 0.3V_{DD}$

Output level

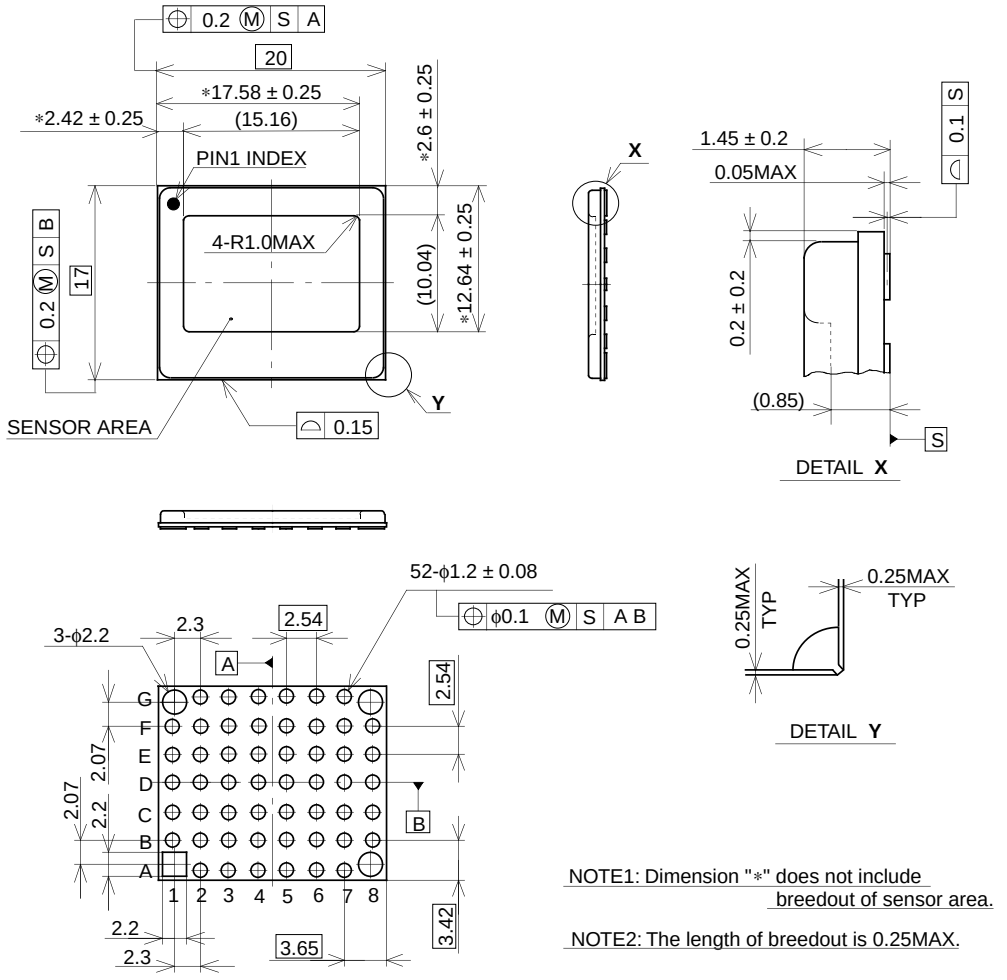
High
$0.65V_{DD}$ ----------
X
$0.35V_{DD}$ ----------
Low

Input/Output Signal



Package Outline Unit: mm

30PIN LLGA (PLASTIC)



NOTE1: Dimension "∗" does not include breedout of sensor area.

NOTE2: The length of breedout is 0.25MAX.

SONY CODE	LLGA-30P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	ORGANIC SUBSTRATE
TERMINAL TREATMENT	GOLD PLATING
TERMINAL MATERIAL	COPPER PLATING
PACKAGE MASS	0.7 g