SK100EL16Y
High Gain Differential Receiver with Variable Output Swing

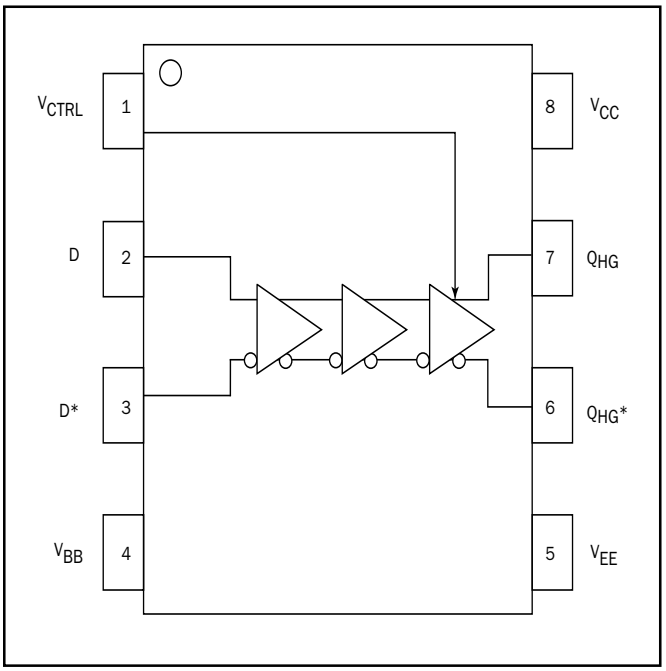
Description

The SK100EL16Y is a high gain differential receiver with variable output swing. Its VCTRL input controls the amplitude of the Q_{HG} and Q_{HG}* outputs. The operating range of the EL16Y control input, VCTRL, is from VBB (large swing) to VCC (min swing), see Figure 2. Simple control of the output swing can be obtained by a variable resistor between the VBB and VCC pins, with wiper driving CTRL. Typical application circuit and results are described in Figures 1a, 1b, and 2.

The SK100EL16Y provides a VBB output for either single-ended use or as a DC bias for AC coupling to the device. The VBB pin should be used only as a bias for the EL16Y as its current sink/source capability is limited. Whenever used, the VBB pin should be bypassed to VCC via a 0.01 µF capacitor.

The VCTRL pin should be bypassed to VCC via a 0.01 µF capacitor when the pin is used.

Functional Block Diagram



Features

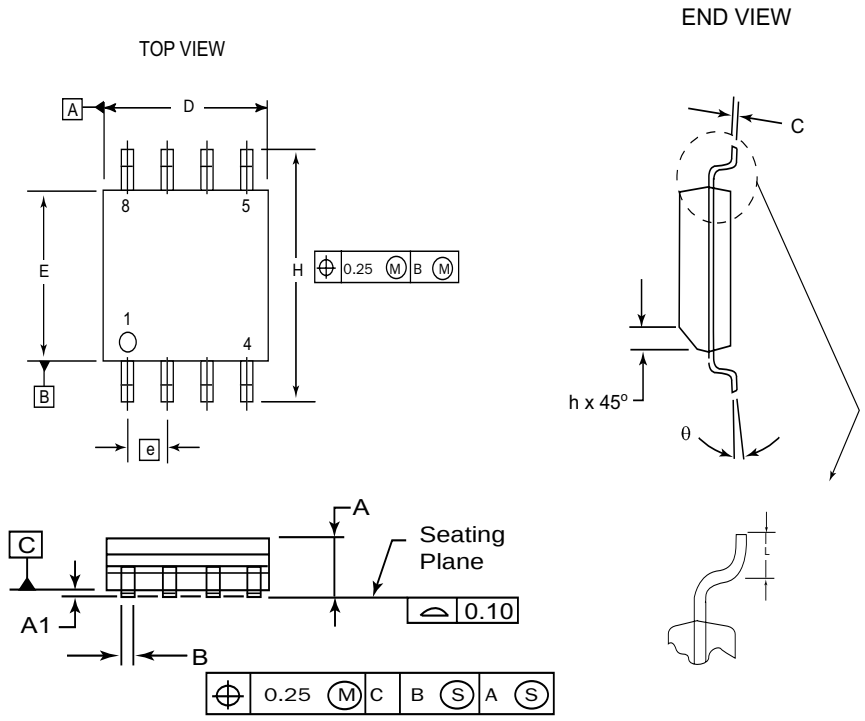
- Extended Supply Voltage Range: (VEE = –5.5V to –3.0V, VCC = 0V) or (VCC = +3.0V to +5.5V, VEE = 0V)
- High Bandwidth Output Transitions
- 400 ps Propagation Delay (typical)
- VBB Output
- New Differential Input Common Mode Range
- ESD Protection of >4000V
- Specified Over Industrial Temperature Range: –40°C to 85°C
- Available in Both 8 Pin SOIC (150 mil) and MSOP (3mm x 3mm) Packages
- Flammability Rate: UL-94 code V-0.
- Moisture Sensitivity: Level 1.

PIN Description

Pin	Function
D, D*	Differential Data Inputs
Q_{HG}, Q_{HG}*	Differential Data Outputs
VBB	VBB Ref Voltage Output
VCTRL	Output Swing Control

Package Information

8 Pin SOIC Package

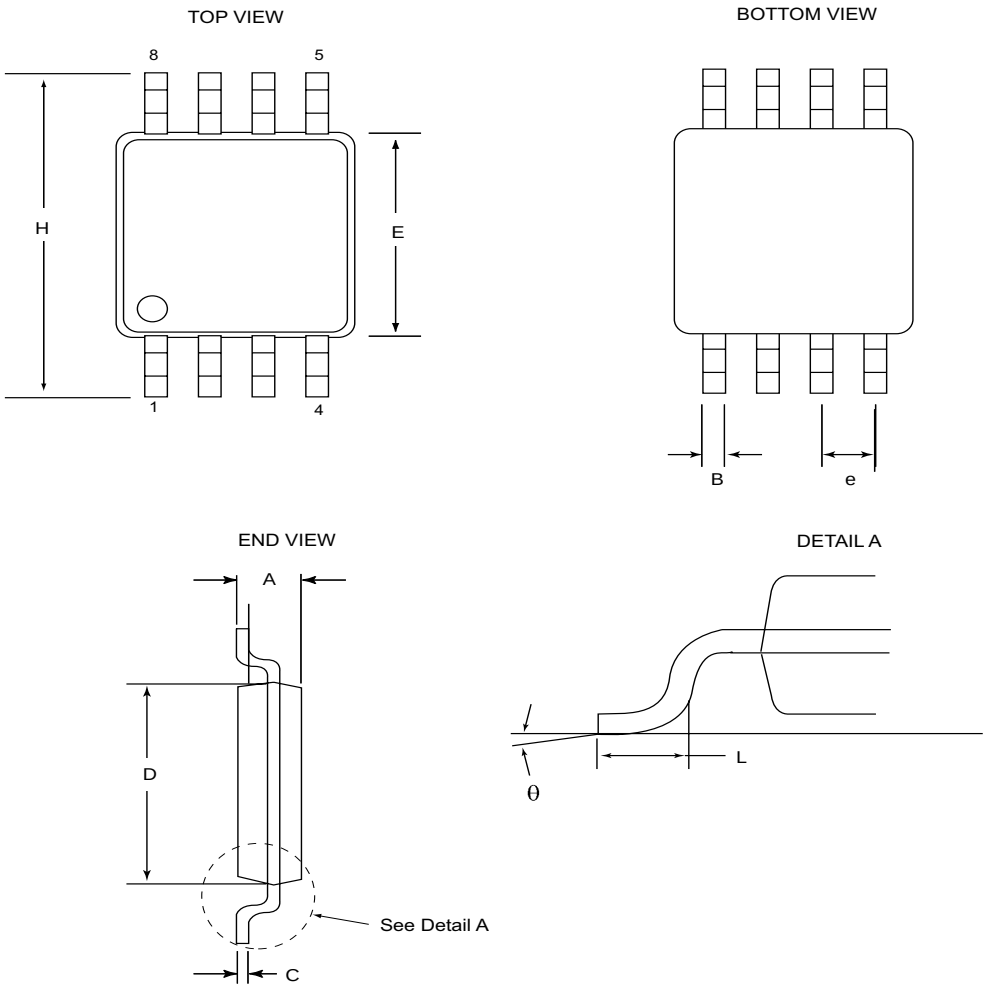


DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

NOTES:
1. Dimensions are in millimeters.
2. Dimensions D and E do no include mold protrusion.
3. Maximum mold protrusion 0.15 per side.
4. Dimension B does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.127 total in excess of the B dimension at maximum material condition.

Package Information *(continued)*

8 Pin MSOP Package



DIM	Millimeters	
	MIN	MAX
A	0.94	1.1
B	0.21	0.45
C	0.13	0.22
D	2.90	3.10
E	2.90	3.10
e	0.65 BSC	
H	4.7	5.1
L	0.4	0.7
θ	0°	6°

NOTES:
1. Dimensions are in mm.
2. Controlling dimension: mm
3. Dimension does not include mold flash or protrusions, either of which shall not exceed 0.20.

DC Characteristics

SK100EL16Y DC Electrical Characteristics *(Note 1)*

(V_{EE} = –3.0V to –5.5V; V_{CC} = 0V; V_{OUT} loaded 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = –40°C		TA = 0°C to +85°C		Unit	Condition
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage [8]	– 1085	– 880	– 1025	– 880	mV	$V_{IN} = V_{IHmax}$ or V_{ILmin}
V_{OL}	Output LOW Voltage [8]	– 1950	– 1555	– 1950	– 1620	mV	$V_{IN} = V_{IHmax}$ or V_{ILmin}
V_{IH}	Input HIGH Voltage	– 1165	– 880	– 1165	– 880	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW Voltage	– 1810	– 1475	– 1810	– 1475	mV	Guaranteed LOW signal for all inputs
V_{BB}	Reference Output Voltage	-1430	-1260	-1430	-1260	mV	
I_{EE}	Power Supply Current		45		45	mA	
I_{IN}	Input Current: D, D* (Diff) VCTRL (SE)		150 150		150 150	µA µA	

AC Characteristics

SK100EL16Y AC Electrical Characteristics

(V_{CC} – V_{EE} = 3.0V to 5.5V; V_{OUT} loaded 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{max}	Maximum Toggle Frequency [3]	2.5			2.5			2.5			2.5			GHz	
t_{PLH} t_{PHL}	Propagation Delay to Output (DIFF)	250	300	350	250	300	350	250	305	360	250	315	380	ps	
A_V	Small Signal Gain [4]		43			43			43			43		dB	
t_{skew}	Duty Cycle Skew [2] (DIFF)		5	20		5	20		5	20		5	20	ps	
t_r , t_f	Output Rise/Fall Times Q_{HG} (20% to 80%)	80	120	140	80	120	140	90	120	150	90	135	180	ps	
V_{CMR}	Common Mode Range [6]	V_{EE}+1.5		VCC	V_{EE}+1.5		VCC	V_{EE}+1.5		VCC	V_{EE}+1.5		VCC	V	
V_{PP}	Differential Input Swing [5]	150		1000	150		1000	150		1000	150		1000	mV	
VO_{P-P}	Output Voltage [7]			200			200			200			200	mV	$V_{CTRL}=V_{CC}$

Notes:

1. 100K circuits are designed to meet the DC specification shown in the table where transverse airflow greater than 500 lfpm is maintained.
2. Duty cycle skew is the difference between T_{PLH} and T_{PHL} propagation delay through a device.
3. F_{max} guaranteed for functionality only. See Figure 3 for typical output swing. VO_{P-P} levels are guaranteed at DC only.
4. The device has a DC gain of ~140.
5. Minimum input swing for which parameters are guaranteed.
6. CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between $VPP_{(min)}$ and 1V. The lower end of the CMR range varies 1:1 with VEE and is equal to VEE + 1.5V.
7. VO_{P-P} is obtained as follows: Voltages of Q_{HG} and Q_{HG}* outputs with respect to VCC are measured. The absolute difference between a high and a low state is equal to VO_{P-P}.
8. The VOH and VOL limits apply when the V_{CTRL} pin is left open. Otherwise, see figure 2.
9. For part ordering description, see HPP Part Ordering Information Data Sheet.

AC Characteristics *(continued)*

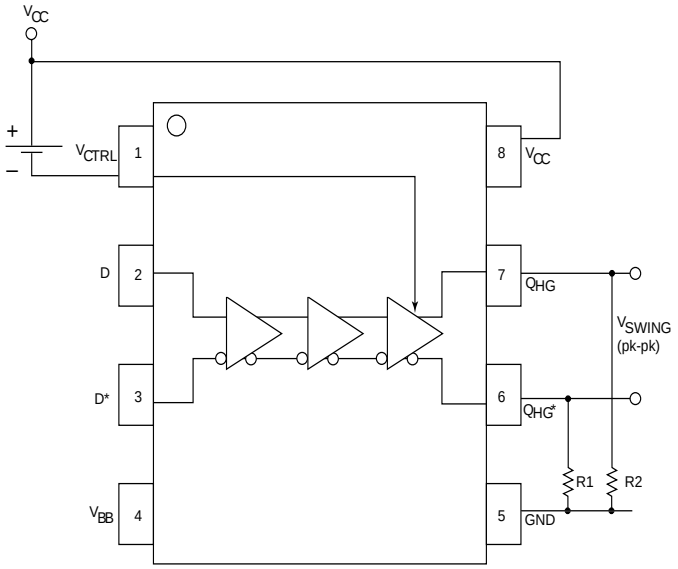


Figure 1A

Note: R1 = R2 150Ω for VCC = 3.3V
R1 = R2 330Ω for VCC = 5.0V

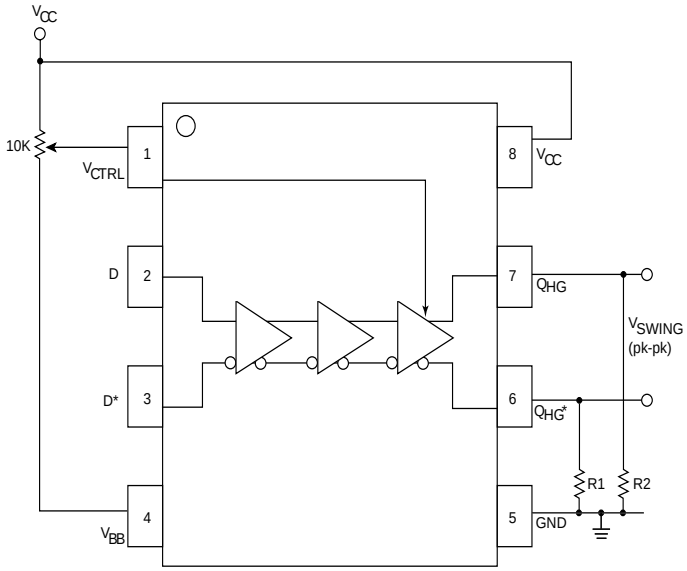


Figure 1B

Note: R1 = R2 150Ω for VCC = 3.3V
R1 = R2 330Ω for VCC = 5.0V

Implementation of Voltage Source

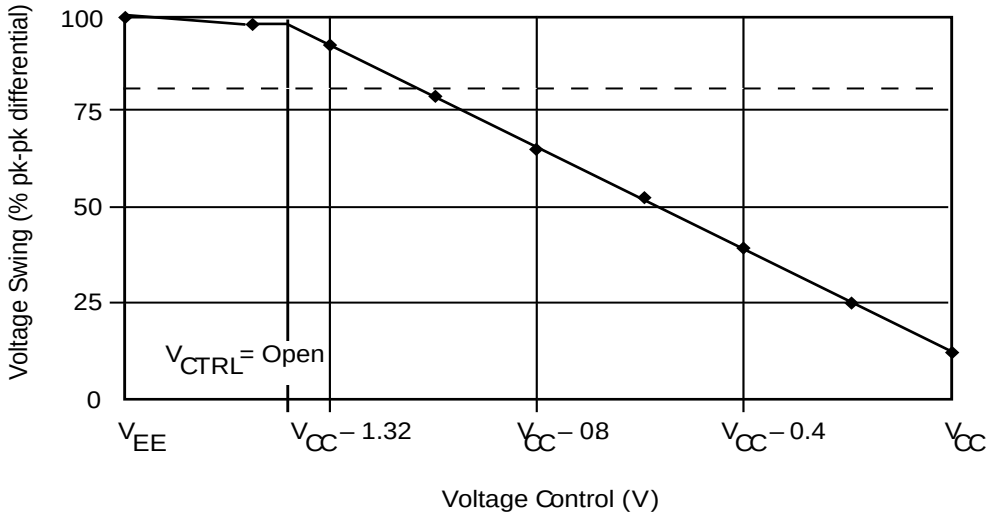


Figure 2. Typical Voltage Output Swing at 25°C

AC Characteristics *(continued)*

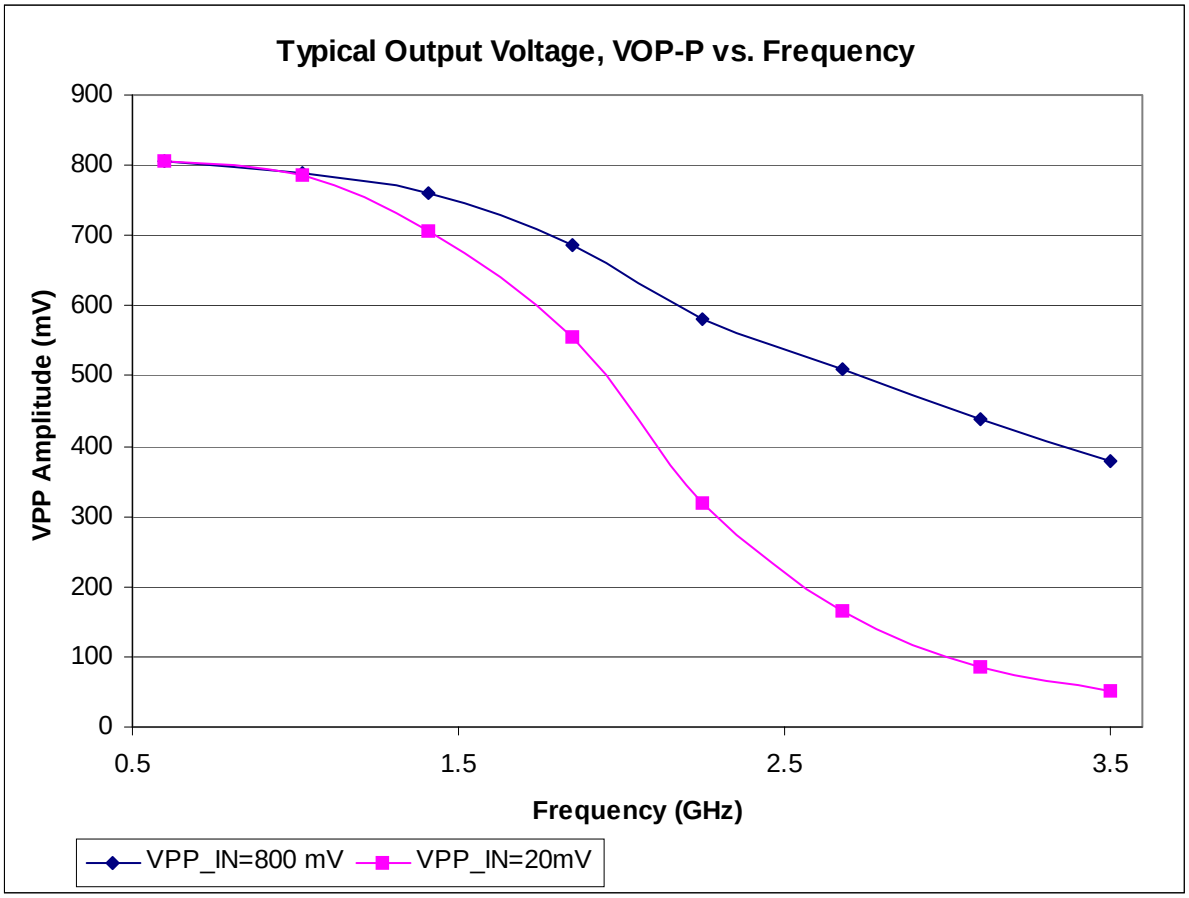


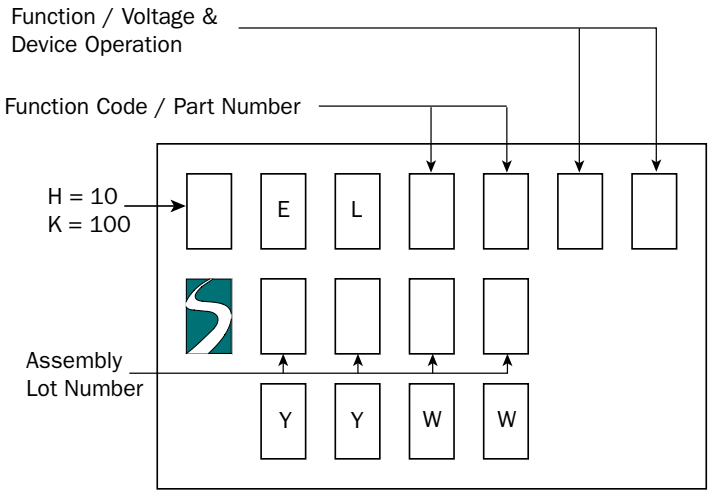
Figure 3. Typical Output VO_{P-P} vs. Frequency

Ordering Information

Ordering Code	Package ID	Temperature Range
SK100EL16YD	8-SOIC	Industrial
SK100EL16YDT	8-SOIC	Industrial
SK100EL16YMS	8-MSOP	Industrial
SK100EL16YMST	8-MSOP	Industrial
SK100EL16YU	Die	

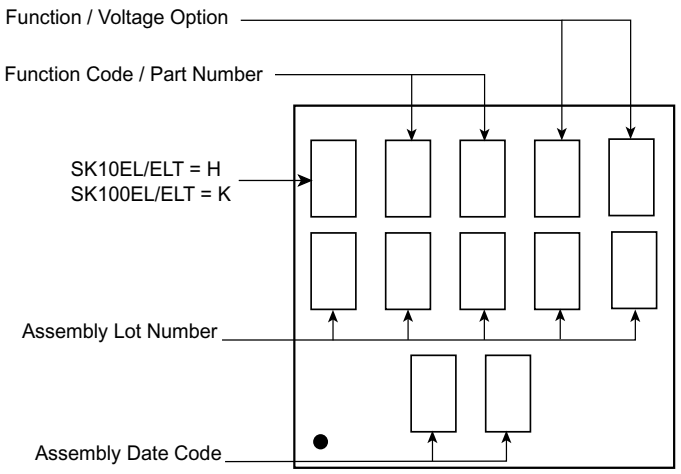
Marking Information

8 PIN SOIC PACKAGE



YY: Last two digits of the Year
WW: Working Week

8/10 PIN MSOP PACKAGES



Application Notes

AN1002 - Interfacing Between ECL / LVECL / PECL / LVPECL - to - TTL / LVTTL / CMOS / LVCMOS
AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices
AN1005 - Using ECL / LVECL Devices as PECL / LVPECL
AN1006 - Designing with 10K and 100K ECL / PECL Devices

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