Ordering number : EN*5611A

CMOS IC

LC378100QM, QT

8 MEG (1048576 words × 8 bits) Mask ROM
Internal Clocked Silicon Gate

Preliminary

Overview

The LC378100QM and LC378100QT are 1,048,576-word × 8-bit organization (8,388,608-bit) mask programmable read only memories. They feature a wide operating voltage range (2.6 to 5.5 V), a 100-ns access time (t_{CA}) at V_{CC} = 4.5 to 5.5 V, and a 200-ns access time at V_{CC} = 2.6 to 3.3 V. Thus these LSIs can be used in a wide range of systems, from 5-V systems that require high-speed access to 3-V systems that use batteries.

Features

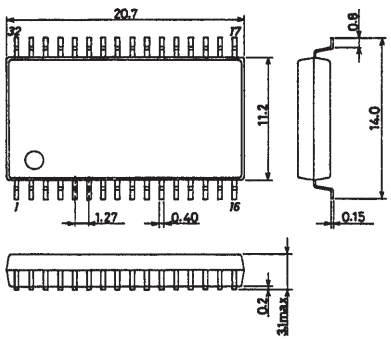
- 1048576 words × 8 bits organization
- Supply voltage range: 2.6 to 5.5
- Fast access time (t_{AA}): 120 ns (max.) V_{CC} = 4.5 to 5.5 V
  (t_{CA}): 100 ns (max.) V_{CC} = 4.5 to 5.5 V
  200 ns (max.) V_{CC} = 2.6 to 5.5 V
- Operating current 55 mA (max.)
- Standby current 30 µA (max.)
- Full static operation (internal clocked type)
- 3 state outputs
- JEDEC standard pin configuration
- Package type
  LC378100QM: SOP32 (525 mil)
  LC378100QT: TSOP32 (8 mm × 20 mm)

Package Dimensions

unit: mm

3205-SOP32

[LC374100QM]

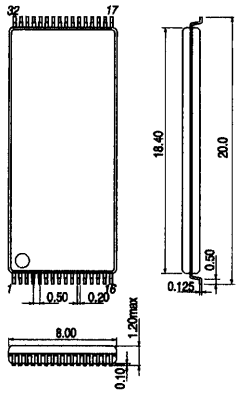


SANYO: SOP32

unit: mm

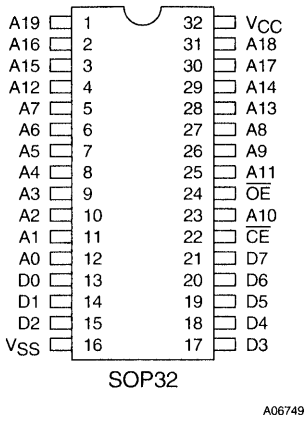
3224-TSOP32

[LC374100QT]



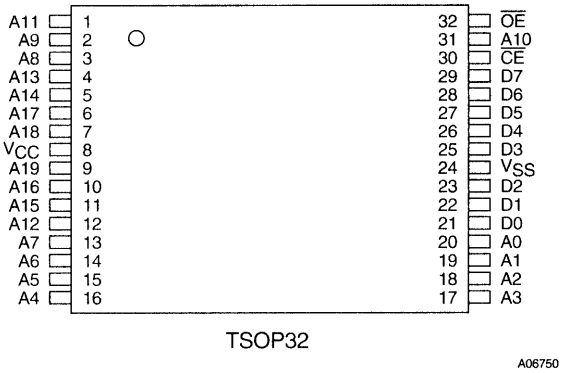
SANYO: TSOP32 (type-I)

Pin Assignments

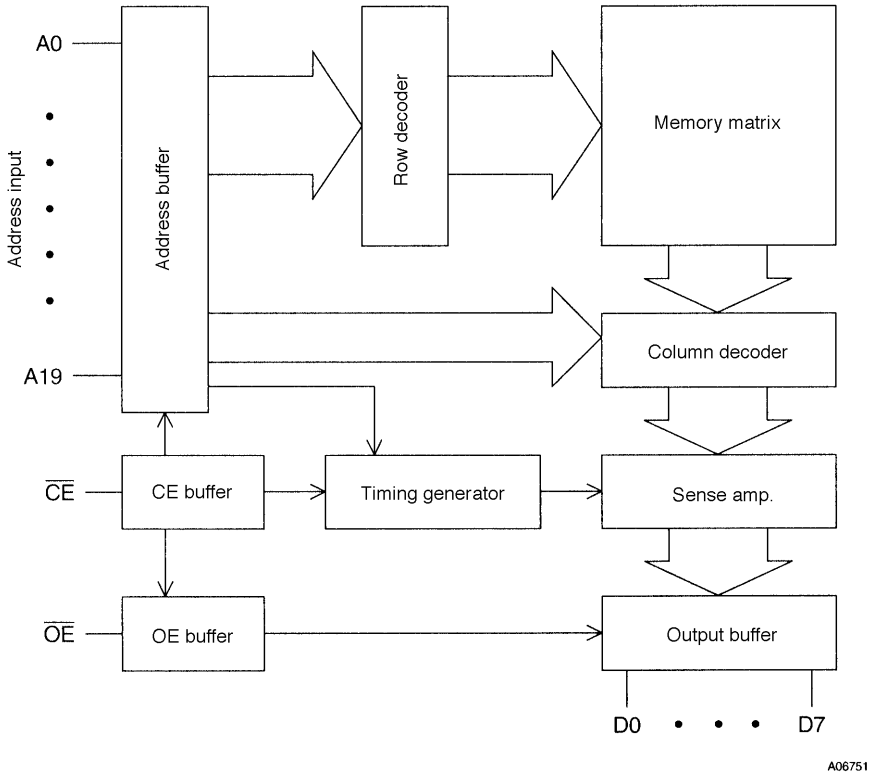


Pin Functions

A0 to A16	Address input
D0 to D7	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
V_{CC}	Power supply
V_{SS}	Ground



Block Diagram



Truth Table

$\overline{CE}$	$\overline{OE}$	Output	Current drain
H	X	High-impedance	Standby mode
L	H	High-impedance	Operating mode
L	L	DOUT	Operating mode

X: H or L level should be offered.

Specifications

Absolute Maximum Ratings *1

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		–0.3 to +7.0	V
Supply input voltage	V_{IN}		–0.3*2 to V_{CC} + 0.3	V
Supply output voltage	V_{OUT}		–0.3 to V_{CC} + 0.3	V
Allowable power dissipation	Pd max	Ta = 25°C; Reference values for the SANYO DIP package	1.0	W
Operating temperature	Topr		–10 to +70	°C
Storage temperature	Tstg		–55 to +125	°C

Note: 1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to Recommended Operating Conditions.
2. V_{IN} (min) = –3.0 V (pulse width ≤ 30 ns)

Input/Output Capacitance* at Ta = 25°C, f = 1.0 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input capacitance	C_{IN}	V_{IN} = 0 V; Reference values for the SANYO DIP package			8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V; Reference values for the SANYO DIP package			10	pF

Note: * This parameter is periodically sampled and not 100% tested.

DC Recommended Operating Ranges at Ta = –10 to +70°C, V_{CC} = 2.6 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		2.6	5.0	5.5	V
Input high level voltage	V_{IH}		2.2		V_{CC} + 0.3	V
Input low level voltage	V_{IL}		–0.3		+0.6	V

DC Electrical Characteristics at Ta = –10 to +70°C, V_{CC} = 2.6 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply current	I_{CCA1}	$\overline{CE}$ = 0.2 V, V_I = V_{CC} – 0.2 V/0.2 V			30	mA
	I_{CCA2}	$\overline{CE}$ = V_{IL}, I_O = 0 mA, V_I = V_{IH}/V_{IL}, f = 10 MHz			55	mA
Standby supply current	I_{CCS1}	$\overline{CE}$ = V_{CC} – 0.2 V			30 (1.0)	μA
	I_{CCS2}	$\overline{CE}$ = V_{IH}			1.0 (300)	mA(μA)
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			±1.0	μA
Output leakage current	I_{LO}	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 to V_{CC}			±1.0	μA
Output high level voltage	V_{OH}	I_{OH} = –0.5 mA	0.8 V_{CC}			V
Output low level voltage	V_{OL}	I_{OL} = 0.5 mA			0.2	V

Note: * Guaranteed at Ta = 25°C

AC Characteristics at Ta = –10 to +70°C, V_{CC} = 2.6 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Cycle time	t_{CYC}		200 (120)			ns
Address access time	t_{AA}				200 (120)	ns
$\overline{CE}$ access time	t_{CA}				200 (100)	ns
$\overline{OE}$ access time	t_{OA}				80 (40)	ns
Output hold time	t_{OH}		20			ns
Output disable time*1	t_{OD}*1				100	ns

Note: 1. t_{OD} is measured from the earlier edge of the $\overline{CE}$ or $\overline{OE}$'s going high impedance.
This parameter is periodically sampled and not 100% tested.
2. Guaranteed at V_{CC} = 4.5 to 5.5 V

AC Test Conditions

Input pulse levels	0.4 to 2.8 V
Input rise/fall time	5 ns
Input timing level	1.5 V
Output timing level	1.5 V
Output load	See Figure 1

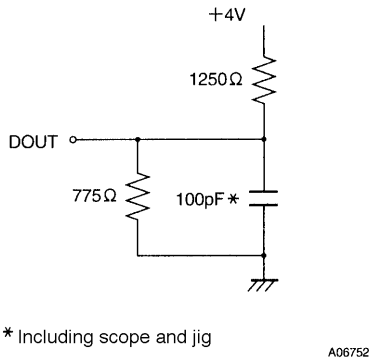
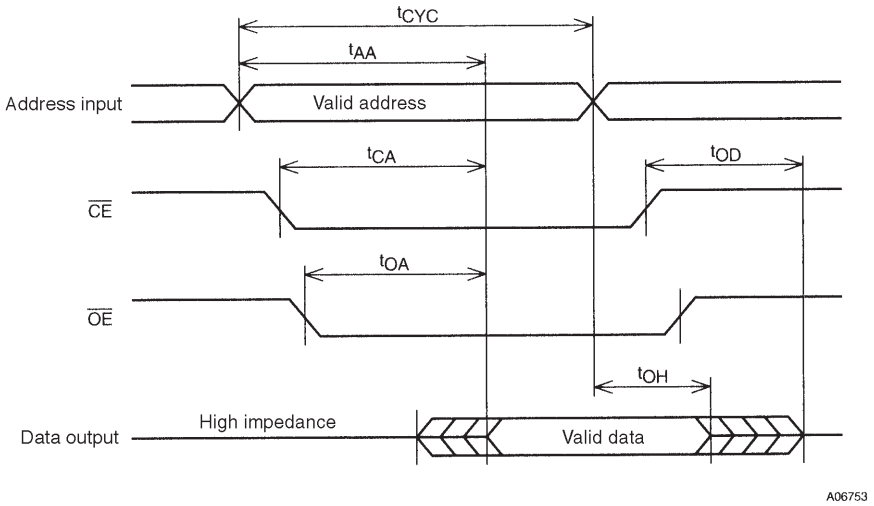


Figure 1 Output Load

Timing Chart



System Design Notes

These LSIs adopt the ATD technique, in which operation starts when a change in either the $\overline{CE}$ or address inputs is detected. This means that the output data immediately after power is applied is invalid. When using these LSIs as program memory for Z80 and similar microprocessors, applications must take into account the fact that valid data will not be output after power is first applied unless the value of either the $\overline{CE}$ or at least one of the address lines is changed after the power supply has stabilized.

Another point due to the use of the ATD technique is that these LSIs are sensitive to input noise. Do not apply voltages outside the allowable DC input levels for extended periods and do not apply input voltages with large noise components.