S3C89V5

8-BIT MICROCONTROLLER
for SMART CARD
Data sheet

Revision 2

SAMSUNG ELECTRONICS

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S3C89V5 8-Bit CMOS Microcontrollers
Data Sheet, Revision 2
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OVERVIEW

The S3C89V5 single-chip CMOS microcontroller is specially designed and packaged for "smart card" applications.
The SAM88RC CPU architecture supports Stop and Idle power-down modes for reduced power consumption. To increase the general-purpose register space, the physical internal register file is logically expanded.
The S3C89V5 has 47K-byte of program memory (ROM), 16K-byte of data memory (EEPROM), 272-byte general-purpose register file and 1024-byte data buffer (SRAM). The following peripherals are integrated on-chip:

— Contact or Contactless mode detection automatically
— ISO 7816 compatible asynchronous serial interface for contact operation
— Energy extraction and supply regulation circuits, clock extraction from 13.56 MHz carrier
— ISO 14443-2 compatible (Type B)
— One 16-bit Random number generator
— Hardware-level EEPROM write inhibit features for data security
— Frequency/Voltage/Temperature/Light exposure/Decapsulation various detectors with flag/reset action
— ROM,RAM,EEPROM BUS Scramble
— Contact UART(T=0, and T=1)
— Contactless UART(Type B)
— 16bit timer
— Hardware CRC logic for Type B
— Hardware DES logic

Data can be loaded into the EEPROM in units ranging from one byte to 32-byte. A typical EEPROM erase or write operation takes 1.5 milliseconds.
A simple yet effective hardware-level security feature based on abnormal voltage, frequency, decapsulation temperature and light exposure detection circuits keeps data stored in PROM/EEPROM.
The S3C89V5's 8-pin COB package and its serial I/O interface are fully compliant with ISO standards 7816, respectively.
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FEATURES

CPU

- SAM88RC 8-bit CPU core
- 78 instructions, including multiply and divide
- STOP and IDLE instructions added to reduce power consumption

Memory

- 47K-byte of ROM for program memory
- 16K-byte of EEPROM for program/data memory
- 1K-byte static RAM for program /data memory
- 272 bytes for general-purpose register file

EEPROM Write Operations

- Programmable EEPROM erase/write time
- Byte-wise to page-wise (32 bytes) EEPROM
- Min. 500,000 erase/write cycles
- Min. 10 years data retention

Data Security

- Invisible ROM code due to implantation
- 32-byte security PROM, hardware protected
- 32-byte non erasable EEPROM
- Unipue serial number for each chip
- Reset operations are selective if abnormal voltage/frequency/temperature/light/power-glitch exposure/decasulation is detected.

Interrupt

- 9 interrupt sources and vectors

Reset

- Power-on reset circuit
- External reset circuit

DES (Data Encryption Standard)

- Built-in triple DES

CRC Calculator

- Built-in triple CRC

UART

- T = 0 and 1 (ISO 7816 compliant)
- Type B (ISO 14443 compliant)

16-bit Random Number Generator

- One 16-bit random number generator with internal ring oscillator

Automatic Operating Mode Detect

- Contact/Contactless

Contactless Specific Features

- 13.56 MHz operation
- 106 Kbps, 212 Kbps or higher data transfer rate
- 10% ASK demodulation
- Load modulation
- Programmable contactless interface parameters

Contact Specific Feature

- Single power supply: 2.7 – 5.5 V
- ISO 7816-3 compatible
- Operating frequency: 1 – 5 MHz

Operating Temperature

- – 25 °C to + 85 °C

Package

- 8-pin COB (conforms to ISO standard 7816)

BLOCK DIAGRAM

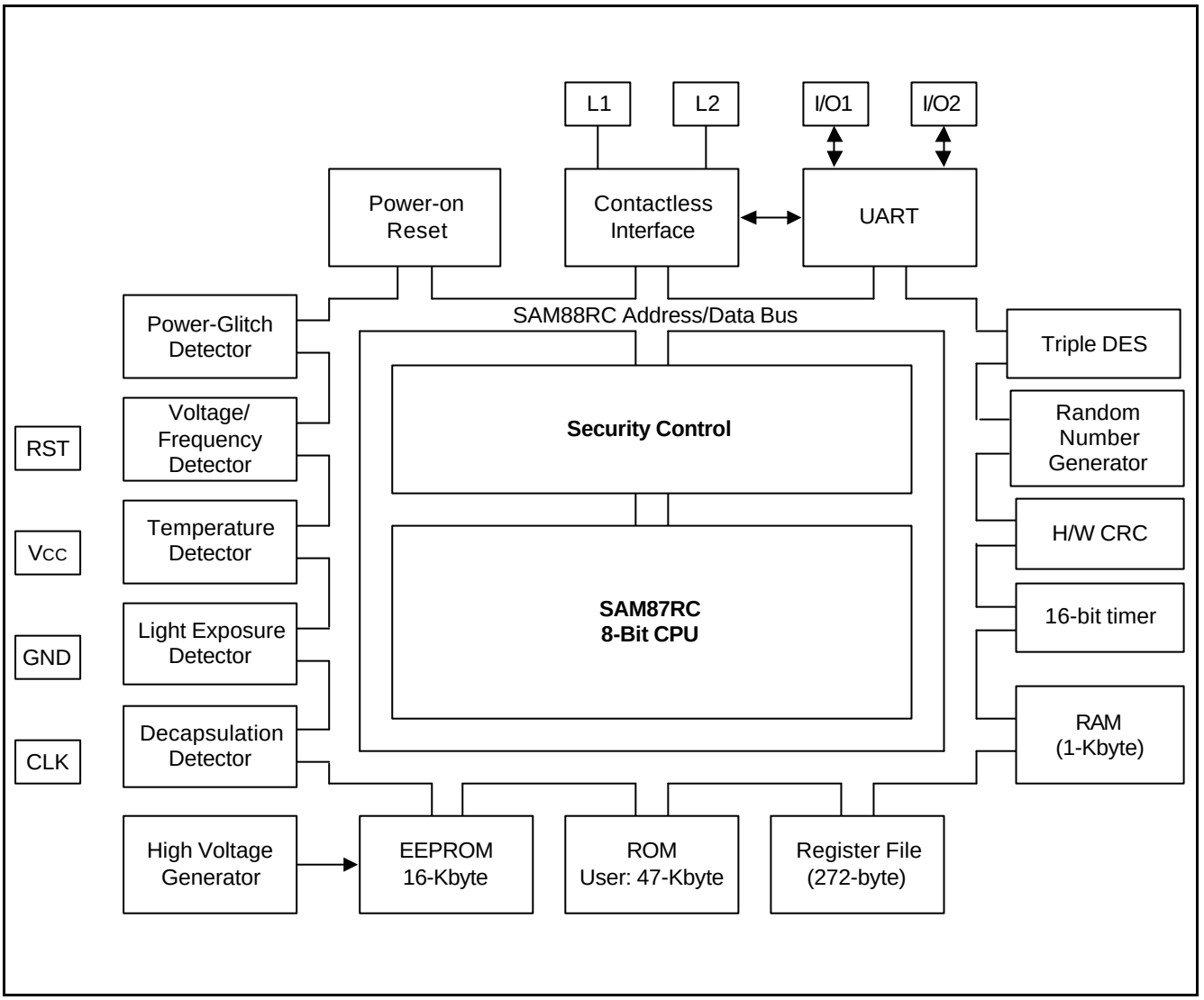

Figure 1. S3C89V5 Block Diagram

SAM88RC OVERVIEW

The SAM88RC instruction set is designed to support large register files. It features a full complement of 8-bit arithmetic and logic operations, including multiply and divide. There are 78 instructions. No special I/O instructions are necessary because I/O control and data registers are mapped directly into the register file. Decimal adjustment is included in binary-coded decimal (BCD) operations. 16-bit word data can be incremented and decremented. Flexible instructions for bit addressing, rotate, and shift operations complete the powerful data manipulation capabilities of the SAM88RC instruction set.

DATA TYPES

The SAM88RC CPU performs operations on bits, bytes, BCD digits, and two-byte words. Bits in the register file can be set, cleared, complemented, and tested. Bits within a byte are numbered from 7 to 0, where bit 0 is the least significant (right-most) bit.

REGISTER ADDRESSING

To access an individual register, an 8-bit address in the range 0-255 or the 4-bit address of a working register should be specified. Paired registers can be used to construct 16-bit data or 16-bit program memory or data memory addresses. For detailed information about register addressing, please refer to Section 2, "Address Spaces."

ADDRESSING MODES

There are seven addressing modes: Register (R), Indirect Register (IR), Indexed (X), Direct (DA), Relative (RA), Immediate (IM), and Indirect (IA). For detailed descriptions of these addressing modes, please refer to Section 3, "Addressing Modes."

MEMORY OVERVIEW

The S3C89V5 has four kinds of memory space:
— Internal program memory (ROM)
— Internal data memory (EEPROM)
— Internal data buffer (RAM)
— Internal register files (RAM)

A 16-bit address bus and an 8-bit data bus support program memory and data memory operations. A separate 8-bit address bus and the 8-bit data bus carry addresses and data between the CPU and the register files.

PROGRAM MEMORY (ROM)

The S3C89V5 has an internal 47K-byte mask-programmable, read-only program memory (ROM). The addresses 0EEH–0FFH of the ROM are reserved as an interrupt vector area.

DATA MEMORY (EEPROM)

The S3C89V5 has a 16K-byte electrically erasable, programmable read-only memory (EEPROM). A flexible and fast programming mode is provided to the user, and 1 to 32 bytes can be written at a time. The time is also programmable.
The first page of EEPROM (C000H-C01FH) is security area for unique serial number (read only) and the second page of EEPROM (C020H-C03FH) is non erasable area for writing only (cannot be erased).
An additional application program can be downloaded in the EEPROM and it can be executed like program memory.

INTERNAL DATA BUFFER (RAM)

The S3C89V5 has a 1K-byte internal data buffer (extended data memory) as static RAM. This memory can be used for I/O communication buffer or internal RAM like internal registers. An external data memory instruction such as LDE, LDED, or LDEI accesses these EEPROM and RAM.
An additional application program can be downloaded in the RAM and it can be executed like program memory.

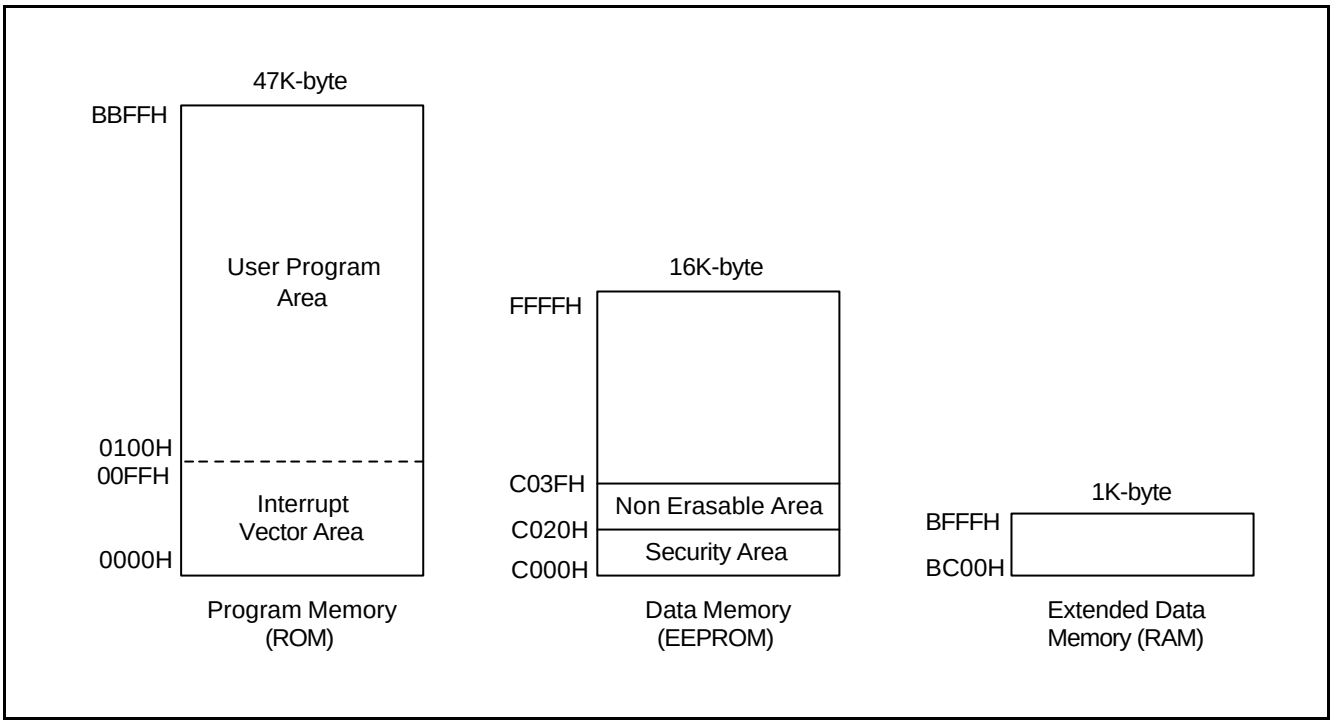

Figure 2. Memory Address Spaces

16-BIT TIMER

The S3C89V5 has one 16-bit timer. It consists of a timer control register(TCON), 16-bit up counter(TCH,TCL) and timer data(TDH,TDL).
The clock source for the timer can be an external clock for contact mode or cpu clock for contactless mode depend on the CFG.4.
The timer generates an interrupt whenever the TDH,TDL value are identical to TCH,TCL respectively.

DES (DATA ENCRYPTION STANDARD)

S3C89V5 has the hardware DES which consists of key register block, data register block, DES rounding block with s-box and p-box permutation, and its control registers as Figure 16-1.
Because each 64-bit DES key, K1 and K2 are write-only register, the key values are read-protected. On the other hand, To be encrypted or decrypted 64-bit message should be loaded into 64-bit DESDATA registers, from DESDATA0(MSB) to DESDATA7(LSB). The DESDATA registers are read/write registers.

DES OPERATION

To execute Single DES, the control sequence is as follows:

— Select bank1 by SB1 instruction

— Loading a 64-bit message into DESDATA0 (MSB) to DESDATA7 (LSB) registers

— Writing DES keys, K1 and/or K2: into Key10 (MSB) to Key17 (LSB) registers for K1, Key20 (MSB) to Key27 (LSB) for K2.

— Select K1 or K2 by DESCON.5

— Select Encryption or Decryption by DESCON.0

— Start to DES operation by DESCON.4

TRIPLE DES OPERATION

Encryption-Decryption-Encryption operation should be executed consecutively for encryption. There are two encryption steps with same key and one decryption step with the other key.
If key1 is used for encryption key, then Key 2 must be used for decryption key.
On the other hand, to decrypt the data, Decryption-Encryption-Decryption operation must be needed. In that case, K1 is for decryption and K2 is encryption key.

UART

S3C89V5 support 2 types of method for serial I/O during contact and/or contactless communication. Those are
— SIO Falling edge interrupt

— UART TX/RX interrupt

You can choose one among two SIO implementation methods as follows:
The first one is software SIO:
— refer to User's Manual Chap 11 "Contact/Contactless I/O interface"

The second one is UART, means hardware SIO

Contact UART

— You can choose 12etu (T=0) or 11etu (T=1) transmission, change extra guard time (EGT), choose parity bit for odd or even and select retry iteration number using CUARTCON1, CUARTCON2 contriol register

— Through ETU cycle registers, you can switch into more high or low baud rate.

Contactless UART

— Using TBMOD register, bit rate selection (106kbps, 212kbps), changing TR1 and EGT from card to reader available for Type B protocol.

ANTENNA INTERFACE

The S3C89V5 has antenna interface circuit as Figure 3, which fulfils power management, modulation and demodulation, and clock extraction for both ISO14443-type B operating with card reader.
The power management means the power supply regulation and the absorption of the extra energy associated with close reader to card operating range.
S3C89V5 can detect and define the operating mode which is contact or contactless operating mode automatically.

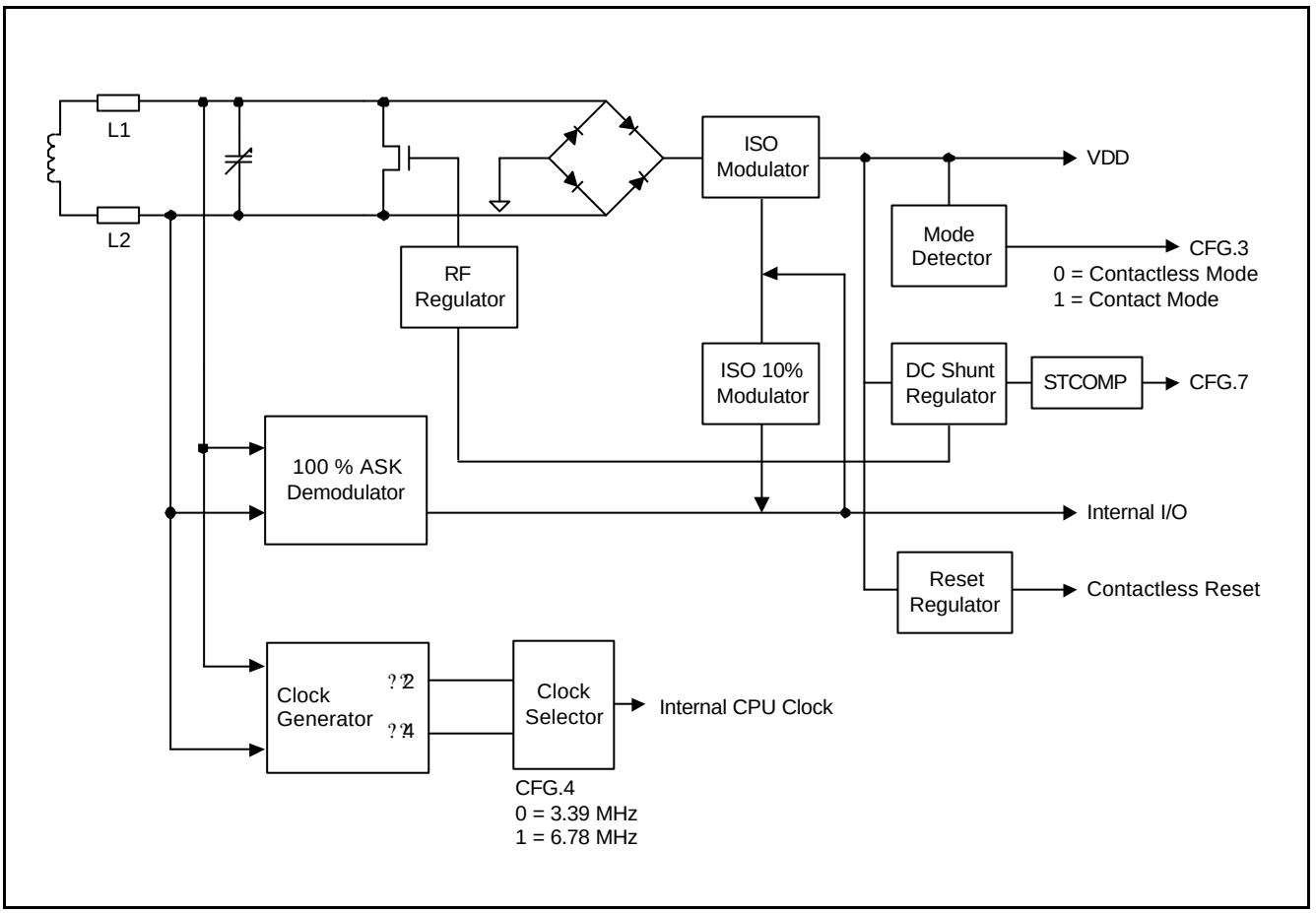

FIGURE 3. ANTENNA INTERFACE

PIN ASSIGNMENTS

Table 1. S3C89V5 Pin Descriptions

Pin Number	Pin Name	Function Description	Pin Type	Circuit Type
C1	V_{DD}	Power input	–	–
C2	RST	System reset input	Input	1
C3	CLK	External clock input	Input	2
C4	I/O2	No connection	–	–
C5	GND	Ground	–	–
C6	NC	No connection	–	–
C7	I/O	Serial data input and output; A pull up resistor should be connected to V_{DD} externally in contact mode	Input/output	3
C8	NC	No connection	–	–

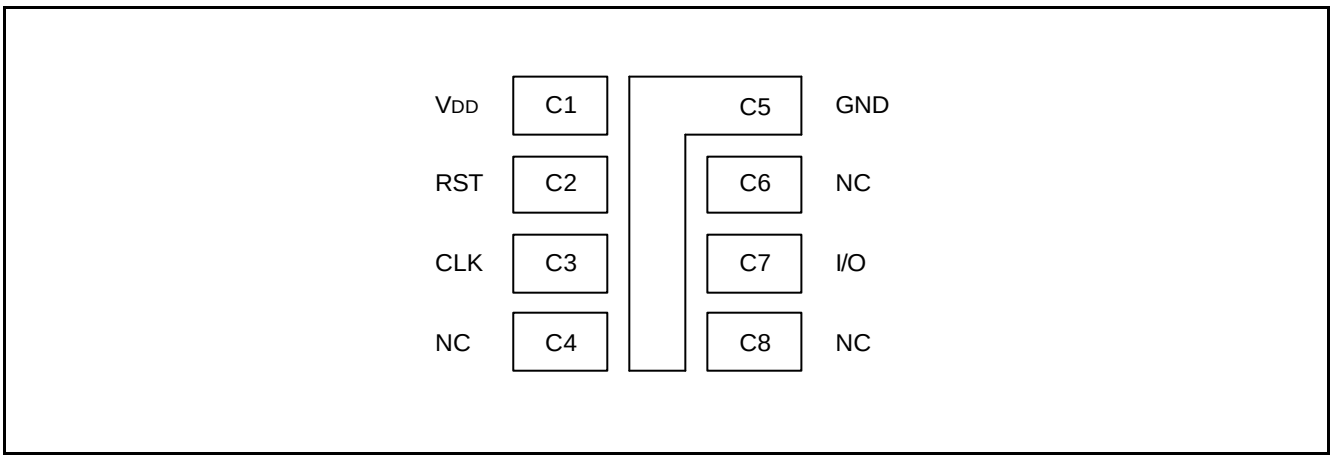

Figure 4. S3C89V5 COB Package Pin Arrangement

ELECTRICAL DATA

Table 2. D.C. Electrical Characteristics (Continued)

(T_A = – 25 ?C to + 85 ?C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD1}	f_{CLK}=5Mhz, 5.5V	-	8	10	mA
		f_{CLK}=5Mhz, 3.3V		4	7.5	
		f_{CLK}=4Mhz, 3.3V		3	6	
Stop current	I_{DD2}	f_{CLK}=1Mhz, 5.5V	-	-	200	μA
	I_{DD3}	f_{CLK}=GND, 5.5V	-	-	100	
Low-voltage detection	V_{LVD}	f_{CLK}=3.579Mhz	2.0	2.3	2.7	V
High-voltage detection	V_{HVD}	f_{CLK}=3.579Mhz	5.5	6.2	7.0	V
Low-frequency detection	F_{LFD}	V_{DD}=5V, 25℃	100	500	1000	khz
High-frequency detection	F_{HFD}	V_{DD}=5V, 25℃	5	6.5	10	Mhz