Document Title

128M x 8 Bit SmartMedia™ Card

Revision History

Revision No	History	Draft Date	Remark
0.0	Initial issue	Sept. 18th 2000	Preliminary
0.1	1. Changed device name - K9Q1G08V0M-SSB0 ---> K9Q1G08V0A-SSB0	Nov. 2th 2000	Preliminary
0.2	1. Changed don't card mode in address cycles - *X can be "High" or "Low" => *L must be set to "Low" 2. Explain how pointer operation works in detail.	Nov. 20th 2000	Preliminary
0.3	1. Updated operation for tRST timing - If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.	Dec.. 6th 2000	

Note : For more detailed features and specifications including FAQ, please refer to Samsung's Flash web site.
http://www.intl.samsungsemi.com/Memory/Flash/datasheets.html

128M x 8 Bit SmartMedia™ Card

FEATURES

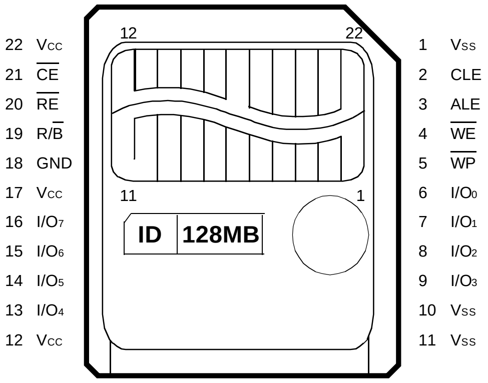
- Single 2.7V~3.6V Supply
- Organization
  - Memory Cell Array : (128M + 4.096K)bit x 8bit
  - Data Register : (512 + 16)bit x8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (16K + 512)Byte
- 528-Byte Page Read Operation
  - Random Access : 10µs(Max.)
  - Serial Page Access : 80ns(Min.)
- Fast Write Cycle Time
  - Program Time : 200µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- 22pad SmartMedia™(SSFDC)
- ID for Copyright Protection

GENERAL DESCRIPTION

The K9Q1G08V0A is a 128M(134,217,728)x8bit NAND Flash Memory with a spare 4.096K(4,194,304)x8bit. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typically 200µs and an erase operation can be performed in typically 2ms on a 16K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verify and margining of data. n, where required, and internal verify and margining of data. Even the write-intensive systems can take advantage of the K9Q1G08V0A′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

The K9Q1G08V0A is an optimum solution for large nonvolatile storage applications such as solid state file storage, digital voice recorder, digital still camera and other portable applications requiring non-volatility.

SmartMedia™ CARD(SSFDC)



22 PAD SmartMedia™

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
GND	Ground
R/$\overline{B}$	Ready/Busy output
Vcc	Power
Vss	Ground
N.C	No Connection

NOTE : Connect all Vcc and Vss pins of each device to common power supply outputs.
Do not leave Vcc or Vss disconnected.

Figure 1. FUNCTIONAL BLOCK DIAGRAM

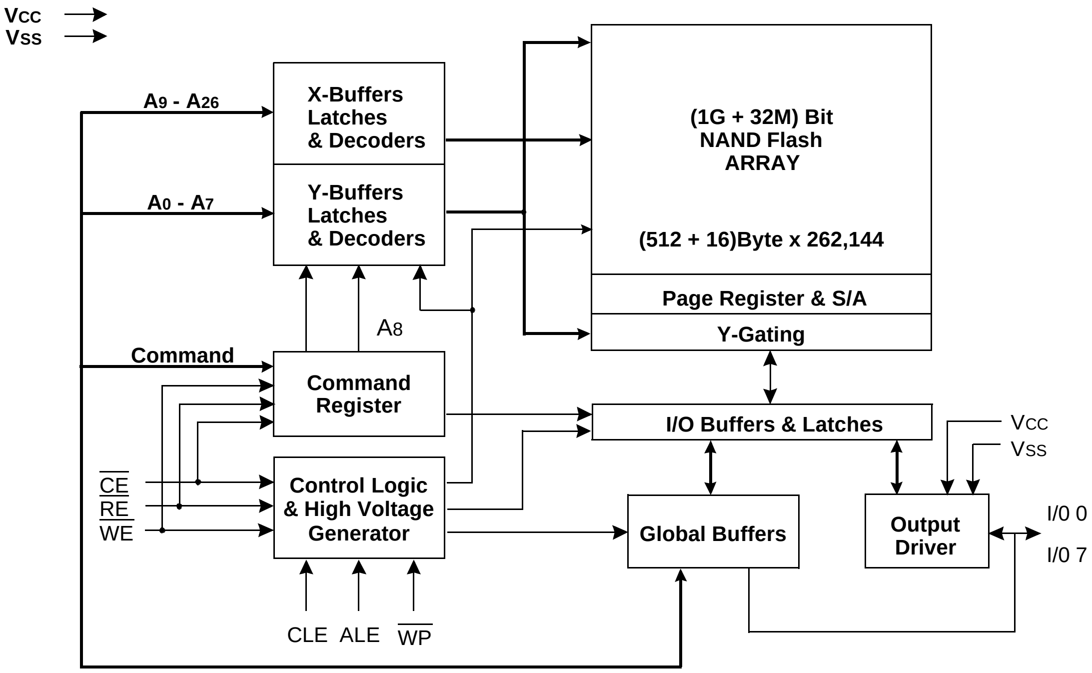
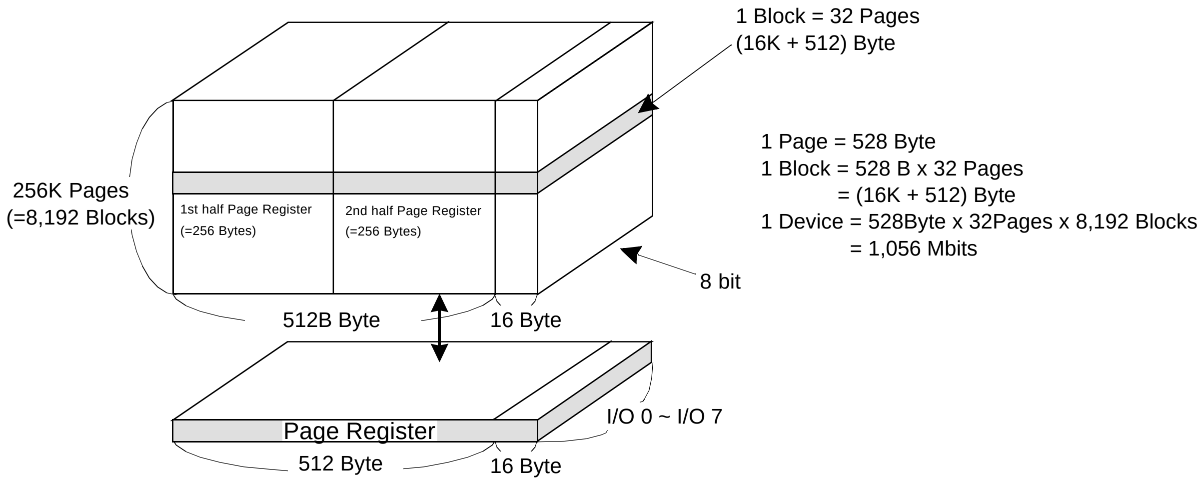


Figure 2. ARRAY ORGANIZATION



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	**Row Address (Page Address)**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	
4th Cycle	A_{25}	A_{26}	*L	*L	*L	*L	*L	*L	

NOTE : Column Address : Starting Address of the Register.
00h Command(Read) : Defines the starting address of the 1st half of the register.
01h Command(Read) : Defines the starting address of the 2nd half of the register.
* A_8 is set to "Low" or "High" by the 00h or 01h Command.
* L must be set to "Low".

PRODUCT INTRODUCTION

The K9Q1G08V0A is a 1,056Mbit(134,217,728 bit) memory organized as 262,144 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 32 pages formed by two NAND structures, totaling 16,896 NAND structures of 16 cells. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 8,192 separately erasable 16K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9Q1G08V0A.

The K9Q1G08V0A has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles: one cycle for erase-setup and another for erase-execution after block address loading. The 128M byte physical space requires 27 addresses, thereby requiring four cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9Q1G08V0A.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h[1]	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	O

NOTE : 1. The 00h command defines starting address of the 1st half of registers.
The 01h command defines starting address of the 2nd half of registers.
After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register(00h) on the next cycle.

PIN DESCRIPTION

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.

Address Latch Enable(ALE)

The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.

Chip Enable($\overline{CE}$)

The $\overline{CE}$ input is the device selection control. When $\overline{CE}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored, and does not return the device to standby mode.

Write Enable($\overline{WE}$)

The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.

Read Enable($\overline{RE}$)

The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.

I/O Port : I/O 0 ~ I/O 7

The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.

Write Protect($\overline{WP}$)

The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready/$\overline{Busy}$(R/$\overline{B}$)

The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN	-0.6 to + 4.6	V
	Vcc	-0.6 to + 4.6	
Temperature Under Bias	TBIAS	-10 to +65	°C
Storage Temperature	TSTG	-20 to +65	°C

NOTE :
1. Minimum DC voltage is -0.3V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, TA=0 to 55°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	2.7	3.3	3.6	V
Supply Voltage	Vss	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	Icc1	tRC=50ns, $\overline{CE}$=VIL, IOUT=0mA	-	10	20	mA
	Program	Icc2	-	-	15	25	
	Erase	Icc3	-	-	15	25	
Stand-by Current(TTL)		ISB1	$\overline{CE}$=VIH, $\overline{WP}$=0V/Vcc	-	-	1	
Stand-by Current(CMOS)		ISB2	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc	-	20	100	µA
Input Leakage Current		ILI	VIN=0 to 3.6V	-	-	±10	
Output Leakage Current		ILO	VOUT=0 to 3.6V	-	-	±10	
Input High Voltage, All inputs		VIH	-	2.0	-	Vcc+0.3	V
Input Low Voltage, All inputs		VIL	-	-0.3	-	0.8	
Output High Voltage Level		VOH	IOH=-400µA	2.4	-	-	
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		IOL(R/$\overline{B}$)	VOL=0.4V	8	10	-	mA

VALID BLOCK

1. The K9Q1G08V0A may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not try to access these invalid blocks for program and erase. Refer to the attached technical notes for a appropriate management of invalid blocks.

2. Per the specification of the physical format version 1.2 by SSFDC forum, minimum 1,000 vaild blocks are guaranteed for each 16MB memory space.

AC TEST CONDITION

(T_A=0 to 55°C, V_{CC}=2.7V~3.6V unless otherwise noted)

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load (3.0V +/-10%)	1 TTL GATE and CL=50pF
Output Load (3.3V +/-10%)	1 TTL GATE and CL=100pF

CAPACITANCE(T_A=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	40	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	40	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(4clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(4clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	sequential Read & Data Output	
L	L	L	H	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program/Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	200	500	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	1	cycle
	Spare Array		-	-	2	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE setup Time	tCLS	20	-	ns
CLE Hold Time	tCLH	40	-	ns
CE setup Time	tCS	20	-	ns
CE Hold Time	tCH	40	-	ns
WE Pulse Width	tWP	40	-	ns
ALE setup Time	tALS	20	-	ns
ALE Hold Time	tALH	40	-	ns
Data setup Time	tDS	30	-	ns
Data Hold Time	tDH	20	-	ns
Write Cycle Time	tWC	80	-	ns
WE High Hold Time	tWH	20	-	ns

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	tR	-	10	µs
ALE to RE Delay(ID read)	tAR1	200	-	ns
ALE to RE Delay(Read cycle)	tAR2	150	-	ns
CE to RE Delay(ID read)	tCR	200	-	ns
Ready to RE Low	tRR	20	-	ns
RE Pulse Width	tRP	40	-	ns
WE High to Busy	tWB	-	200	ns
Read Cycle Time	tRC	80	-	ns
RE Access Time	tREA	-	45	ns
RE High to Output Hi-Z	tRHZ	15	30	ns
CE High to Output Hi-Z	tCHZ	-	30	ns
RE High Hold Time	tREH	20	-	ns
Output Hi-Z to RE Low	tIR	0	-	ns
Last RE High to Busy(at sequential read)	tRB	-	200	ns
CE High to Ready(in case of interception by CE at read)	tCRY	-	50 +tr(R/B)(1)	ns
CE High Hold Time(at the last serial read)(2)	tCEH	250	-	ns
RE Low to Status Output	tRSTO	-	45	ns
CE Low to Status Output	tCSTO	-	55	ns
WE High to RE Low	tWHR	60	-	ns
RE access time(Read ID)	tREADID	-	45	ns
Device Resetting Time(Read/Program/Erase)	tRST	-	5/10/500(3)	µs

NOTE :
1. The time to Ready depends on the value of the pull-up resistor tied R/B pin.
2. To break the sequential read cycle, CE must be held high for longer time than tCEH.
3. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

SmartMedia Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping.

Identifying Invalid Block(s)

SSFDC Forum specifies the logical format and physical format to ensure compatibility of SmartMedia. Samsung pre-formats SmartMedia in the Forum-compliant format prior to shipping. Physical format standard by SSFDC Forum specifies that for the invalid blocks the 6th byte in the spare area (column address 517 for 4MB SmartMedia and higher densities, 261 for 2MB SmartMedia, respectively) contains two or more "0" bits to indicate a invalid block. Other than the blocks with format data and the invalid blocks are erased(FFh). Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 1). Any intentional erasure of the original invalid block information is prohibited.

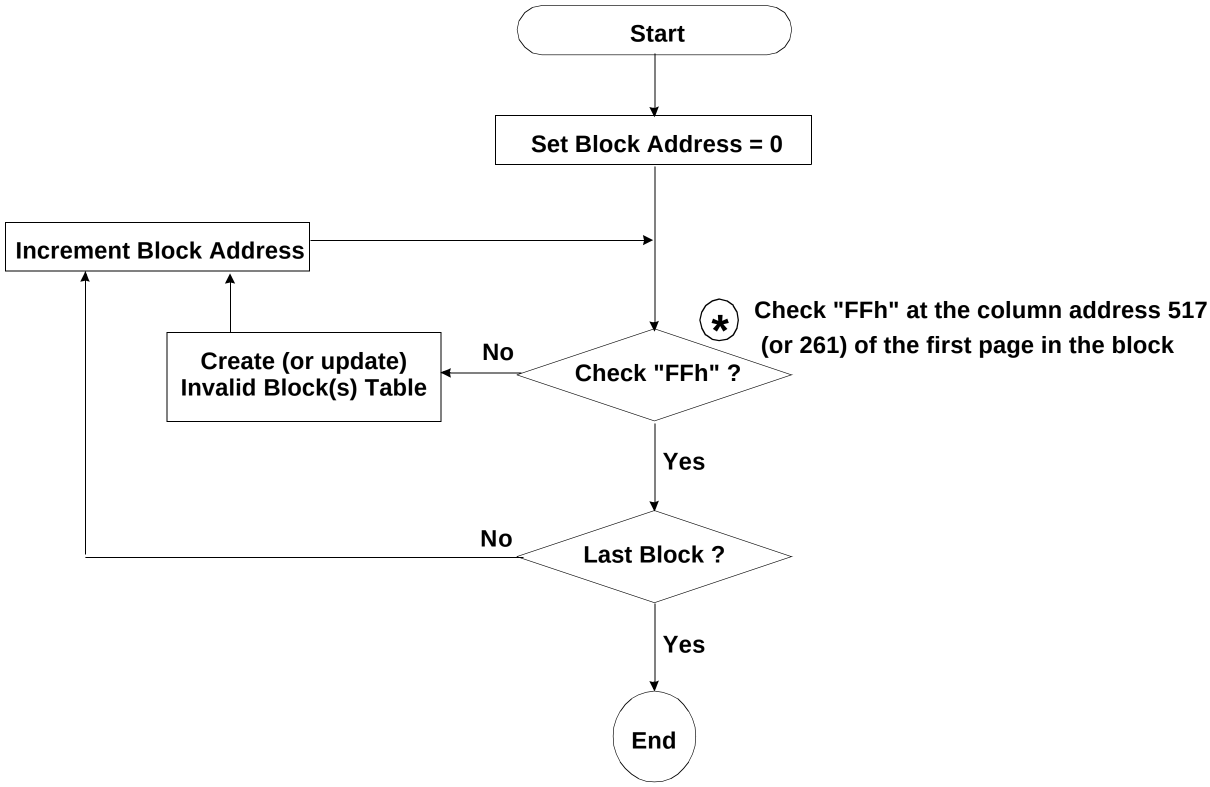


Figure 1. Flow chart to create invalid block table.

SmartMedia Technical Notes (Continued)

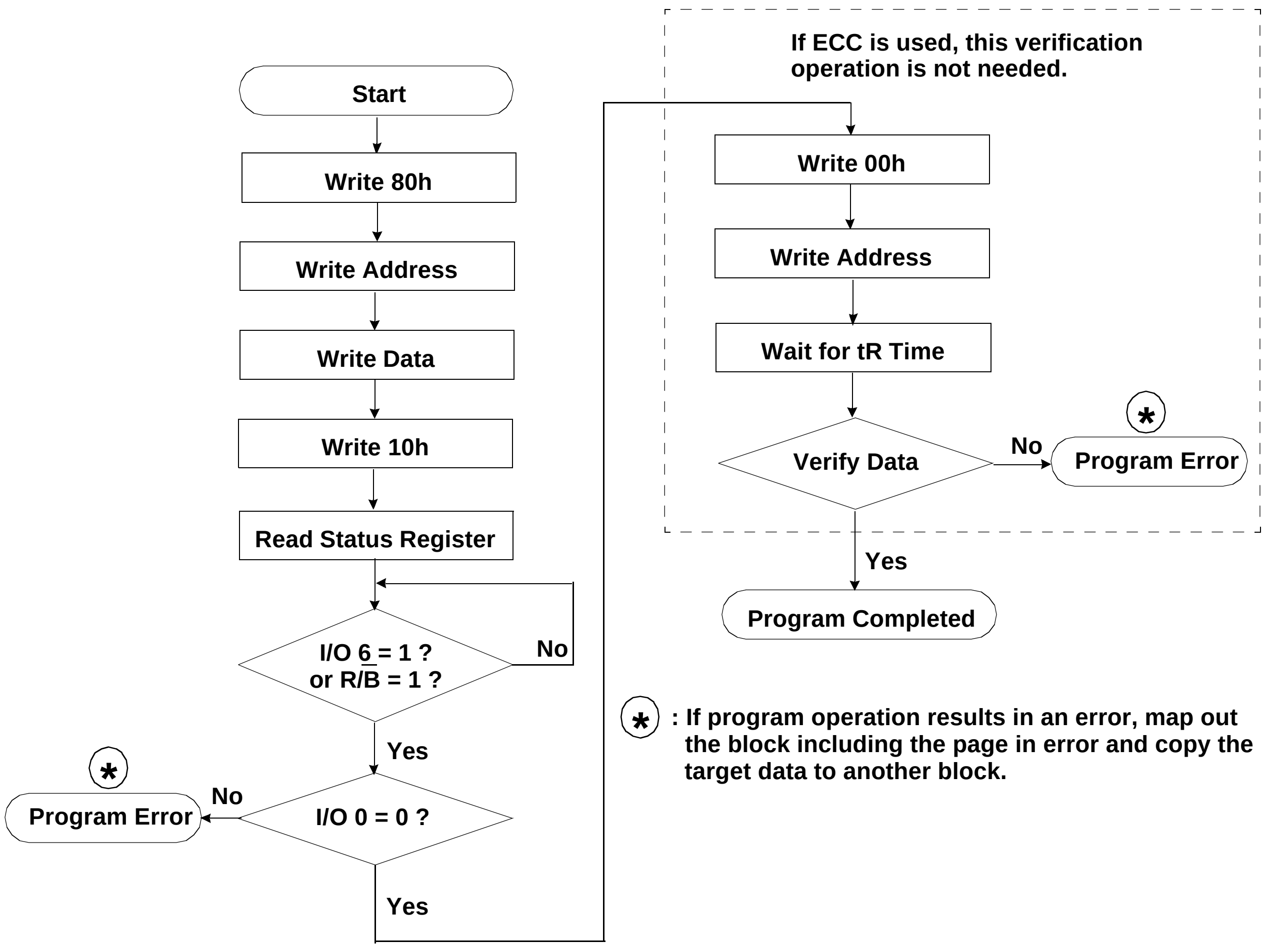
Error in write or read operation

Over its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

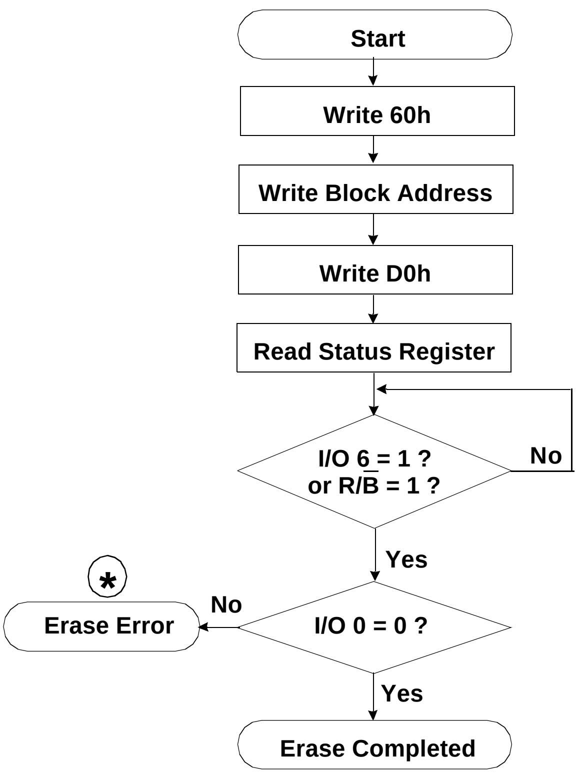
ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Program Flow Chart

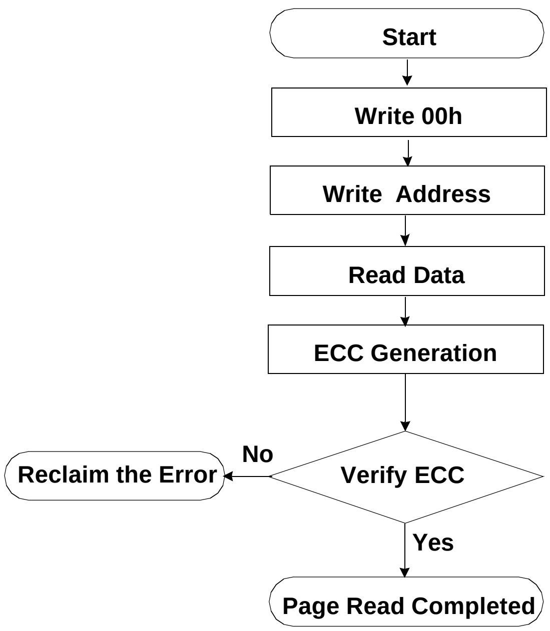


SmartMedia Technical Notes (Continued)

Erase Flow Chart

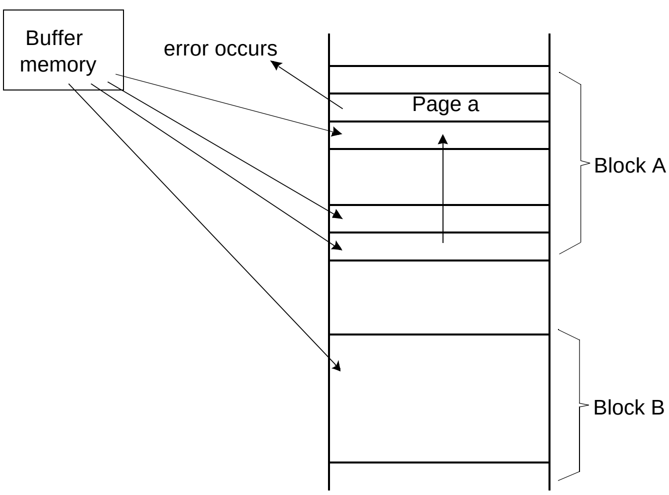


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement



When the error happens with page "a" of Block "A", try to write the data into another Block "B" from an external buffer. Then, prevent further system access to Block "A" (by creating a "invalid block" table or other appropriate scheme.)

Pointer Operation of K9Q1G08V0A

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. '00h' command sets the pointer to 'A' area(0~255byte), '01h' command sets the pointer to 'B' area(256~511byte), and '50h' command sets the pointer to 'C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). '00h' or '50h' is sustained until another address pointer command is inputted. '01h' command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with '01h' command, the address pointer returns to 'A' area by itself. To program data starting from 'A' or 'C' area, '00h' or '50h' command must be inputted before '80h' command is written. A complete read operation prior to '80h' command is not necessary. To program data starting from 'B' area, '01h' command must be inputted right before '80h' command is written.

Table 1. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

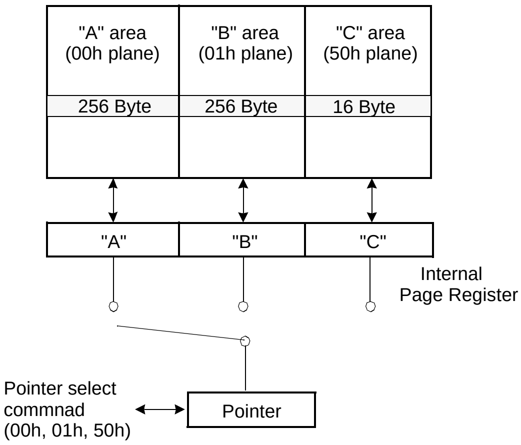
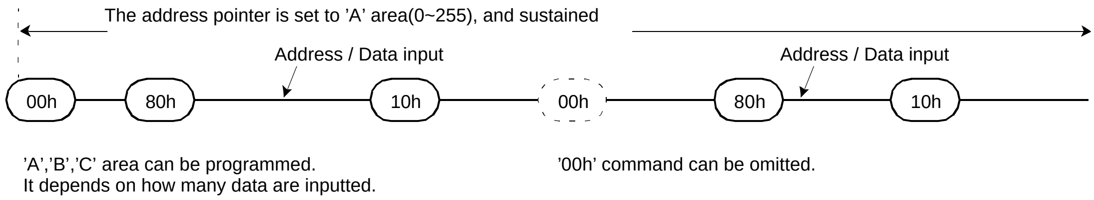
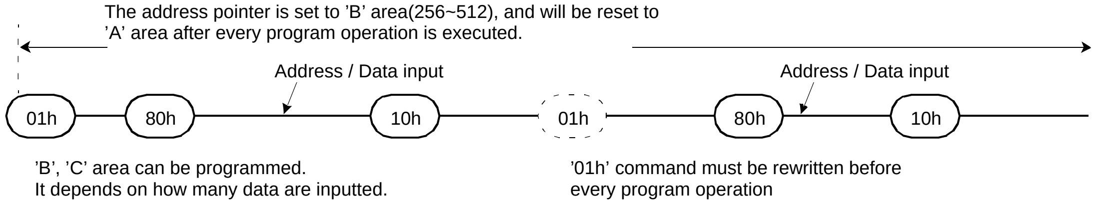


Figure 2. Block Diagram of Pointer Operation

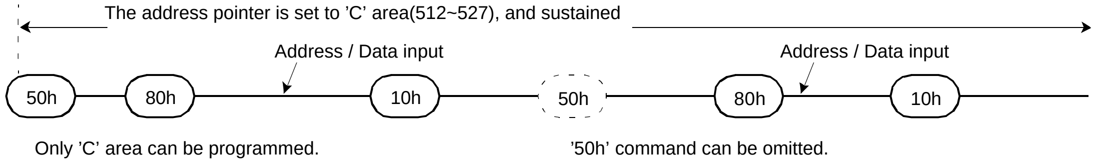
(1) Command input sequence for programming 'A' area



(2) Command input sequence for programming 'B' area



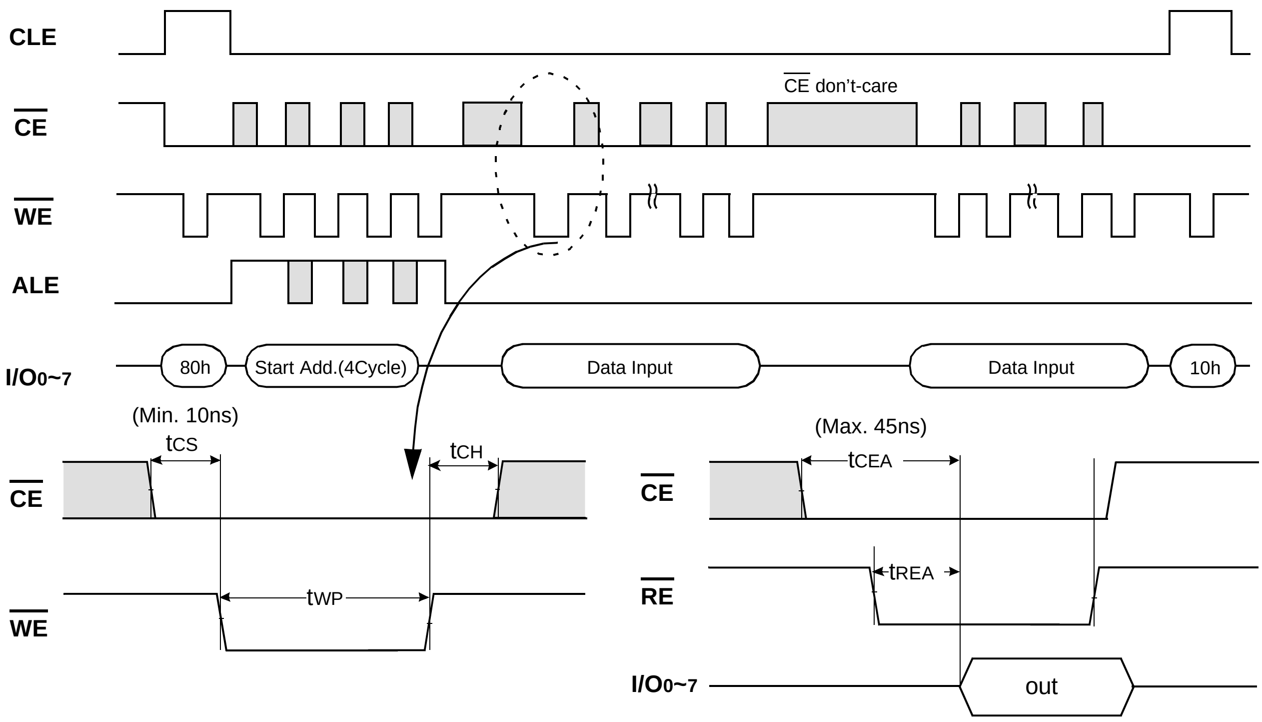
(3) Command input sequence for programming 'C' area



System Interface Using CE don't-care.

For an easier system interface, CE may be inactive during the data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating CE during the data-loading and reading would provide significant savings in power consumption.

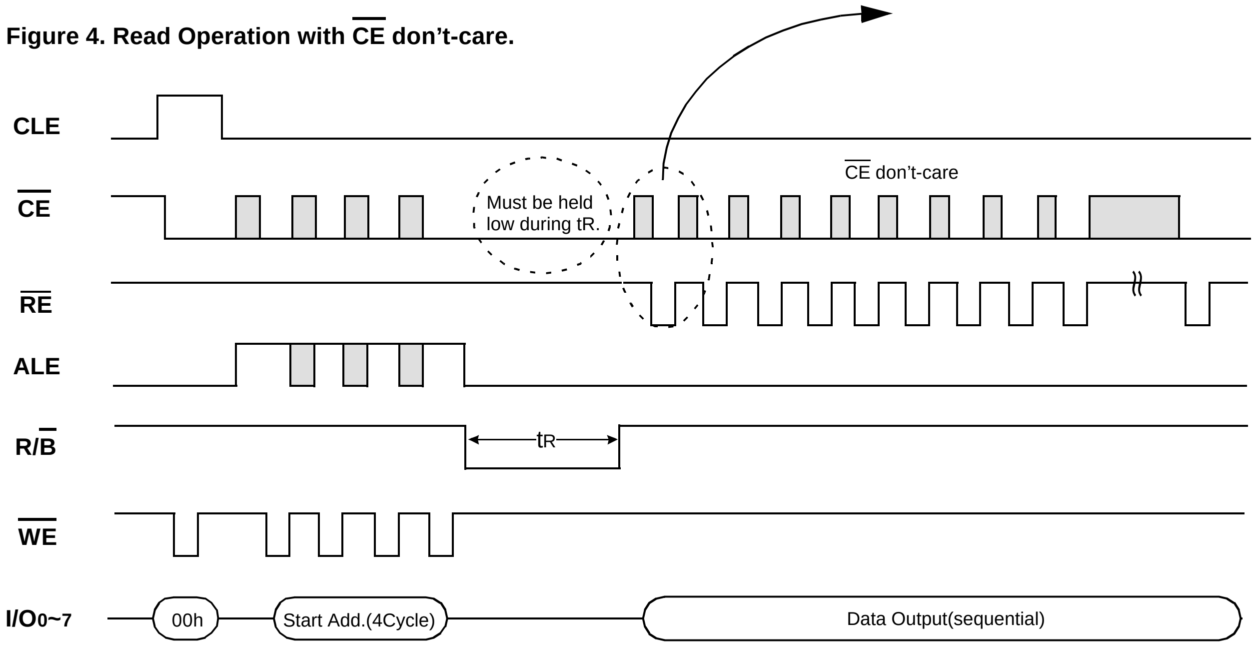
Figure 3. Program Operation with CE don't-care.



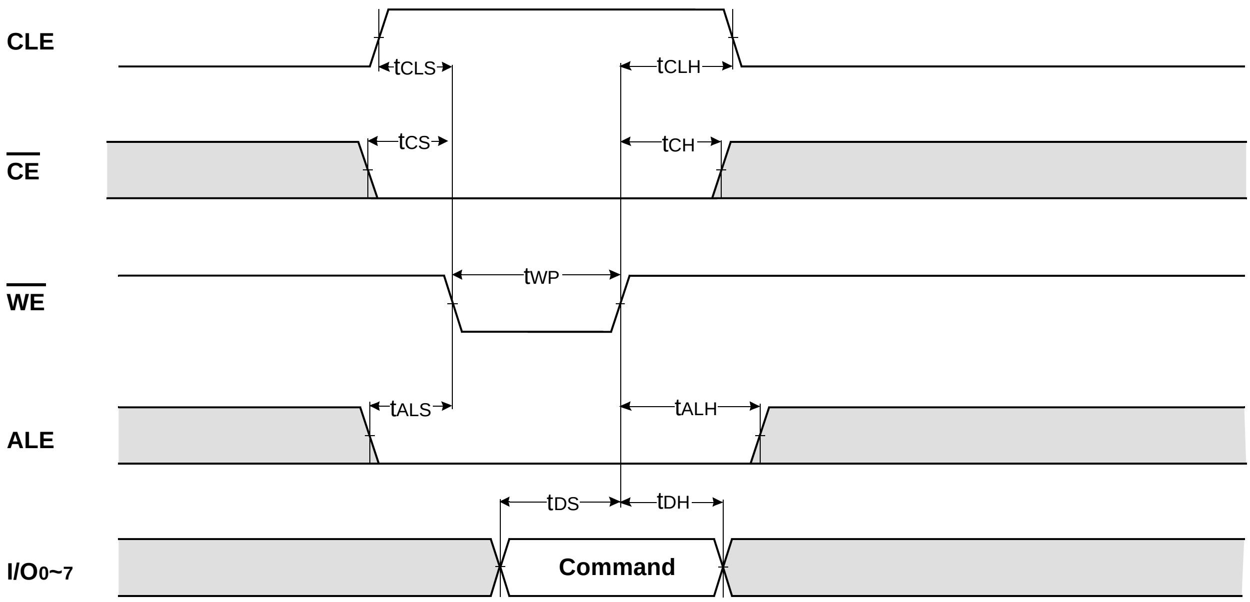
Timing requirements : If CE is is exerted high during data-loading, tCS must be minimum 10ns and tWC must be increased accordingly.

Timing requirements : If CE is exerted high during sequential data-reading, the falling edge of CE to valid data(tCEA) must be kept greater than 45ns.

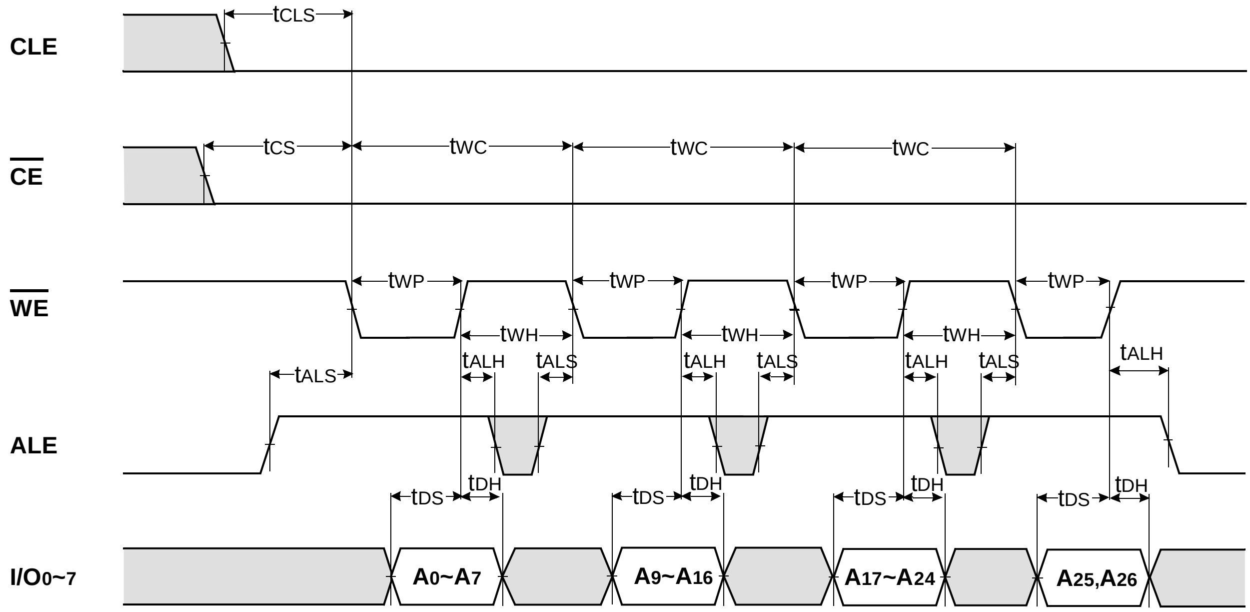
Figure 4. Read Operation with CE don't-care.



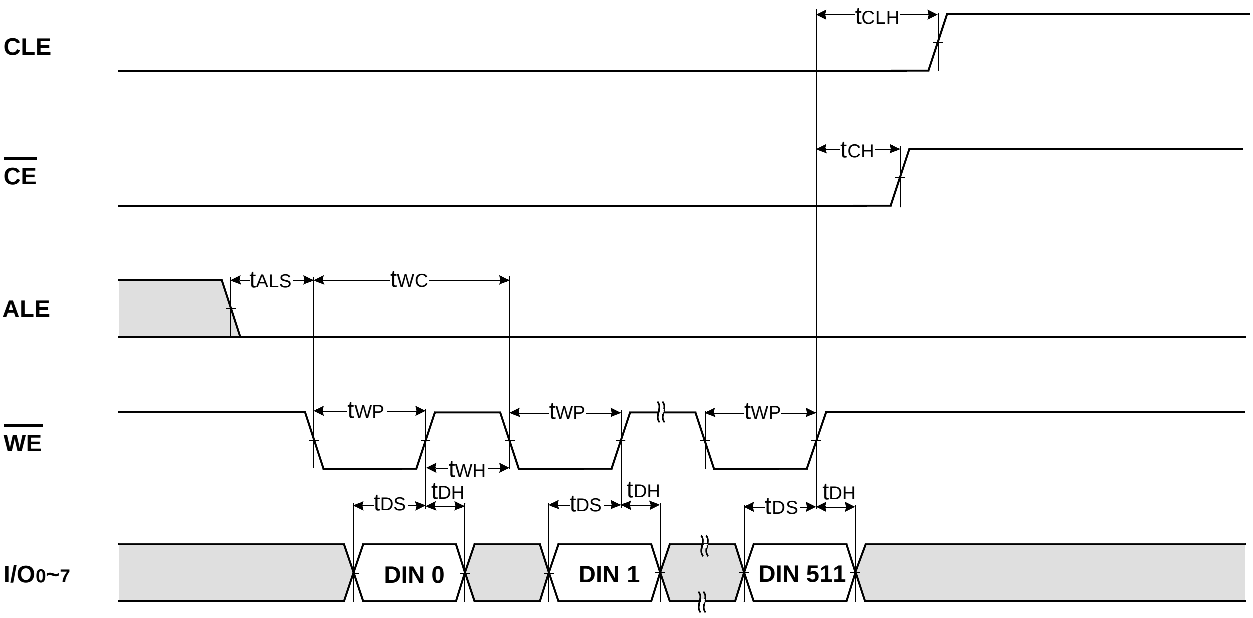
*** Command Latch Cycle**



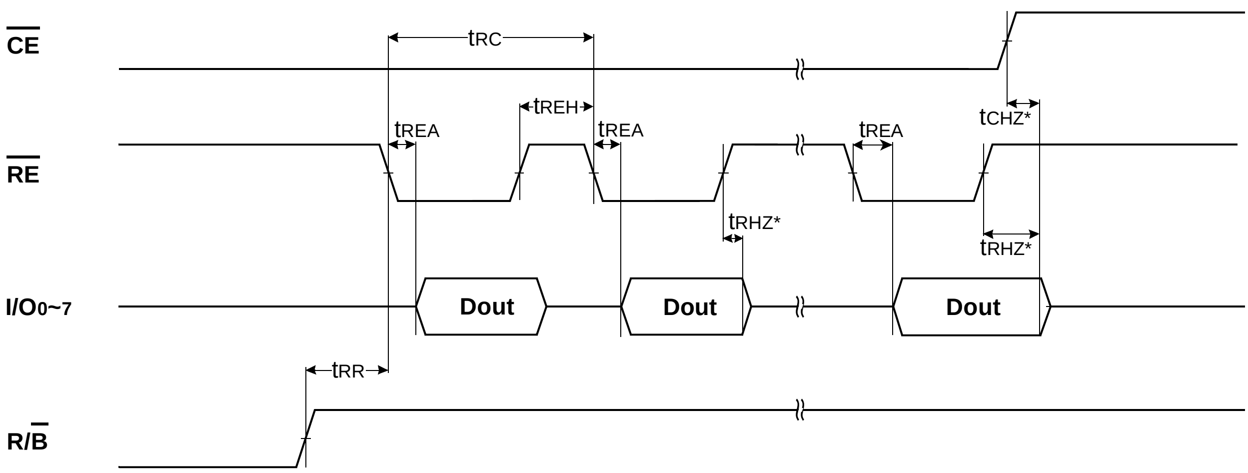
*** Address Latch Cycle**



* Input Data Latch Cycle

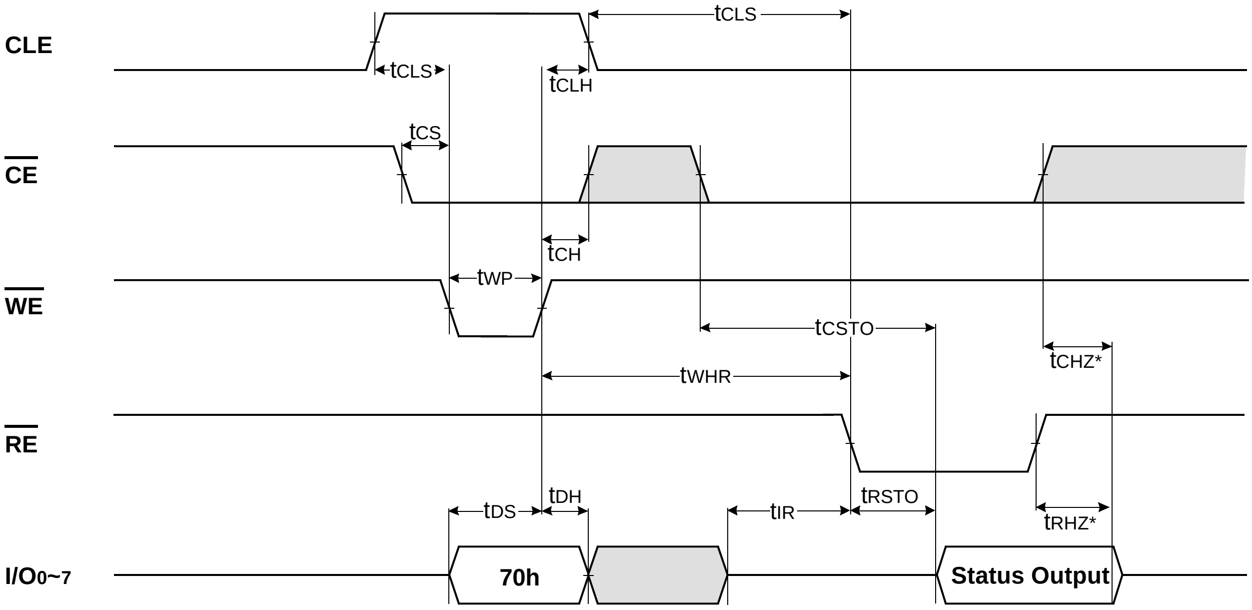


* Sequential Out Cycle after Read(CLE=L, WE=H, ALE=L)

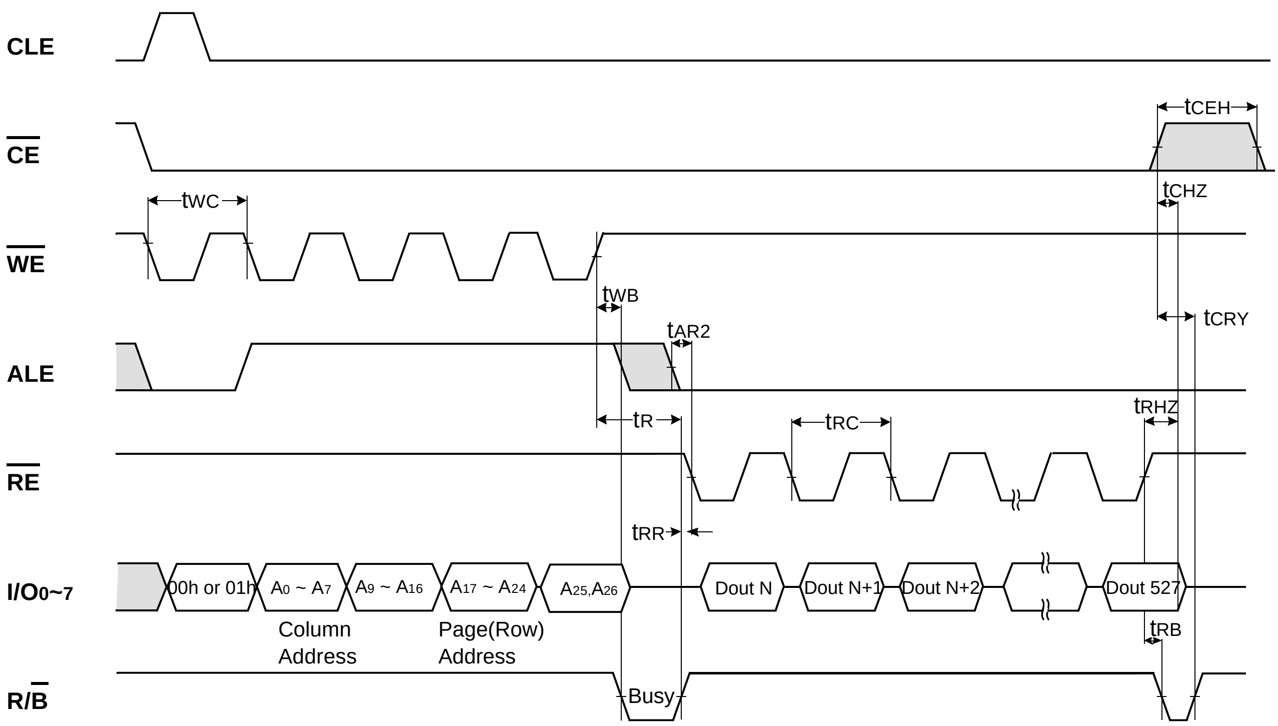


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

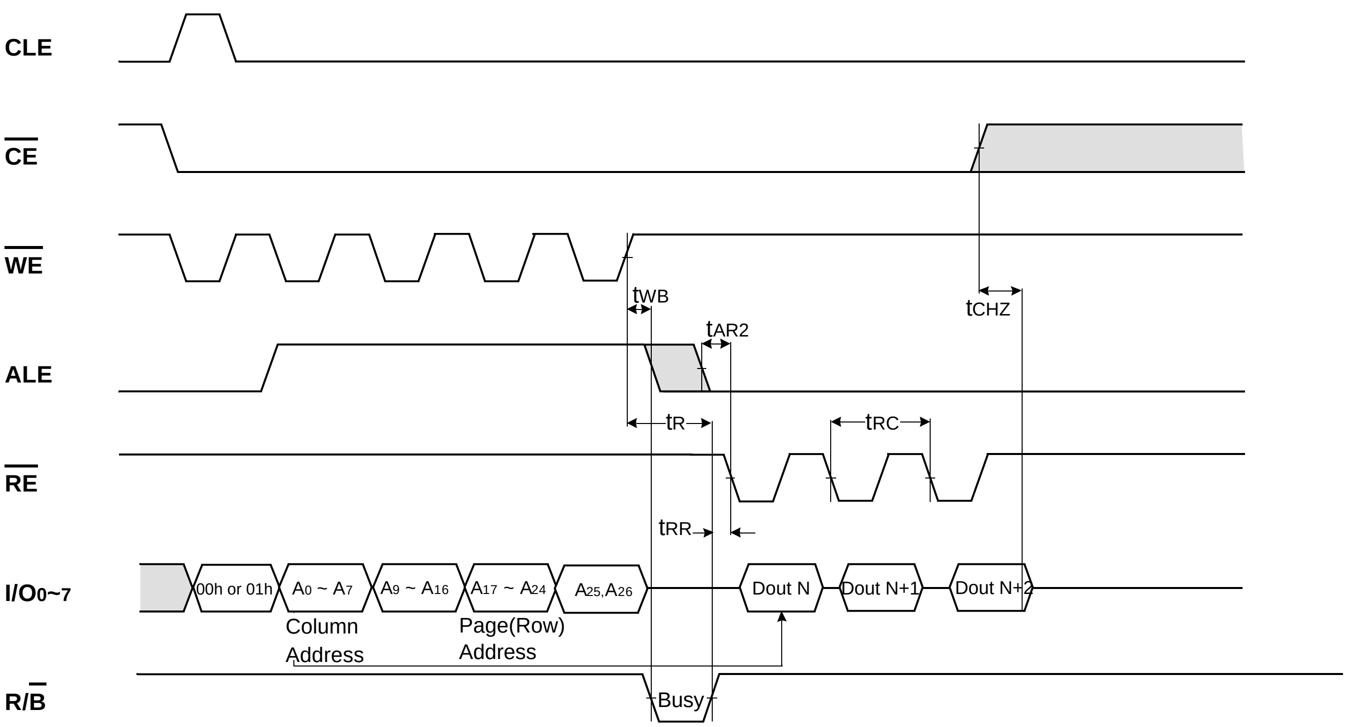
* Status Read Cycle



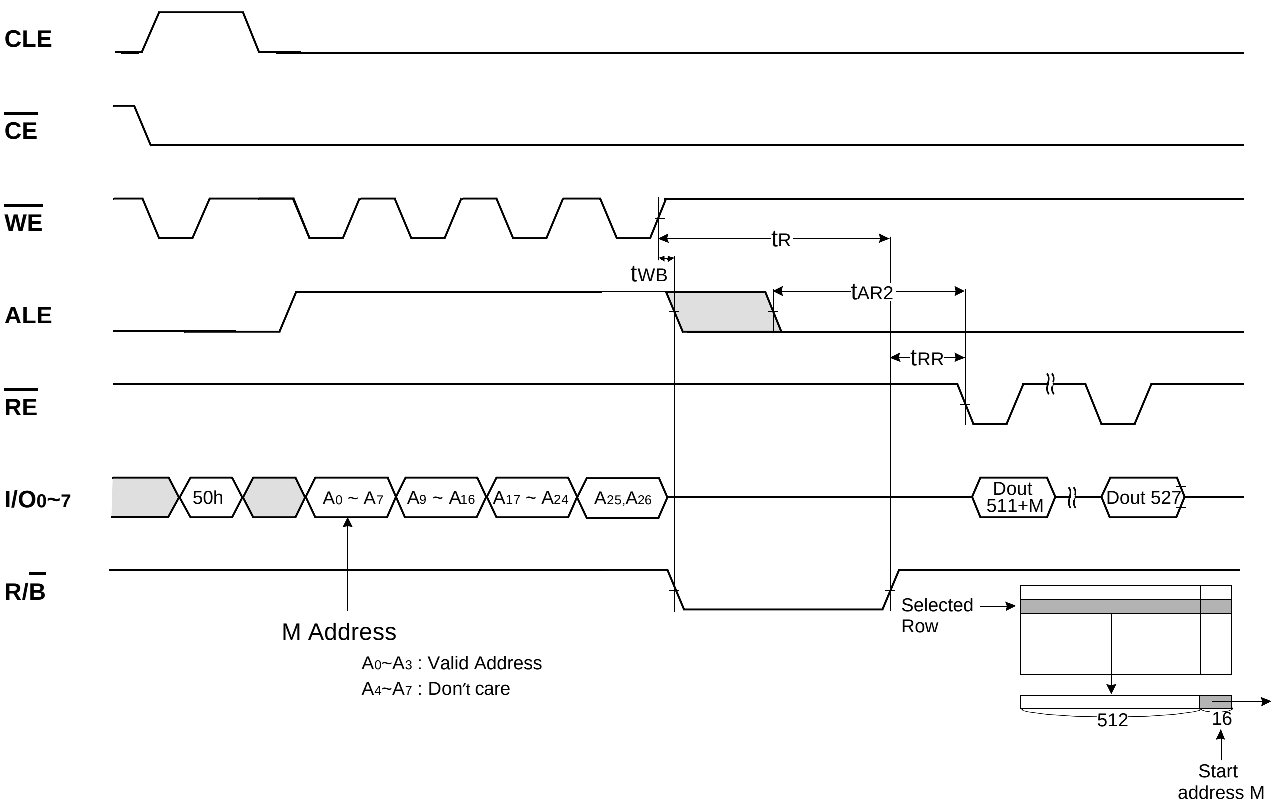
READ1 OPERATION(READ ONE PAGE)



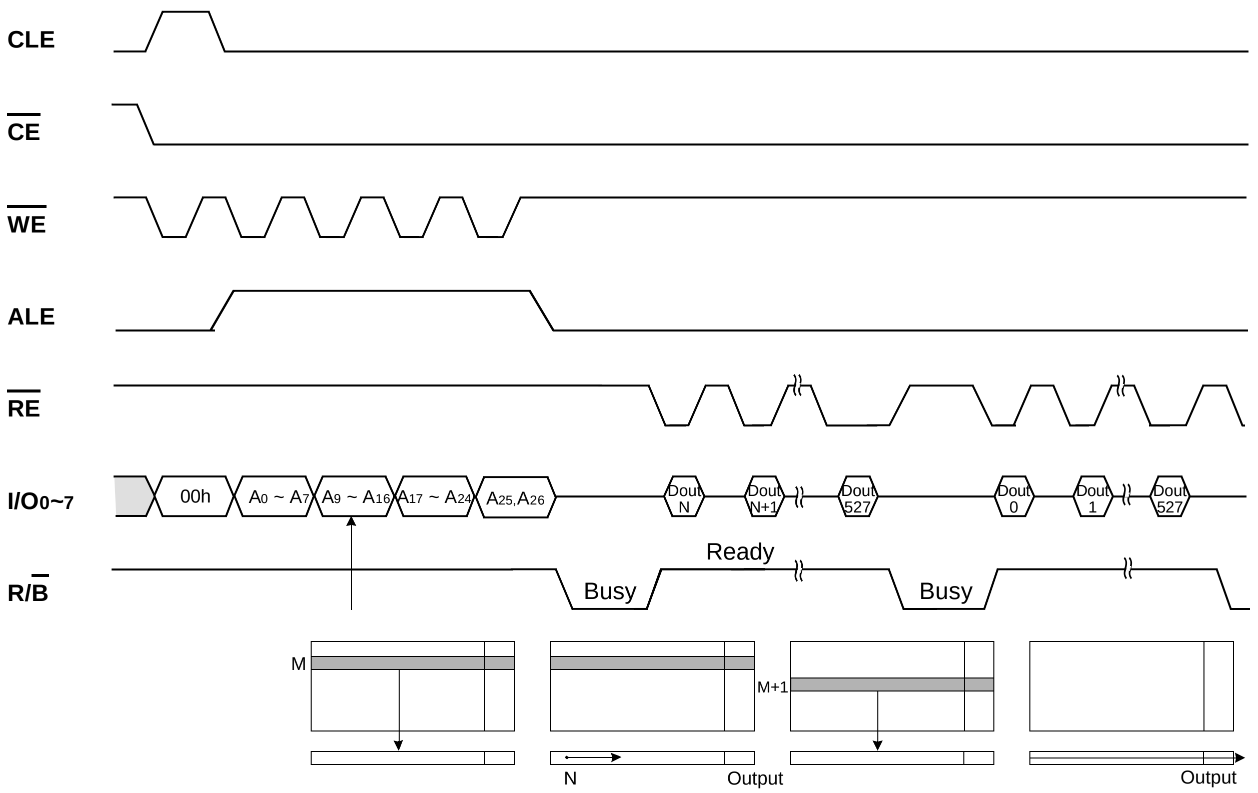
READ1 OPERATION(INTERCEPTED BY CE)



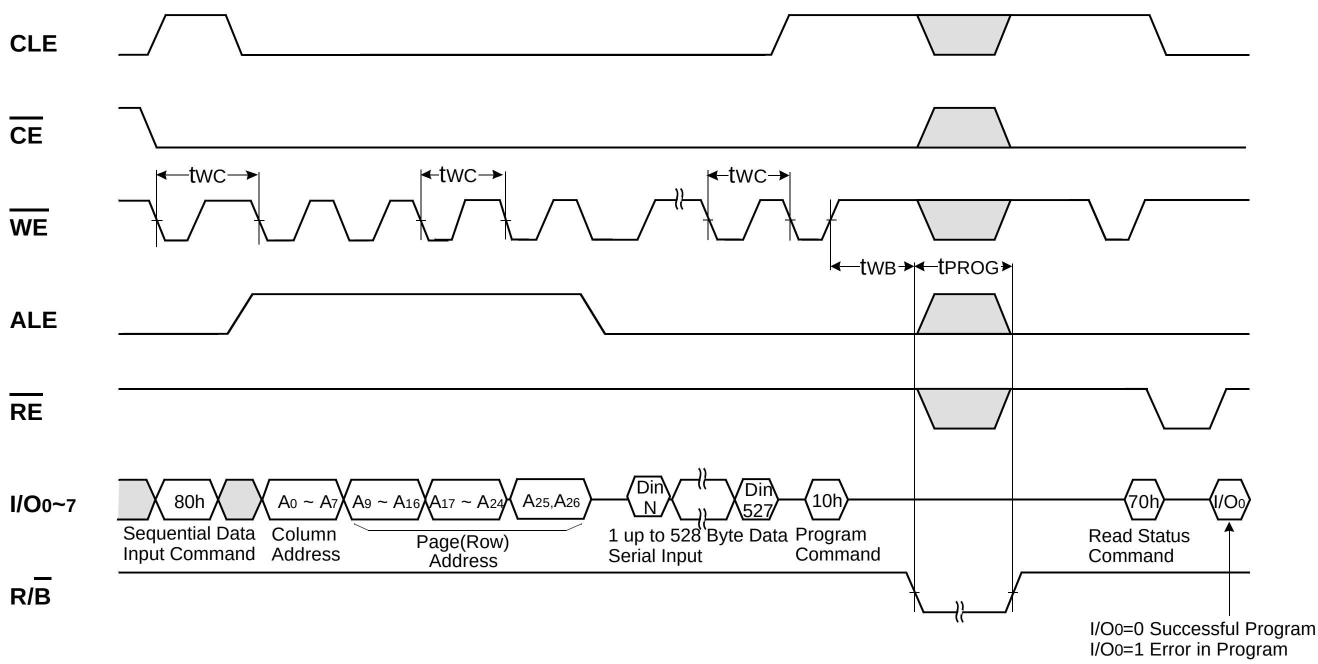
READ2 OPERATION(READ ONE PAGE)



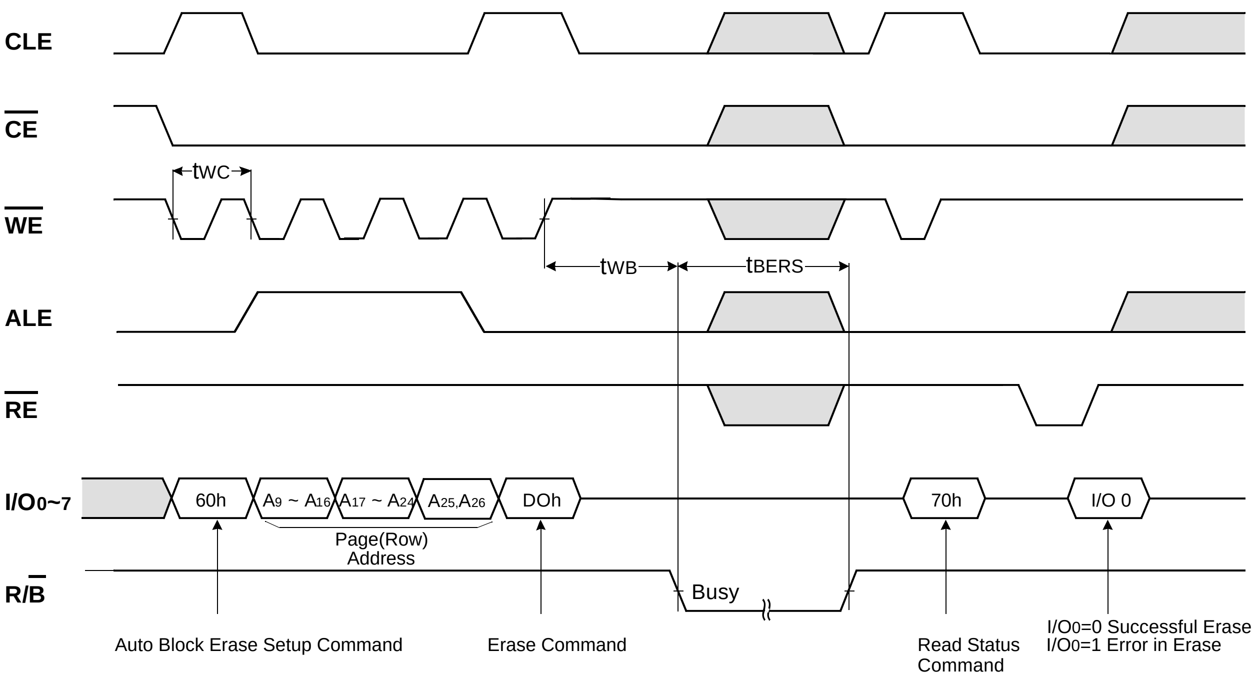
SEQUENTIAL ROW READ OPERATION (WITHIN A BLOCK)



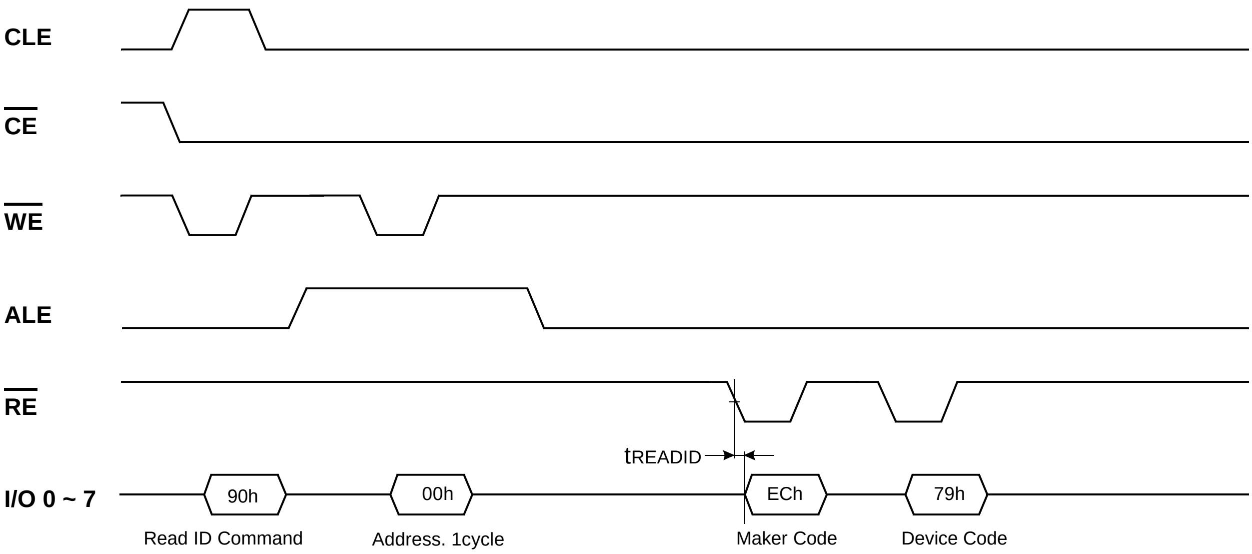
PAGE PROGRAM OPERATION



BLOCK ERASE OPERATION(ERASE ONE BLOCK)



MANUFACTURE & DEVICE ID READ OPERATION

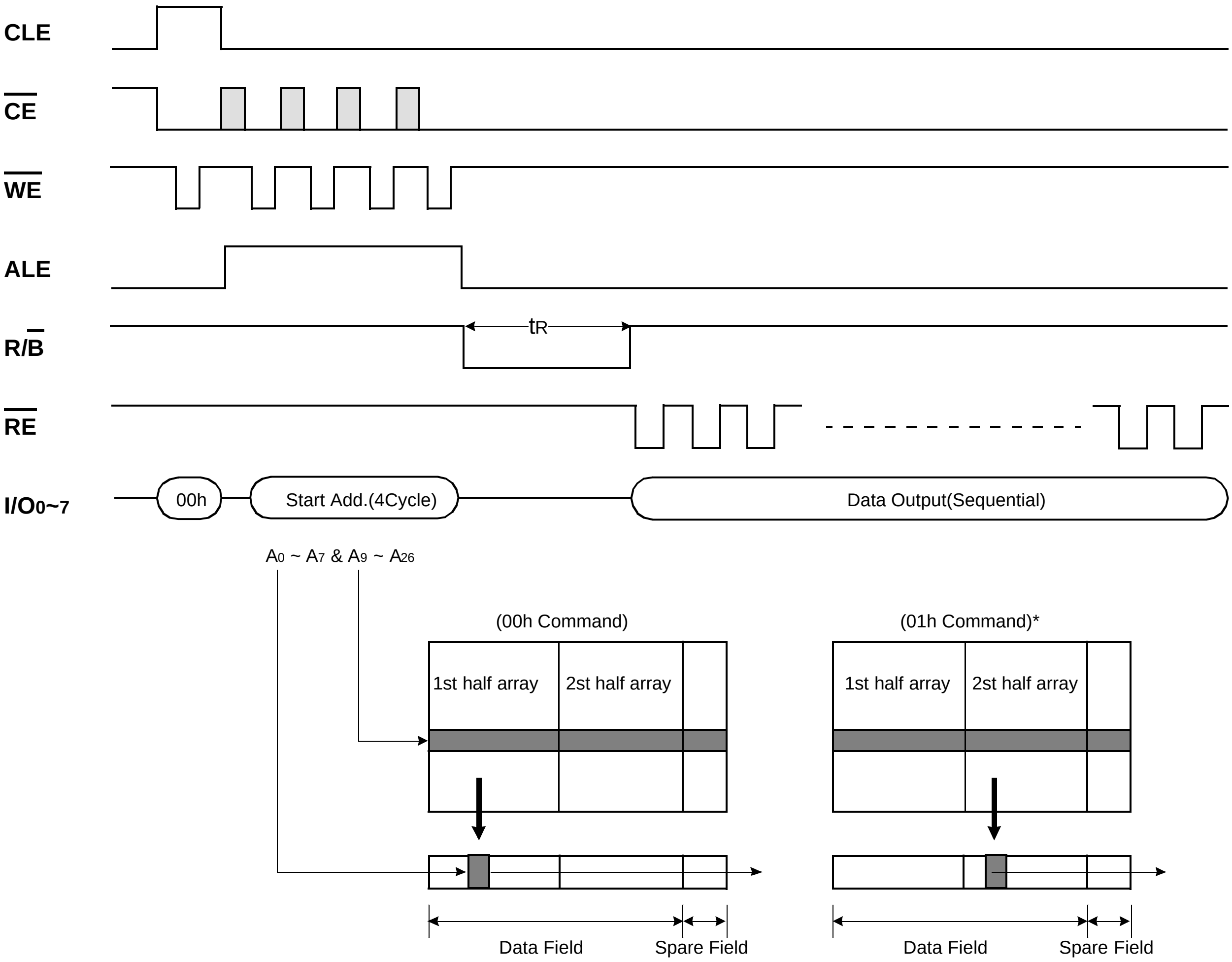


DEVICE OPERATION

PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with four address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read.
The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10µs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing RE. High to low transitions of the RE clock output the data stating from the selected column address up to the last column address.
After the data of last column address is clocked out, the next page is automatically selected for sequential row read.
Waiting 10µs again allows reading the selected page. The sequential row read operation is terminated by bringing CE high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures 3 thru 6 show typical sequence and timings for each read operation.

Figure 3. Read1 Operation



* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Figure 4. Read2 Operation

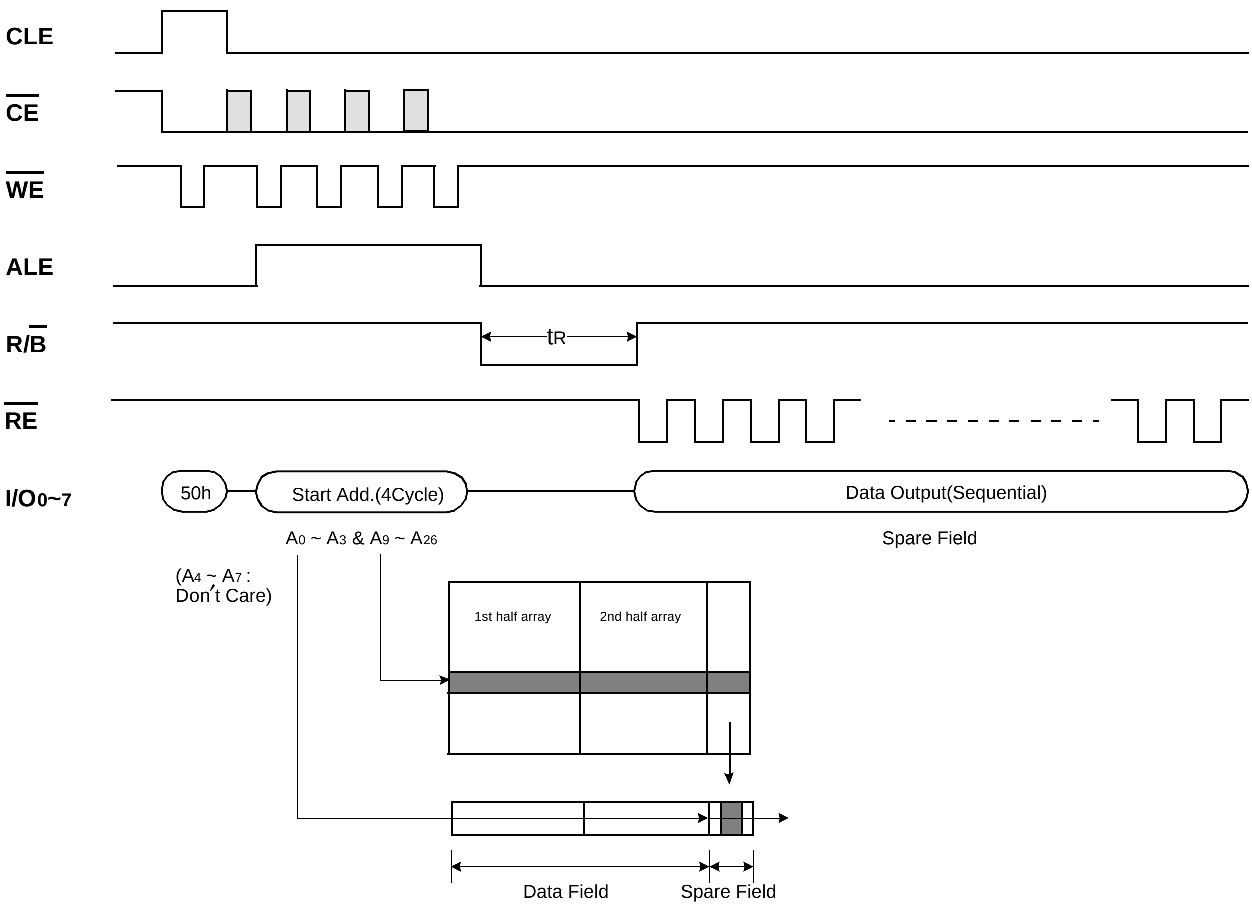
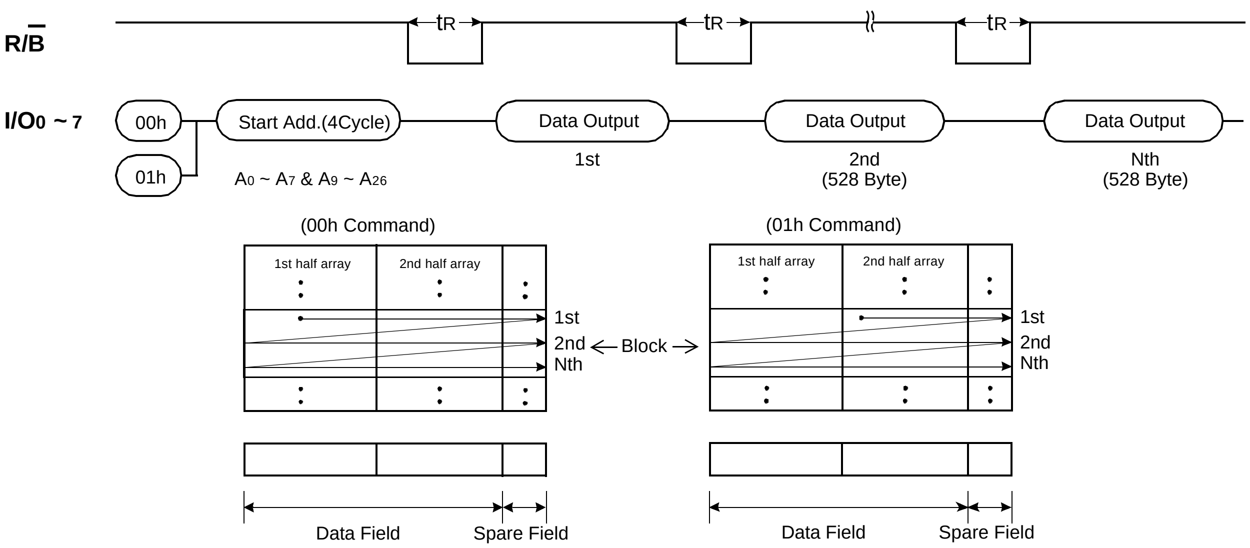
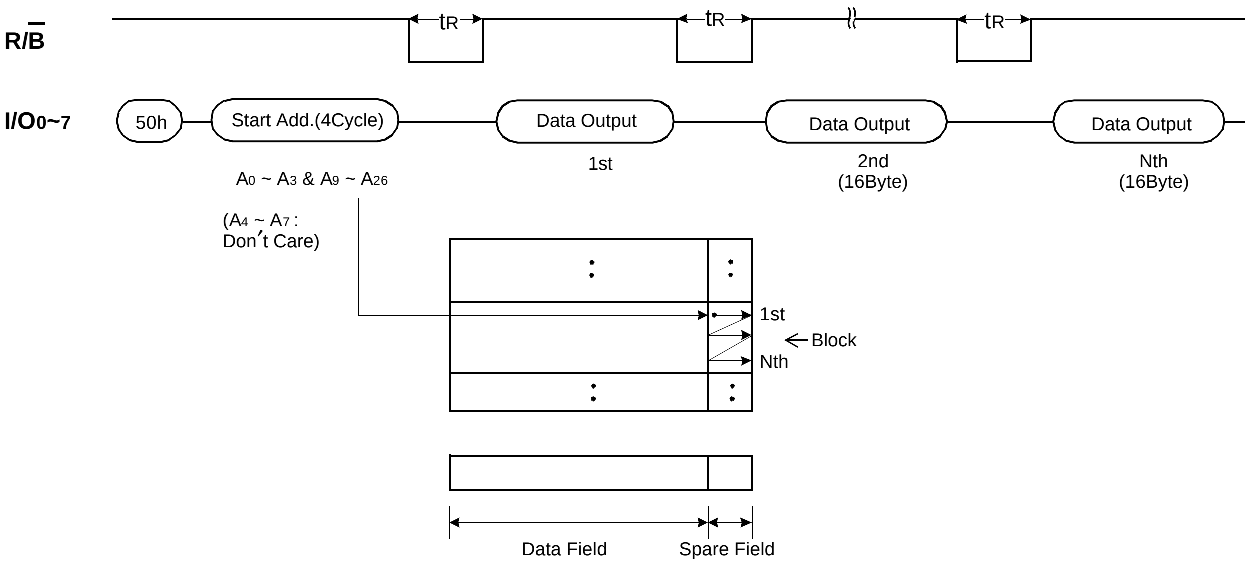


Figure 5. Sequential Row Read1 Operation



The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is read-out, the sequential read operation must be terminated by bringing CE high. When the page address moves onto the next block, read command and address must be given.

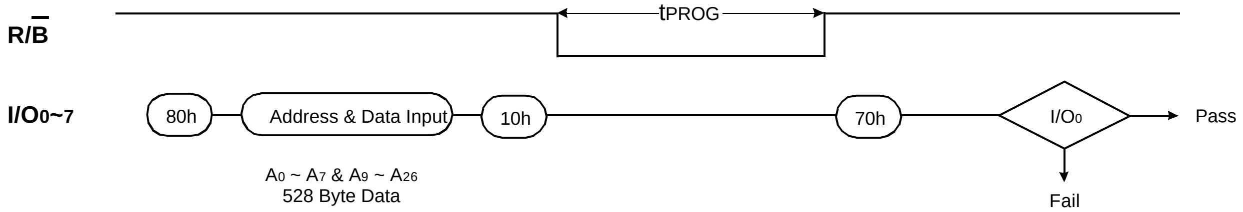
Figure 6. Sequential Row Read2 Operation



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with RE and CE low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 7). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

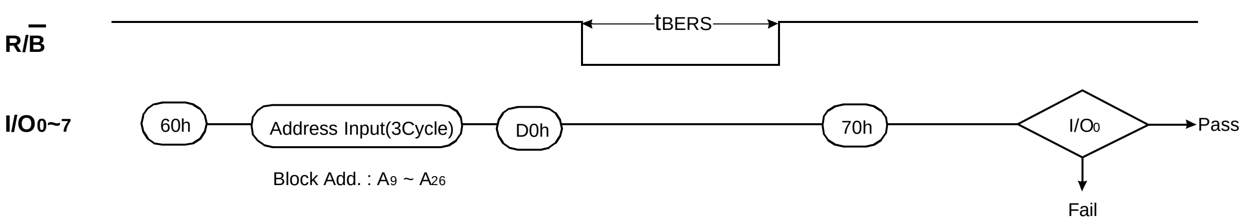
Figure 7. Program & Read Status Operation



BLOCK ERASE

The Erase operation is done on a block(16K Byte) basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{14} to A_{26} is valid while A_9 to A_{13} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 8 details the sequence.

Figure 8. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

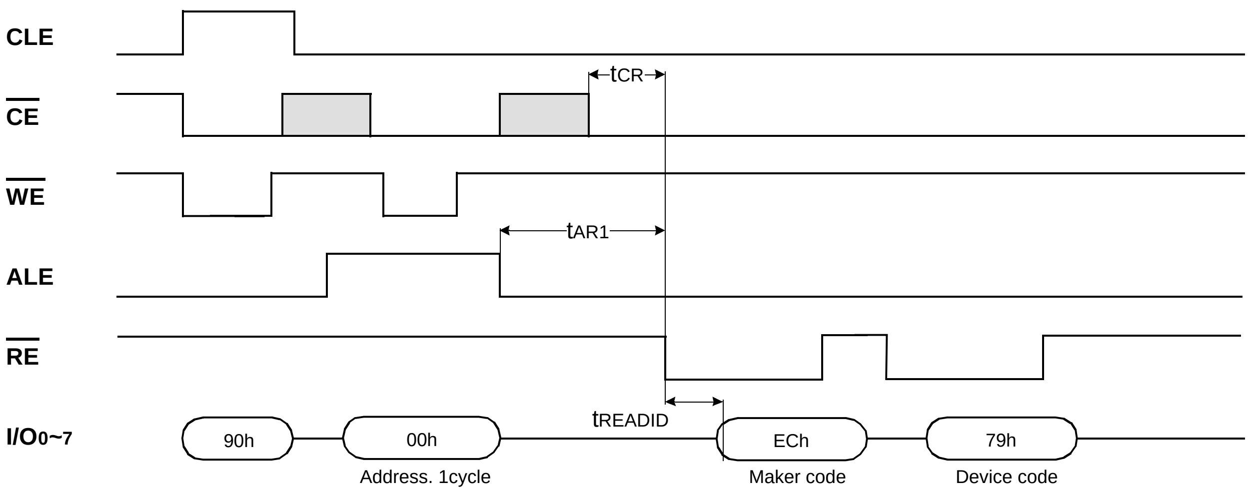
Table2. Read Staus Register Definition

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECH), and the device code (79H) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 9 shows the operation sequence.

Figure 9. Read ID Operation



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 10 below.

Figure 10. RESET Operation

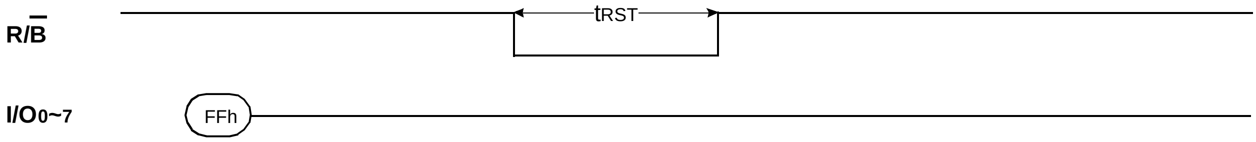
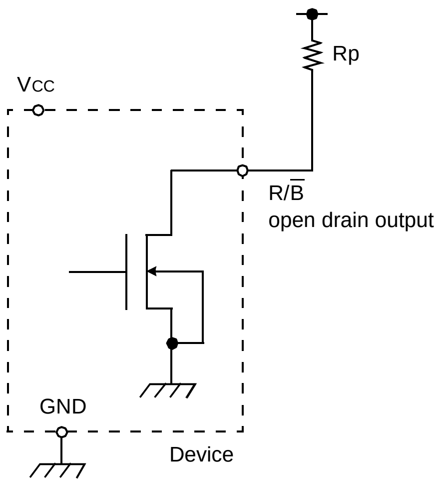


Table3. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. An appropriate pull-up resister is required for proper operation and the value may be calculated by the following equation.



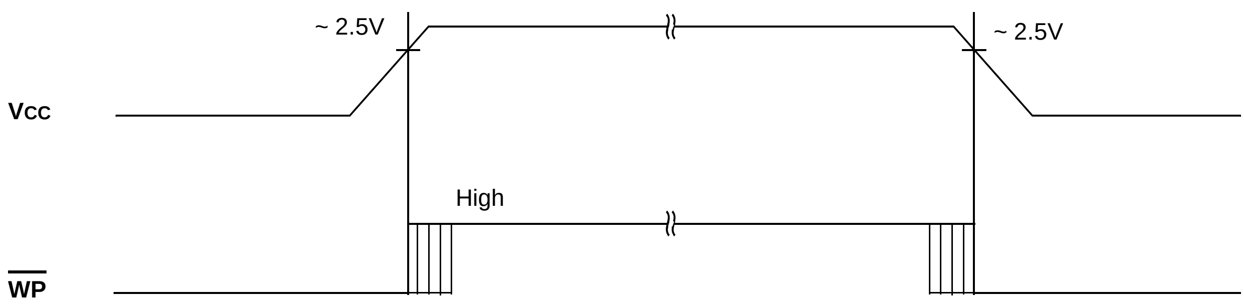
$$Rp = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

DATA PROTECTION

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down as shown in Figure 11. The two step command sequence for program/erase provides additional software protection.

Figure 11. AC Waveforms for Power Transition



DIMENSIONS

Unit:mm

22 PAD SOLID STATE FLOPPY DISK CARD (3.3V)

SOLID STATE PRODUCT OUTLINE