GENERAL DESCRIPTION

The BW0406X_lgisdn is Sigma-Delta CODEC for speech and telephony applications. The product contains both digital IIR/FIR filter and smoothing filter. The normal input and output channels have m/A law format with 38dB signal to distortion ratio.

The input and output of this device is compressed form(A-law, m-law) and 14bit linear which can be easily determined by control select pins

An on-chip voltage reference circuit is included to allow the single supply operation

FEATURES

— Single chip voice line Codec
(A/D, D/A converter included)

— Oversampled Sigma Delta modulator/Demodulator

— Input/Output format : 8bit u-law/A-law and linear 14bit
- These three types are easily selectible by control pins
- When serial interface mode, the 14bit linear data has 16bit format with two don't care bits from LSB

— Sigma Delta ADC
- 256X Oversampling
- On chip Decimation Filter
- On chip Smoothing Filter

— Sigma Delta DAC
- 256X Oversampling
- On chip 256X Interpolation Filter
- On chip Analog Post Filter

— Single ended Input and Output.

— Sampling Rate of 8~11KHz

— On chip voltage reference circuitry

— Single +3.3V Power Supply

— 2Vpp In, Output signal swing

— Power Consumption
- Operating Mode : 10mW Typ(3.3V)
- Powerdown Mode : 33uW Typ(3.3V)

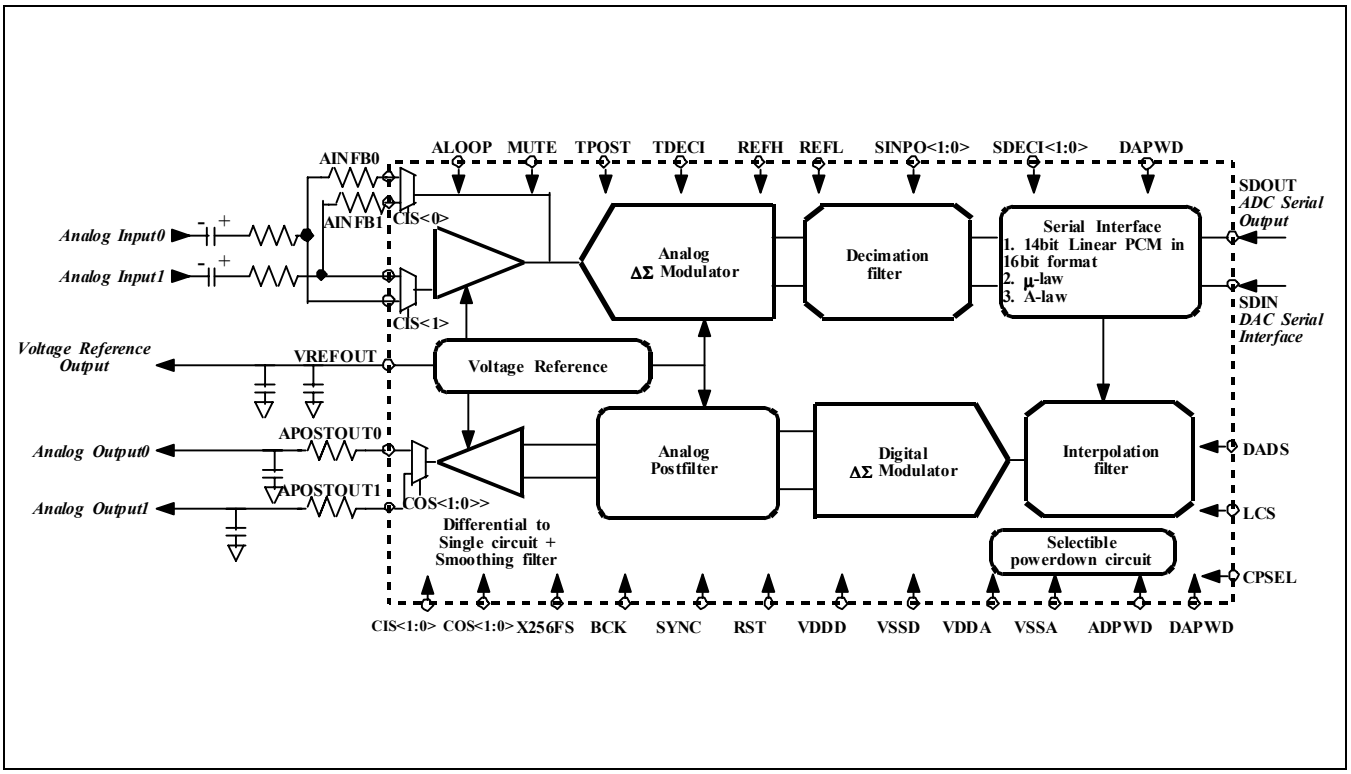
TYPICAL APPLICATIONS

— Speech Processing (Recognition, Synthesis, Compression etc.)

— Telephony

— Modem

BLOCK DIAGRAM WITH INPUT/OUPUT APPLICATION



CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
VDDA	AP	vdda	Analog Power (+3.3V)
VSSA	AG	vssa	Analog Ground (0.0V)
REFH	AP	piar50_bb	Analog Reference Power(+3.3V)
REFL	AG	piar50_bb	Analog Reference Ground (0.0V)
AMODIN0	AI	piar50_bb	ADC Analog input 0
AMODIN1	AI	piar50_bb	ADC Analog input 1
MUTE	DI	picc_bb	Analog Mute select (High active)
ALOOP	DI	picc_bb	Analog loop back select (High active)
VREFOUT	AO	poar50_bb	Vref output
AINFB0	AB	poar50_bb	Analog Input Gain control 0
AINFB1	AB	poar50_bb	Analog Input Gain control 1
APOSTOUT0	AO	poar50_bb	DAC Analog output 0
APOSTOUT1	AO	poar50_bb	DAC Analog output 1
ADPWD	DI	picc_bb	Power Down1 (High active)
DAPWD	DI	picc_bb	Power Down2 (High active)
RST	DI	picc_bb	Digital Reset (High active)
X256FS	DI	picc_bb	256*Sampling Freq.(FS) Clock
SYNC	DI	picc_bb	Sampling Freq.(FS) Clock
SDECI<1:0>	DI	picc_bb	ADC Digital Filter input select
TDECI	DI	picc_bb	ADC Digital Filter Test input
SINPO<1:0>	DI	picc_bb	DAC Post Filter input select
SDIN	DI	picc_bb	Serial Data Input
TPOST	DI	picc_bb	DAC Post Filter Test input
LCS	DI	picc_bb	Linear/Compand data select (Low/High)
CPSEL	DI	picc_bb	m-law/A-law select (Low/High)
VSSD	DG	vssd	Digital Ground
VDDD	DP	vddd	Digital Power Supply
SDOUT	DO	pot2_bb	Serial Data Output
BCK	DI	picc_bb	Bit Clock
DADS	DO	pot2_bb	DAC Modulator output
CIS<1:0>	DI	picc_bb	Analog Input Select Pins
COS<1:0>	DI	pot2_bb	Analog Output Select Pins

NOTES:

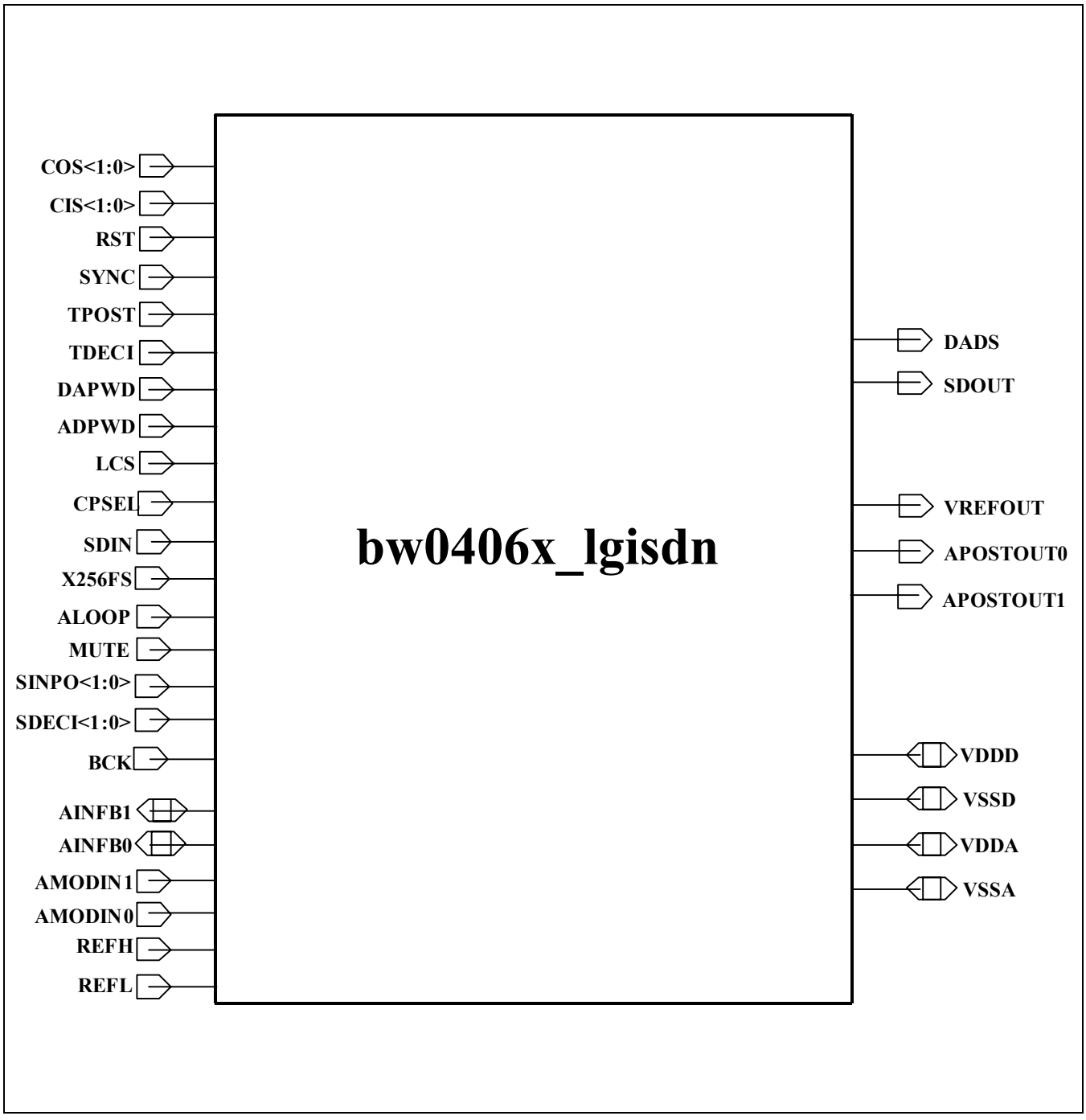
1. This pin description is not fixed, but recommended.
2. The Power pin(VDDA,VDDD) must be connected by DIODE_SLOT2.
3. The Ground pin (VSSA, VSSD) must be connected bye DIODE_SLOT2.
4. SDECI<1:0>, TDECI -> Decimation Filter Block test pin.
5. SINPO<1:0>, TPOST -> Post Filter Block test pin.
6. To operate the power down mode, the two control select pins, ADPWD and DAPWD must be activated simultaneously.
7. The followings are the input/output selection and mute control pins, so use these pins instead MUTE pin.

CIS<1:0>	STATUS	COS<1:0>	STATUS
0 : 0	AMODIN1 is MUTE, AMODIN0 is MUTE	0 : 0	APOSTOUT1 is MUTE, APOSTOUT0 is MUTE
0 : 1	AMODIN1 is MUTE, AMODIN0 is ACTIVE	0 : 1	APOSTOUT1 is MUTE, APOSTOUT0 is ACTIVE
1 : 0	AMODIN1 is ACTIVE, AMODIN0 is MUTE	1 : 0	APOSTOUT1 is ACTIVE, APOSTOUT0 is MUTE
1 : 1	AMODIN1 is ACTIVE, AMODIN0 is ACTIVE	1 : 1	APOSTOUT1 is ACTIVE, APOSTOUT0 is ACTIVE

I/O Type Abbr.

— AI: Analog Input
— DI: Digital Input
— AO: Analog Output
— DO: Digital Output
— AB: Analog Bidirectional
— DB: Digital Bidirectional
— AP: Analog Power
— DP: Digital Power
— AG: Analog Ground
— DG: Digital Ground

CORE CONFIGURTION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	VDDD	-0.3 to 3.8	V
Digital Input Voltage	D_{IN}	-0.3 to 3.8	V
Storage Temperature Range	Tstg	-40 to 125	°C
Operating Temperature Range	Topr	0 to 70	°C

NOTES:

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values ke+pt within the following operating conditions and function operations under any of these conditions is not implied.
2. All voltages are measured with respect to VSS(VSSA or VSSD) unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDA • VSSA VDDD • VSSD	3.15	3.3	3.45	V
Supply Voltage Difference	VDDA • VDDD	0.1	0.0	0.1	V
Digital Input Voltage Range		2.7	3.3	3.6	V
Analog Input Voltage Range		–	2	–	Vpp

NOTE: It is strongly recommended that all the supply pins (VDDA, VDDD) be powered from the same source to avoid power latch up.

CONTROL CLOCK CHARACTERISTICS

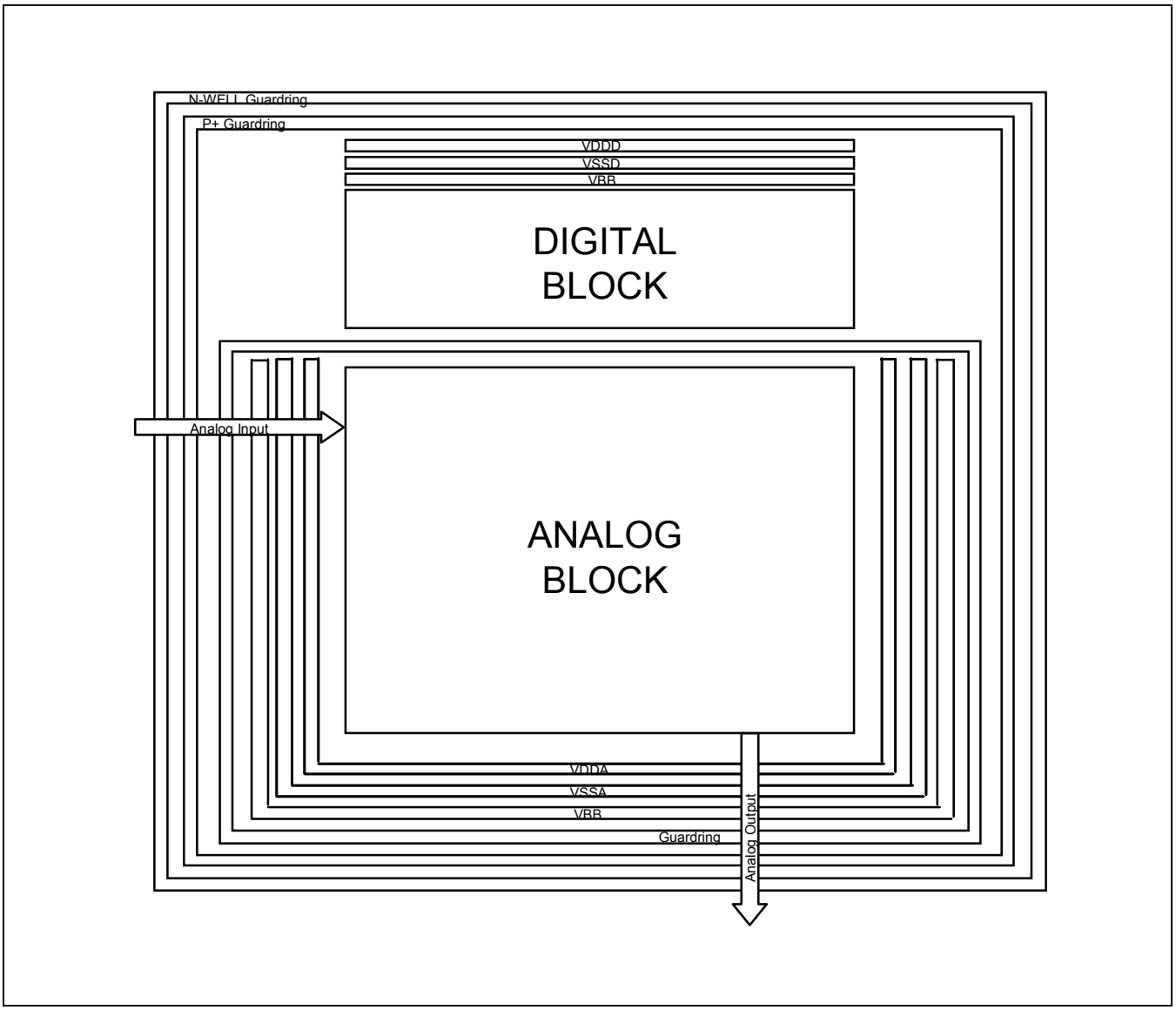
Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
X256FS		1.843	2.048	2.816	MHz	Fs=8KHz
Minimum Pulse Width Low Minimum Pulse Width High		390 390	–	160 160	ns ns	
SYNC Frequency (Fs clock)		–	8	–	KHz	
Duty Cycle		40	–	60	%	

AC ELECTRICAL CHARACTERISTICS

(Measurement Bandwidth is 20Hz-4KHz. Full scale input sine wave 1KHz, FS=8KHz, @VDDA=3.3V, Ta=25°C, Unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution		–	14	–	Bits	
Sampling rate		–	8	–	KHz	–
ADC Analog Input Characteristics						
* Signal to Distortion Ratio		35	38	–	dB	0dB Input : m/A Law compand
		67	70	–	dB	0dB Input : Linear
		28	29.5	–	dB	-40dB Input : u-Law compand
			29			-40dB Input : A-Law compand
		23	25	–	dB	-45dB Input : u-Law compand
			24			-45dB Input : A-Law compand
Offset Error		–	–	±20	mV	–
Input Voltage Range		–	2	–	Vpp	–
DAC Analog Input Characteristics						
* Signal to Distortion Ratio		35	38	–	dB	0dB Input : m/A Law compand
		67	70	–	dB	0dB Input : Linear
		30	33.5	–	dB	-40dB Input : u-Law compand
		29	32			-40dB Input : A-Law compand
		25	30	–	dB	-45dB Input : u-Law compand
		24	27			-45dB Input : A-Law compand
Offset Error		–	–	±20	mV	–
Output Voltage Range		–	2	–	Vp--p	–
Digital Filter Specification						
Passband		0		0.4	Fs	
Passband Ripple			+/-0.25		dB	
Stopband		0.4		0.6375	Fs	
Stopband Attenuation			-40		dB	
Power Supply						
Power comsumption (3.3v Operating Mode) Analog Digital		–	– 2.5 0.5	– 3 0.7	mA	–
Power comsumption (3.3v Powerdown Mode)		–	10	–	mA	

CORE LAYOUT GUIDE



NOTES:

1. The layout of bw0406x consists of digital part and analog part.
   The digital part and the analog part must be divided.
2. The substrate of digital and analog part is seperated from digital and analog ground so that it can minimize noise through substrate.
3. It is recommended that you use thick analog power metal. when connecting to PAD, and the path should be kept as short as possible.
4. Digital power and analog power are used separately.
5. When the core block is connected to other blocks, it must be double guardring using N-well and P+active to remove the substrate and coupling noise.
   In that case, the power metal should be connected to PAD directly.
6. Digital input signal lines must be same length to reduce the difference of delay.

CORE EVALUATION GUIDE

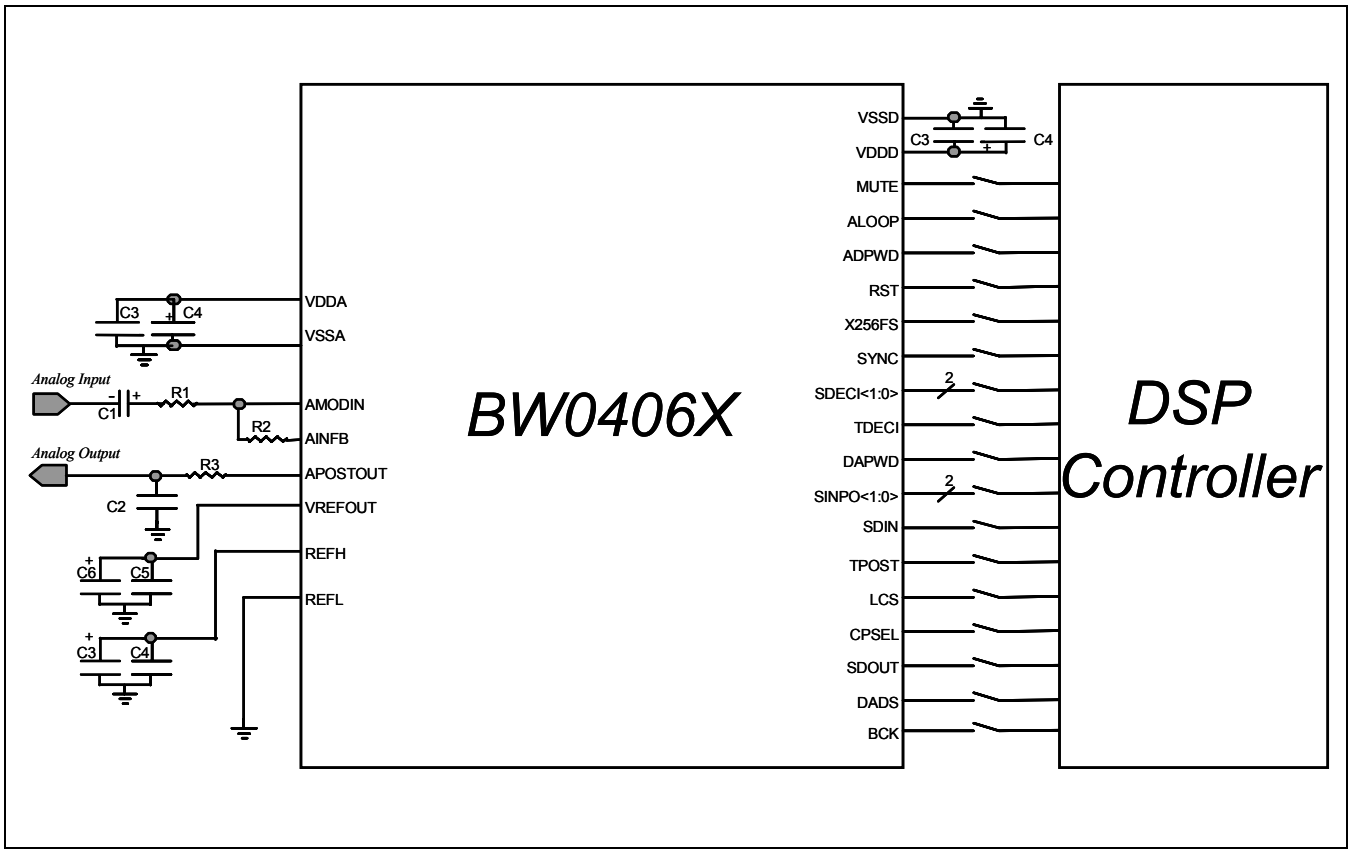


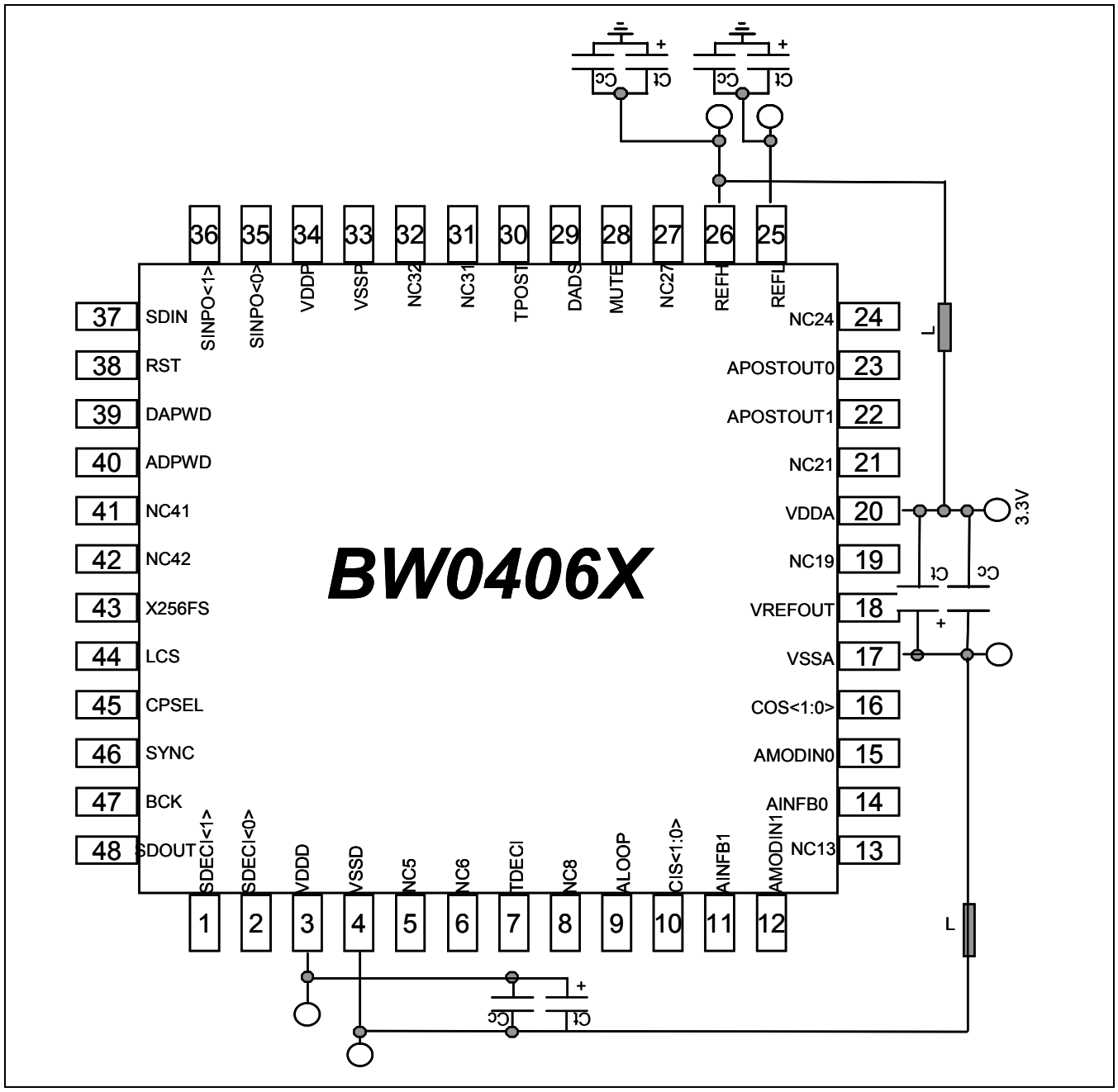
Table 1. The Connection User Guide Line for Embedded Core Test

Location	Description
C3	0.1mF TANTALUM CAPACITOR
C4, C6	10mF CERAMIC CAPACITOR
C1	0.33mF TANTALUM CAPACITOR
C2	75pF CERAMIC CAPACITOR
R1, R2	50kW RESISTOR
R3	200kW RESISTOR
C5	0.1uF TANTALUM CAPACITOR

NOTES:

1. If SDOUT is externally shorted with SDIN, The CODEC is achieved to loop-back test mode(ADC->DAC).
2. If end users want to test CODEC in integrated chip, The above pin must be extracted to the PAD(pin 14).
3. The analog power/ground must be separated from digital power/ground.
4. CPSEL = 1; A-law select, 0; m-law select
5. I/O TYPE PP and PG denote PAD Power and PAD Ground respectively.
6. Power typical value:
   VDDA = VDDD = 3.3V, VSSA = VSSD = 0.0V

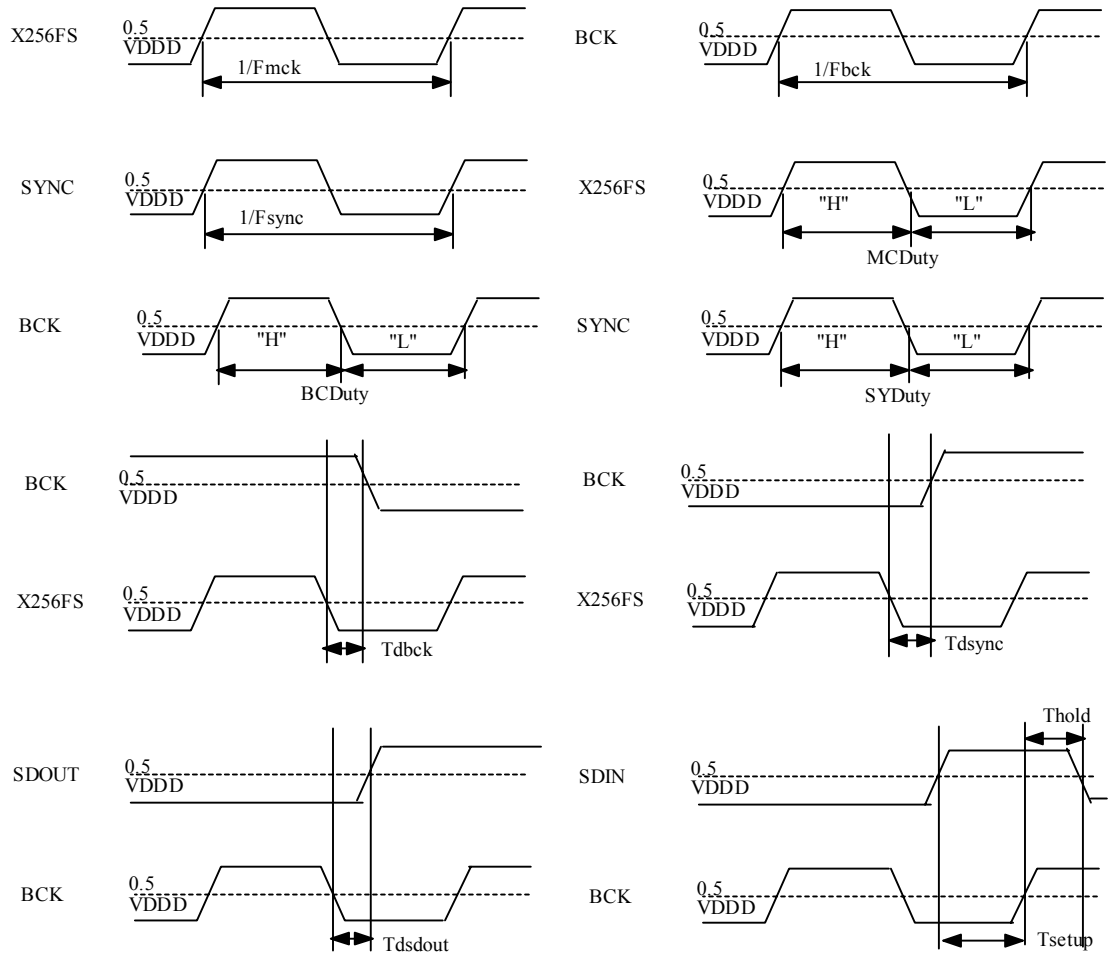
PACKAGE CONFIGURATION



LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR
L	FERRITE BEAD (0.1mH)

CONTROL CLOCKS CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
X256FS Frequency	Fmck	–	2.048	–	MHz
BCK Frequency	Fbck	–	256	–	KHz
SYNC Frequency	Fsync	–	8	–	KHz
X256FS Duty cycle (H:L)	MCDuty	40:60	50:50	60:40	%
BCK Duty cycle (H:L)	BCDuty	40:60	50:50	60:40	%
SYNC Duty cycle (H:L)	SYDuty	40:60	50:50	60:40	%
X256FS Falling and BCK Edge Delay(Hold)	Tdbck	5	10	15	ns
X256FS Falling and SYNC Edge Delay(Hold)	Tdsync	5	10	15	ns
BCK Falling and SDOUT Delay	Tdsdout	5	10	15	ns
BCK Rising and SDIN Setup	Tsetup	10	15	20	ns
BCK Rising and SDIN Hold	Thold	10	15	20	ns



*Notes : BCK rising edge must NOT occur at the same time as SYNC edge.

SAMSUNG ELECTRONICS

TIMING DIAGRAM

The frame of sync clock(SYNC) transitions determine the start of the serial data.

Input data

- All input data are clocked in by the falling edge of BCK.
- 14bit, 2's complement or 8bit A-law, u-law data format.

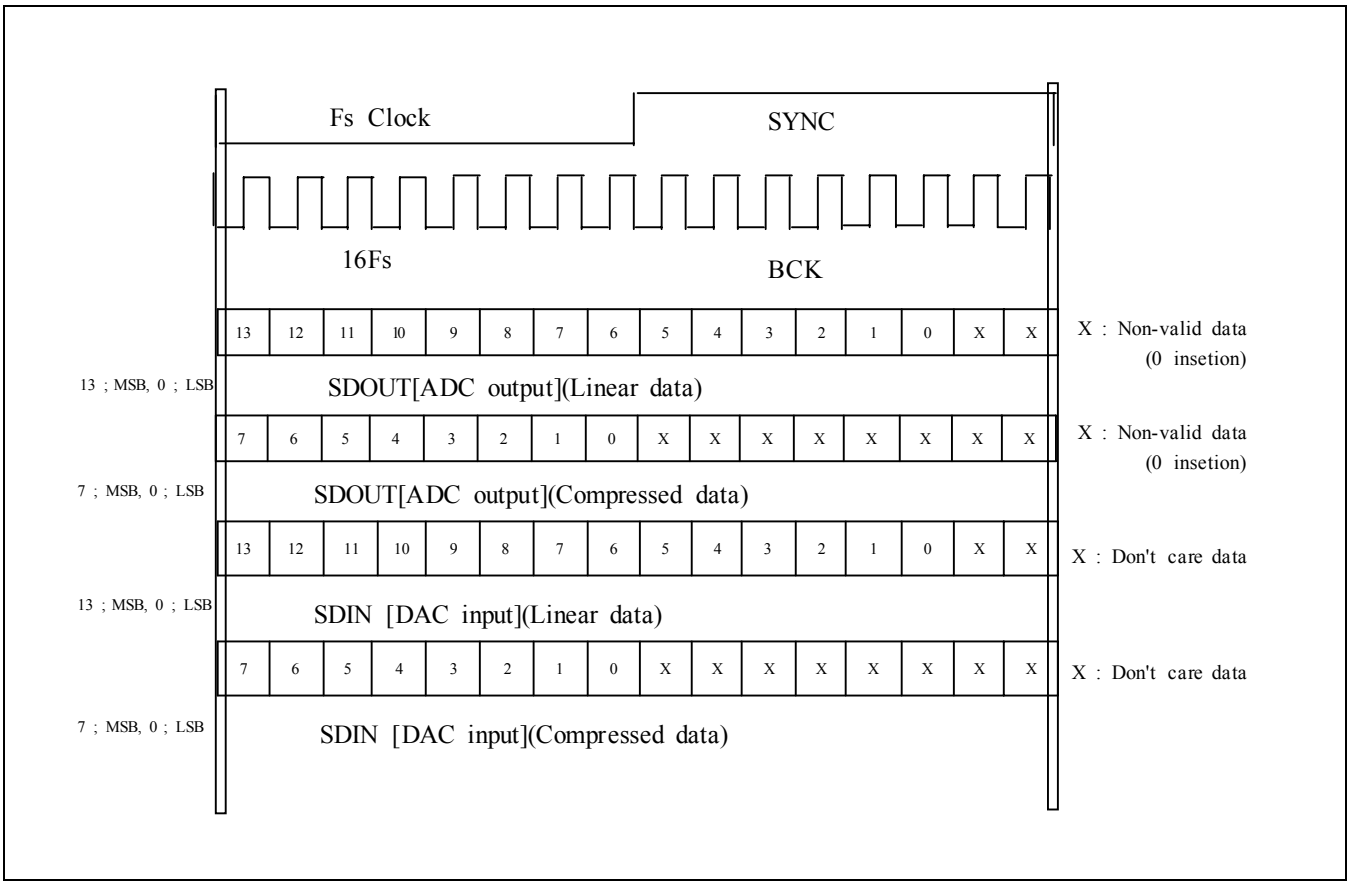
Output data

- All output data are clocked out by the falling edge of BCK.
- 14bit, 2's complement or 8bit A-law, u-law data format.

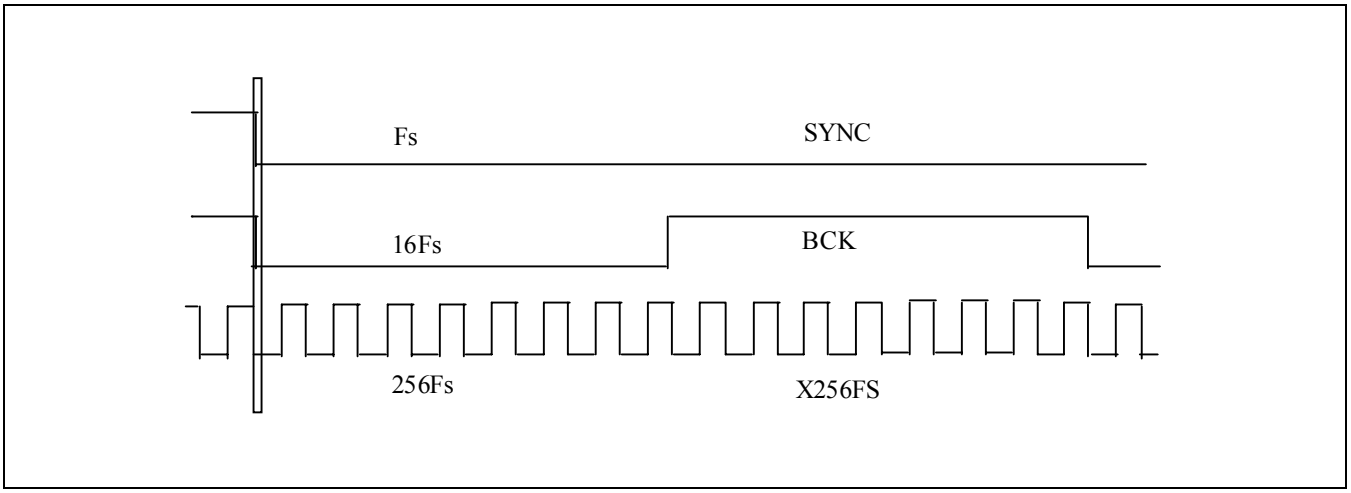
NOTES:

1. SYNC clock is at sampling frequency, Fs
2. 14bit linear data has 16bit serial data format, this is accomplished by 16FS (= Fs clock x 16) and two don't care bits are added from LSB, to fit into 16bit format.

Codec serial interface timing diagram

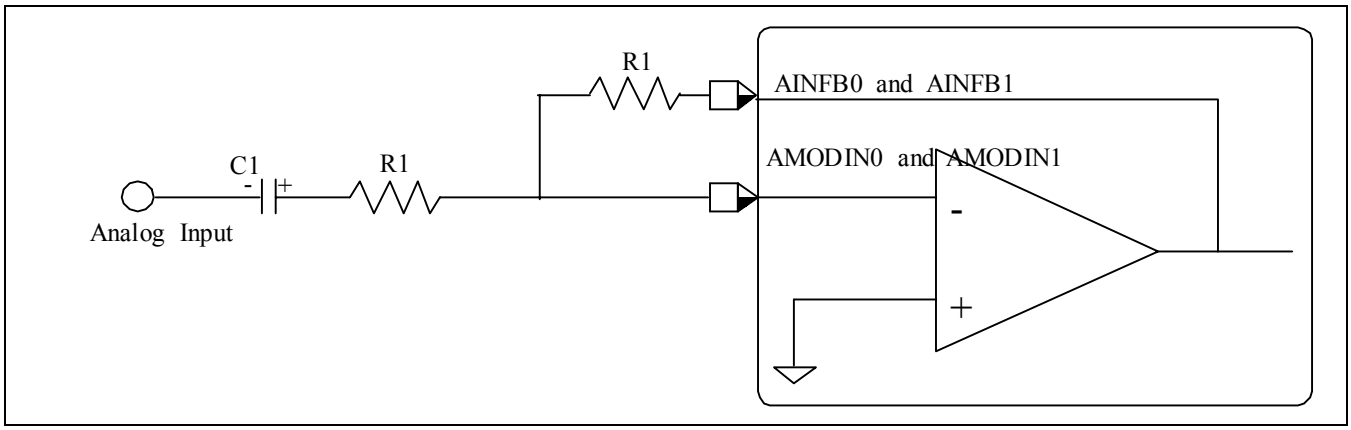


Codec clock interface timing diagram



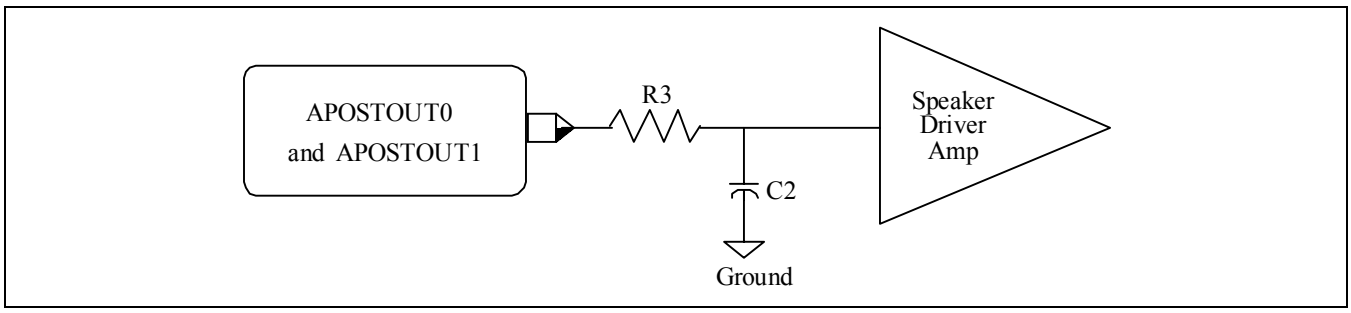
INPUT/OUTPUT APPLICATION GUIDE

1. Input stage application guide



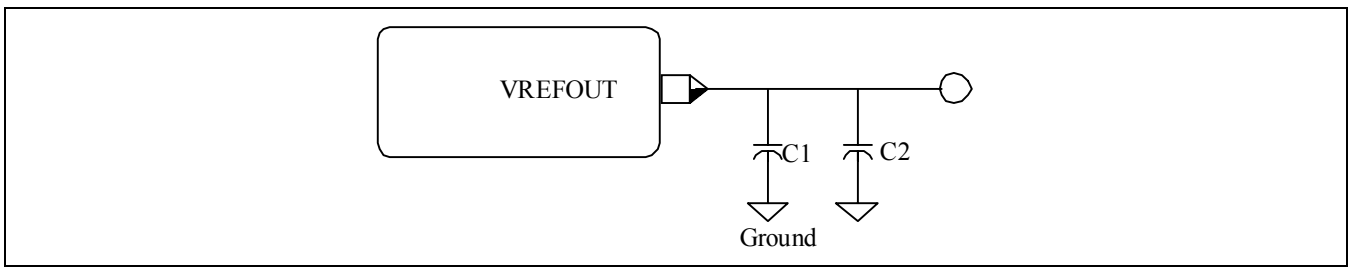
Typhical value of R1 and C1
R1 > 50KΩ
C1 = 0.33mF

2. Output stage application guide



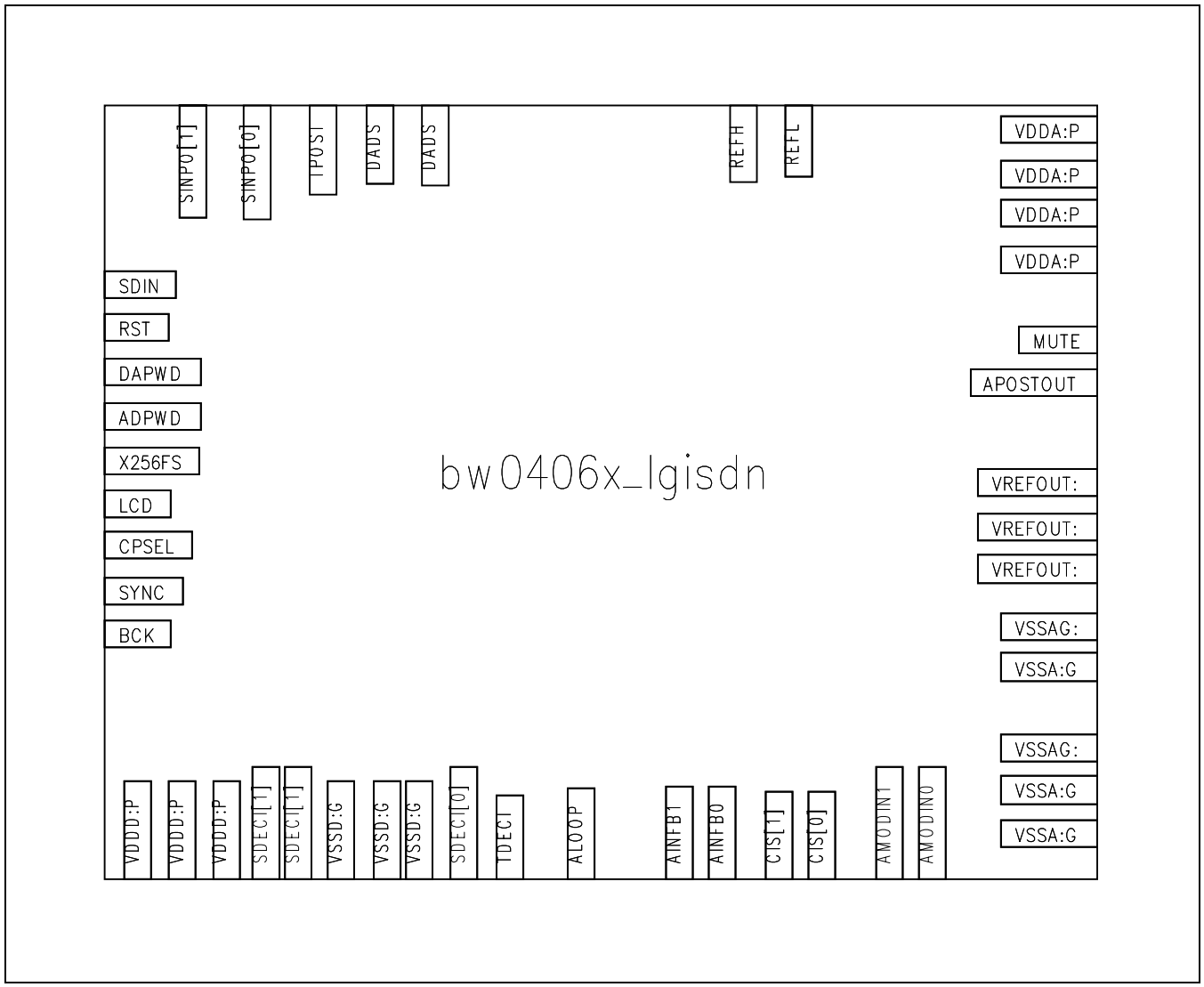
How to determine the value of R3 and C2.
C2 = 1.5*10-5/R3
For example : If you choose R3 as 200KΩ, then the value of C3 is 75pF.

3. VREFOUT port application guide

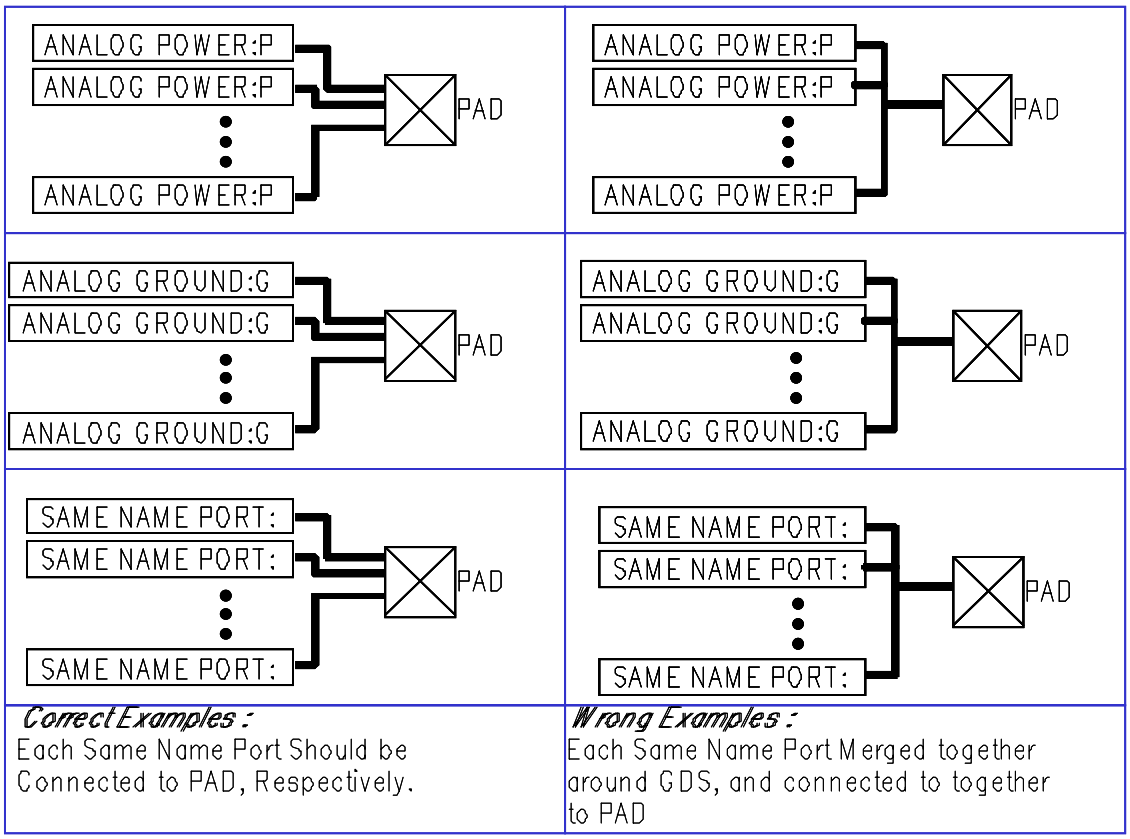


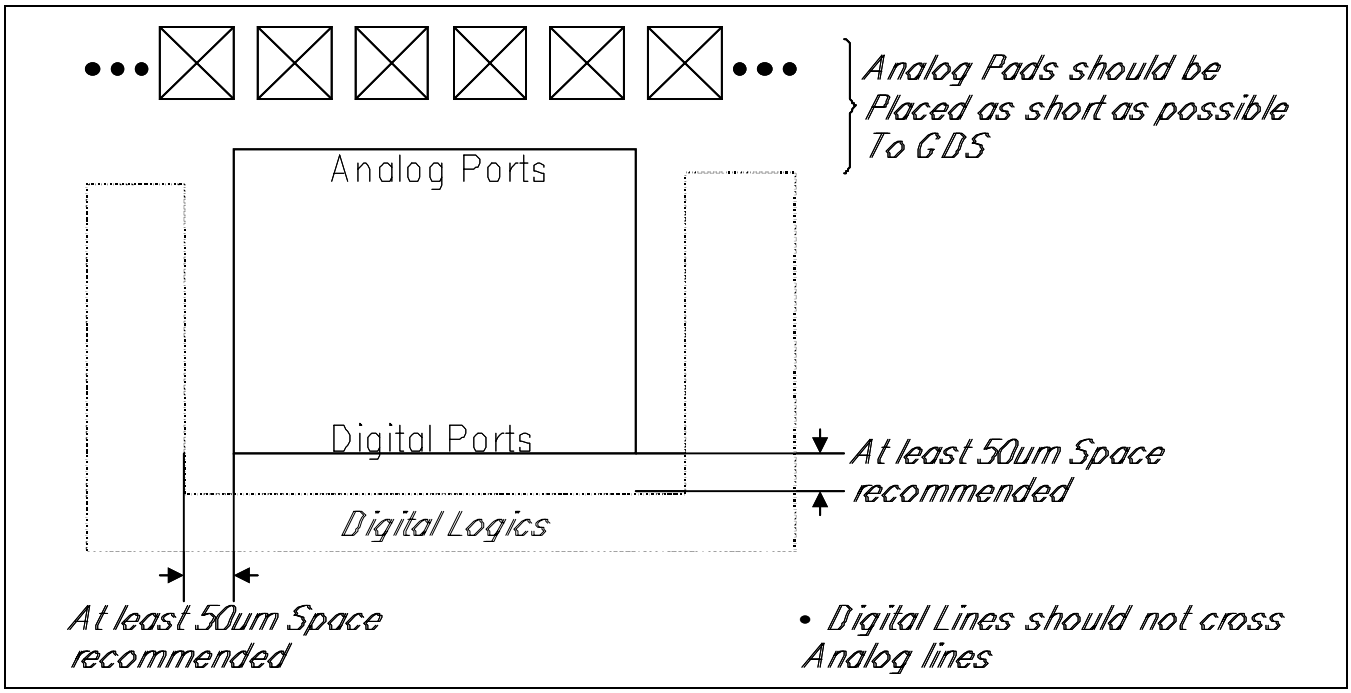
C1 = 0.1mF, C2 = 10mF
Note : The user should dispose the C1 and C2 as the order shown above and dispose the capacitors to VREFOUT pin as close as possibe.

PHANTOM CELL INFORMATION



LAYOUT GUIDE





FEEDBACK REQUEST

It should be quite helpful to our CODEC core development if you specify your system requirements on CODEC in the following characteristic checking table and fill out the additional questions.

We appreciate your interest in our products. Thank you very much.

— Could you explain external/internal pin configurations as required?

Specially requested function list :

1. What is your signal band to use, 3.6KHz? 4KHz? or 4.8KHz?
2. What is your analog in/output signal voltage swing? and what kind of format do your want as analog signal in/ouput: single or differential format? If you can, Please let us know, what is your exact in/output signal spec.
3. What is your minimum S/N+D spec?
4. Do you want linear phase characteristic or you don't care on digital filter spec?
5. Could you give us exact design spec of speech codec? (For example, A-law, u-law and so on.)

REVISION HISTORY

Version	Date	Modified Items	Comments
Ver 1.0	02.04.28	- p5: Digital Filter Specification added - p12: Phantom Cell Information added - p13: Layout Guide added	
Ver 1.1	02.07.30	- p1: a typo corrected	