GENERAL DESCRIPTION

The AL1214H is a CMOS 10-bit D/A converter for general applications. Its maximum conversion rate is 80MSPS and supply voltage is 5V single. An external 3.2V voltage reference (VREF) and a single resister (RSET) control the full-scale output current.

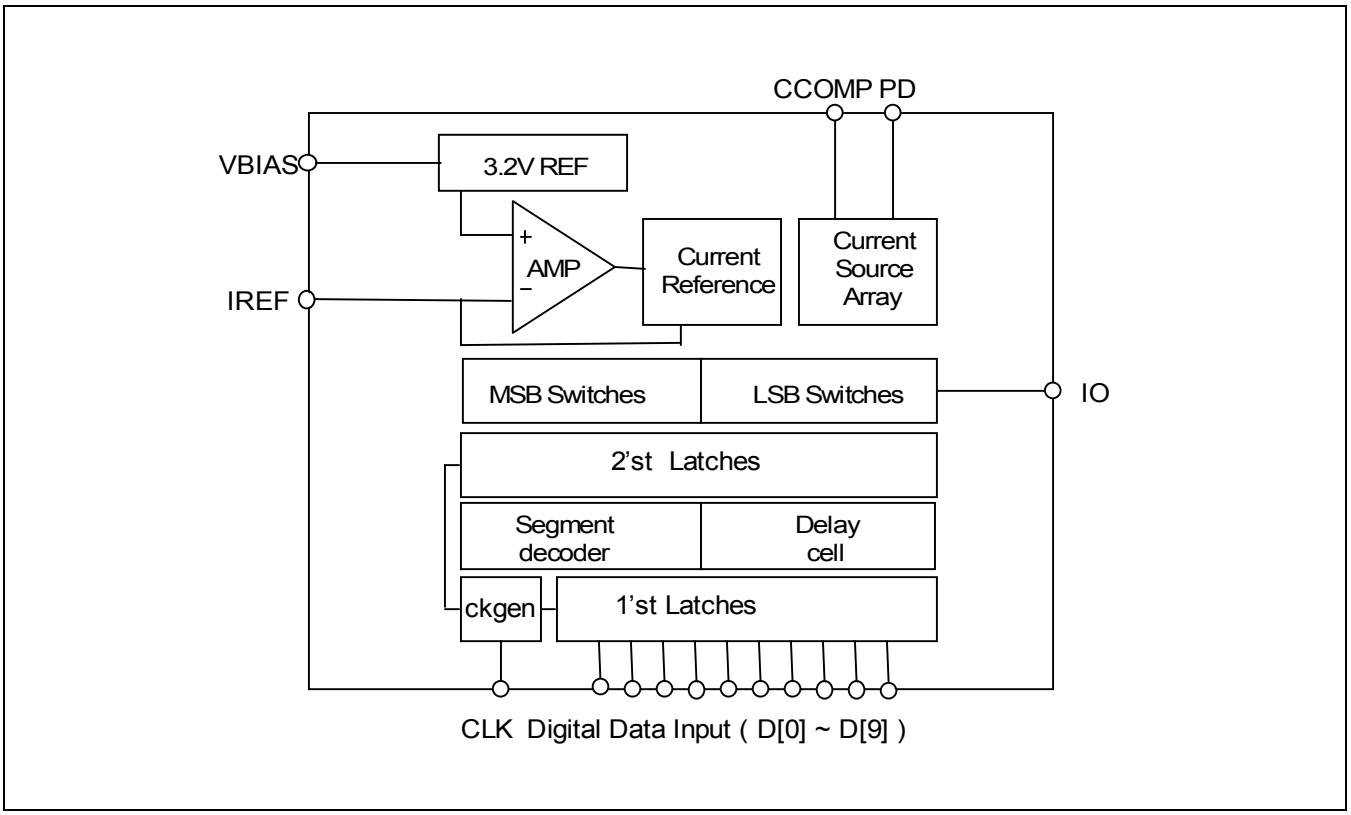
FEATURES

- 0.5um CMOS device technology
- 2 clock pipeline operation
- 5V CMOS monolithic construction
- ± 1LSB differential linearity (typical)
- ± 1LSB integral linearity (typical)
- External voltage reference
- 10-bit voltage parallel input

TYPICAL APPLICATIONS

- High Definition Television (HDTV)
- Hard Disk Drive (HDD)
- High Resolution Color Graphics
- CAE/CAD/CAM
- General Video application

FUNCTIONAL BLOCK DIAGRAM



Ver1.6 (Apr. 2002)

CORE PIN DESCRIPTION

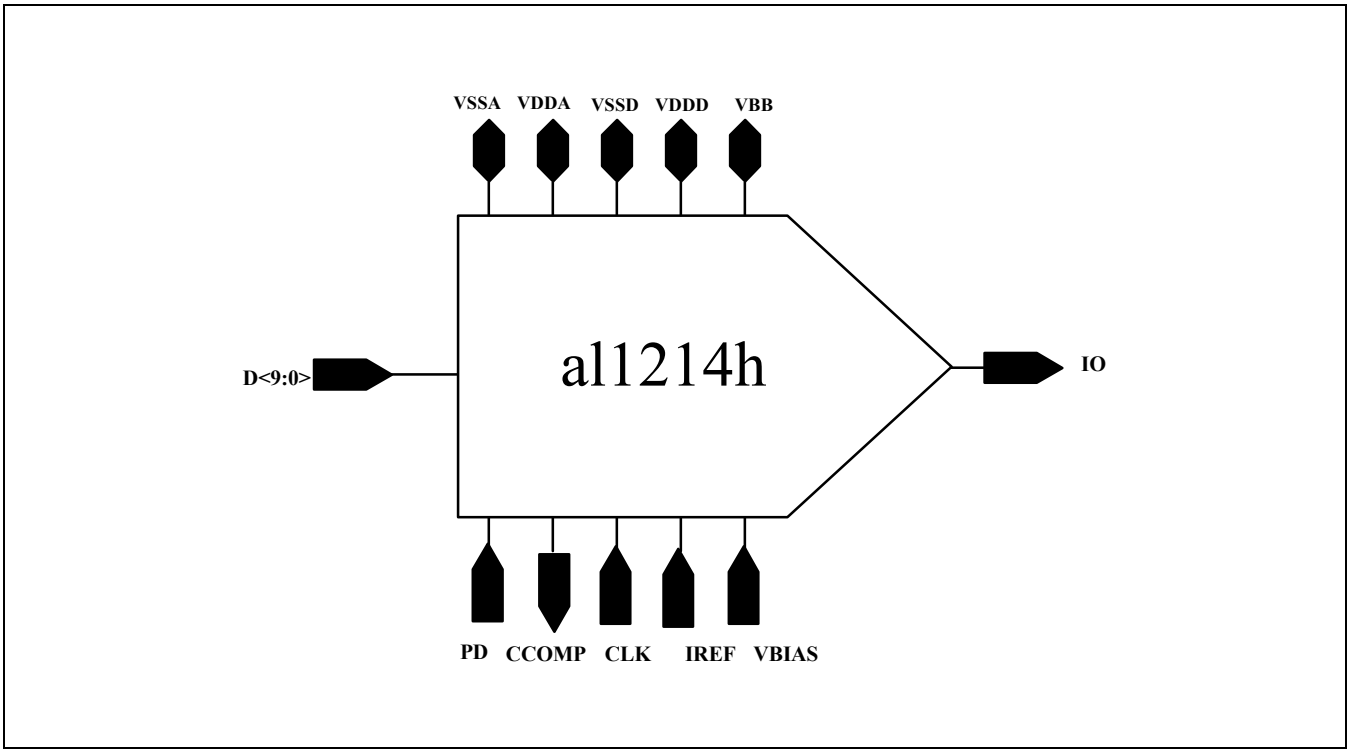
Name	I/O Type	I/O Pad	Pin Description
IO	AO	poa_bb_50option	Analog Output (output Range : 2Vpp)
D<9:0>	DI	pic_bb	Digital input
PD	DI	pic_bb	high = power saving standby mode (normally = gnd)
CLK	DI	pic_bb	Clock Input
VBIAS	AI	poa_bb_50option	External Bias (3.2V)
IREF	AI	poa_bb_50option	Full Sale Adjust Control
CCOMP	AO	poa_bb_50option	Using Compensation Capacitor
VDDA	AP	vdda	Analog Power
VSSA	AG	vssa	Analog Ground
VDDD	DP	vddd	Digital Power
VSSD	DG	vssd	Digital Ground
VBB	AG	vbba	Analog Ground (bulk bias)

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Analog Output
- AB :Analog Bi-direction
- DB :Digital Bi-direction

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Min	Unit
Supply Voltage	VDDD,VDDA	7.0	V
Reference Input Voltage	Vin	VSSD-0.3 to VDDD+0.3	V
Operating Temperature Range	Topr	0 to +70	°C
Storage Temperature Range	Tstg	-40 to +125	°C

NOTES:

1. Absolute maximum rating values applied individually while all other parameters are within specified operating condition. Function operation under any of these conditions is not implied.
2. Applied voltage must be current limited to specified range
3. Absolute maximum ratings are value beyond which the device may be damaged permanently. Normal operation is not guaranteed.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	VDDD-VSSD VDDA-VSSA	4.75	5.0	5.25	V
Digital Input Voltage High	VIH	4.5	-	-	V
Digital Input Voltage Low	VIL	-	-	0.5	V
Operating Temperature Range	TOPR	0	-	70	°C
Clock Cycle Time	Tclk	-	12.5	-	ns
Clock Pulse Width High	Tpwh	-	6.2	-	ns
Clock Pulse Width Low	Tpwl	-	6.2	-	ns

NOTES:

1. It is strongly recommended that to avoid power latch-up all the supply pins (VDDA,VDDD) are driven from the same source.
2. Voltage on any digital pin that goes below VSSD (Digital Ground) by less than 0.3V can induce destructive latch-up

DC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Resolution	-	8		-	Bits
Differential Linearity Error	DLE	-	0.3	± 1	LSB
Integral Linearity Error	ILE	-	0.5	± 1	LSB
Monotonicity	-	-	Guaranteed	-	-
Full Scale	FS	1.9	2.0	2.1	V
Maximum Output Compliance	VOC	-0.3	-	+1.5	V
External Reference Voltage	VBIAS	-	3.2	-	V
Reference Current	Iref	-	1.4	-	mA

NOTES:

1. Converter Specifications (unless otherwise specified)
   VDDA = 5.0V VDDD = 5.0V
   VSSA = GND VSSD = GND Ta = 25°C
   HDD application : RL = 160Ω, Rset = 1kΩ, VBIAS = 3.2V
   Video application : RL = 37.5Ω, Rset = 463Ω, VBIAS = 3.2V
2. TBD : To Be Determined

AC ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Clock Rate	fc	-	-	80	MHz
Analog Output Rise Time	Tr	-	12	15	ns
Analog Output Fall Time	Tf	-	13	15	ns
Analog Output Settling Time	Ts	-	91	100	ns
Clock and Data Feed through	FDTHR	-29	-27	-25	dB
Glitch Impulse	GI	-146	-114	-90	pv-sec
Pipeline Delay	Tpd	-	2	-	Clocks
Supply Current	Idd	-	22	25	mA
Signal to Noise Distortion Ratio	SND	-	-53	-47	dB

NOTES:

1. The parameters are not tested through the temperature range, but these are guaranteed over the full temperature range.
2. Clock and data feed through is a function of the amount of overshoot and undershoot on the digital inputs. Settling time does not include clock and data feed through. Glitch impulse include clock and data feed through.

FUNCTIONAL DESCRIPTION

This is a 10-bit 80MSPS digital to analog data converter and uses segment architecture for 5-bit of MSB sides and binary-weighted architecture for 5-bit of LSB side. It contains of 1'st latch block, decoder block, 2nd latch block, AMP block, CM (current mirror) block and analog switch block. This core uses reference current to decide the 1LSB current size by dividing the reference current by 116 times. So the reference current must be constant and the switch's physical real size can be constant by using AMP block with high DC gain. The most significant block of this core is analog switch block and it must maintain the uniformity at each switch, so layout designer must care of the matching characteristics on analog switch and CM block. And more than 80% of supply current is dissipated at analog switch block and AMP block. And it uses samsung (SEC) standard cell as all digital cell of latch , decoder and buffer. And to adjust full current output, you must decide the "Rset" resistor value (connected to IREF pin). Its voltage output can be obtained by connecting Rload (connected to IO pin) .

Linearity Error : Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Monotonicity : A D/A converter is monatomic if the output either increases or remains constants as the digital input increases.

Offset Error : The deviation of the output current from the ideal of zero is called offset error. For IO , 0mV output expected when the inputs are all 0s.

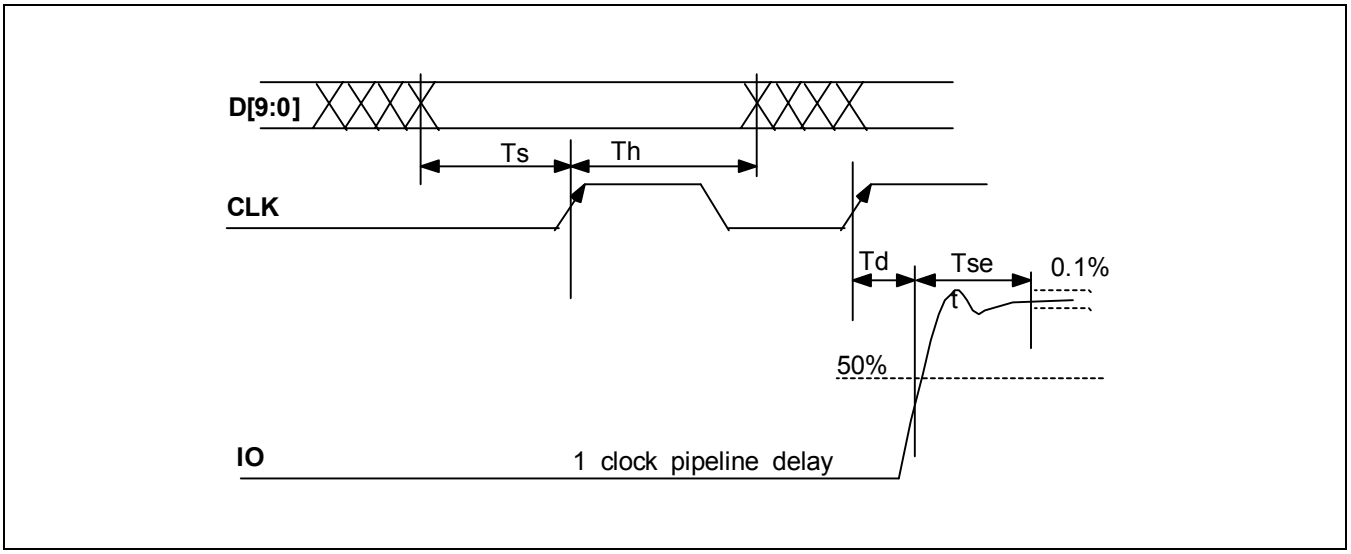
Gain Errors : The difference between the actual andideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range : The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Settling Time : The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition

Glitch Impulse : Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s

TIMING DIAGRAM



NOTES:

1. Output delay measured from the 50%point of the rising edge of CLK to the full scale transition
2. Settling time measured from the 50% point of full scale transition to the output remaining within ± 1 , ±2LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

PC BOARD LAYOUT CONSIDERATIONS

1. PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and de-coupled this trace length between groups of VDD (VDDA, VDDD) pins short as possible so as to minimize inductive ringing.

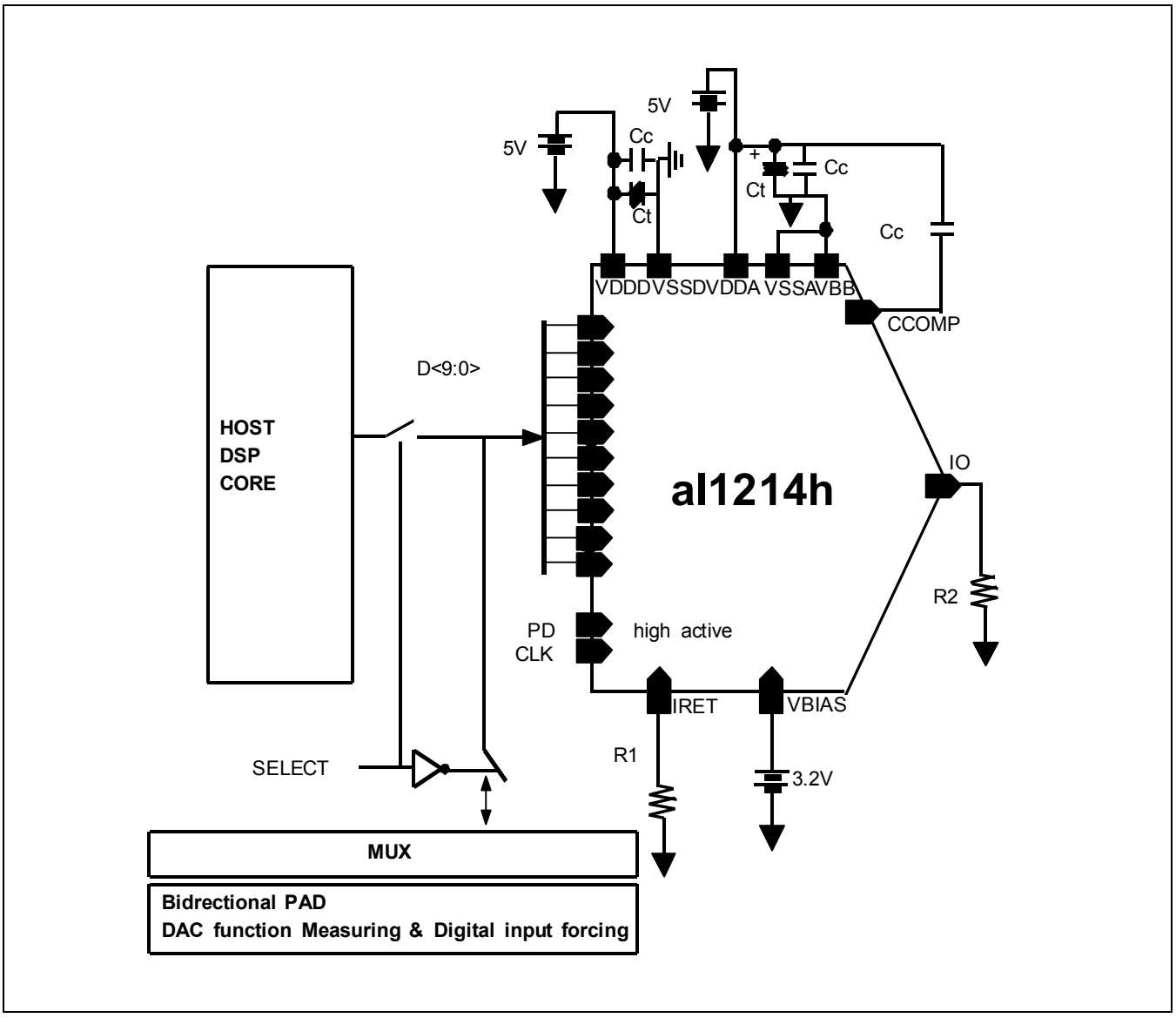
2. Supply Decoupling and Planes

For the de-coupling capacitor between the power line and the ground line, 0.1uF ceramic capacitor is used in parallel with a 10uF tantalum capacitor. The digital power plane (VDDD) and analog power plane (VDDA) are connected through a ferrite bead, and also the digital ground plane (VSSD) and the analog ground plane (VSSA). This ferrite bead should be located within 3inches of the AL1214H. The analog power plane supplies power to the AL1214H of the analog output pin and related devices.

3. Analog Signal Interconnection

To minimized noise pickup and reflections due to impedance mismatch, the AL1214H should be located as close as possible to the output connector.
The line between DAC output and monitor input should also be regarded as a transmission line. Due to the fact, it can cause problems in transmission line mismatch. As a solution to these problems, the double-termination methods used. By using this, both ends of the termination lines are matched, providing an ideal, non-reflective system.

CORE EVALUATION GUIDE



Location	Description (for HDD)	Description (for VIDEO)
Cc	0.1uF	0.1uF
Ct	10uF	10uF
R1	1kΩ	463 Ω
R2	160 Ω	37.5 Ω
V(IO)	2Vpp	1Vpp

Testability

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D<9:0>) See above figure. Only if it is, you can check the main function (Linearity), and output (IO), VBIAS, IREF, and CCOMP pins are reserved for external use.

Analysis

The voltage applied to VBIAS is measured at IREF node . And the voltage value is proportioned to the reference current value of resistor which is connected to IREF node. So you can estimate the full scale current value by measuring the voltage, and check the DC characteristics of the OPAMP. For reference, as VREF applied to VBIAS node is given at IREF node, the current flowing through RSET is given as VREF/RSET. The voltage is scaled factor of 1/116 for HDD and 1/456 for VIDEO. The full scale current is given as the decimal value equivocal to the digital code.

- **Resolution**

  If you want to change the resolution, use as many appear bits as you want and connect the rest lower bits to the ground as above diagram which is 8-bit application.

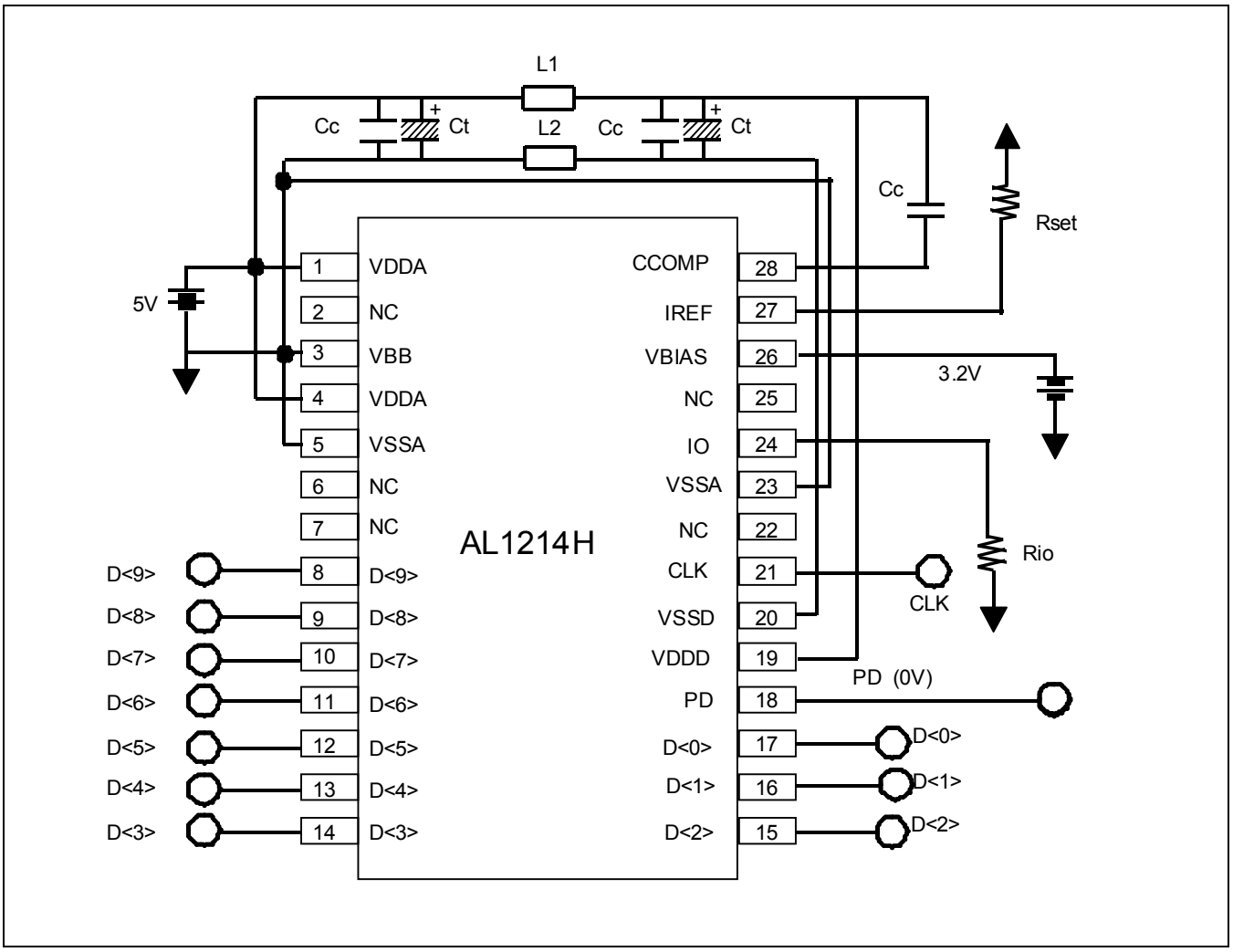
- **Output Range Alteration**

  In order to change the output swing, use following equation.

  Vout = { Vref/(RSET*116) }*DAC_CODE*Rio

  Output swing width is a function of Vi (VBIAS = 3.2V , Vref = 1.4V) , RSET (1kΩ or 463Ω), and Rio (160Ω or 37.5Ω) maximum output swing width is (2Vpp or 1Vpp)

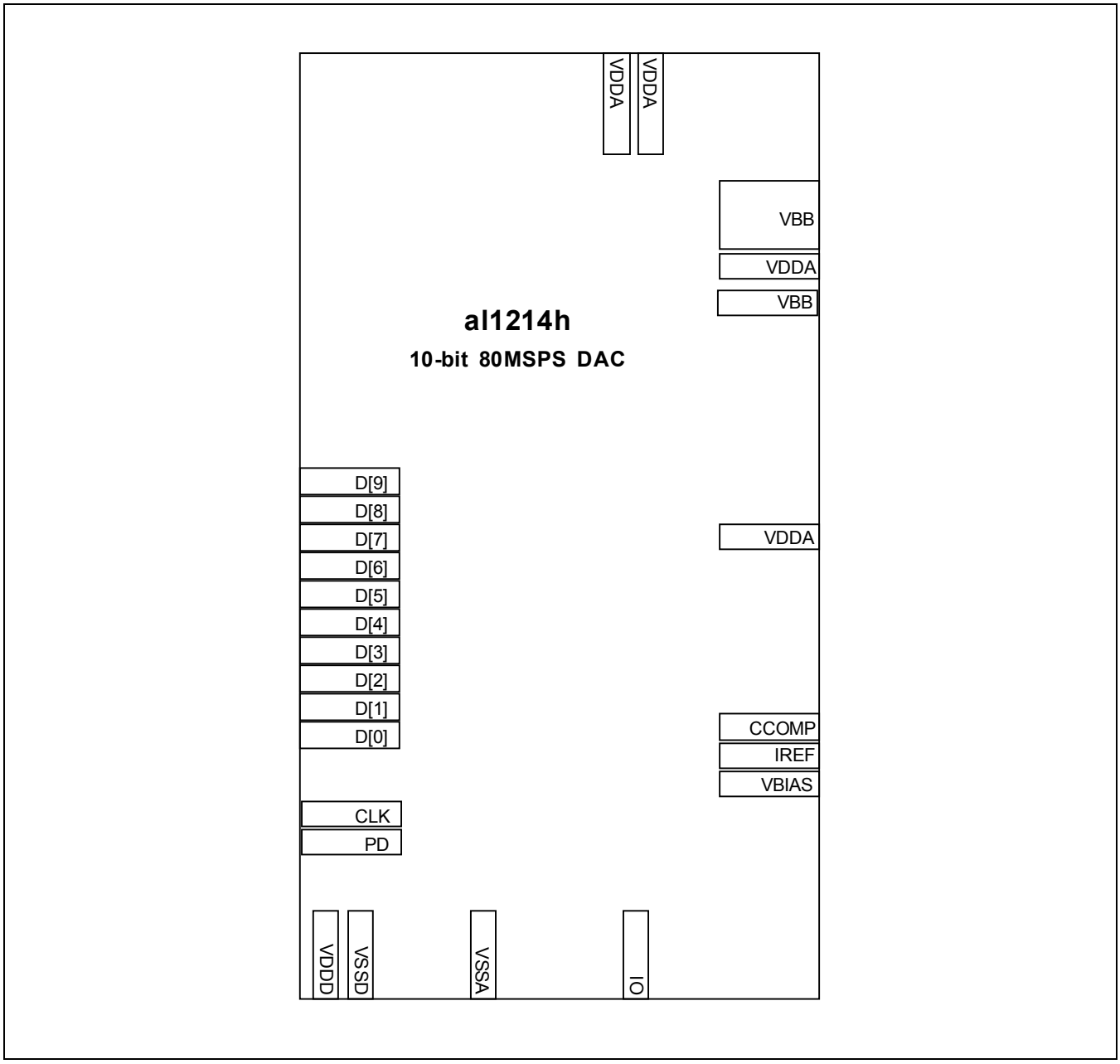
PACKAGE CONFIGURATION



Location	Description (for HDD)	Description (for VIDEO)
V(Rio)	2Vpp	1Vpp
Ct	10uF TANTALUM CAPACITOR	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR	0.1uF CERAMIC CAPACITOR
L1, L2	FERRITE BEAD (0.1mh)	FERRITE BEAD (0.1mH)
Rset	1kΩ	463Ω
Rio	160Ω	37.5Ω

PHANTOM CELL INFORMATION

— Pins of the core can be assigned externally (Package pins) or internally (internal ports) depending on design methods.
The term "External" implies that the pins should be assigned externally like power pins.
The term "External/internal" implies that the applications of these pins depend on the user.



Pin Name	Pin Usage	Pin Layout Guide
VDDA	External	- Maintain the large width of lines as far as the pads. - Place the port positions to minimize the length of power lines. - Do not merge the analog powers with another power from other blocks. - Use good power and ground source on board.
VSSA	External	
VBB	External	
VDDD	External	
VSSD	External	
CCOMP	External	- Do not overlap with digital lines. - Maintain the shortest path to pads.
IREF	External	- Separate from all other analog signals - Maintain the larger width and the shorter length as far as the pads. - Separate from all other digital lines.
VBIAS	External	
IO	External	
CLK	External/Internal	- Separated from the analog clean signals if possible. - Do not exceed the length by 1,000um.
PD	External/Internal	
D[9]	External/Internal	
D[8]	External/Internal	
D[7]	External/Internal	
D[6]	External/Internal	
D[5]	External/Internal	
D[4]	External/Internal	
D[3]	External/Internal	
D[2]	External/Internal	
D[1]	External/Internal	
D[0]	External/Internal	

FEEDBACK REQUEST

We appreciate your interest in products. If you have further questions, please specify in the attached form. Thank you very much.

DC / AC ELECTRICAL CHARACTERISTIC						
Characteristics		**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Supply Voltage					V	
Power dissipation					mW	
Resolution					Bits	
Analog Output Voltage					V	
Operating Temperature					°C	
Output Load Capacitor					pF	
Output Load Resistor					Ohm	
Integral Non-Linearity Error					LSB	
Differential Non-Linearity Error					LSB	
Maximum Conversion Rate					MHz	
VOLTAGE OUTPUT DAC						
Reference Voltage	TOP BOTTOM				V	
Analog Output Voltage Range					V	
Digital Input Format		Binary Code or 2's Complement Code				
CURRENT OUTPUT DAC						
Analog Output Maximum Current					mA	
Analog Output Maximum Signal Frequency					MHz	
Reference Voltage					V	
External Resistor for Current Setting(RSET)					Ohm	
Pipeline Delay					sec	

— Do you need 3.3V and 5V power supply in your system?

VERSION LIST

Version	Date	Modified Items	Comments
Ver 1..0	98.05.01	Original version published	
Ver 1.4	99.12.13	1. Test configuration correction 2. Font correction	
Ver 1.5	00.02.22	1.power port addition 2.I/O pad cell change	
Ver 1.6	02.04.20	1. Modify the phantom cell guide	