GENERAL DESCRIPTION

The AL1213H is a CMOS 9-Bit D/A converter for general application. This digital to analog converter consists of a R-2R ladder block & an Op amp block. Its maximum conversion rate is 0.5MSPS.

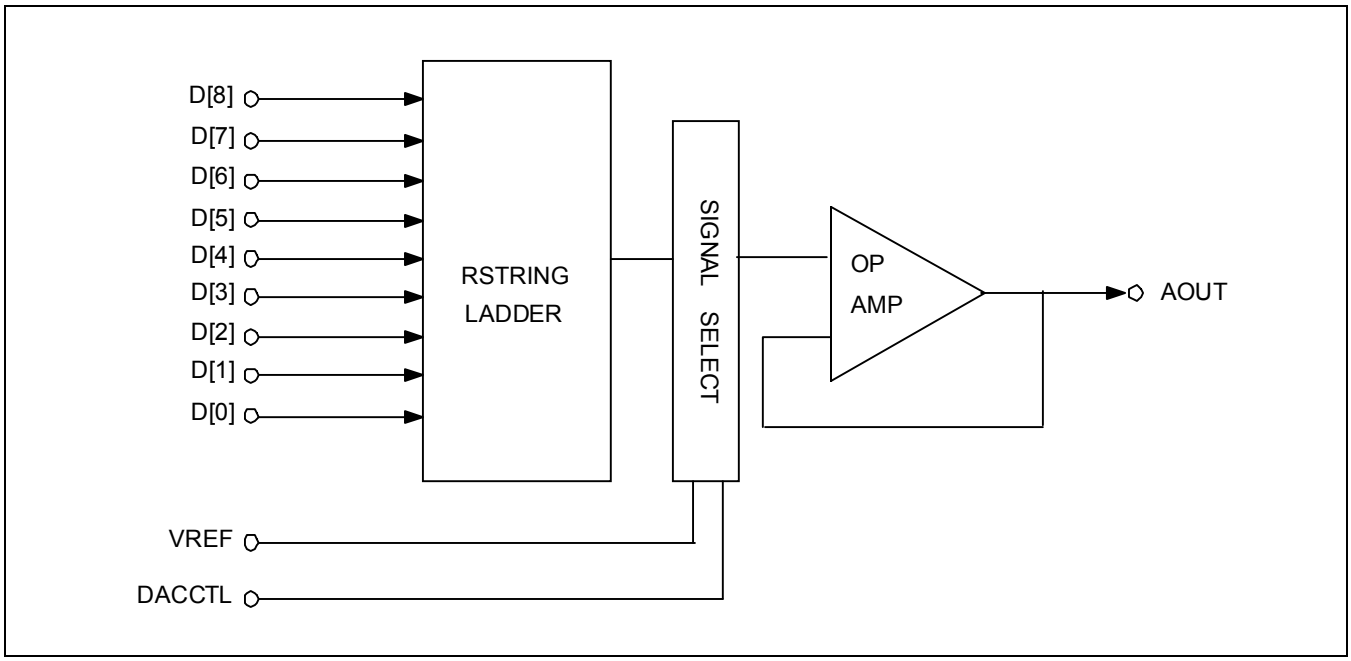
FEATURES

- Resolution : 9-Bit
- Differential Linearity Error : ± 0.16 LSB (TYP)
- Maximum Conversion Rate : 0.5MSPS
- Supply Voltage : 5V
- Single Voltage Output : 0V to 5V
- Operation Temperature Range : 0°C to 70°C

TYPICAL APPLICATIONS

- DVD
- CDP
- General purpose Digital to Analog Conversion

FUNCTIONAL BLOCK DIAGRAM



Rev 2.1 (Apr. 2002)

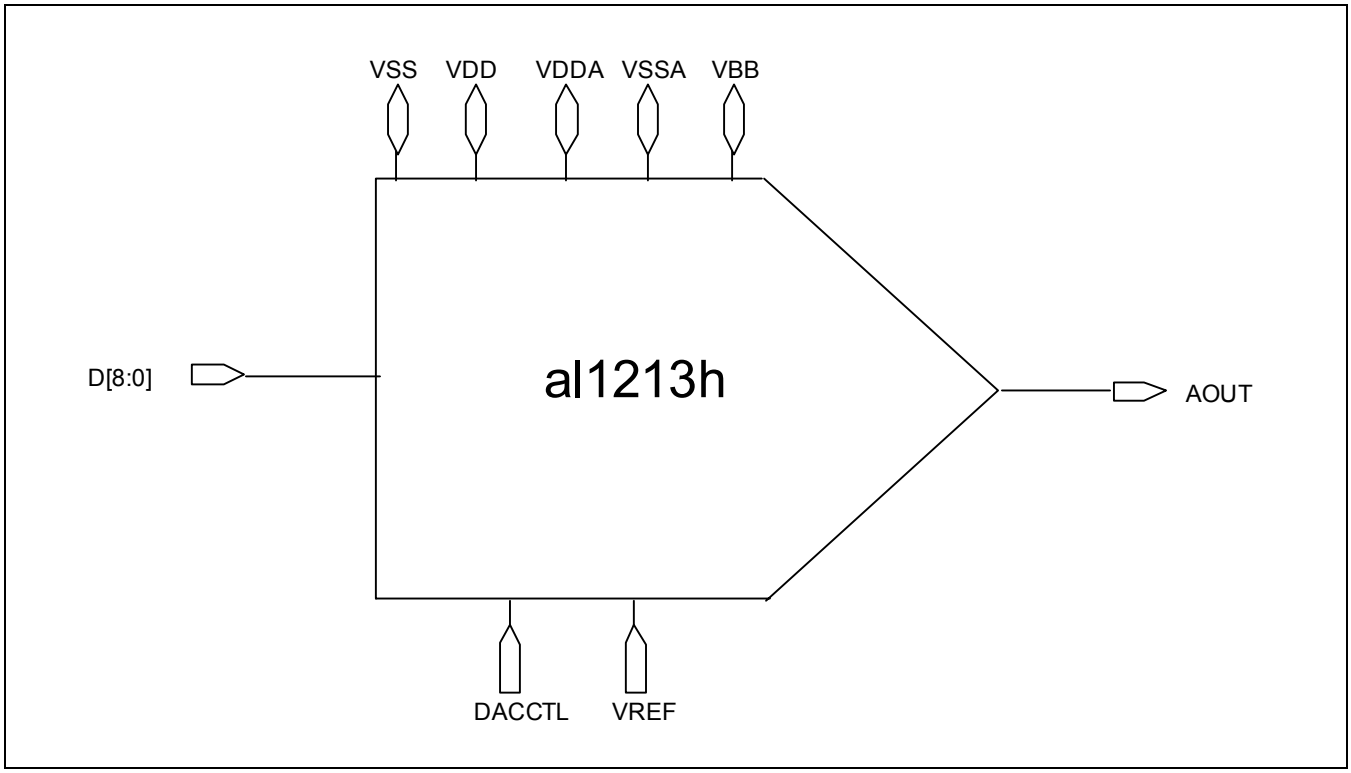
CORE PIN DESCRIPTION

Name	I/O Type	I/O Pad	Pin Description
VDDA	AP	vdda	Analog Power
VSSA	AG	vssa	Analog Ground
VDD	DP	vddd	Digital Power
VSS	DG	vssd	Digital Ground
D[0] ~ D[8]	DI	picc_bb	Digital Input Data
DACCTL	DI	picc_bb	Signal Select signal
VREF	AI	pia_bb	Voltage Reference Top (5V)
AOUT	AO	poa_bb	Analog Voltage Output
VBB	AG	vbb	Analog Ground

I/O TYPE ABBR

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AP : Analog Power
- AG : Analog Ground
- AB : Analog Bi-direction port
- DB : Digital Bi-direction port
- DP : Digital Power
- DG : Digital Ground
- DB : Digital Sub Bias

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Typ	Unit
Supply Voltage	VDD VDDA	5	V
Reference Input Voltage	VRT VRB	5.0 0.0	V V
Digital Input Voltage LOW	Vinh	5.0	V
HIGH	Vinl	0.0	V
Operating Temperature	Top	0 to 70	°C

NOTES :

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions not implied.
2. All voltages are measured with respect to VSSA,VDDD unless otherwise specified.

RECOMMENDED OPERATING CONDITIONS

Characteristics		Symbol	Min	Typ	Max	Unit
Supply Voltage		VDD VDDA	4.75	5.0	5.25	V
Reference Input Voltage		VRT VRB	- -	5.0 0.0	- -	V V
Digital Input Voltage	HIGH	Vinh	0.7 VDDD	-	-	V
	LOW	Vinl	-	-	0.3 VDDD	V
Operating Temperature		Top	0	-	70	°C

NOTE: It is strongly recommended that to avoid power latch-up all the supply pins (VDDA,VDDD) be driven from the same source.

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications : VDD = VDDA = 5V, VSS = VSSA = VBB = 0V, Top = 25°C, VREF = 2.5V, DACCTL = 0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
Resolution	-	-	9	-	Bits
Differential Linearity Error	DLE	-	0.16	± 1	LSB
Integral Linearity Error	ILE	-	1.1	± 1.5	LSB
Maximum Output Voltage	-	4.75	5	5.25	V
LSB Size	-	9.4	9.8	10.1	mV

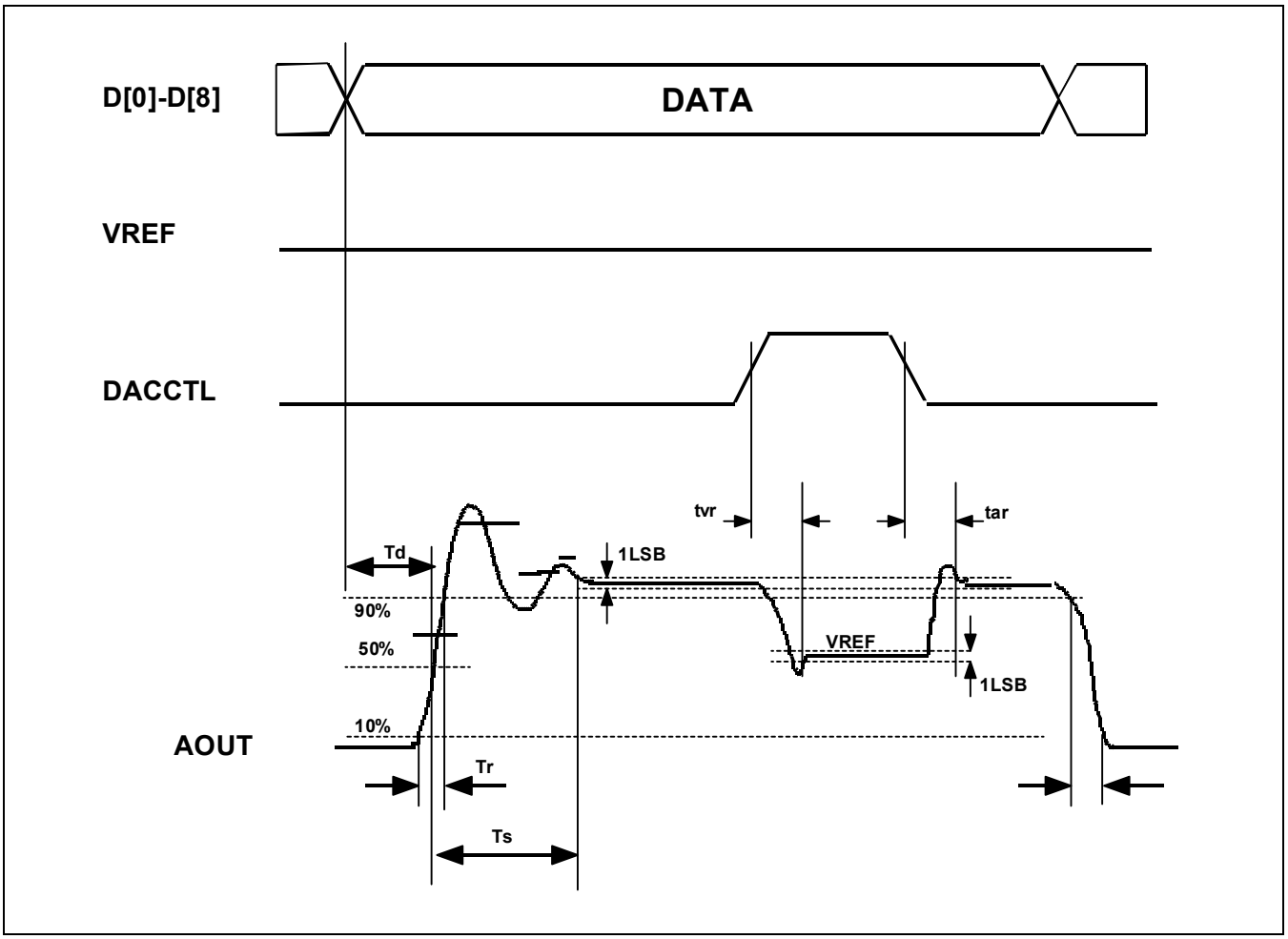
AC ELECTRICAL CHARACTERISTICS

(Converter Specifications : VDD = VDDA = 5V, VSS = VSSA = VBB = 0V, Top = 25°C, VREF = 2.5V, DACCTL = 0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Test Conditions
Conversion Rate	fc	-	-	0.5	MSPS	data = 0.5MHz
Dynamic Supply Current	Ivdd	2.0	3.0	7.0	mA	fc = 0.5MHz (load cap = 25pF)
Analog Output Delay	Td	-	190	300	ns	fc = 0.5MHz Data: All High
Analog Output Rise Time	Tr	-	230	320	ns	fc = 0.5MHz Data: All Low → All High
Analog Output Fall Time	Tf	-	230	320	ns	fc = 0.5MHz Data: All High → All Low
Center Code Rising Time	Trd	-	0.3	0.4	ms	fc = 0.5MHz Data: 111111111 → 000000000
Slew Rate	SR	-	10	12	V/ms	fc = 0.5MHz Data: All High → All Low
*Reference Voltage Output Response Time	tvr	-	350	-	ns	VREF(arbitrary) DACCTL = High
*Analog Output Recovery Time	tar	-	350	-	ns	DACCTL = Low Data(arbitrary)

*** NOTE:** These above items are verified in simulation

TIMING DIAGRAM

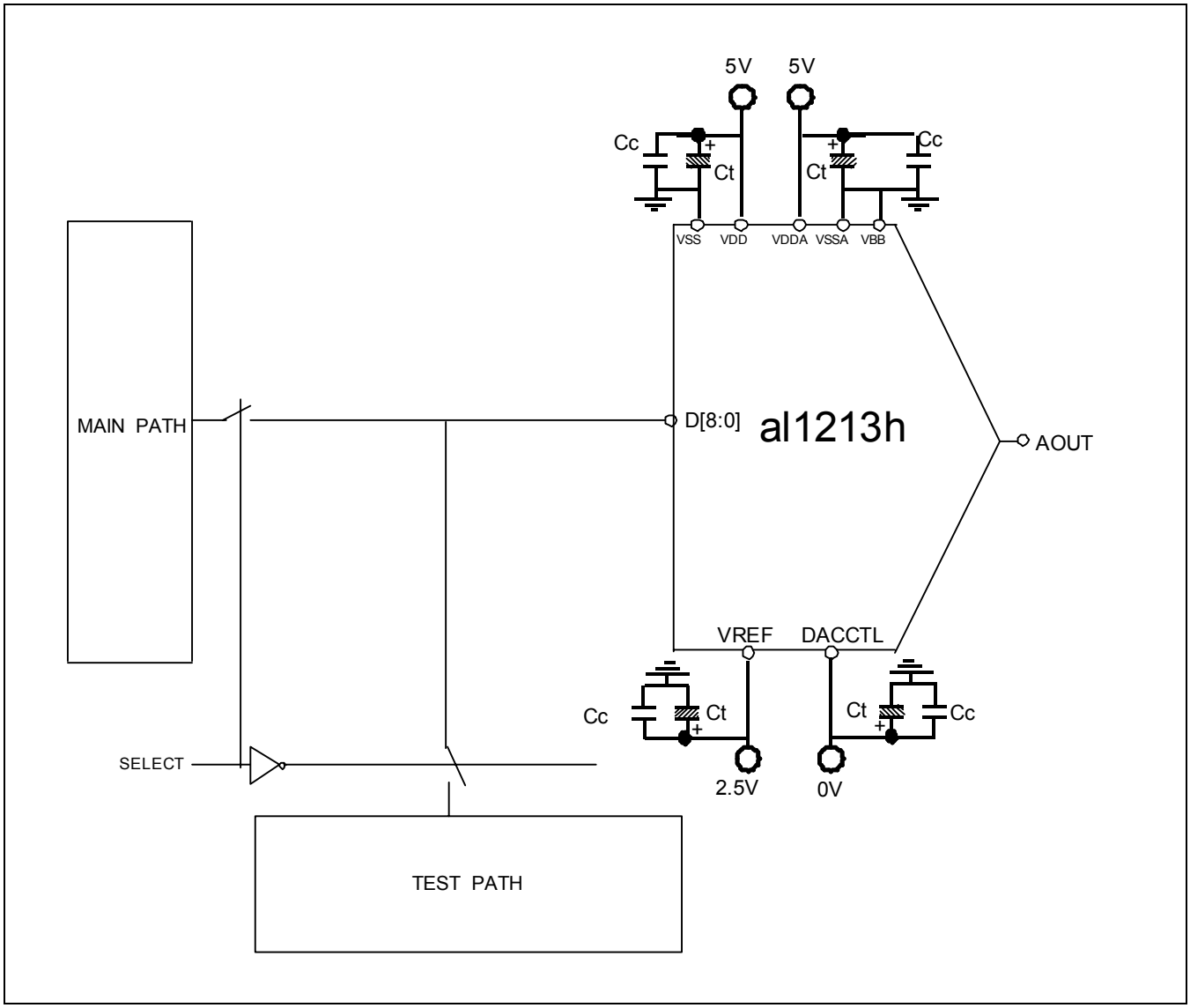


1. Output delay measured from the 50% point of the rising edge of input data to the full scale transition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/2 LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

FUNCTION DESCRIPTION

1. The AL1213H has a 1-of-512 decoder, a R-String Block for 9-bit and an Opamp Block for driving Output.
2. The decoder has 512 digital outputs and only one of them is valid.
   The R-string block consists of R-array with 512 resistors and 512 CMOS switches and decides to output voltage according to 512 digital inputs generated by 1-of-512 decoder.
3. $$VRstring = \frac{VRT - VRB}{2^9} \sum_{n=0}^{8} (2^n * Dn)$$
4. Output of the R-string Block is driven by OP-amp.

CORE EVALUATION GUIDE

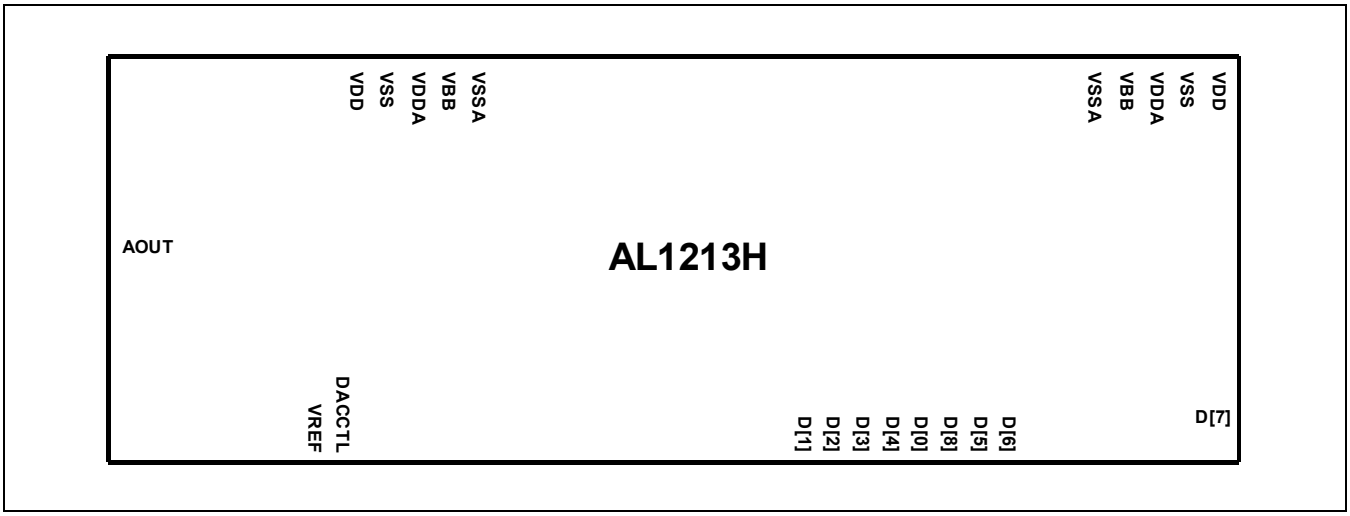


Location	Description
Ct	10µF TANTALUM CAPACITOR
Cc	0.1µF CERAMIC CAPACITOR

TESTABILITY

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D[0] ~ D[8]). See above figure. Only if it is, you can check the main function (Linearity)

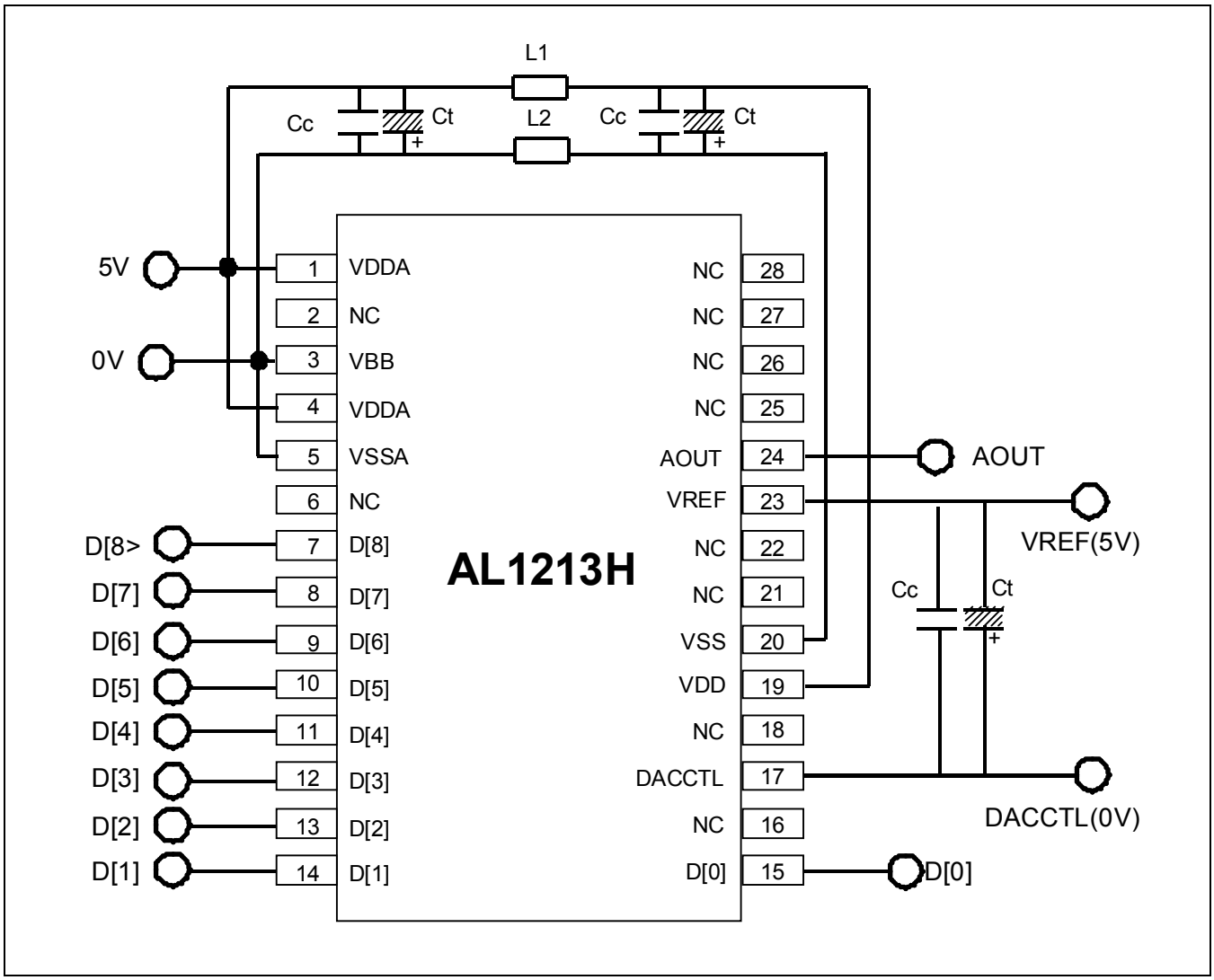
PHANTOM CELL INFORMATION



Pin Name	Property	Pin Usage	Pin Layout Guide
D[8:0]	DI	Internal/External	1. Digital Input Signal lines must have same length to reduce propagation delay.
DACCTL	DI	Internal/External	
VREF	AB	Internal/External	1. Voltage reference lines (VRT/VRB) must be wide metal to reduce voltage drop of metal lines. 2. VOUT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.
AOUT	AO	Internal/External	
VDDA	AP	External	1. It is recommended that you use thick analog power metal. When connected to PAD, the path should be kept as short as possible. 2. Digital power and analog power are separately used.
VSSA	AG	External	
VDD	DP	External	
VSS	DG	External	
VBB	AG	External	

1. When the core block is connected to other blocks, it must be double guard-ring using N-well and P+ active to remove the substrate and coupling noise.
   In that case, the power metal should be connected to PAD directly.
2. The Bulk power is used to reduce the influence of substrate noise.

PACKAGE CONFIGURATION



Location	Description
Ct	10μF TANTALUM CAPACITOR
Cc	0.1μF CERAMIC CAPACITOR
L1, L2	FERRITE BEAD (0.1mh)

PACKAGE PIN DESCRIPTION

Name	Pin No	I/O Type	Pin Description
VDDA	1,4	AP	Analog Power
VBB	3	AG	Analog Ground
VSSA	5	AG	Analog Ground
D[0] ~ D[8]	7~15	DI	Digital Input Data
DACCTL	17	DI	Digital Input Data
VDD	19	DP	Digital Power
VSS	20	DG	Digital Ground
VREF	23	AI	Voltage Reference Voltage (2.5V)
AOUT	24	AO	Analog Voltage Output
NC	2,6,7,16,18,21 22,25,26,27,28	DO	No Connection

PC BOARD LAYOUT CONSIDERATIONS

PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of VDD (VDDA, VDD) and VSS (VSSA, VSS) pins should be as short as possible so as to minimize inductive ringing.

Supply Decoupling and Planes

For the decoupling capacitor between the power line and the ground line, 0.1μF ceramic capacitor is used in parallel with a 10μF tantalum capacitor. The digital power plane (VDD) and analog power plane (VDDA) are connected through a ferrite bead, and also the digital ground plane (VSS) and the analog ground plane (VSSA). This ferrite bead should be located within 3inches of the AL1213H. The analog power plane supplies power to the AL1213H of the analog output pin and related devices.

FEEDBACK REQUEST

We appreciate your interest in out products. If you have further questions, please specify in the attached form. Thank you very much.

DC / AC ELECTRICAL CHARACTERISTIC					
Characteristics	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				mF	
Output Load Resistor				Ω	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	
VOLTAGE OUTPUT DAC					
Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				
CURRENT OUTPUT DAC					
Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				MHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				Ω	
Pipeline Delay				sec	

— Do you want to Power down mode?

— Do you want to Internal Reference Voltage (BGR)?

— Which do you want to Serial Input TYPE or parallel Input TYPE?

— Do you need 3.3V and 5V power supply in your system?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.0	Jun.'98	Original version published	
Ver 2.0	Feb.'00	Core layout Guide update	
Ver 2.1	Apr.'02	Phantom Cell information update	