

**Typical Applications**

- Narrow and Broadband Commercial and Military Radio Designs
- Linear and Saturated Amplifiers
- Gain Stage or Driver Amplifiers for MWRadio/Optical Designs

**Product Description**

The NDA-210-D InGaP/GaAs HBT MMIC distributed amplifier is a low-cost, high-performance solution for high frequency RF, microwave, or optical amplification needs. This 50Ω matched distributed amplifier is based on a reliable HBT proprietary MMIC design, providing unsurpassed performance for small-signal applications. Designed with an external bias resistor, the NDA-210-D provides flexibility and stability. In addition, the NDA-210-D chip was designed with an additional ground via to enable low junction temperature operation. NDA-series distributed amplifiers provide design flexibility by incorporating AGC functionality into their designs.

UNITS: INCHES  
[mm]



**Optimum Technology Matching® Applied**

- |   |                                   |                                       |
|---|-----------------------------------|---------------------------------------|
| <input type="checkbox"/> Si BJT               | <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> GaAs MESFET  |
| <input type="checkbox"/> Si Bi-CMOS           | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si CMOS      |
| <input checked="" type="checkbox"/> InGaP/HBT | <input type="checkbox"/> GaN HEMT | <input type="checkbox"/> SiGe Bi-CMOS |

**Package Style: Die**

**Features**

- Reliable, Low-Cost HBT Design
- 5.0dB Gain, +12.6dBm P1dB @ 2.0GHz
- High P1dB of +13.4dBm @ 6.0GHz and +9.0dBm @ 14.0GHz
- Fixed Gain or AGC Operation
- 50Ω I/O Matched for High Freq. Use

**Ordering Information**

NDA-210-D      InGaP/GaAs HBT MMIC Distributed Amplifier DC to 17GHz - Die Only (100 pieces minimum order)

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**Functional Block Diagram**

# NDA-210-D

## Absolute Maximum Ratings

Parameter	Rating	Unit
RF Input Power	+15	dBm
Power Dissipation	300	mW
Device Current, I <sub>CC1</sub>	42	mA
Device Current, I <sub>CC2</sub>	42	mA
Output Device Voltage, V <sub>C2</sub>	3.5	V
Junction Temperature, T <sub>j</sub>	200	°C
Operating Temperature	-45 to +85	°C
Storage Temperature	-65 to +150	°C

Exceeding any one or a combination of these limits may cause permanent damage.



**Caution!** ESD sensitive device.

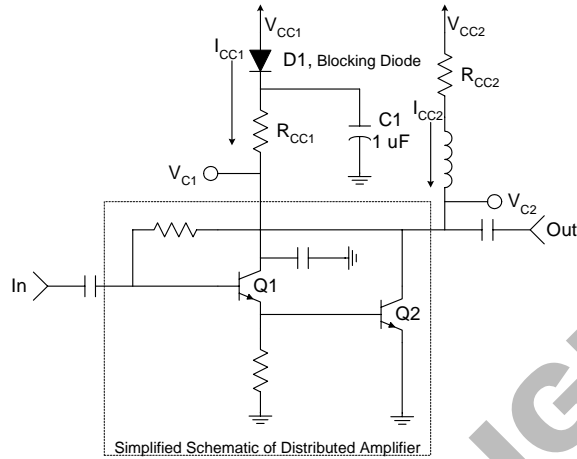
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					V <sub>CC1</sub> =+10V, V <sub>CC2</sub> =+10V, V <sub>C1</sub> =+4.71V, V <sub>C2</sub> =+2.98V, I <sub>CC1</sub> =29mA, I <sub>CC2</sub> =36mA, Z <sub>0</sub> =50Ω, T <sub>A</sub> =+25°C
Small Signal Power Gain, S <sub>21</sub>	5.0	6.0		dB	f=0.1GHz to 4.0GHz
		7.0		dB	f=4.0GHz to 6.0GHz
	7.5	9.0		dB	f=6.0GHz to 10.0GHz
	4.0	6.0		dB	f=10.0GHz to 17.0GHz
Input and Output VSWR		2.3:1			f=0.1GHz to 4.0GHz
		2.0:1			f=4.0GHz to 10.0GHz
		3.0:1			f=10.0GHz to 17.0GHz
Bandwidth, BW		17.5		GHz	BW3 (3dB)
Output Power @ 1dB Compression		12.6		dBm	f=2.0GHz
		13.4		dBm	f=6.0GHz
		9.0		dBm	f=14.0GHz
Noise Figure, NF		6.5		dB	f=2.0GHz
Third Order Intercept, IP3		+23.0		dBm	f=2.0GHz
Reverse Isolation, S <sub>12</sub>		-13		dB	f=0.1GHz to 17.0GHz
Output Device Voltage, V <sub>C2</sub>	2.70	2.98	3.20	V	
AGC Control Voltage, V <sub>C1</sub>		4.7		V	
Gain Temperature Coefficient, δG <sub>T</sub> /δT		-0.0015		dB/°C	
<b>MTTF versus Junction Temperature</b>					
Case Temperature		85		°C	
Junction Temperature		144		°C	
MTTF		>1,000,000		hours	
<b>Thermal Resistance</b>					
θ <sub>JC</sub>		242		°C/W	$\frac{J_T - T_{CASE}}{V_D \cdot I_{CC}} = \theta_{JC} (\text{°C/Watt})$

Suggested Voltage Supply: V<sub>CC1</sub>≥4.7V, V<sub>CC2</sub>≥5.0V

### Typical Bias Configuration

Application notes related to biasing circuit, device footprint, and thermal considerations are available on request.



Bias Resistor Selection	
$R_{CC1}$ :	For $4.7V < V_{CC1} < 5.0V$
	$R_{CC1} = 0\Omega$
	For $5.0V < V_{CC1} < 10.0V$
	$R_{CC1} = V_{CC1} - 4.7 / 0.029\Omega$
$R_{CC2}$ :	For $5.0V < V_{CC2} < 10.0V$
	$R_{CC2} = V_{CC2} - 2.98 / 0.036\Omega$

Typical Bias Parameters for $V_{CC1} = V_{CC2} = 10V$ :							
$V_{CC1}$ (V)	$V_{CC2}$ (V)	$I_{CC1}$ (mA)	$V_{C1}$ (V)	$R_{CC1}$ ( $\Omega$ )	$I_{CC2}$ (mA)	$V_{C2}$ (V)	$R_{CC2}$ ( $\Omega$ )
10	10	29	4.7	180	36	2.98	195

## Chip Outline Drawing - NDA-210-D

Chip Dimensions: 0.027" x 0.022" x 0.004"

UNITS: INCHES  
[mm]



## Sales Criteria - Unpackaged Die

### Die Sales Information

- All segmented die are sold 100% DC-tested. Testing parameters for wafer-level sales of die material shall be negotiated on a case-by-case basis.
- Segmented die are selected for customer shipment in accordance with RFMD Document #6000152 - Die Product Final Visual Inspection Criteria<sup>1</sup>.
- Segmented die has a minimum sales volume of 100 pieces per order. A maximum of 400 die per carrier is allowable.

### Die Packaging

- All die are packaged in GelPak ESD protective containers with the following specification: O.D.=2" X2", Capacity=400 Die (20X20 segments), Retention Level=High(X8).
- GelPak ESD protective containers are placed in a static shield bag. RFMD recommends that once the bag is opened the GelPak/s should be stored in a controlled nitrogen environment. Do not press on the cover of a closed GelPak, handle by the edges only. Do not vacuum seal bags containing GelPak containers.
- Precaution must be taken to minimize vibration of packaging during handling, as die can shift during transit<sup>2</sup>.

### Package Storage

- Unit packages should be kept in a dry nitrogen environment for optimal assembly, performance, and reliability.
- Precaution must be taken to minimize vibration of packaging during handling, as die can shift during transit<sup>2</sup>.

### Die Handling

- Proper ESD precautions must be taken when handling die material.
- Die should be handled using vacuum pick-up equipment, or handled along the long side with a sharp pair of tweezers. Do not touch die with any part of the body.
- When using automated pick-up and placement equipment, ensure that force impact is set correctly. Excessive force may damage GaAs devices.

**Die Attach**

- The die attach process mechanically attaches the die to the circuit substrate. In addition, the utilization of proper die attach processes electrically connect the ground to the trace on which the chip is mounted. It also establishes the thermal path by which heat can leave the chip.
- Die should be mounted to a clean, flat surface. Epoxy or eutectic die attach are both acceptable attachment methods. Top and bottom metallization are gold. Conductive silver-filled epoxies are recommended. This procedure involves the use of epoxy to form a joint between the backside gold of the chip and the metallized area of the substrate.
- All connections should be made on the topside of the die. It is essential to performance that the backside be well grounded and that the length of topside interconnects be minimized.
- Some die utilize vias for effective grounding. Care must be exercised when mounting die to preclude excess run-out on the topside.

**Die Wire Bonding**

- Electrical connections to the chip are made through wire bonds. Either wedge or ball bonding methods are acceptable practices for wire bonding.
- All bond wires should be made as short as possible.

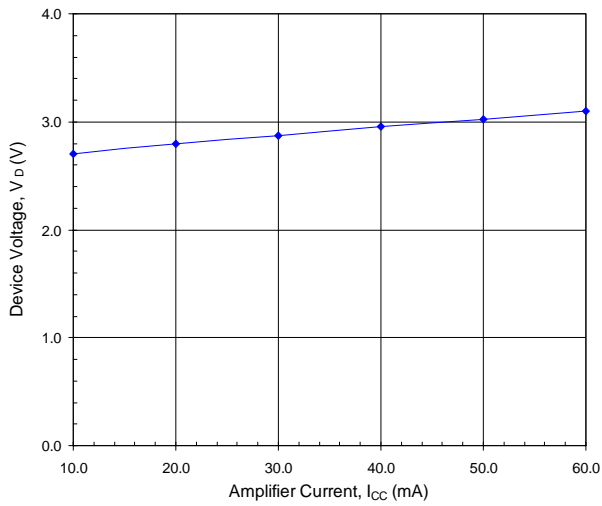
**Notes**

<sup>1</sup>RFMD Document #6000152 - Die Product Final Visual Inspection Criteria. This document provides guidance for die inspection personnel to determine final visual acceptance of die product prior to shipping to customers.

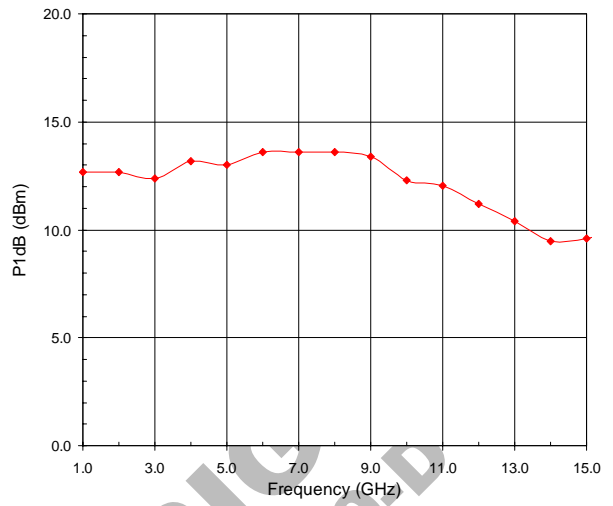
<sup>2</sup>RFMD takes precautions to ensure that die product is shipped in accordance with quality standards established to minimize material shift. However, due to the physical size of die-level product, RFMD does not guarantee that material will not shift during transit, especially under extreme handling circumstances. Product replacement due to material shift will be at the discretion of RFMD.

# NDA-210-D

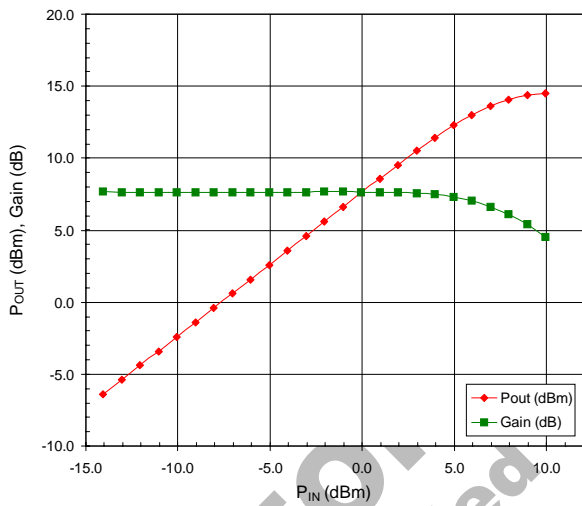
Device Voltage versus Amplifier Current



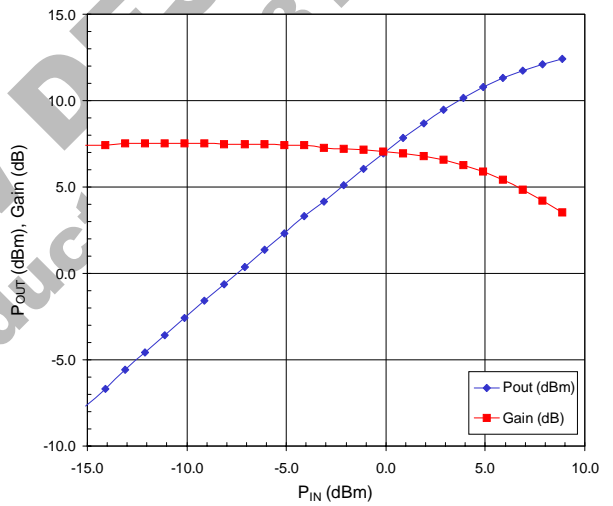
P1dB versus Frequency at 25°C



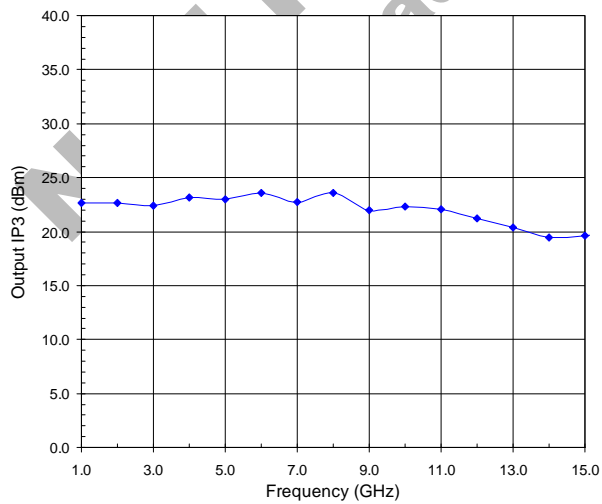
$P_{OUT}/Gain$  versus  $P_{IN}$  at 6 GHz



$P_{OUT}/Gain$  versus  $P_{IN}$  at 14 GHz



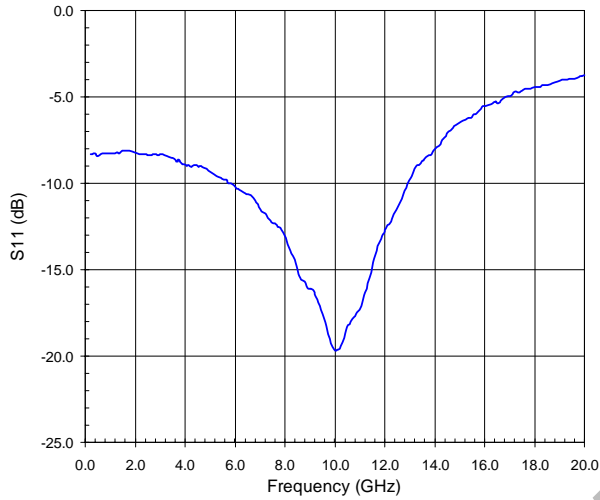
Third Order Intercept versus Frequency at 25°C



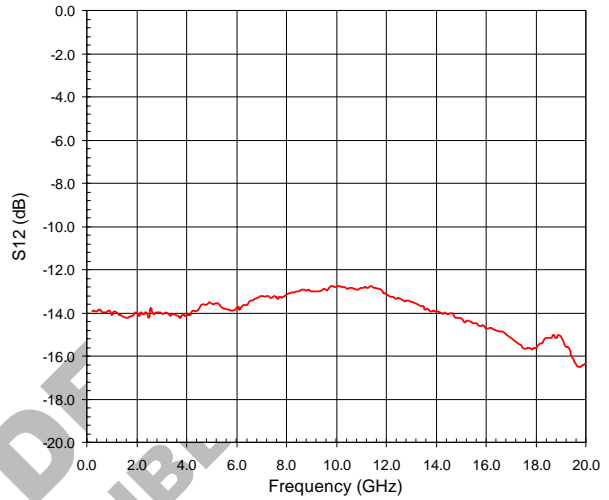
Note: The s-parameter gain results shown below include device performance as well as evaluation board and connector loss variations. The insertion losses of the evaluation board and connectors are as follows:

- 1 GHz to 4GHz=-0.06dB
- 5GHz to 9GHz=-0.22dB
- 10GHz to 14GHz=-0.50dB
- 15GHz to 20GHz=-1.08dB

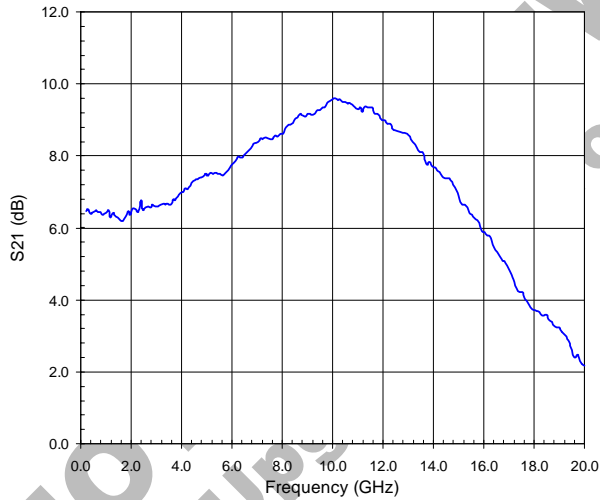
**S11 versus Frequency**



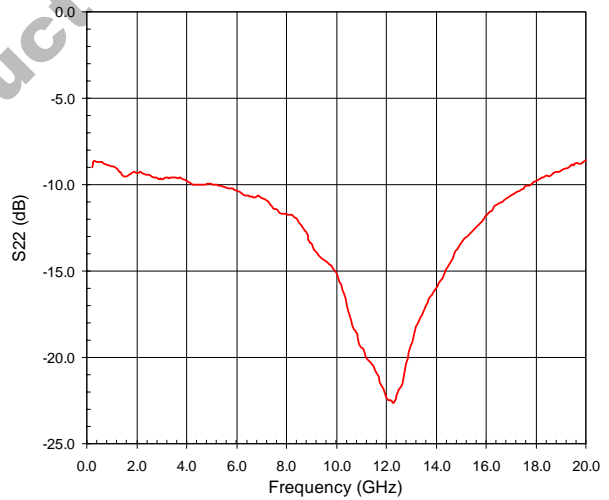
**S12 versus Frequency**



**S21 versus Frequency**



**S22 versus Frequency**



**NOT FOR NEW DESIGNS**  
**See Upgraded Product NBB-310-D**