

Eclipse-II Family Data Sheet



●●●●● Ultra-Low Power FPGA Combining Performance, Density, and Embedded RAM

Device Highlights

Flexible Programmable Logic

- 0.18 μ , six layer metal CMOS process
- 1.8 V VCC, 1.8/2.5/3.3 V drive capable I/O
- Up to 4,008 dedicated flip-flops
- Up to 55.2 K embedded SRAM bits
- Up to 310 I/O
- Up to 335 user available pins
- Up to 370 K system gates
- IEEE 1149.1 boundary scan testing compliant
- Low power capability

Embedded Dual Port SRAM

- Up to twenty-four 2,304 bit dual port high performance SRAM blocks
- RAM/ROM/FIFO wizard for automatic configuration
- Configurable and cascadable aspect ratio

Programmable I/O

- High performance I/O cell with Tco of 3 ns
- Programmable slew rate control
- Programmable I/O standards:
 - LVTTTL, LVCMOS, LVCMOS18, PCI, GTL+, SSTL2, and SSTL3
 - Independent I/O banks capable of supporting multiple standards in one device
 - I/O register configurations: Input, Output, Output Enable (OE)

Advanced Clock Network

- Multiple dedicated low skew clock networks
- High drive input-only networks
- Quadrant-based segmentable clock networks
- User programmable Phase Locked Loops (PLL)

Embedded Computational Units (ECUs)

Hardwired DSP building blocks with integrated Multiply, Add, and Accumulate functions.

Security Features

The QuickLogic products come with secure ViaLink® technology that protects intellectual property from design theft and reverse engineering. No external configuration memory needed; instant-on at power-up.

Figure 1: Eclipse-II Block Diagram

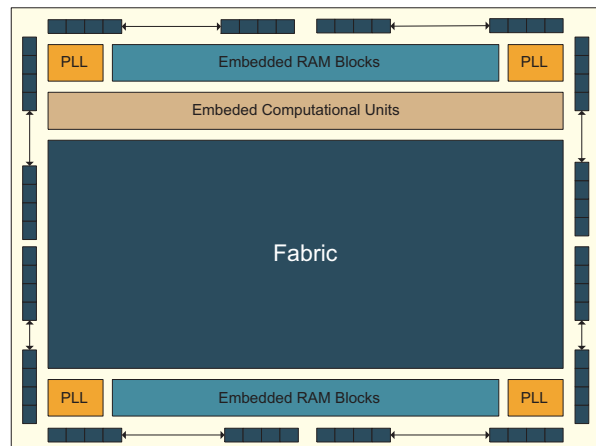


Table 1: Eclipse-II Product Family Members

		QL8025	QL8050	QL8150	QL8250	QL8325
Max Gates		47,052	63,840	188,946	248,160	320,640
Logic Array		16 x 8	16 x 16	32 x 20	40 x 24	48 x 32
Logic Cells		128	256	640	960	1,536
Max Flip-Flops		526	884	1,697	2,670	4,002
Max I/O		90	92	143	250	310
RAM Modules		4	4	16	20	24
RAM Bits		9,216	9,216	36,864	46,100	55,300
PLLs		-	-	-	4	4
ECUs		-	-	-	10	12
Packages	VQFP	100	100	-	-	-
	TFBGA (0.8 mm)	196	196	196	-	-
	PQFP	-	-	208	208	208
	LFBGA (0.8 mm)	-	-	-	280	280
	BGA (1.0 mm)	-	-	-	484	484

Table 2: Max I/O per Device/Package Combination

Device	100 VQFP	196 TFBGA	208 PQFP	280 LFBGA	484 PBGA
QL8025	62	90	-	-	-
QL8050	62	92	-	-	-
QL8150	-	100	143	-	-
QL8250	-	-	115	163	250
QL8325	-	-	115	163	310

QuickWorks Design Software

The QuickWorks® package provides the most complete ESP and FPGA software solution from design entry to logic synthesis, to place and route, and simulation. The package provides a solution for designers who use third-party tools from Cadence, Mentor, OrCAD, Synopsys, Viewlogic, and other third-party tools for design entry, synthesis, or simulation.

Process Data

Eclipse-II is fabricated on a 0.18 μ m, six layer metal CMOS process. The core voltage is 1.8 V and the I/Os are up to 3.3 V drive/tolerant. The Eclipse-II product line is available in commercial, industrial, and military temperature grades.

Programmable Logic Architectural Overview

The Eclipse-II logic cell structure is presented in **Figure 2**. This architectural feature addresses today's register-intensive designs.

Table 3: Performance Standards

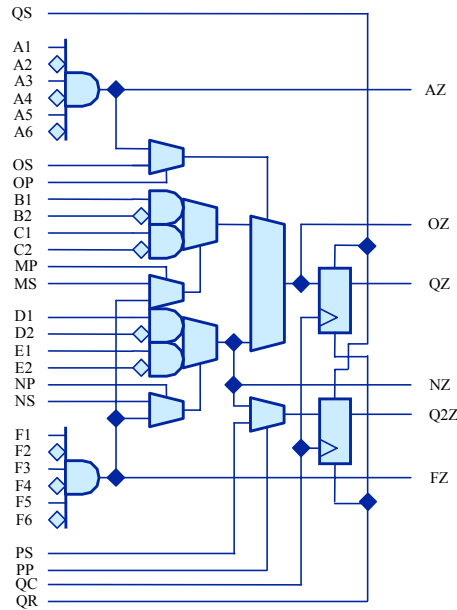
Function	Description	Slowest Speed Grade	Fastest Speed Grade
Multiplexer	16:1	2.8 ns	2.4 ns
Parity Tree	24	3.4 ns	2.9 ns
	36	4.6 ns	3.9 ns
Counter	16 bit	275 MHz	328 MHz
	32 bit	250 MHz	300 MHz
FIFO	128 x 32	197 MHz	235 MHz
	128 x 64	188 MHz	266 MHz
	256 x 16	208 MHz	248 MHz
Clock-to-Out		4 ns	3.3 ns
System clock		200 MHz	300 MHz

The Eclipse-II logic cell structure presented in **Figure 2** is a dual register, multiplexor-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. Both registers share CLK, SET, and RESET inputs. The second register has a two-to-one multiplexer controlling its input. The register can be loaded from the NZ output or directly from a dedicated input.

NOTE: The input PP is not an "input" in the classical sense. It is a static input to the logic cell and selects which path (NZ or PS) is used as an input to the Q2Z register. All other inputs are dynamic and can be connected to multiple routing channels.

The complete logic cell consists of two six-input AND gates, four two-input AND gates, seven two-to-one multiplexers, and two D flip-flops with asynchronous SET and RESET controls. The cell has a fan-in of 30 (including register control lines), fits a wide range of functions with up to 17 simultaneous inputs, and has six outputs (four combinatorial and two registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay while other architectures require two or more levels of delay.

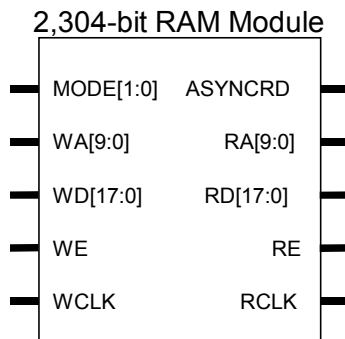
Figure 2: Eclipse-II Logic Cell



RAM Modules

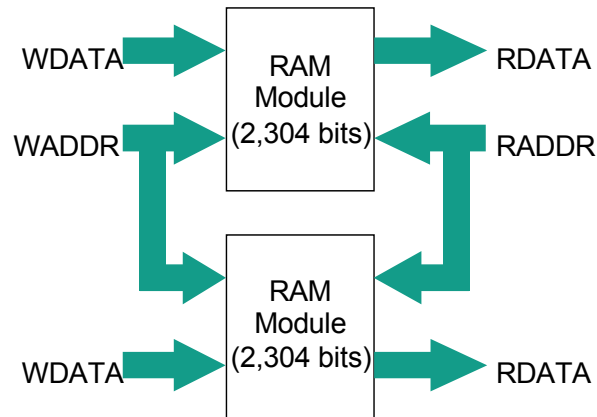
The Eclipse-II Product Family includes up to 24 dual-port 2,304-bit RAM modules for implementing RAM, ROM, and FIFO functions. Each module is user-configurable into four different block organizations and can be cascaded horizontally to increase their effective width, or vertically to increase their effective depth as shown in **Figure 4**.

Figure 3: 2,304-bit RAM Module



The number of RAM modules varies from 4 to 24 blocks for a total of 9.2 K to 55.3 K bits of RAM. Using two "mode" pins, designers can configure each module into 128 x 18 (Mode 0), 256 x 9 (Mode 1), 512 x 4 (Mode 2), or 1024 x 2 blocks (Mode 3). The blocks are also easily cascadable to increase their effective width and/or depth (see **Figure 4**).

Figure 4: Cascaded RAM Modules



The RAM modules are dual-port, with completely independent READ and WRITE ports and separate READ and WRITE clocks. The READ ports support asynchronous and synchronous operation, while the WRITE ports support synchronous operation. Each port has 18 data lines and 10 address lines, allowing word lengths of up to 18 bits and address spaces of up to 1,024 words. Depending on the mode selected, however, some higher order data or address lines may not be used.

The Write Enable (WE) line acts as a clock enable for synchronous write operation. The Read Enable (RE) acts as a clock enable for synchronous READ operation (ASYNCRD input low), or as a flow-through enable for asynchronous READ operation (ASYNCRD input high).

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules.

A similar technique can be used to create depths greater than 512 words. In this case address signals higher than the ninth bit are encoded onto the write enable (WE) input for WRITE operations. The READ data outputs are multiplexed together using encoded higher READ address bits for the multiplexer SELECT signals.

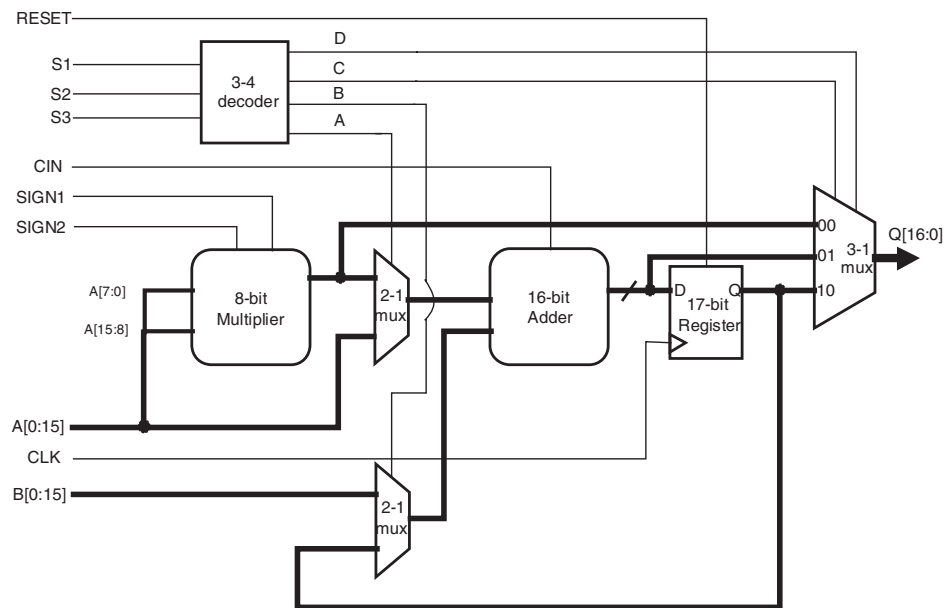
The RAM blocks can be loaded with data generated internally (typically for RAM or FIFO functions) or with data from an external PROM (typically for ROM functions).

Embedded Computational Unit (ECU)

Traditional Programmable Logic architectures do not implement arithmetic functions efficiently or effectively—these functions require high logic cell usage while garnering only moderate performance results.

The Eclipse-II architecture allows for functionality above and beyond that achievable using programmable logic devices. By embedding a dynamically reconfigurable computational unit, the Eclipse-II device can address various arithmetic functions efficiently. This approach offers greater performance than traditional programmable logic implementations. The embedded block is implemented at the transistor level as shown in **Figure 5**.

Figure 5: ECU Block Diagram



The Eclipse-II ECU blocks (Table 4) are placed next to the SRAM circuitry for efficient memory/instruction fetch and addressing for DSP algorithmic implementations.

Table 4: Eclipse-II ECU Blocks

Device	ECUs
QL8325	12
QL8250	10
QL8150	0
QL8050	0
QL8025	0

Up to twelve 8-bit MAC functions can be implemented per cycle for a total of 1 billion MACs/s when clocked at 100 MHz. Additional multiply-accumulate functions can be implemented in the programmable logic.

The modes for the ECU block are dynamically re-programmable through the programmable logic.

Table 5: ECU Mode Select Criteria

Instruction			Operation	ECU Performance ^a , -8 WCC		
S1	S2	S3		t _{PD}	t _{SU}	t _{CO}
0	0	0	Multiply	6.6 ns max		
0	0	1	Multiply-Add	8.8 ns max		
0	1	0	Accumulate ^b		3.9 ns min	1.2 ns max
0	1	1	Add	3.1 ns max		
1	0	0	Multiply (registered) ^c		9.6 ns min	1.2 ns max
1	0	1	Multiply- Add (registered)		9.6 ns min	1.2 ns max
1	1	0	Multiply - Accumulate		9.6 ns min	1.2 ns max
1	1	1	Add (registered)		3.9 ns min	1.2 ns max

a. t_{PD}, t_{SU} and t_{CO} do not include routing paths in/out of the ECU block.

b. Internal feedback path in ECU restricts max clk frequency to 238 MHz.

c. B [15:0] set to zero.

NOTE: Timing numbers in **Table 5** represent -8 Worst Case Commercial conditions.

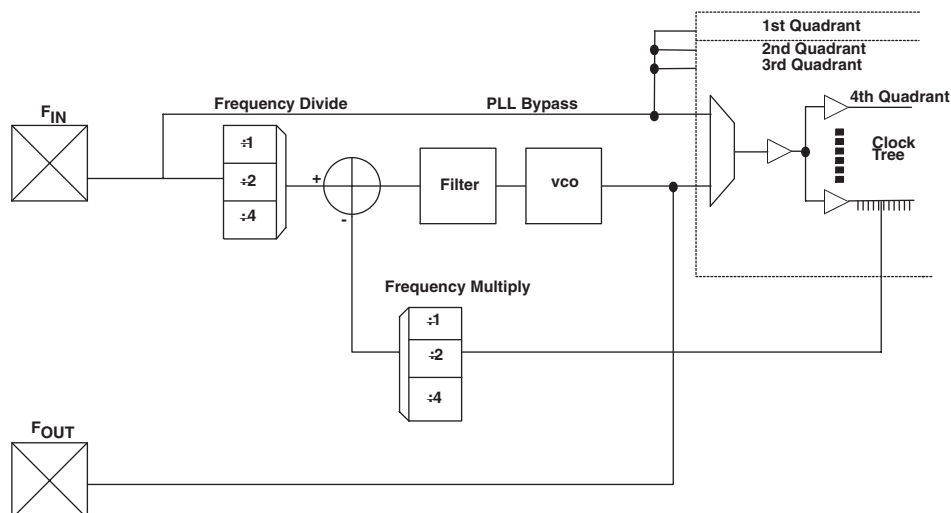
Phase Locked Loop (PLL) Information

Instead of requiring extra components, designers simply need to instantiate one of the pre-configured models (described in this section). The QuickLogic built-in PLLs support a wider range of frequencies than many other PLLs. These PLLs also have the ability to support different ranges of frequency multiplications or divisions, driving the device at a faster or slower rate than the incoming clock frequency. When PLLs are cascaded, the clock signal must be routed off-chip through the PLLPAD_OUT pin prior to routing into another PLL; internal routing cannot be used for cascading PLLs.

PLLs achieve a very short clock-to-out time—generally less than 3 ns. This low clock-to-out time is achieved by the PLL subtracting the clock tree delay through the feedback path, effectively making the clock tree delay zero.

Figure 6 illustrates a QuickLogic PLL.

Figure 6: PLL Block Diagram



F_{in} represents a very stable high-frequency input clock and produces an accurate signal reference. This signal can either bypass the PLL entirely, thus entering the clock tree directly, or it can pass through the PLL itself.

Within the PLL, a voltage-controlled oscillator (VCO) is added to the circuit. The external F_{in} signal and the local VCO form a control loop. The VCO is multiplied or divided down to the reference frequency, so that a phase detector (the crossed circle in **Figure 6**) can compare the two signals. If the phases of the external and local signals are not within the tolerance required, the phase detector sends a signal through the charge pump and loop filter (**Figure 6**). The charge pump generates an error voltage to bring the VCO back into alignment, and the loop filter removes any high frequency noise before the error voltage enters the VCO. This new VCO signal enters the clock tree to drive the chip's circuitry.

F_{out} represents the clock signal emerging from the output pad (the output signal PLLPAD_OUT is explained in **Table 7**). This clock signal is meaningful only when the PLL is configured for external use; otherwise, it remains in high Z state.

Most QuickLogic products contain four PLLs. The PLL presented in **Figure 6** controls the clock tree in the fourth quadrant of its FPGA. QuickLogic PLLs compensate for the additional delay created by the clock tree itself, as previously noted, by subtracting the clock tree delay through the feedback path.

For more specific information on the Phase Locked Loops, see QuickLogic Application Note 58 at <http://www.quicklogic.com/images/appnote58.pdf>.

PLL Modes of Operation

QuickLogic PLLs have eight modes of operation, based on the input frequency and desired output frequency—**Table 6** indicates the features of each mode.

NOTE: "HF" stands for "high frequency" and "LF" stands for "low frequency."

Table 6: PLL Mode Frequencies

PLL Model	Output Frequency	Input Frequency Range	Output Frequency Range
PLL_HF	Same as input	66 MHz–150 MHz	66 MHz–150 MHz
PLL_LF	Same as input	25 MHz–133 MHz	25 MHz–133 MHz
PLL_MULT2HF	2x	50 MHz–125 MHz	100 MHz–250 MHz
PLL_MULT2LF	2x	16 MHz–50 MHz	32 MHz–100 MHz
PLL_DIV2HF	1/2x	100 MHz–250 MHz	50 MHz–125 MHz
PLL_DIV2LF	1/2x	50 MHz–100 MHz	25 MHz–50 MHz
PLL_MULT4	4x	16 MHz–40 MHz	64 MHz–160 MHz
PLL_DIV4	1/4x	100 MHz–300 MHz	25 MHz–75 MHz

The input frequency can range from 16 MHz to 300 MHz, while output frequency ranges from 25 MHz to 250 MHz. When you add PLLs to your top-level design, be sure that the PLL mode matches your desired input and output frequencies.

PLL Signals

Table 7 summarizes the key signals in QuickLogic PLLs.

Table 7: QuickLogic PLL Signals

Signal Name	Description
PLLCLK_IN	Input clock signal
PLL_RESET	Active High Reset If PLL_RESET is asserted, then CLKNET_OUT and PLLPAD_OUT are reset to 0. This signal must be asserted and then released in order for the LOCK_DETECT to work.
ONn_OFFCHIP	PLL output This signal selects whether the PLL will drive the internal clock network or be used off-chip. This is a static signal, not a dynamic signal. Tied to GND = outgoing signal drives internal gates. Tied to VCC = outgoing signal used off-chip.
CLKNET_OUT	Out to internal gates This signal bypasses the PLL logic before driving the internal gates. Note that this signal cannot be used in the same quadrant where the PLL signal is used (PLLCLK_OUT).
PLLCLK_OUT	Out from PLL to internal gates This signal can drive the internal gates after going through the PLL. For this to work, ONn_OFFCHIP must be tied to GND.
PLLPAD_OUT	Out to off-chip This outgoing signal is used off-chip. For this configuration the ONn_OFFCHIP signal must be tied to VCC.
LOCK_DETECT	Active High Lock detection signal NOTE: For simulation purposes, this signal gets asserted after 10 clock cycles. However, it can take a maximum of 200 clock cycles to sync with the input clock upon release of the PLL_RESET signal.

NOTE: Because PLLCLK_IN and PLL_RESET signals have PLL_INPAD, and PLLPAD_OUT has OUTPAD, you do not need to add additional pads to your design.

I/O Cell Structure

Eclipse-II features a variety of distinct I/O pins to maximize performance, functionality, and flexibility with bi-directional I/O pins and input-only pins. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single ended I/O standards, VCCIO specifies the input tolerance and the output drive. For voltage referenced I/O standards (e.g SSTL), the voltage supplied to the INREF pins in each bank specifies the input switch point. For example, the VCCIO pins must be tied to a 3.3 V supply to provide 3.3 V compliance. Eclipse-II can also support the LVDS and LVPECL I/O standards with the use of external resistors (see **Table 8**).

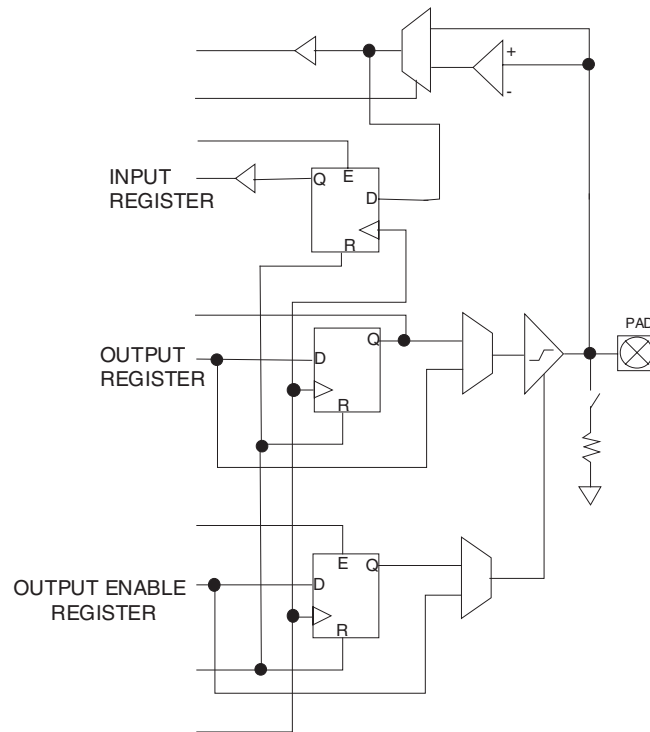
Table 8: I/O Standards and Applications

I/O Standard	Reference Voltage	Output Voltage	Application
LVTTTL	n/a	3.3 V	General Purpose
LVC MOS25	n/a	2.5 V	General Purpose
LVC MOS18	n/a	1.8 V	General Purpose
PCI	n/a	3.3 V	PCI Bus Applications
GTL+	1	n/a	Backplane
SSTL3	1.5	3.3 V	SDRAM
SSTL2	1.25	2.5 V	SDRAM

As designs become more complex and requirements more stringent, several application-specific I/O standards have emerged for specific applications. I/O standards for processors, memories, and a variety of bus applications have become commonplace and a requirement for many systems. In addition, I/O timing has become a greater issue with specific requirements for setup, hold, clock to out, and switching times. Eclipse-II has addressed these new system requirements and now includes a completely new I/O cell which consists of programmable I/Os as well as a new cell structure consisting of three registers—Input, Output, and OE.

Eclipse-II offers banks of programmable I/Os that address many of the bus standards that are popular today. As shown in **Figure 7** each bi-directional I/O pin is associated with an I/O cell which features an input register, an input buffer, an output register, a three-state output buffer, an output enable register, and 2 two-to-one output multiplexers.

Figure 7: Eclipse-II I/O Cell



The bi-directional I/O pin options can be programmed for input, output, or bi-directional operation. As shown in **Figure 7**, each bi-directional I/O pin is associated with an I/O cell which features an input register, an input buffer, an output register, a three-state output buffer, an output enable register, and 2 two-to-one multiplexers. The select lines of the two-to-one multiplexers are static and must be connected to either VCC or GND.

For input functions, I/O pins can provide combinatorial, registered data, or both options simultaneously to the logic array. For combinatorial input operation, data is routed from I/O pins through the input buffer to the array logic. For registered input operation, I/O pins drive the D input of input cell registers, allowing data to be captured with fast set-up times without consuming internal logic cell resources. The comparator and multiplexor in the input path allows for native support of I/O standards with reference points offset from traditional ground.

For output functions, I/O pins can receive combinatorial or registered data from the logic array. For combinatorial output operation, data is routed from the logic array through a multiplexer to the I/O pin. For registered output operation, the array logic drives the D input of the output cell register which in turn drives the I/O pin through a multiplexer. The multiplexer allows either a combinatorial or a registered signal to be driven to the I/O pin. The addition of an output register will also decrease the Tco. Since the output register does not need to drive the routing the length of the output path is also reduced.

The three-state output buffer controls the flow of data from the array logic to the I/O pin and allows the I/O pin to act as an input and/or output. The buffer's output enable can be individually controlled by the logic cell array or any pin (through the regular routing resources), or it can be bank-controlled through one of the global networks. The signal can also be either combinatorial or registered. This is identical to that of the flow for the output cell. For combinatorial control operation data is routed from the logic array through a multiplexer to the three-state control. The IOCTRL pins can directly drive the OE and CLK signals for all I/O cells within the same bank.

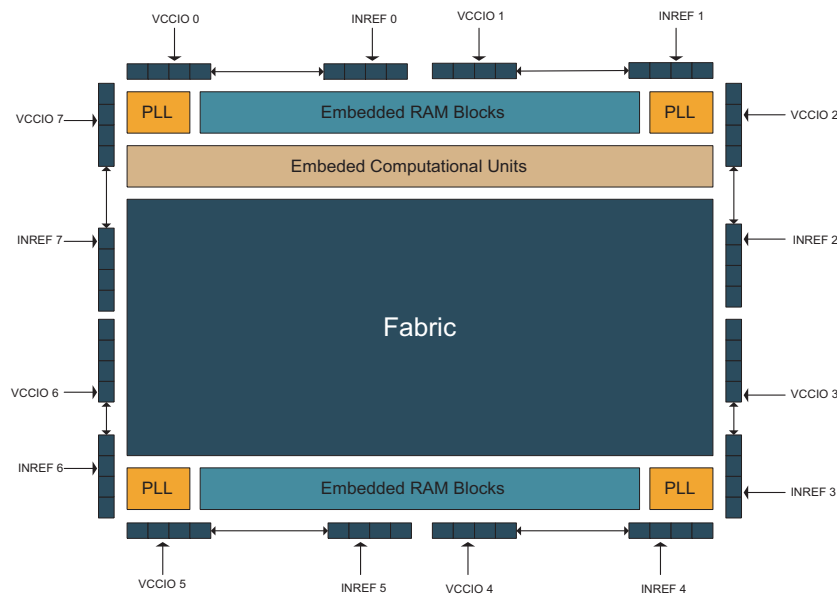
For registered control operation, the array logic drives the D input of the OE cell register which in turn drives the three-state control through a multiplexer. The multiplexer allows either a combinatorial or a registered signal to be driven to the three-state control.

When I/O pins are unused, the OE controls can be permanently disabled, allowing the output cell register to be used for registered feedback into the logic array.

I/O cell registers are controlled by clock, clock enable, and reset signals, which can come from the regular routing resources, from one of the global networks, or from two IOCTRL input pins per bank of I/O's. The CLK and RESET signals share common lines, while the clock enables for each register can be independently controlled. I/O interface support is programmable on a per bank basis. The two larger Eclipse-II devices contain eight I/O banks. The two smaller Eclipse-II devices contain two I/O banks per device. **Figure 8** illustrates the I/O bank configurations.

Each I/O bank is independent of other I/O banks and each I/O bank has its own VCCIO and INREF supply inputs. A mixture of different I/O standards can be used on the device; however, there is a limitation as to which I/O standards can be supported within a given bank. Only standards that share a common VCCIO and INREF can be shared within the same bank (e.g. PCI and LVTTL).

Figure 8: Multiple I/O Banks



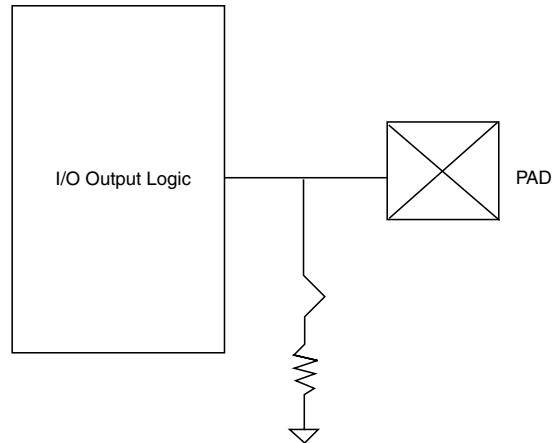
Programmable Slew Rate

Each I/O has programmable slew rate capability—the slew rate can be either fast or slow. The slower rate can be used to reduce the switching times of each I/O.

Programmable Weak Pull-Down

A programmable Weak Pull-Down resistor is available on each I/O. The I/O Weak Pull-Down eliminates the need for external pull down resistors for used I/Os as shown in **Figure 9**. The spec for pull-down current is maximum of 150 μA under worst case condition.

Figure 9: Programmable I/O Weak Pull-Down

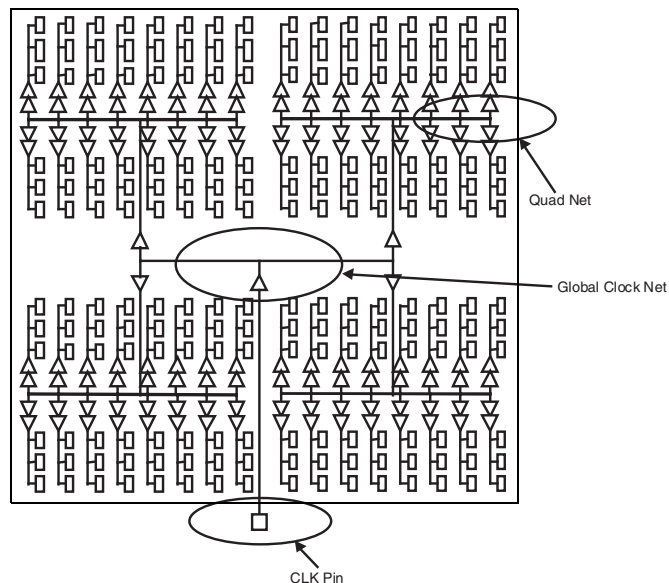


Clock Networks

Global Clocks

There are a maximum of eight global clock networks in each Eclipse-II device. Global clocks can drive logic cells and I/O registers, ECUs, and RAM blocks in the device. All global clocks have access to a Quad Net (local clock network) connection with a programmable connection to the logic cell's register clock input.

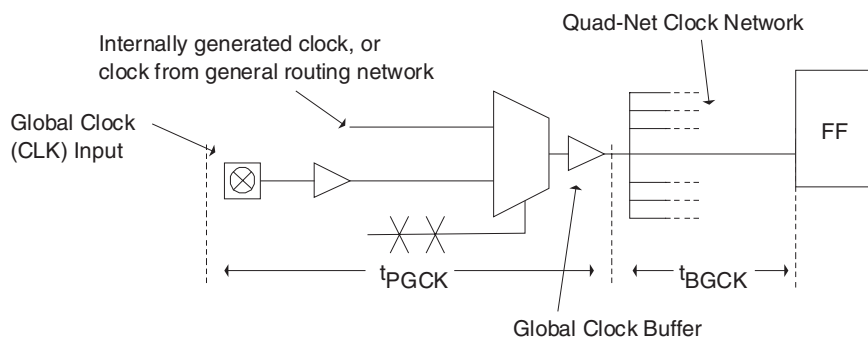
Figure 10: Global Clock Architecture



Quad-Net Network

There are five Quad-Net local clock networks in each quadrant for a total of 20 in a device. Each Quad-Net is local to a quadrant. Before driving the columns clock buffers, the quad-net is driven by the output of a mux which selects between the CLK pin input and an internally generated clock source (see **Figure 11**).

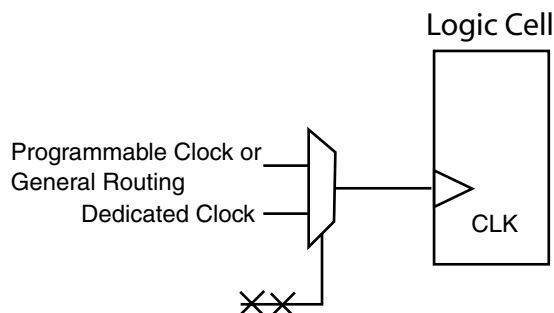
Figure 11: Global Clock Structure Schematic



Dedicated Clock

There is one dedicated clock in the two larger devices of the Eclipse-II Family (QL8325 and QL8250). This clock connects to the clock input of the Logic Cell and I/O registers, and RAM blocks through a hardwired connection and is multiplexed with the programmable clock input. The dedicated clock provides a fast global network with low skew. Users have the ability to select either the dedicated clock or the programmable clock (**Figure 12**).

Figure 12: Dedicated Clock Circuitry within Logic Cell



NOTE: For more information on the clocking capabilities of Eclipse-II FPGAs, see QuickLogic Application Note 68 at <http://www.quicklogic.com/images/appnote68.pdf>.

I/O Control and Local Hi-Drives

Each bank of I/Os has two input-only pins that can be programmed to drive the RST, CLK, and EN inputs of I/Os in that bank. These input-only pins also serve as high drive inputs to a quadrant. These buffers can be driven by the internal logic both as an I/O control or high drive. For I/O constrained designs, these pins can be used for general purpose inputs. To have more general purpose I/Os in the 208 PQFP package, the I/O controls pins are not bonded out. The performance of these drives is presented in **Table 9**.

Table 9: I/O Control Network/Local High-Drive

Destination TT, 25 C, 2.5 V	From Pad	From Array
I/O (far)	1.00 ns	1.14 ns
I/O (near)	0.63 ns	0.78 ns
Skew	0.37 ns	0.36 ns

Table 10 shows the total number of I/O control pins per device/package combination. These pins are not bonded out in the smaller devices and packages. This increases the number of bi-directional user I/Os available.

Table 10: I/O Control Pins per Device/Package Combination

Device	100 VQFP	196 TFBGA	208 PQFP	280 LFBGA	484 BGA
QL8025	-	-	Not available	Not available	Not available
QL8050	-	-	Not available	Not available	Not available
QL8150	Not available	-	-	Not available	Not available
QL8250	Not available	Not available	-	16	16
QL8325	Not available	Not available	-	16	16

Programmable Logic Routing

Eclipse-II devices are delivered with six types of routing resources as follows: short (sometimes called segmented) wires, dual wires, quad wires, express wires, distributed networks, and default wires. Short wires span the length of one logic cell, always in the vertical direction. Dual wires run horizontally and span the length of two logic cells. Short and dual wires are predominantly used for local connections. Default wires supply VCC and GND (Logic '1' and Logic '0') to each column of logic cells.

Quad wires have passive link interconnect elements every fourth logic cell. As a result, these wires are typically used to implement intermediate length or medium fan-out nets.

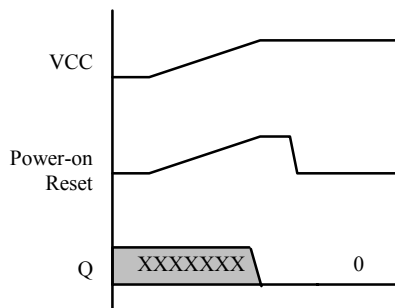
Express lines run the length of the programmable logic uninterrupted. Each of these lines has a higher capacitance than a quad, dual, or short wire, but less capacitance than shorter wires connected to run the length of the device. The resistance will also be lower because the express wires don't require the use of "pass" links. Express wires provide higher performance for long routes or high fan-out nets.

Distributed networks are described in **Clock Networks** on page 13. These wires span the programmable logic and are driven by quad-net buffers.

Global Power-On Reset (POR)

The Eclipse-II family of devices features a global power-on reset. This reset is hardwired to all registers and resets them to Logic '0' upon power-up of the device. In QuickLogic devices, the asynchronous Reset input to flip-flops has priority over the Set input; therefore, the Global POR will reset all flip-flops during power-up. If you want to set the flip-flops to Logic '1', you must assert the "Set" signal after the Global POR signal has been deasserted.

Figure 13: Power-On Reset

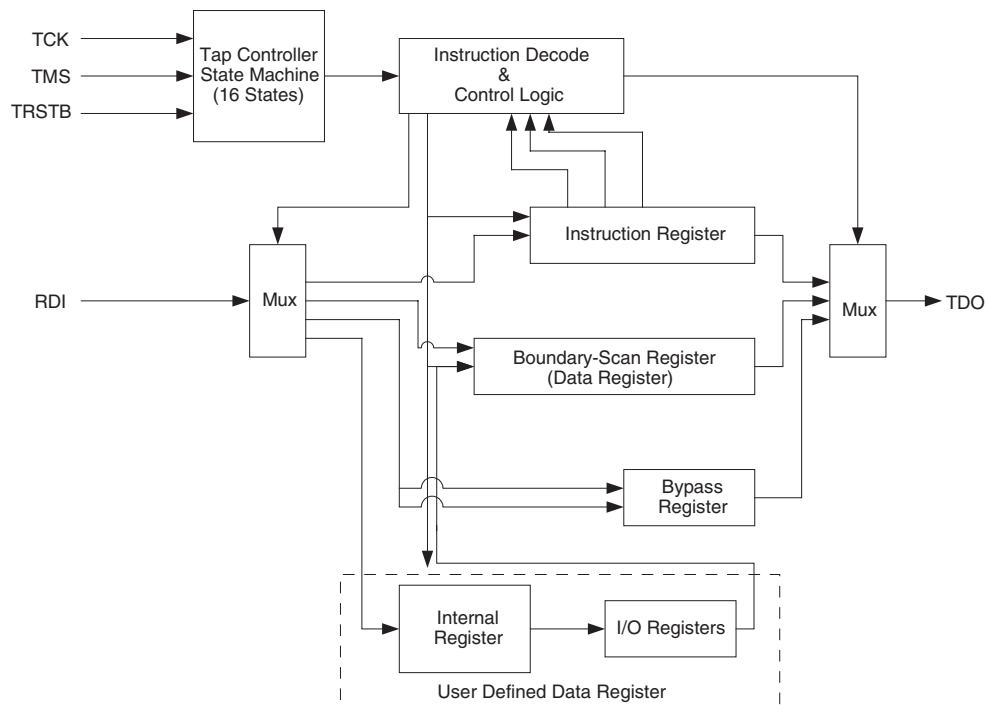


Low Power Mode

Power consumption of all Eclipse-II devices can be reduced significantly by de-activating the charge pumps inside the architecture. By applying 3.3 V to the VPUMP pin, the internal charge pump is de-activated—this effectively reduces the static and dynamic power consumption of the device. The Eclipse-II device is fully functional and operational in the Low Power mode. Users who have a 3.3 V supply available in their system should take advantage of this low power feature by tying the VPUMP pin to 3.3 V. Otherwise, if a 3.3 V supply is not available, this pin should be tied to ground.

Joint Test Access Group (JTAG) Information

Figure 14: JTAG Block Diagram



Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, one problem being the accessibility of test points. JTAG formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (through the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed through a data scan operation, allowing users to sample the functional data entering and leaving the device.

- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

JTAG BSDL Support

- BSDL-Boundary Scan Description Language
- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/ package combinations from QuickLogic
- Extensive industry support available and ATVG (Automatic Test Vector Generation)

Security Fuses

There are two security links: one to disable reading logic from the array, and the second to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs. The option to program these fuses is selectable via QuickWorks in the Tools/Options/Device Programming window in SpDE.

Flexibility Fuse

The flexibility link enables Power-Up loading of the Embedded RAM blocks. If the link is programmed, the Power Up Loading state machine is activated during power-up of the device. The state machine communicates with an external EPROM via the JTAG pins to download memory contents into the on-chip RAM. If the link is not programmed, Power-Up Loading is not enabled and the JTAG pins function as they normally would. The option to program this bit is selectable via QuickWorks in the Tools/Options/Device Programming window in SpDE. For more information on Power-Up Loading, see QuickLogic Application Note 55 at <http://www.quicklogic.com/images/appnote55.pdf>.

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 11** through **Table 13**.

Table 11: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 2.0 V	DC Input Current	±20 mA
VCCIO Voltage	-0.5 V to 4.0 V	ESD Pad Protection	±2000 V
INREF Voltage	0.5 V to VCCIO	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to VCCIO + 0.5 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C
Latch-up Immunity	±100 mA		

Table 12: Recommended Operating Range

Symbol	Parameter	Military		Industrial		Commercial		Unit	
		Min	Max	Min	Max	Min	Max		
VCC	Supply Voltage	1.71	1.89	1.71	1.89	1.71	1.89	V	
VCCIO	I/O Input Tolerance Voltage	1.71	3.60	1.71	3.60	1.71	3.60	V	
TA	Ambient Temperature	-55	-	-40	85	0	70	°C	
TC	Case Temperature	-	125	-	-	-	-	°C	
K	Delay Factor	-6 Speed Grade	0.48	1.47	0.49	1.38	0.53	1.35	n/a
		-7 Speed Grade	0.47	1.31	0.49	1.23	0.52	1.20	n/a
		-8 Speed Grade	0.45	1.23	0.46	1.16	0.49	1.13	n/a

Table 13: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
II	I or I/O Input Leakage Current	VI = VCCIO or GND	-10	10	μA
IOZ	3-State Output Leakage Current	VI = VCCIO or GND	-	10	μA
CI	I/O Input Capacitance ^a	-	-	8	pF
CCLOCK	Clock Input Capacitance	-	-	8	pF
IOS	Output Short Circuit Current ^b	VO = GND VO = VCC	-15 40	-180 210	mA mA
IDED	D.C. Supply Current on VDED	-	-	-	μA
IREF	D.C. Supply Current on INREF	-	-10	10	μA
IPD	Current on programmable pull-down	VCCIO = 3.6 V VCCIO = 2.5 V VCCIO = 1.8 V	-	150	μA
ICCIO	D.C. Supply Current on VCCIO	VCCIO = 1.8 V VCCIO = 2.5 V VCCIO = 3.3 V	-	-	μA
IPUMP	D.C. Supply Current on VPUMP	VPUMP = 3.3 V	-	-	μA
IPLL	D.C. Supply Current on each VCCPLL	2.5 V 3.3 V	-	-	μA

a. Capacitance is sample tested only. Clock pins are 12 pF maximum.

b. Only one output at a time. Duration should not exceed 30 seconds.

Table 14: ICC Characteristics

Device	VPUMP = 0 V	VPUMP = 3.3 V
QL8025	-	-
QL8050	-	-
QL8150	-	-
QL8250 ^{a, b}	2 mA	-
QL8325 ^{a, b}	2 mA	-

a. For -6/-7/-8 commercial grade devices only. Maximum ICC is 3 mA for all industrial grade devices and 5 mA for all military devices.

b. ICC is for current drawn by VCC and VDED. If any PLLs are used, see **Table 13** for current drawn by each PLL.

Table 15: DC Input and Output Levels^a

Symbol	INREF		V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
	V _{MIN}	V _{MAX}	V _{MIN}	V _{MAX}	V _{MIN}	V _{MAX}	V _{MAX}	V _{MIN}	mA	mA
LVTTTL	n/a	n/a	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVC MOS2	n/a	n/a	-0.3	0.7	1.7	VCCIO + 0.3	0.7	1.7	2.0	-2.0
LVC MOS18	n/a	n/a	-0.3	0.63	1.2	VCCIO + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x VCCIO	0.5 x V _{CCIO}	VCCIO + 0.5	0.1 x VCCIO	0.9 x VCCIO	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	VCCIO + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	1.10	1.90	8	-8

a. The data provided in **Table 8** and **Table 9** are JEDEC and PCI Specifications. QuickLogic devices either meet or exceed these requirements. For data specific to QuickLogic I/Os, see preceding **Table 20** through **Table 23**, **Figure 7** through **Figure 9**, and **Figure 23** through **Figure 26**.

NOTE: All CLK, IOCTRL, JTAG, and PLLIN pins are clamped to the VDED rail. Therefore, these pins can be driven up to VDED+ 0.3 V.

AC Characteristics

The AC Specifications (at $V_{CC} = 1.8\text{ V}$, $T_A = 25^\circ\text{ C}$, Worst Case Corner, Speed Grade = -8 ($K = 1.01$)) are provided from **Table 16** through **Table 25**. Logic Cell diagrams and waveforms are provided from **Figure 15** through **Figure 26**.

Figure 15: Eclipse-II Logic Cell

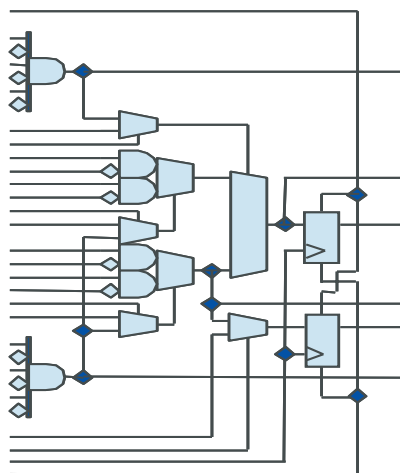


Table 16: Logic Cells

Symbol	Parameter	Value	
		Min	Max
t_{PD}	Combinatorial Delay of the longest path: time taken by the combinatorial circuit to output	-	0.257 ns
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	0.22 ns	-
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	-
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge.	-	0.255 ns
t_{CWHI}	Clock High Time: required minimum time the clock stays high	0.46 ns	-
t_{CWLO}	Clock Low Time: required minimum time that the clock stays low	0.46 ns	-
t_{SET}	Set Delay: time between when the flip-flop is "set" (high) and when the output is consequently "set" (high)	-	0.18 ns
t_{RESET}	Reset Delay: time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	-	0.09 ns
t_{SW}	Set Width: time that the SET signal must remain high/low	0.3 ns	-
t_{RW}	Reset Width: time that the RESET signal must remain high/low	0.3 ns	-

Figure 16: Logic Cell Flip-Flop

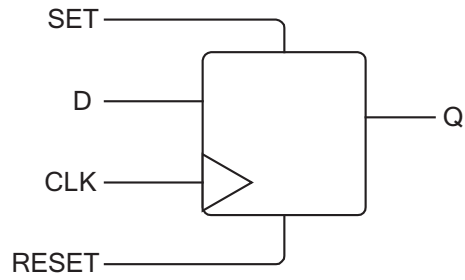


Figure 17: Logic Cell Flip-Flop Timings—First Waveform

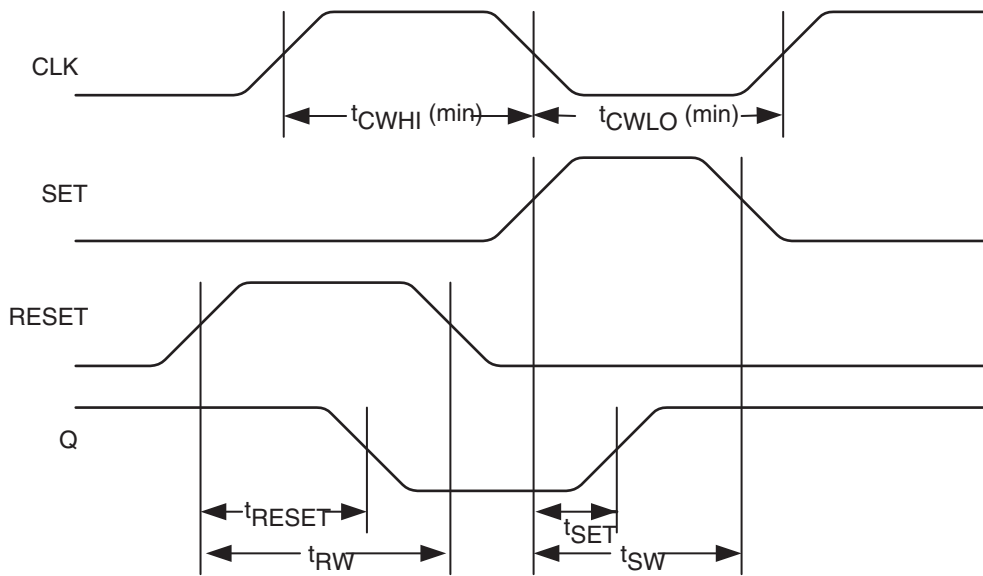


Figure 18: Logic Cell Flip-Flop Timings—Second Waveform

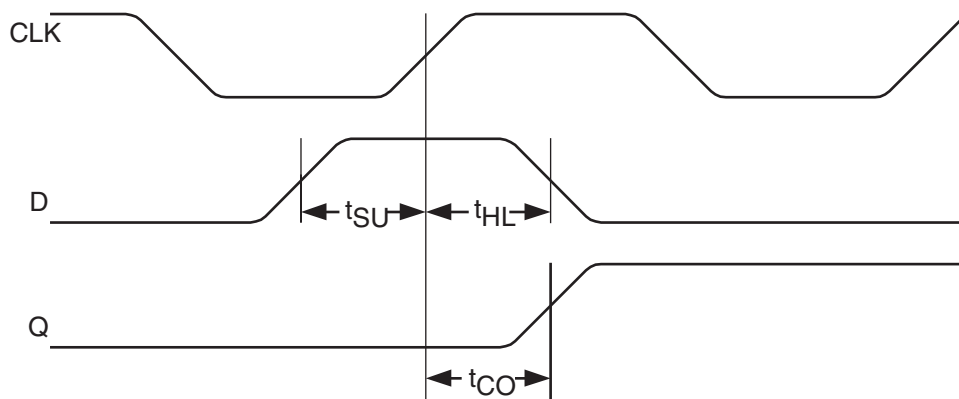


Table 17: Eclipse-II Global Clock Delay

Clock Segment	Parameter	Value	
		Min	Max
t_{PGCK}	Global clock pin delay to quad net	-	1.34 ns
t_{BGCK}	Global clock tree delay (quad net to flip-flop)	-	0.56 ns

NOTE: When using a PLL, t_{PGCK} and t_{BGCK} are effectively zero due to delay adjustment by Phase Locked Loop feedback path.

Figure 19: Global Clock Structure Timing Elements

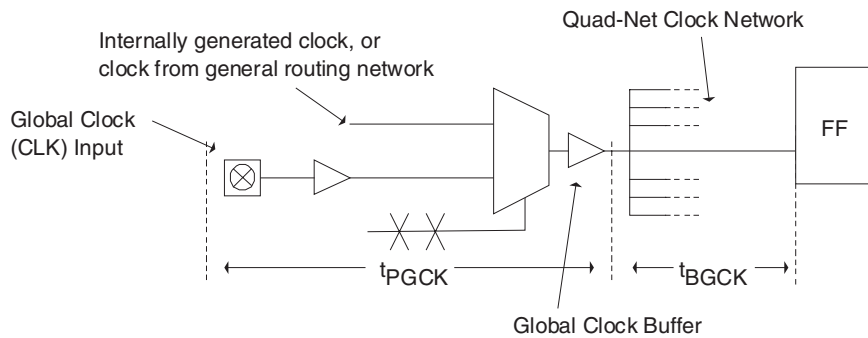


Figure 20: Dual-Port SRAM Cell

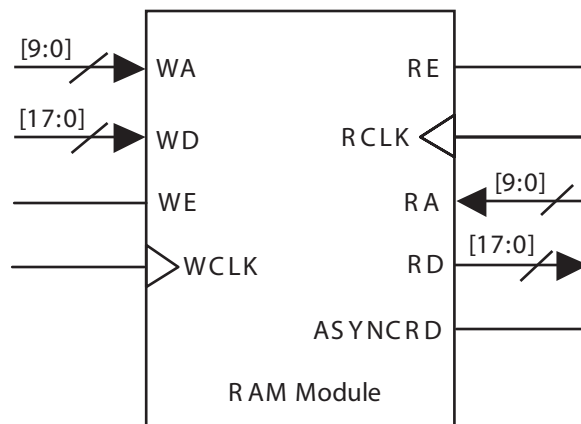


Table 18: RAM Cell Synchronous Write Timing

Symbol	Parameter	Value	
		Min	Max
RAM Cell Synchronous Write Timing			
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.675 ns	-
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.654 ns	-
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWE}	WE setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.623 ns	-
t_{HWE}	WE hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{WCRD}	WCLK to RD (WA = RA): time between the active WRITE CLOCK edge and the time when the data is available at RD	-	4.38 ns

Figure 21: RAM Cell Synchronous Write Timing

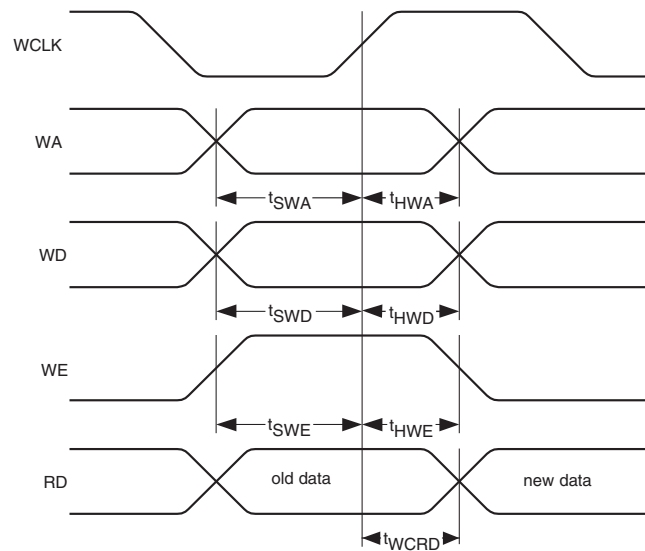


Table 19: RAM Cell Synchronous and Asynchronous Read Timing

Symbol	Parameter	Value	
		Min	Max
RAM Cell Synchronous Read Timing			
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.686 ns	-
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0 ns	-
t_{SRE}	RE setup time to WCLK: time the READ ENABLE must be stable before the active edge of the READ CLOCK	0.243 ns	-
t_{HRE}	RE hold time to WCLK: time the READ ENABLE must be stable after the active edge of the READ CLOCK	0 ns	-
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD	-	4.38 ns
RAM Cell Asynchronous Read Timing			
t_{PDRD}	RA to RD: time between when the READ ADDRESS is input and when the DATA is output	-	2.06 ns

Figure 22: RAM Cell Synchronous and Asynchronous Read Timing

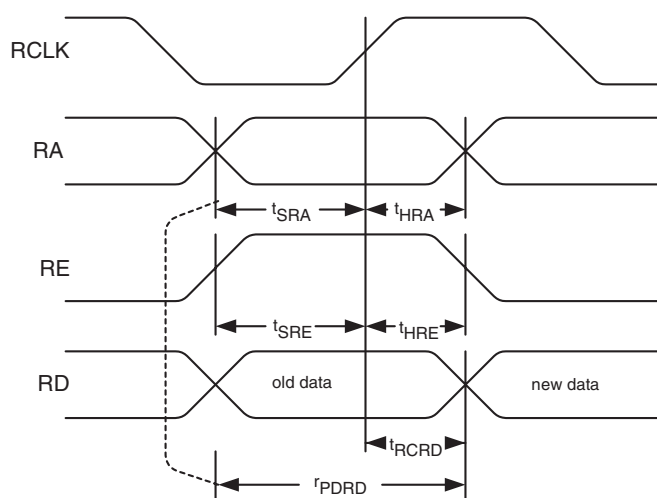


Figure 23: Eclipse-II I/O Cell Output Path

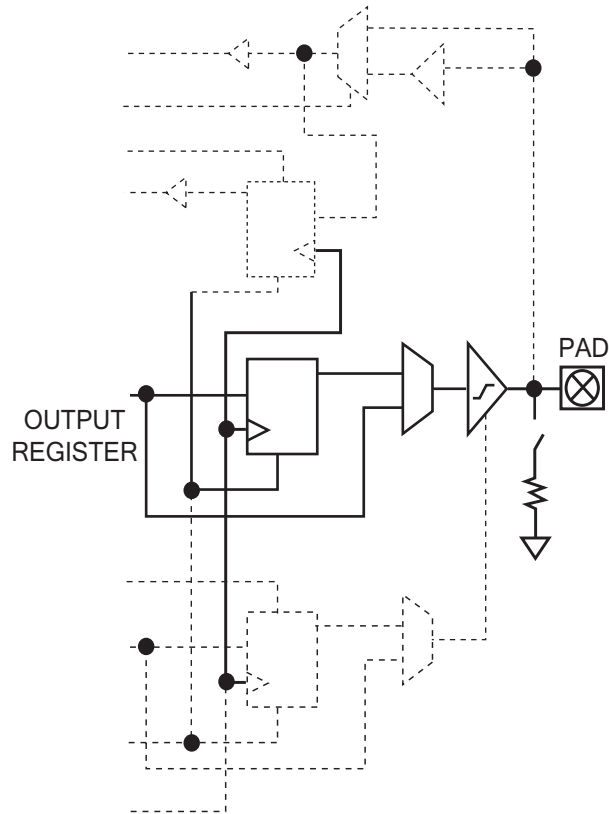


Figure 24: Eclipse-II I/O Cell Output Enable Timing

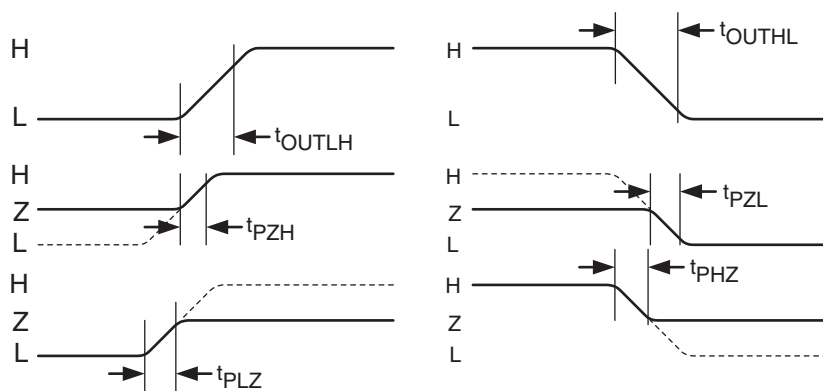


Table 20: Eclipse-II I/O Cell Output Timing

Symbol	Parameter	Value (ns)	
		Min	Max
Output Register Cell Only			
t_{OUTLH}	Output Delay low to high (90% of H)	-	2.594
t_{OUTHl}	Output Delay high to low (10% of L)	-	2.163
t_{PZH}	Output Delay tri-state to high (90% of H)	-	3.056
t_{PZL}	Output Delay tri-state to low (10% of L)	-	2.709
t_{PHZ}	Output Delay high to tri-State	-	3.434
t_{PLZ}	Output Delay low to tri-State	-	3.318
t_{COP}	Clock-to-out delay (does not include clock tree delays)	-	2.667 (fast slew) 8.999 (slow slew)

Table 21: Output Slew Rates @ VCCIO = 3.3 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	2.8 V/ns	1.0 V/ns
Falling Edge	2.86 V/ns	1.0 V/ns

Table 22: Output Slew Rates @ VCCIO = 2.5 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	1.7 V/ns	0.6 V/ns
Falling Edge	1.9 V/ns	0.6 V/ns

Table 23: Output Slew Rates @ VCCIO = 1.8 V, T = 25° C

	Fast Slew	Slow Slew
Rising Edge	-	-
Falling Edge	-	-

Figure 25: Eclipse-II I/O Cell Input Path

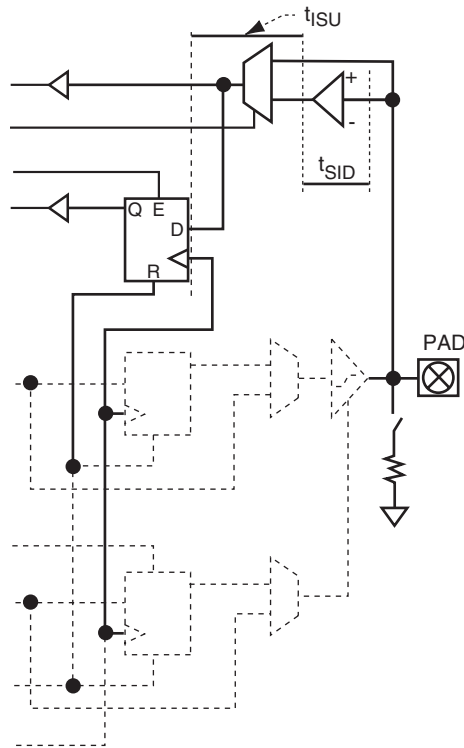


Figure 26: Eclipse-II Input Register Cell Timing

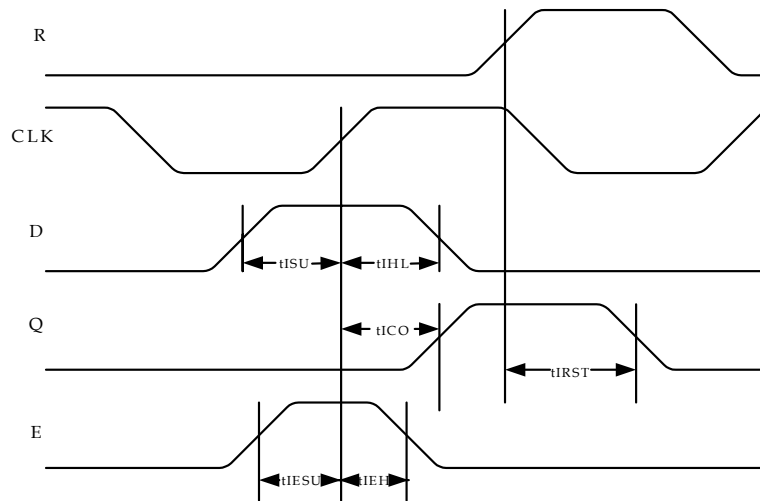


Table 24: I/O Input Register Cell Timing

Symbol	Parameter	Value	
		Min	Max
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.50 ns	-
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	-	0 ns
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output after the active clock edge	-	1.08 ns
t_{IRST}	Input register reset delay: time between when the flip-flop is “reset”(low) and when the output is consequently “reset” (low)	-	0.99 ns
t_{IESU}	Input register clock enable setup time: time “enable” must be stable before the active clock edge	0.37 ns	-
t_{IEH}	Input register clock enable hold time: time “enable” must be stable after the active clock edge	0 ns	-

Table 25: I/O Input Buffer Delays

Symbol	Parameter	Value	
		Min	Max
t_{SID} (LVTTTL)	LVTTTL input delay: Low Voltage TTL for 3.3 V applications	-	0.34 ns
t_{SID} (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5 V and lower applications	-	0.42 ns
t_{SID} (LVCMOS18)	LVCMOS18 input delay: Low Voltage CMOS for 1.8 V applications	-	-
t_{SID} (GTL+)	GTL+ input delay: Gunning Transceiver Logic	-	0.68 ns
t_{SID} (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3 V	-	0.55 ns
t_{SID} (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5 V	-	0.61 ns

Package Thermal Characteristics

Thermal Resistance Equations:

$$\theta_{JC} = (T_J - T_C) / P$$

$$\theta_{JA} = (T_J - T_A) / P$$

$$P_{MAX} = (T_{JMAX} - T_{AMAX}) / \theta_{JA}$$

Parameter Description:

θ_{JC} : Junction-to-case thermal resistance

θ_{JA} : Junction-to-ambient thermal resistance

T_J : Junction temperature

T_A : Ambient temperature

P: Power dissipated by the device while operating

P_{MAX} : The maximum power dissipation for the device

T_{JMAX} : Maximum junction temperature

T_{AMAX} : Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 150° C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 26**, pick an appropriate T_{AMAX} and use:

$$P_{MAX} = (150^\circ \text{ C} - T_{AMAX}) / \theta_{JA}$$

Table 26: Package Thermal Characteristics

Device	Package Description			θ_{JA} (° C/W)		
	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM
QL8325 QL6325E	PS	PBGA	484	26.6	24.1	21.8
	PT	LF-PBGA	280	34	13.6	29.9
	PQ	PQFP	208	32	28	26.5
QL8250 QL6250E	PS	PBGA	484	26.6	24.1	21.8
	PT	LF-PBGA	280	34	13.6	29.9
	PQ	PQFP	208	32	28	26.5
QL8150	PT	TF-PBGA	196	40	38	35.2
	PQ	PQFP	208	43.6	41	39
QL8050	PT	TF-PBGA	196	54	51.8	48
	PV	VQFP	100	43	41.3	38.8
QL8025	PT	TF-PBGA	196	54	51.8	48
	PV	VQFP	100	43	41.3	38.8

Kv and Kt Graphs

Figure 27: Voltage Factor vs. Supply Voltage

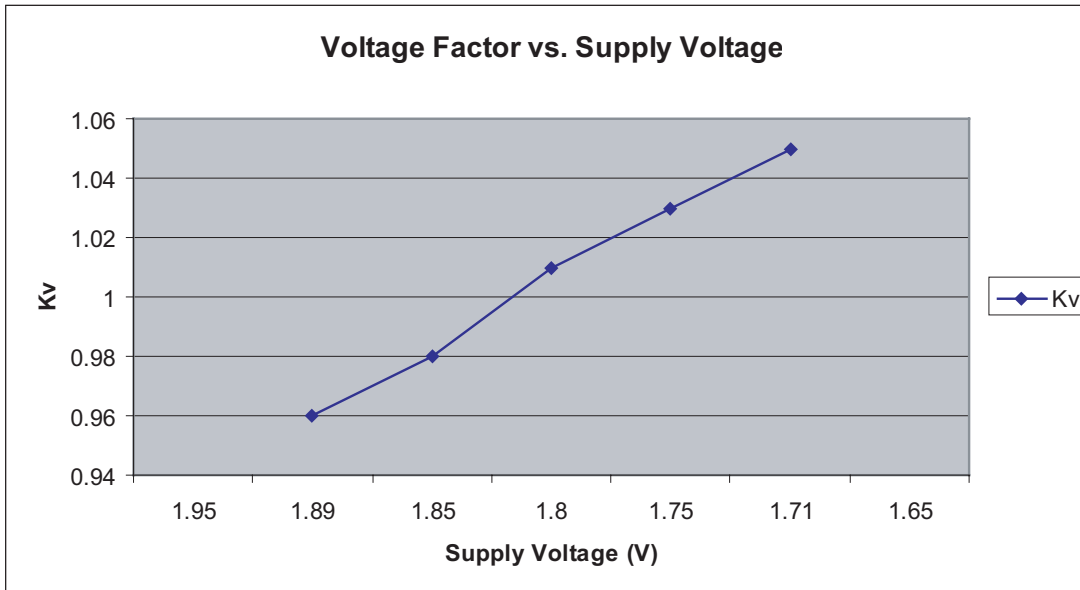
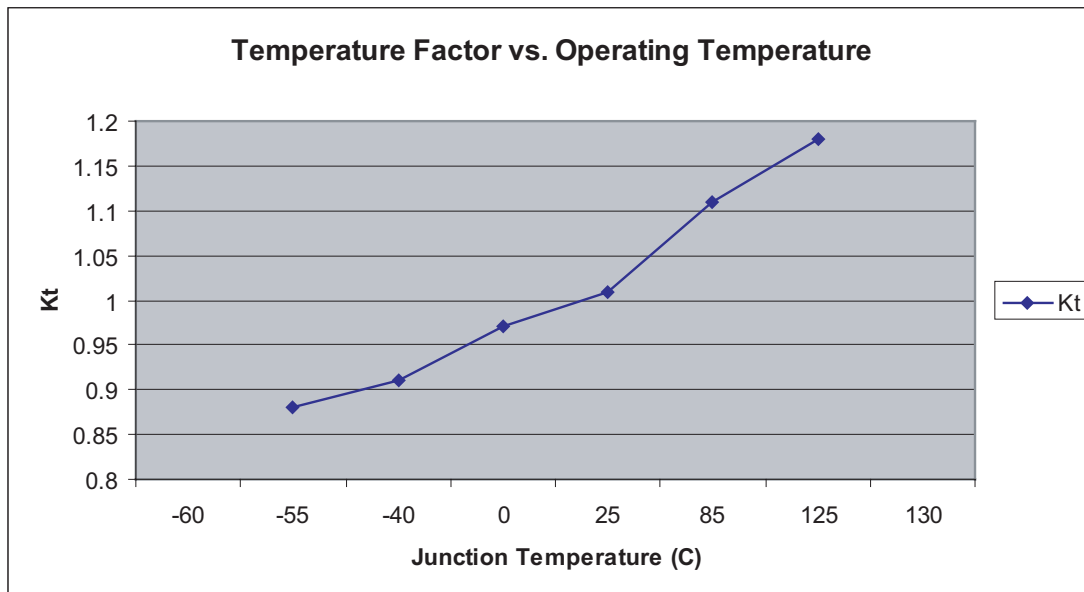


Figure 28: Temperature Factor vs. Operating Temperature



Power vs. Operating Frequency

The basic power equation which best models power consumption is given below:

$$P_{\text{TOTAL}} = 0.350 + f[0.0031 \eta_{\text{LC}} + 0.0948 \eta_{\text{CKBF}} + 0.01 \eta_{\text{CLBF}} + 0.0263 \eta_{\text{CKLD}} + 0.543 \eta_{\text{RAM}} + 0.20 \eta_{\text{PLL}} + 0.0035 \eta_{\text{INP}} + 0.0257 \eta_{\text{OUTP}}] \text{ (mW)}$$

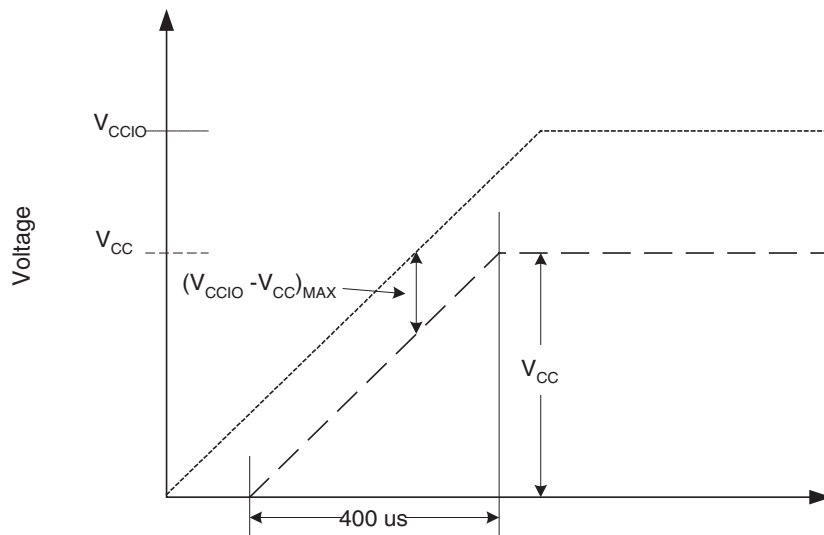
Where:

- η_{LC} is the total number of logic cells in the design
- η_{CKBF} = # of clock buffers
- η_{CLBF} = # of column clock buffers
- η_{CKLD} = # of loads connected to the column clock buffers
- η_{RAM} = # of RAM blocks
- η_{PLL} = # of PLLs
- η_{INP} is the number of input pins
- η_{OUTP} is the number of output pins

NOTE: To learn more about power consumption, see QuickLogic Application Note 60 at <http://www.quicklogic.com/images/appnote60.pdf>.

Power-up Sequencing

Figure 29: Power-up Sequencing



When powering up a device, the VCC/VCCIO rails must take 400 μ s or longer to reach the maximum value (refer to **Figure 29**).

NOTE: Ramping VCC/VCCIO to the maximum voltage faster than 400 μ s can cause the device to behave improperly.

For users with a limited power budget, keep $(V_{\text{CCIO}} - V_{\text{CC}})_{\text{MAX}} \leq 500 \text{ mV}$ when ramping up the power supply.

Pin Descriptions

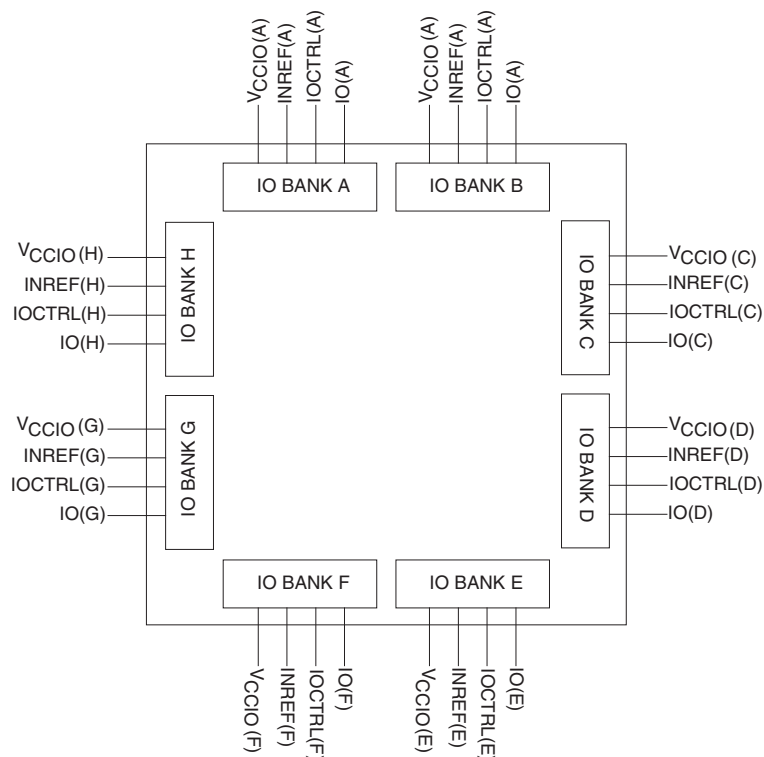
Table 27: Pin Descriptions

Pin	Direction	Function	Description
JTAG Pin Descriptions			
TDI/RSI	I	Test Data In for JTAG/RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VDED if unused
TRSTB/RRO	I/O	Active low Reset for JTAG/RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused
TMS	I	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VDED if not used for JTAG
TCK	I	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VDED or GND if not used for JTAG
TDO/RCO	O	Test data out for JTAG/RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization
Dedicated Pin Descriptions			
CLK	I	Global clock network pin	Low skew global clock. This pin provides access to a dedicated, distributed network capable of driving the CLOCK, SET, RESET, F1, and A2 inputs to the Logic Cell, READ, and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, CLOCK of the ECUs, and Output Enables of the I/Os. The voltage tolerance of this pin is specified by VDED.
I/O(A)	I/O	Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The A inside the parenthesis means that the I/O is located in Bank A. If an I/O is not used, SpDE (QuickWorks Tool) provides the option of tying that pin to GND, VCC, or TriState.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The A inside the parenthesis means that VCCIO is located in BANK A. Every I/O pin in Bank A will be tolerant of VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.
PLLIN	I	PLL clock input	Clock input for PLL. The voltage tolerance of this pin is specified by VDED.
DEDCLK	I	Dedicated clock pin	Very low skew global clock. This pin provides access to a dedicated, distributed clock network capable of driving the CLOCK inputs of all sequential elements of the device (e.g., RAM, Flip Flops). The voltage tolerance of this pin is specified by VDED.
GNDPLL	I	Ground pin for PLL	Connect to GND.

Table 27: Pin Descriptions (Continued)

Pin	Direction	Function	Description
INREF(A)	I	Differential reference voltage	The INREF is the reference voltage pin for GTL+, SSTL2, and STTL3 standards. Follow the recommendations provided in Table 15 for the appropriate standard. The A inside the parenthesis means that INREF is located in BANK A. This pin should be tied to GND if voltage referenced standards are not used.
PLLOUT	O	PLL output pin	Dedicated PLL output pin. May be left unconnected if PLL is not configured to drive off-chip.
IOCTRL(A)	I	Highdrive input	This pin provides fast RESET, SET, CLOCK, and ENABLE access to the I/O cell flip-flops, providing fast clock-to-out and fast I/O response times. This pin can also double as a high-drive pin to the internal logic cells. The A inside the parenthesis means that IOCTRL is located in Bank A. There is an internal pulldown resistor to GND on this pin. This pin should be tied to GND if it is not used. For backwards compatibility with Eclipse and EclipsePlus, it can be tied to VDED or GND. If tied to VDED, it will draw no more than 20 μ A per IOCTRL pin due to the pulldown resistor. The voltage tolerance of this pin is specified by VDED.
VPUMP	I	Charge Pump Disable	This pin disables the internal charge pump for lower static power consumption. To disable the charge pump, connect VPUMP to 3.3 V. If the Disable Charge Pump feature is not used, connect VPUMP to GND. For backwards compatibility with Eclipse and EclipsePlus devices, connect VPUMP to GND.
VDED	I	Voltage tolerance for clocks, JTAG, and IOCTRL/Voltage Drive for PLLOUT and JTAG pins	This pin specifies the input voltage tolerance for CLK, DEDCLK, PLLIN, JTAG, and IOCTRL dedicated input pins, as well as the output voltage drive for PLLOUT and JTAG pins. If the PLLs are used, VDED must be the same as VCCPLL. For backwards compatibility with Eclipse and EclipsePlus devices, connect VDED to 2.5 V.
VCCPLL	I	Power Supply pin for PLL	Connect to 2.5 V supply or 3.3 V supply. For backwards compatibility with Eclipse and EclipsePlus devices, connect to 2.5 V. To minimize static power consumption when designs do not utilize the PLLs, you may connect VCCPLL to GND. If VCCPLL is grounded, the PLL is disabled.

Figure 30: I/O Banks with Relevant Pins



Recommended Unused Pin Terminations for Eclipse-II Devices

All unused, general purpose I/O pins can be tied to VCC, GND, or HIZ (high impedance) internally using the Configuration Editor. This option is given in the bottom-right corner of the placement window. To use the Placement Editor, choose **Constraint > Fix Placement** in the Option pull-down menu of SpDE.

The rest of the pins should be terminated at the board level in the manner presented in **Table 28**.

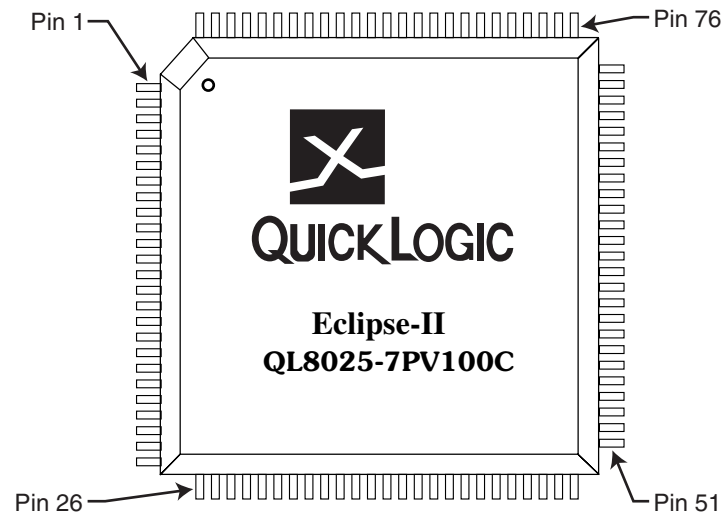
Table 28: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
PLLOUT<x> ^a	Unused PLL output pins must be connected to VDED or GND so that their associated input buffers never float. Utilized PLL output pins that route the PLL clock outside of the chip should not be tied to either VDED or GND.
IOCTRL<y> ^b	There is an internal pulldown resistor to GND on this pin. This pin should be tied to GND if it is not used. For backwards compatibility with Eclipse, it can be tied to VDED or GND. If tied to VDED, it will draw no more than 20 μ A per IOCTRL pin due to the pulldown resistor.
CLK/PLLIN<x>	Any unused clock pins should be connected to VDED or GND.
PLLRST<x>	If a PLL module is not used, then the associated PLLRST<x> must be connected to VDED or GND. If VCCPLL is grounded, then PLLRST must be grounded also. If VCCPLL is driven by 2.5 V or 3.3 V, PLLRST must be driven by the same voltage.
INREF<y>	If an I/O bank does not require the use of the INREF signal the pin should be connected to GND.

a. x represents a number.

b. y represents an alphabetical character.

QL8025 - 100 VQFP Pinout Diagram



QL8025 - 100 VQFP Pinout Table

Table 29: QL8025 - 100 VQFP Pinout Table

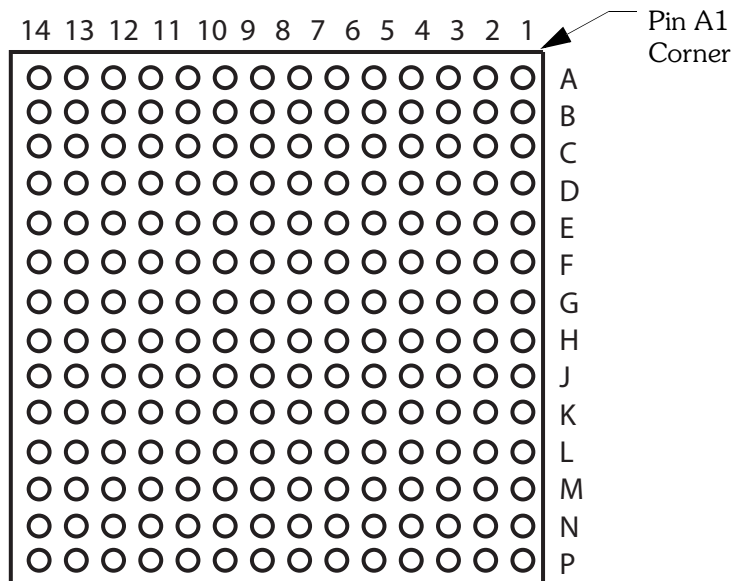
Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GND	21	I/O(A)	41	VCC	61	I/O(B)	81	I/O(B)
2	GND	22	I/O(A)	42	I/O(A)	62	I/O(B)	82	I/O(B)
3	I/O(A)	23	I/O(A)	43	I/O(A)	63	CLK(2)	83	I/O(B)
4	I/O(A)	24	I/O(A)	44	I/O(A)	64	CLK(3)	84	VCC
5	I/O(A)	25	TDO	45	I/O(A)	65	VCC	85	I/O(B)
6	VCC	26	I/O(A)	46	I/O(A)	66	CLK(4)	86	I/O(B)
7	I/O(A)	27	GND	47	VCCIO(A)	67	TMS	87	VCC
8	I/O(A)	28	I/O(A)	48	I/O(A)	68	I/O(B)	88	TCK
9	VCCIO(A)	29	VCCIO(A)	49	VPUMP	69	GND	89	VDED
10	I/O(A)	30	I/O(A)	50	I/O(A)	70	I/O(B)	90	I/O(B)
11	TDI	31	I/O(A)	51	GND	71	I/O(B)	91	GND
12	CLK(0)	32	I/O(A)	52	I/O(B)	72	I/O(B)	92	I/O(B)
13	CLK(1)	33	I/O(A)	53	I/O(B)	73	I/O(B)	93	I/O(B)
14	VCC	34	I/O(A)	54	I/O(B)	74	I/O(B)	94	I/O(B)
15	I/O(A)	35	VCC	55	VCC	75	I/O(B)	95	I/O(B)
16	VDED	36	TRSTB	56	I/O(B)	76	GND	96	I/O(B)
17	I/O(A)	37	VDED	57	INREF	77	I/O(B)	97	I/O(B)
18	GND	38	I/O(A)	58	I/O(B)	78	VCCIO(B)	98	VCCIO(B)
19	I/O(A)	39	I/O(A)	59	I/O(B)	79	I/O(B)	99	I/O(B)
20	I/O(A)	40	GND	60	VCCIO(B)	80	I/O(B)	100	I/O(B)

QL8025 - 196 TF-PBGA Pinout Diagram

Top



Bottom

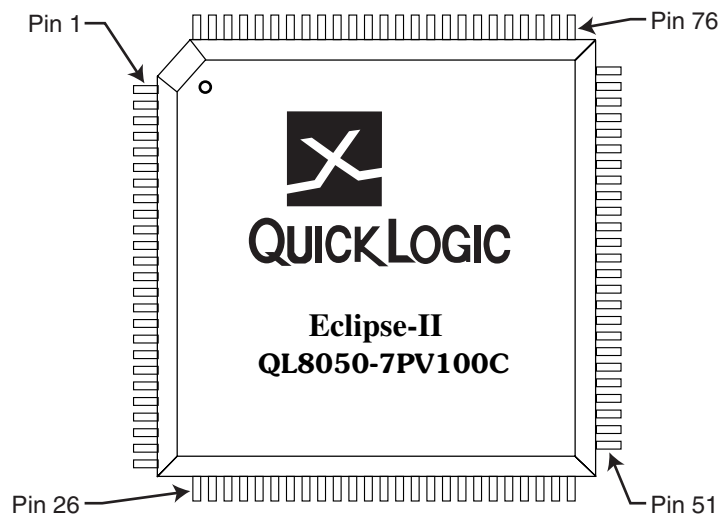


QL8025 - 196 TF-PBGA Pinout Table

Table 30: QL8025 - 196 TF-PBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1		C13		F11		J9		M7	
A2		C14		F12		J10		M8	
A3		D1		F13		J11		M9	
A4		D2		F14		J12		M10	
A5		D3		G1		J13		M11	
A6		D4		G2		J14		M12	
A7		D5		G3		K1		M13	
A8		D6		G4		K2		M14	
A9		D7		G5		K3		N1	
A10		D8		G6		K4		N2	
A11		D9		G7		K5		N3	
A12		D10		G8		K6		N4	
A13		D11		G9		K7		N5	
A14		D12		G10		K8		N6	
B1		D13		G11		K9		N7	
B2		D14		G12		K10		N8	
B3		E1		G13		K11		N9	
B4		E2		G14		K12		N10	
B5		E3		H1		K13		N11	
B6		E4		H2		K14		N12	
B7		E5		H3		L1		N13	
B8		E6		H4		L2		N14	
B9		E7		H5		L3		P1	
B10		E8		H6		L4		P2	
B11		E9		H7		L5		P3	
B12		E10		H8		L6		P4	
B13		E11		H9		L7		P5	
B14		E12		H10		L8		P6	
C1		E13		H11		L9		P7	
C2		E14		H12		L10		P8	
C3		F1		H13		L11		P9	
C4		F2		H14		L12		P10	
C5		F3		J1		L13		P11	
C6		F4		J2		L14		P12	
C7		F5		J3		M1		P13	
C8		F6		J4		M2		P14	
C9		F7		J5		M3			
C10		F8		J6		M4			
C11		F9		J7		M5			
C12		F10		J8		M6			

QL8050 - 100 VQFP Pinout Diagram



QL8050 - 100 VQFP Pinout Table

Table 31: QL8050 - 100 VQFP Pinout Table

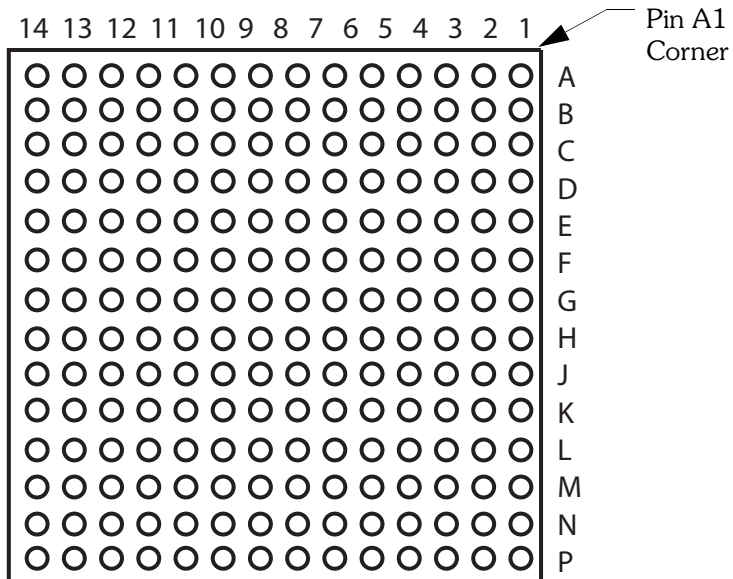
Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GND	21	I/O(A)	41	VCC	61	I/O(B)	81	I/O(B)
2	GND	22	I/O(A)	42	I/O(A)	62	I/O(B)	82	I/O(B)
3	I/O(A)	23	I/O(A)	43	I/O(A)	63	CLK(2)	83	I/O(B)
4	I/O(A)	24	I/O(A)	44	I/O(A)	64	CLK(3)	84	VCC
5	I/O(A)	25	TDO	45	I/O(A)	65	VCC	85	I/O(B)
6	VCC	26	I/O(A)	46	I/O(A)	66	CLK(4)	86	I/O(B)
7	I/O(A)	27	GND	47	VCCIO(A)	67	TMS	87	VCC
8	I/O(A)	28	I/O(A)	48	I/O(A)	68	I/O(B)	88	TCK
9	VCCIO(A)	29	VCCIO(A)	49	VPUMP	69	GND	89	VDED
10	I/O(A)	30	I/O(A)	50	I/O(A)	70	I/O(B)	90	I/O(B)
11	TDI	31	I/O(A)	51	GND	71	I/O(B)	91	GND
12	CLK(0)	32	I/O(A)	52	I/O(B)	72	I/O(B)	92	I/O(B)
13	CLK(1)	33	I/O(A)	53	I/O(B)	73	I/O(B)	93	I/O(B)
14	VCC	34	I/O(A)	54	I/O(B)	74	I/O(B)	94	I/O(B)
15	I/O(A)	35	VCC	55	VCC	75	I/O(B)	95	I/O(B)
16	VDED	36	TRSTB	56	I/O(B)	76	GND	96	I/O(B)
17	I/O(A)	37	VDED	57	INREF	77	I/O(B)	97	I/O(B)
18	GND	38	I/O(A)	58	I/O(B)	78	VCCIO(B)	98	VCCIO(B)
19	I/O(A)	39	I/O(A)	59	I/O(B)	79	I/O(B)	99	I/O(B)
20	I/O(A)	40	GND	60	VCCIO(B)	80	I/O(B)	100	I/O(B)

QL8050 - 196 TF-PBGA Pinout Diagram

Top



Bottom



QL8050 - 196 TF-PBGA Pinout Table

Table 32: QL8050 - 196 TF-PBGA Pinout Table

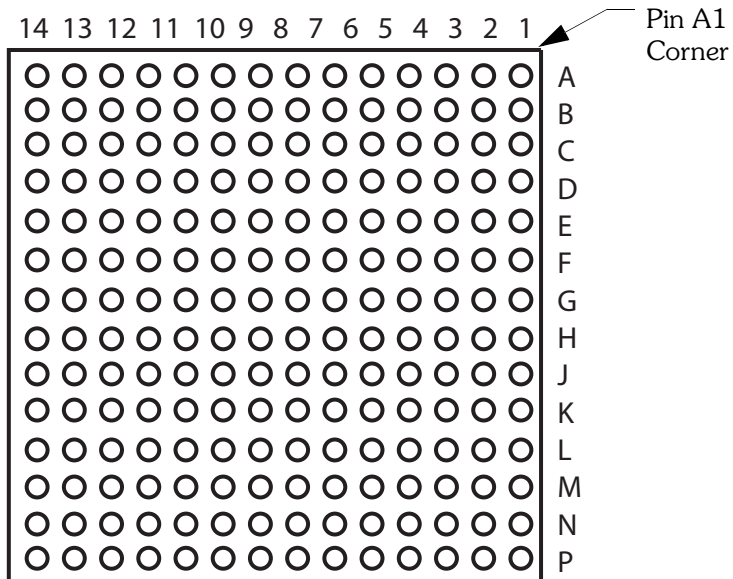
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1		C13		F11		J9		M7	
A2		C14		F12		J10		M8	
A3		D1		F13		J11		M9	
A4		D2		F14		J12		M10	
A5		D3		G1		J13		M11	
A6		D4		G2		J14		M12	
A7		D5		G3		K1		M13	
A8		D6		G4		K2		M14	
A9		D7		G5		K3		N1	
A10		D8		G6		K4		N2	
A11		D9		G7		K5		N3	
A12		D10		G8		K6		N4	
A13		D11		G9		K7		N5	
A14		D12		G10		K8		N6	
B1		D13		G11		K9		N7	
B2		D14		G12		K10		N8	
B3		E1		G13		K11		N9	
B4		E2		G14		K12		N10	
B5		E3		H1		K13		N11	
B6		E4		H2		K14		N12	
B7		E5		H3		L1		N13	
B8		E6		H4		L2		N14	
B9		E7		H5		L3		P1	
B10		E8		H6		L4		P2	
B11		E9		H7		L5		P3	
B12		E10		H8		L6		P4	
B13		E11		H9		L7		P5	
B14		E12		H10		L8		P6	
C1		E13		H11		L9		P7	
C2		E14		H12		L10		P8	
C3		F1		H13		L11		P9	
C4		F2		H14		L12		P10	
C5		F3		J1		L13		P11	
C6		F4		J2		L14		P12	
C7		F5		J3		M1		P13	
C8		F6		J4		M2		P14	
C9		F7		J5		M3			
C10		F8		J6		M4			
C11		F9		J7		M5			
C12		F10		J8		M6			

QL8150 - 196 TF-PBGA Pinout Diagram

Top



Bottom



QL8150 - 196 TF-PBGA Pinout Table

Table 33: QL8150 - 196 TF-PBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1		C13		F11		J9		M7	
A2		C14		F12		J10		M8	
A3		D1		F13		J11		M9	
A4		D2		F14		J12		M10	
A5		D3		G1		J13		M11	
A6		D4		G2		J14		M12	
A7		D5		G3		K1		M13	
A8		D6		G4		K2		M14	
A9		D7		G5		K3		N1	
A10		D8		G6		K4		N2	
A11		D9		G7		K5		N3	
A12		D10		G8		K6		N4	
A13		D11		G9		K7		N5	
A14		D12		G10		K8		N6	
B1		D13		G11		K9		N7	
B2		D14		G12		K10		N8	
B3		E1		G13		K11		N9	
B4		E2		G14		K12		N10	
B5		E3		H1		K13		N11	
B6		E4		H2		K14		N12	
B7		E5		H3		L1		N13	
B8		E6		H4		L2		N14	
B9		E7		H5		L3		P1	
B10		E8		H6		L4		P2	
B11		E9		H7		L5		P3	
B12		E10		H8		L6		P4	
B13		E11		H9		L7		P5	
B14		E12		H10		L8		P6	
C1		E13		H11		L9		P7	
C2		E14		H12		L10		P8	
C3		F1		H13		L11		P9	
C4		F2		H14		L12		P10	
C5		F3		J1		L13		P11	
C6		F4		J2		L14		P12	
C7		F5		J3		M1		P13	
C8		F6		J4		M2		P14	
C9		F7		J5		M3			
C10		F8		J6		M4			
C11		F9		J7		M5			
C12		F10		J8		M6			

QL8150 - 208 PQFP Pinout Diagram



QL8150 - 208 PQFP Pinout Table

Table 34: QL8150 - 208 PQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O(A)	43	I/O(A)	85	I/O(A)	127	I/O(B)	169	I/O(B)
2	I/O(A)	44	VCCIO(A)	86	VCC	128	CLK(2)	170	I/O(B)
3	GND	45	I/O(A)	87	I/O(A)	129	VDED	171	I/O(B)
4	GND	46	VCC	88	I/O(A)	130	CLK(3)	172	I/O(B)
5	I/O(A)	47	I/O(A)	89	VCC	131	VCC	173	I/O(B)
6	I/O(A)	48	I/O(A)	90	I/O(A)	132	CLK(4)	174	I/O(B)
7	I/O(A)	49	GND	91	I/O(A)	133	TMS	175	VCC
8	VCCIO(A)	50	TDO	92	I/O(A)	134	I/O(B)	176	I/O(B)
9	I/O(A)	51	I/O(A)	93	I/O(A)	135	I/O(B)	177	VCCIO(B)
10	I/O(A)	52	GND	94	I/O(A)	136	I/O(B)	178	GND
11	I/O(A)	53	I/O(A)	95	I/O(A)	137	GND	179	I/O(B)
12	VCC	54	I/O(A)	96	I/O(A)	138	VCCIO(B)	180	I/O(B)
13	I/O(A)	55	I/O(A)	97	I/O(A)	139	I/O(B)	181	I/O(B)
14	I/O(A)	56	VDED	98	VCCIO(A)	140	I/O(B)	182	VCC
15	I/O(A)	57	I/O(A)	99	I/O(A)	141	I/O(B)	183	TCK
16	I/O(A)	58	GND	100	I/O(A)	142	I/O(B)	184	VDED
17	I/O(A)	59	I/O(A)	101	VPUMP	143	I/O(B)	185	I/O(B)
18	I/O(A)	60	VCCIO(A)	102	I/O(A)	144	I/O(B)	186	I/O(B)
19	VCCIO(A)	61	I/O(A)	103	I/O(A)	145	I/O(B)	187	I/O(B)
20	I/O(A)	62	I/O(A)	104	GND	146	VCC	188	GND
21	GND	63	I/O(A)	105	I/O(B)	147	I/O(B)	189	VCCIO(B)
22	I/O(A)	64	I/O(A)	106	I/O(B)	148	I/O(B)	190	I/O(B)
23	TDI	65	I/O(A)	107	I/O(B)	149	I/O(B)	191	I/O(B)
24	CLK(0)	66	I/O(A)	108	GND	150	VCCIO(B)	192	I/O(B)
25	CLK(1)	67	I/O(A)	109	I/O(B)	151	I/O(B)	193	I/O(B)
26	VCC	68	I/O(A)	110	I/O(B)	152	I/O(B)	194	I/O(B)
27	I/O(A)	69	I/O(A)	111	VCCIO(B)	153	GND	195	VCC
28	I/O(A)	70	I/O(A)	112	I/O(B)	154	I/O(B)	196	I/O(B)
29	VDED	71	I/O(A)	113	VCC	155	I/O(B)	197	I/O(B)
30	I/O(A)	72	VCCIO(A)	114	I/O(B)	156	GND	198	I/O(B)
31	I/O(A)	73	I/O(A)	115	I/O(B)	157	I/O(B)	199	I/O(B)
32	I/O(A)	74	I/O(A)	116	I/O(B)	158	I/O(B)	200	I/O(B)
33	GND	75	GND	117	I/O(B)	159	I/O(B)	201	I/O(B)
34	VCCIO(A)	76	VCC	118	INREF	160	GND	202	I/O(B)
35	I/O(A)	77	I/O(A)	119	I/O(B)	161	I/O(B)	203	VCCIO(B)
36	I/O(A)	78	TRSTB	120	I/O(B)	162	VCCIO(B)	204	GND
37	I/O(A)	79	VDED	121	I/O(B)	163	I/O(B)	205	I/O(B)
38	I/O(A)	80	I/O(A)	122	VCCIO(B)	164	I/O(B)	206	I/O(B)
39	I/O(A)	81	I/O(A)	123	GND	165	VCC	207	I/O(B)
40	I/O(A)	82	I/O(A)	124	I/O(B)	166	I/O(B)	208	I/O(B)
41	I/O(A)	83	GND	125	I/O(B)	167	I/O(B)		
42	I/O(A)	84	VCCIO(A)	126	I/O(B)	168	I/O(B)		

QL8250 - 208 PQFP Pinout Diagram



QL8250 - 208 PQFP Pinout Table

Table 35: QL8250 - 208 PQFP Pinout Table

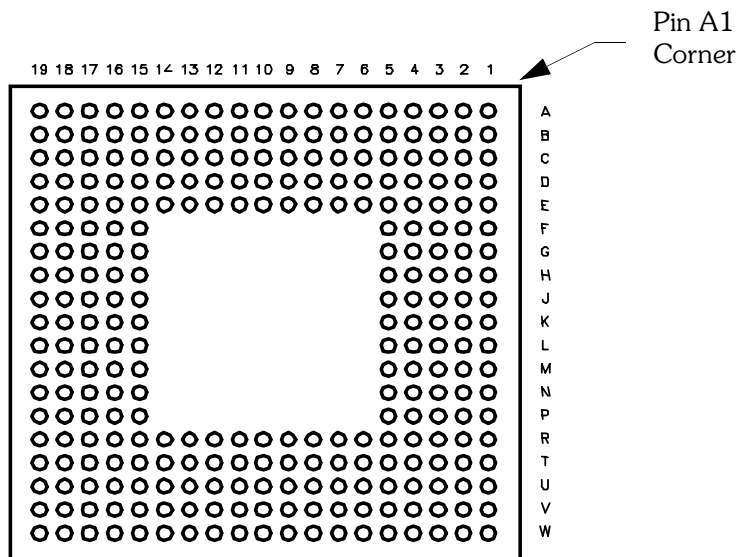
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
1	PLLST(3)	43	I/O(B)	85	I/O(D)	127	CLK(5),PLLIN(3)	169	I/O(G)
2	VCCPLL(3)	44	VCCIO(B)	86	VCC	128	CLK(6)	170	INREF(G)
3	GND	45	I/O(B)	87	I/O(D)	129	VDED	171	I/O(G)
4	GND	46	VCC	88	I/O(D)	130	CLK(7)	172	I/O(G)
5	I/O(A)	47	I/O(B)	89	VCC	131	VCC	173	I/O(G)
6	I/O(A)	48	I/O(B)	90	I/O(D)	132	CLK(8)	174	I/O(G)
7	I/O(A)	49	GND	91	I/O(D)	133	TMS	175	VCC
8	VCCIO(A)	50	TDO	92	I/O(D)	134	I/O(F)	176	I/O(G)
9	I/O(A)	51	PLLOUT(1)	93	INREF(D)	135	I/O(F)	177	VCCIO(G)
10	I/O(A)	52	GNDPLL(2)	94	I/O(D)	136	I/O(F)	178	GND
11	I/O(A)	53	GND	95	I/O(D)	137	GND	179	I/O(G)
12	VCC	54	VCCPLL(2)	96	I/O(D)	138	VCCIO(F)	180	I/O(G)
13	INREF(A)	55	PLLST(2)	97	I/O(D)	139	I/O(F)	181	I/O(G)
14	I/O(A)	56	VDED	98	VCCIO(D)	140	I/O(F)	182	VCC
15	I/O(A)	57	I/O(C)	99	I/O(D)	141	I/O(F)	183	TCK
16	I/O(A)	58	GND	100	I/O(D)	142	I/O(F)	184	VCC
17	I/O(A)	59	I/O(C)	101	VPUMP	143	I/O(F)	185	I/O(H)
18	I/O(A)	60	VCCIO(C)	102	PLLOUT(0)	144	I/O(F)	186	I/O(H)
19	VCCIO(A)	61	I/O(C)	103	GND	145	INREF(F)	187	I/O(H)
20	I/O(A)	62	I/O(C)	104	GNDPLL(1)	146	VCC	188	GND
21	GND	63	I/O(C)	105	PLLST(1)	147	I/O(F)	189	VCCIO(H)
22	I/O(A)	64	I/O(C)	106	VCCPLL(1)	148	I/O(F)	190	I/O(H)
23	TDI	65	I/O(C)	107	I/O(E)	149	I/O(F)	191	I/O(H)
24	CLK(0)	66	I/O(C)	108	GND	150	VCCIO(F)	192	I/O(H)
25	CLK(1)	67	I/O(C)	109	I/O(E)	151	I/O(F)	193	I/O(H)
26	VCC	68	INREF(C)	110	I/O(E)	152	I/O(F)	194	INREF(H)
27	CLK(2),PLLIN(2)	69	I/O(C)	111	VCCIO(E)	153	GND	195	VCC
28	CLK(3),PLLIN(1)	70	I/O(C)	112	I/O(E)	154	I/O(F)	196	I/O(H)
29	VDED	71	I/O(C)	113	VCC	155	PLLOUT(3)	197	I/O(H)
30	CLK(4),DEDCLK, PLLIN(0)	72	VCCIO(C)	114	I/O(E)	156	GNDPLL(0)	198	I/O(H)
31	I/O(B)	73	I/O(C)	115	I/O(E)	157	GND	199	I/O(H)
32	I/O(B)	74	I/O(C)	116	I/O(E)	158	VCCPLL(0)	200	I/O(H)
33	GND	75	GND	117	I/O(E)	159	PLLST(0)	201	I/O(H)
34	VCCIO(B)	76	VCC	118	INREF(E)	160	GND	202	I/O(H)
35	I/O(B)	77	I/O(C)	119	I/O(E)	161	I/O(G)	203	VCCIO(H)
36	I/O(B)	78	TRSTB	120	I/O(E)	162	VCCIO(G)	204	GND
37	I/O(B)	79	VCC	121	I/O(E)	163	I/O(G)	205	I/O(H)
38	I/O(B)	80	I/O(D)	122	VCCIO(E)	164	I/O(G)	206	PLLOUT(2)
39	I/O(B)	81	I/O(D)	123	GND	165	VCC	207	GND
40	INREF(B)	82	I/O(D)	124	I/O(E)	166	I/O(G)	208	GNDPLL(3)
41	I/O(B)	83	GND	125	I/O(E)	167	I/O(G)		
42	I/O(B)	84	VCCIO(D)	126	I/O(E)	168	I/O(G)		

QL8250 - 280 LF-PBGA Pinout Diagram

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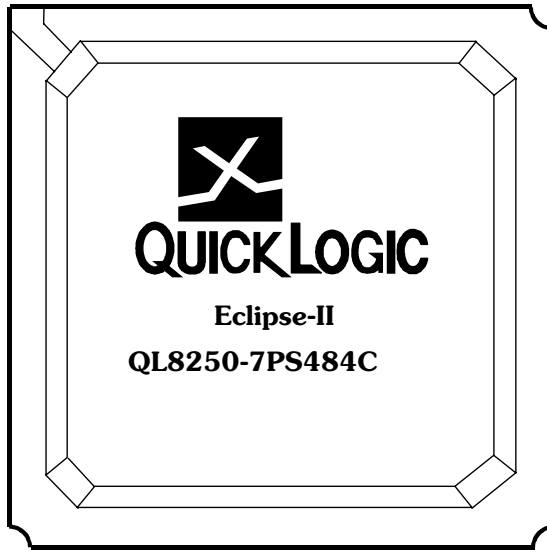
QL8250 - 280 LF-PBGA Pinout Table

Table 36: QL8250 - 280 LF-PBGA Pinout Table

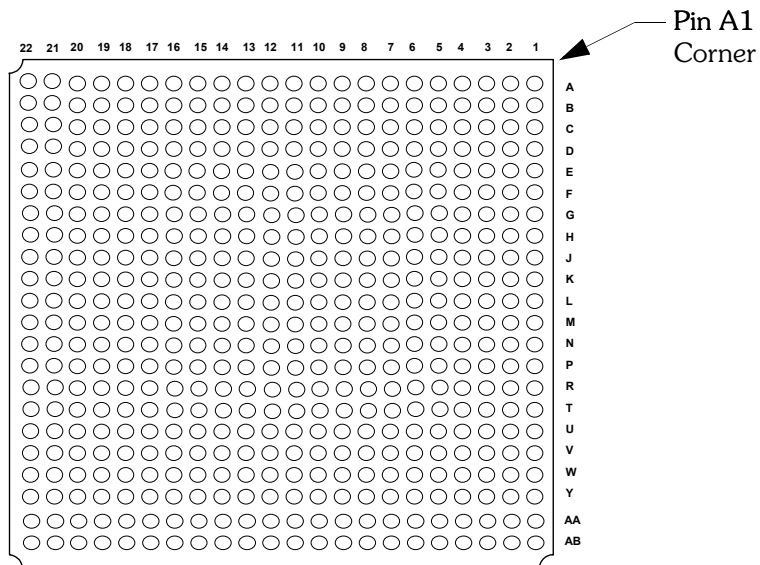
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	PLLOUT(3)	C10	CLK(5) /PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	VCCIO(E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	VCCIO(B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	VCC	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	VCC	U17	TDO
A6	IOCTRL(F)	C15	VCCIO(E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLRST(2)
A7	I/O(F)	C16	I/O(E)	F15	VCC	L3	VCCIO(H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	VCC	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	VCC	R12	VCC	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	VCC	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	VDED	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	VCCIO(C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	VCCIO(C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	VCC	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	VCC	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLRST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4) DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	VCC	T3	I/O(A)	V12	I/O(B)
B1	PLLRST(0)	D10	I/O(E)	G18	I/O(D)	M15	VDED	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	VCC	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	VCC	N3	I/O(H)	T11	CLK(3) /PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	VCC	N4	I/O(H)	T12	I/O(B)	W2	PLLRST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	VCC	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	VCC	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	VCCIO(G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	VCCPLL(2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	VCCIO(G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	VCC	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	VCCPLL(1)	E7	VCC	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	VDED	J15	VCC	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	VCC	J16	I/O(C)	P4	INREF(H)	U3	VCCPLL(3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	VCCIO(D)	P5	VCC	U4	I/O(A)	W13	I/O(B)
C2	VCCPLL(0)	E11	GND	J18	I/O(D)	P15	GND	U5	VCCIO(A)	W14	IOCTRL(B)
C3	I/O(F)	E12	VCC	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	VCC	K1	VCC	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	VCCIO(F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	VPUMP	K3	I/O(G)	P19	I/O(C)	U9	VCCIO(A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	VCCIO(D)	K5	GND	R2	I/O(H)	U11	VCCIO(B)		
C9	VCCIO(F)	E18	INREF(D)	K15	GND	R3	VCCIO(H)	U12	I/O(B)		

QL8250 - 484 PBGA Pinout Diagram

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QL8250 - 484 PBGA Pinout Table

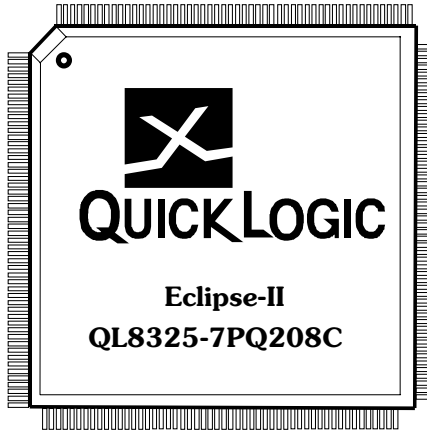
Table 37: QL8250 - 484 PBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	NC	C1	NC	E1	IOCTRL(A)	G1	NC	J1	I/O(A)	L1	CLK(4), DEDCLK, PLLIN(0)
A2	PLLST(3)	C2	I/O(A)	E2	I/O(A)	G2	NC	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	VCCPLL(3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2),PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	NC	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	NC	C6	NC	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	NC	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	NC	E8	I/O(H)	G8	I/O(H)	J8	VCC	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	NC	C10	NC	E10	I/O(H)	G10	NC	J10	VCC	L10	GND
A11	NC	C11	I/O(H)	E11	VCC	G11	I/O(G)	J11	VCC	L11	GND
A12	TCK	C12	NC	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	NC	J13	VCC	L13	GND
A14	I/O(G)	C14	NC	E14	NC	G14	NC	J14	GND	L14	VCC
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	VCC	L15	VCC
A16	NC	C16	I/O(G)	E16	I/O(G)	G16	VPUMP	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	NC	E17	INREF(G)	G17	VCCIO(F)	J17	VCCIO(F)	L17	VCCIO(F)
A18	I/O(G)	C18	I/O(G)	E18	NC	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	NC	G21	INREF(F)	J21	I/O(F)	L21	NC
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	NC	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3),PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	NC
B6	I/O(H)	D6	I/O(H)	F6	VCCIO(A)	H6	VCCIO(A)	K6	VCCIO(A)	M6	VCCIO(B)
B7	I/O(H)	D7	NC	F7	VCCIO(H)	H7	I/O(H)	K7	NC	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	VCC	M8	VCC
B9	I/O(H)	D9	NC	F9	VCCIO(H)	H9	VCC	K9	VCC	M9	VCC
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	VCC	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	VCCIO(H)	H11	VDED	K11	GND	M11	GND
B12	NC	D12	I/O(G)	F12	VCCIO(G)	H12	GND	K12	GND	M12	GND
B13	NC	D13	I/O(G)	F13	I/O(G)	H13	VCC	K13	GND	M13	GND
B14	NC	D14	I/O(G)	F14	VCCIO(G)	H14	VCC	K14	VCC	M14	GND
B15	NC	D15	IOCTRL(G)	F15	NC	H15	GND	K15	VCC	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	VCCIO(G)	H16	I/O(F)	K16	NC	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	NC	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	NC	K18	I/O(F)	M18	I/O(E)
B19	PLLST(0)	D19	VCCPLL(0)	F19	I/O(F)	H19	I/O(F)	K19	NC	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5),PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	NC	K22	NC	M22	TMS

Table 37: QL8250 - 484 PBGA Pinout Table (Continued)

Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
N1	NC	P16	I/O(E)	T9	NC	V2	I/O(B)	W17	NC	AA10	I/O(C)
N2	I/O(B)	P17	NC	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	NC	AA12	I/O(D)
N4	NC	P19	NC	T12	NC	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	NC	W21	NC	AA14	I/O(D)
N6	NC	P21	I/O(E)	T14	NC	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	NC	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	NC
N8	VCC	R1	I/O(B)	T16	GND	V9	NC	Y2	I/O(B)	AA17	NC
N9	VCC	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	VCCPLL(2)	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	NC	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	NC	V12	VCC	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	NC	V13	NC	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	NC	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	VCC	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	VCC	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	VCC	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLL(2)
N17	VCCIO(E)	R10	VCC	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	NC	AB5	I/O(B)
N19	I/O(E)	R12	VDED	U5	I/O(B)	V20	I/O(E)	Y13	NC	AB6	I/O(C)
N20	I/O(E)	R13	VCC	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	VCC	U7	VCCIO(C)	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	NC	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	NC	R16	I/O(D)	U9	VCCIO(C)	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	VCCIO(E)	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	NC
P3	I/O(B)	R18	I/O(E)	U11	VCCIO(C)	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	VCCIO(D)	W5	I/O(B)	Y20	PLL(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	NC
P6	VCCIO(B)	R21	I/O(E)	U14	VCCIO(D)	W7	NC	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	NC	W8	NC	AA1	TDO	AB16	IOCTRL(D)
P8	VCC	T1	I/O(B)	U16	VCCIO(D)	W9	NC	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	VCCIO(E)	W10	NC	AA3	GND	AB18	I/O(D)
P10	VCC	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	NC	AA5	I/O(C)	AB20	GND
P12	VCC	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	VCCPLL(1)
P13	VCC	T6	VCCIO(B)	U21	NC	W14	NC	AA7	NC	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	VDED	T8	I/O(C)	V1	I/O(B)	W16	NC	AA9	NC		

QL8325 - 208 PQFP Pinout Diagram



QL8325 - 208 PQFP Pinout Table

Table 38: QL8325 - 208 PQFP Pinout Table

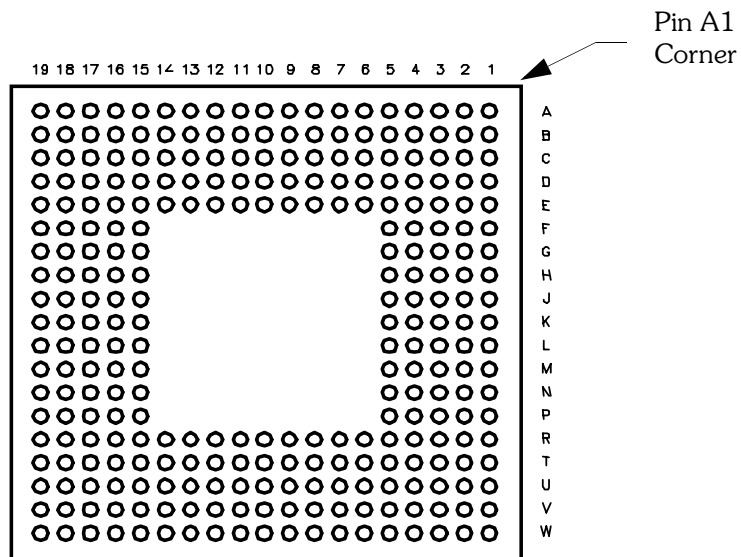
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
1	PLLST(3)	43	I/O(B)	85	I/O(D)	127	CLK(5),PLLIN(3)	169	I/O(G)
2	VCCPLL(3)	44	VCCIO(B)	86	VCC	128	CLK(6)	170	INREF(G)
3	GND	45	I/O(B)	87	I/O(D)	129	VDED	171	I/O(G)
4	GND	46	VCC	88	I/O(D)	130	CLK(7)	172	I/O(G)
5	I/O(A)	47	I/O(B)	89	VCC	131	VCC	173	I/O(G)
6	I/O(A)	48	I/O(B)	90	I/O(D)	132	CLK(8)	174	I/O(G)
7	I/O(A)	49	GND	91	I/O(D)	133	TMS	175	VCC
8	VCCIO(A)	50	TDO	92	I/O(D)	134	I/O(F)	176	I/O(G)
9	I/O(A)	51	PLLOUT(1)	93	INREF(D)	135	I/O(F)	177	VCCIO(G)
10	I/O(A)	52	GNDPLL(2)	94	I/O(D)	136	I/O(F)	178	GND
11	I/O(A)	53	GND	95	I/O(D)	137	GND	179	I/O(G)
12	VCC	54	VCCPLL(2)	96	I/O(D)	138	VCCIO(F)	180	I/O(G)
13	INREF(A)	55	PLLST(2)	97	I/O(D)	139	I/O(F)	181	I/O(G)
14	I/O(A)	56	VDED	98	VCCIO(D)	140	I/O(F)	182	VCC
15	I/O(A)	57	I/O(C)	99	I/O(D)	141	I/O(F)	183	TCK
16	I/O(A)	58	GND	100	I/O(D)	142	I/O(F)	184	VCC
17	I/O(A)	59	I/O(C)	101	VPUMP	143	I/O(F)	185	I/O(H)
18	I/O(A)	60	VCCIO(C)	102	PLLOUT(0)	144	I/O(F)	186	I/O(H)
19	VCCIO(A)	61	I/O(C)	103	GND	145	INREF(F)	187	I/O(H)
20	I/O(A)	62	I/O(C)	104	GNDPLL(1)	146	VCC	188	GND
21	GND	63	I/O(C)	105	PLLST(1)	147	I/O(F)	189	VCCIO(H)
22	I/O(A)	64	I/O(C)	106	VCCPLL(1)	148	I/O(F)	190	I/O(H)
23	TDI	65	I/O(C)	107	I/O(E)	149	I/O(F)	191	I/O(H)
24	CLK(0)	66	I/O(C)	108	GND	150	VCCIO(F)	192	I/O(H)
25	CLK(1)	67	I/O(C)	109	I/O(E)	151	I/O(F)	193	I/O(H)
26	VCC	68	INREF(C)	110	I/O(E)	152	I/O(F)	194	INREF(H)
27	CLK(2),PLLIN(2)	69	I/O(C)	111	VCCIO(E)	153	GND	195	VCC
28	CLK(3),PLLIN(1)	70	I/O(C)	112	I/O(E)	154	I/O(F)	196	I/O(H)
29	VDED	71	I/O(C)	113	VCC	155	PLLOUT(3)	197	I/O(H)
30	CLK(4),DEDCLK, PLLIN(0)	72	VCCIO(C)	114	I/O(E)	156	GNDPLL(0)	198	I/O(H)
31	I/O(B)	73	I/O(C)	115	I/O(E)	157	GND	199	I/O(H)
32	I/O(B)	74	I/O(C)	116	I/O(E)	158	VCCPLL(0)	200	I/O(H)
33	GND	75	GND	117	I/O(E)	159	PLLST(0)	201	I/O(H)
34	VCCIO(B)	76	VCC	118	INREF(E)	160	GND	202	I/O(H)
35	I/O(B)	77	I/O(C)	119	I/O(E)	161	I/O(G)	203	VCCIO(H)
36	I/O(B)	78	TRSTB	120	I/O(E)	162	VCCIO(G)	204	GND
37	I/O(B)	79	VCC	121	I/O(E)	163	I/O(G)	205	I/O(H)
38	I/O(B)	80	I/O(D)	122	VCCIO(E)	164	I/O(G)	206	PLLOUT(2)
39	I/O(B)	81	I/O(D)	123	GND	165	VCC	207	GND
40	INREF(B)	82	I/O(D)	124	I/O(E)	166	I/O(G)	208	GNDPLL(3)
41	I/O(B)	83	GND	125	I/O(E)	167	I/O(G)		
42	I/O(B)	84	VCCIO(D)	126	I/O(E)	168	I/O(G)		

QL8325 - 280 LF-PBGA Pinout Diagram

Top



Bottom



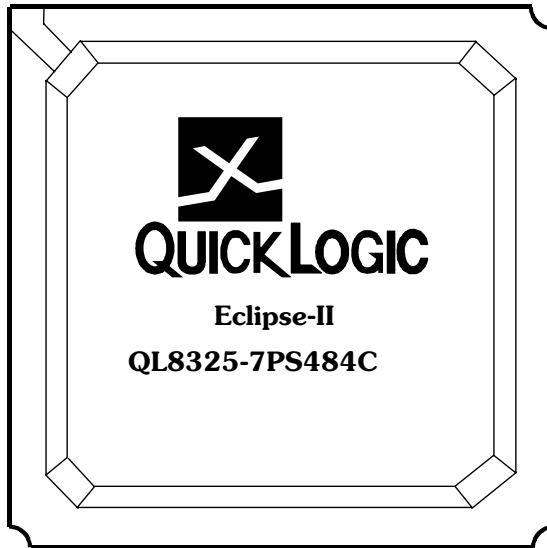
QL8325 - 280 LF-PBGA Pinout Table

Table 39: QL8325 - 280 LF-PBGA Pinout Table

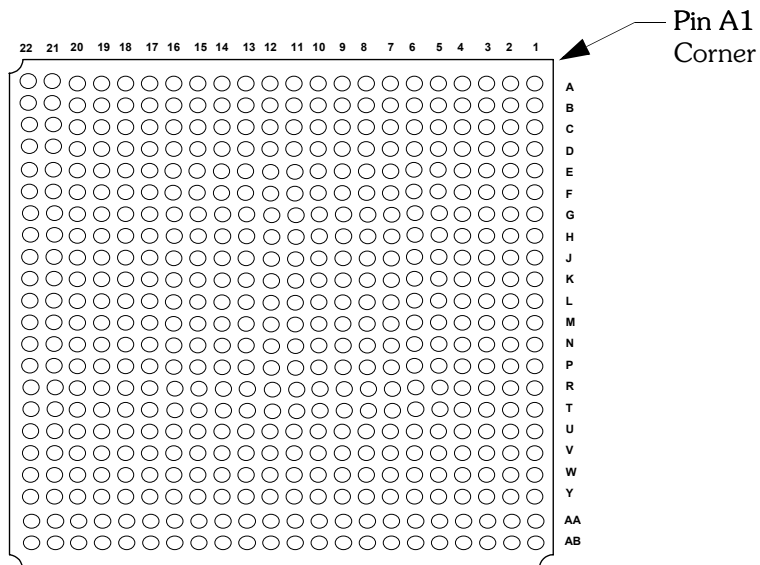
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	PLLOUT(3)	C10	CLK(5) /PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	VCCIO(E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	VCCIO(B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	VCC	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	VCC	U17	TDO
A6	IOCTRL(F)	C15	VCCIO(E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLRST(2)
A7	I/O(F)	C16	I/O(E)	F15	VCC	L3	VCCIO(H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	VCC	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	VCC	R12	VCC	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	VCC	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	VDED	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	VCCIO(C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	VCCIO(C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	VCC	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	VCC	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLRST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4) DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	VCC	T3	I/O(A)	V12	I/O(B)
B1	PLLRST(0)	D10	I/O(E)	G18	I/O(D)	M15	VDED	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	VCC	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	VCC	N3	I/O(H)	T11	CLK(3) /PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	VCC	N4	I/O(H)	T12	I/O(B)	W2	PLLRST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	VCC	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	VCC	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	VCCIO(G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	VCCPLL(2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	VCCIO(G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	VCC	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	VCCPLL(1)	E7	VCC	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	VDED	J15	VCC	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	VCC	J16	I/O(C)	P4	INREF(H)	U3	VCCPLL(3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	VCCIO(D)	P5	VCC	U4	I/O(A)	W13	I/O(B)
C2	VCCPLL(0)	E11	GND	J18	I/O(D)	P15	GND	U5	VCCIO(A)	W14	IOCTRL(B)
C3	I/O(F)	E12	VCC	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	VCC	K1	VCC	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	VCCIO(F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	VPUMP	K3	I/O(G)	P19	I/O(C)	U9	VCCIO(A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	VCCIO(D)	K5	GND	R2	I/O(H)	U11	VCCIO(B)		
C9	VCCIO(F)	E18	INREF(D)	K15	GND	R3	VCCIO(H)	U12	I/O(B)		

QL8325 - 484 PBGA Pinout Diagram

Top



Bottom



QL8325 - 484 PBGA Pinout Table

Table 40: QL8325 - 484 PBGA Pinout Table

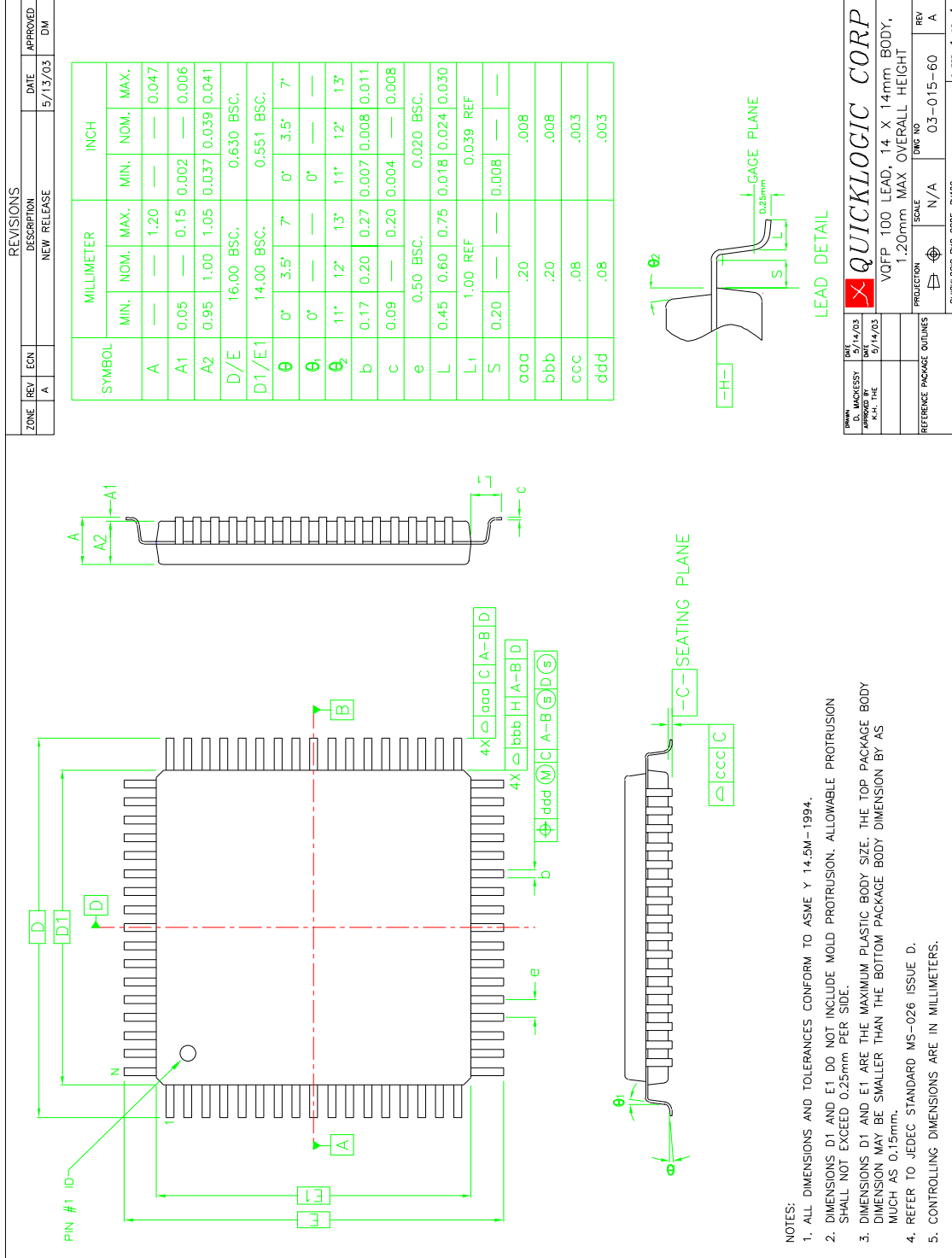
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	I/O(A)	C1	I/O(A)	E1	IOCTRL(A)	G1	I/O(A)	J1	I/O(A)	L1	CLK(4) DEDCLK/ PLLIN(0)
A2	PLLRST(3)	C2	I/O(A)	E2	I/O(A)	G2	I/O(A)	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	VCCPLL(3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/ PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	I/O(A)	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	I/O(H)	C6	I/O(H)	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	N/C	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	I/O(H)	E8	I/O(H)	G8	I/O(H)	J8	VCC	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	N/C	C10	I/O(H)	E10	I/O(H)	G10	I/O(H)	J10	VCC	L10	GND
A11	N/C	C11	I/O(H)	E11	VCC	G11	I/O(G)	J11	VCC	L11	GND
A12	TCK	C12	I/O(H)	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	I/O(G)	J13	VCC	L13	GND
A14	I/O(G)	C14	I/O(G)	E14	I/O(G)	G14	I/O(G)	J14	GND	L14	VCC
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	VCC	L15	VCC
A16	I/O(G)	C16	I/O(G)	E16	I/O(G)	G16	VPUMP	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	I/O(G)	E17	INREF(G)	G17	VCCIO(F)	J17	VCCIO(F)	L17	VCCIO(F)
A18	I/O(G)	C18	I/O(G)	E18	I/O(G)	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	I/O(F)	G21	INREF(F)	J21	I/O(F)	L21	I/O(F)
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	I/O(A)	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/ PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	I/O(B)
B6	I/O(H)	D6	I/O(H)	F6	VCCIO(A)	H6	VCCIO(A)	K6	VCCIO(A)	M6	VCCIO(B)
B7	I/O(H)	D7	I/O(H)	F7	VCCIO(H)	H7	I/O(H)	K7	I/O(A)	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	VCC	M8	VCC
B9	I/O(H)	D9	I/O(H)	F9	VCCIO(H)	H9	VCC	K9	VCC	M9	VCC
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	VCC	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	VCCIO(H)	H11	VDED	K11	GND	M11	GND
B12	N/C	D12	I/O(G)	F12	VCCIO(G)	H12	GND	K12	GND	M12	GND
B13	N/C	D13	I/O(G)	F13	I/O(G)	H13	VCC	K13	GND	M13	GND
B14	N/C	D14	I/O(G)	F14	VCCIO(G)	H14	VCC	K14	VCC	M14	GND
B15	I/O(G)	D15	IOCTRL(G)	F15	N/C	H15	GND	K15	VCC	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	VCCIO(G)	H16	I/O(F)	K16	I/O(F)	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	N/C	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	I/O(F)	K18	I/O(F)	M18	I/O(E)
B19	PLLRST(0)	D19	VCCPLL(0)	F19	I/O(F)	H19	I/O(F)	K19	I/O(F)	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/ PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	I/O(F)	K22	I/O(F)	M22	TMS

Table 40: QL8325 - 484 PBGA Pinout Table (Continued)

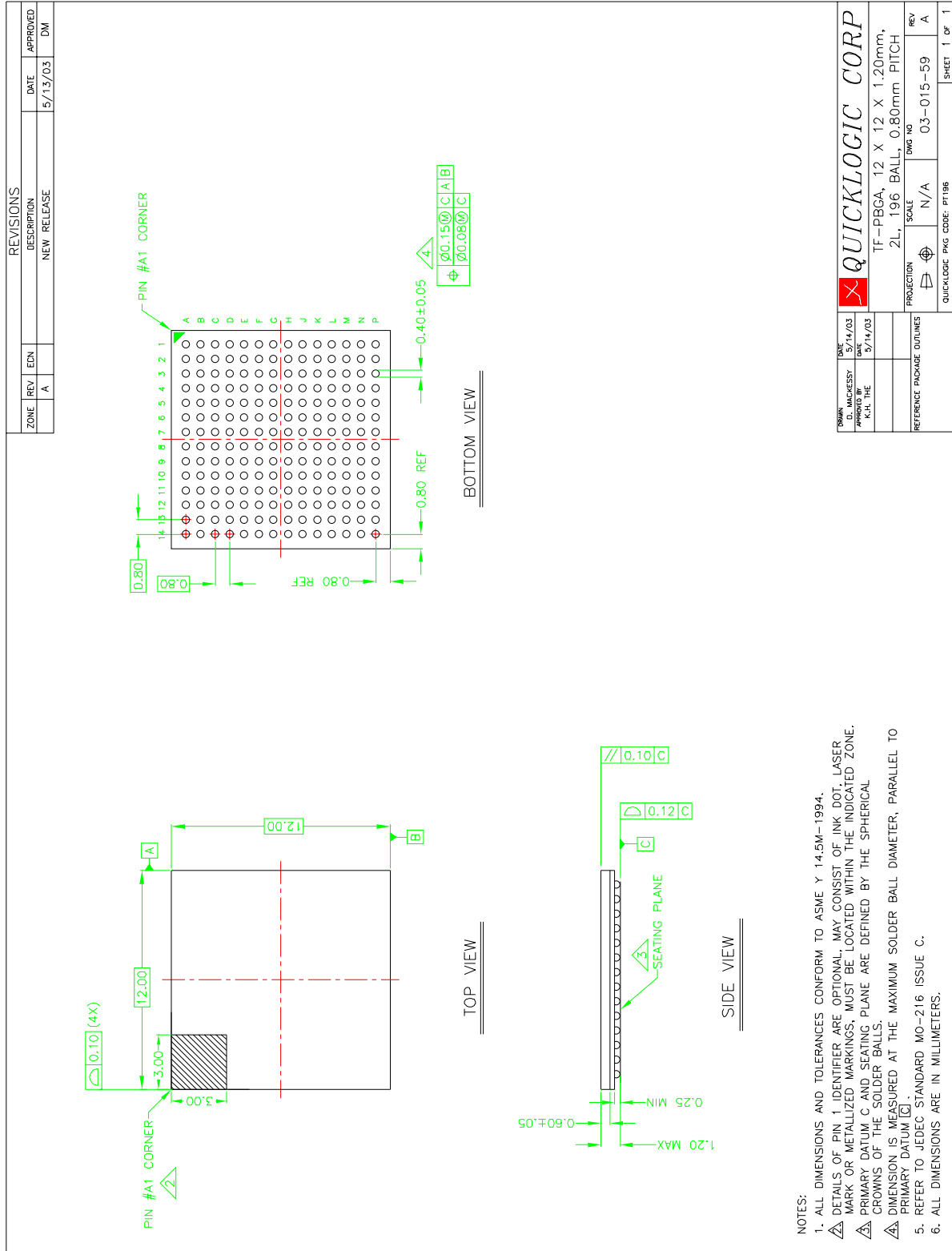
Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function	Ball	Function
N1	I/O(B)	P16	I/O(E)	T9	N/C	V2	I/O(B)	W17	I/O(D)	AA10	I/O(C)
N2	I/O(B)	P17	I/O(E)	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	I/O(E)	AA12	I/O(D)
N4	I/O(B)	P19	I/O(E)	T12	N/C	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	I/O(C)	W21	I/O(E)	AA14	I/O(D)
N6	I/O(B)	P21	I/O(E)	T14	N/C	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	I/O(B)	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	I/O(D)
N8	VCC	R1	I/O(B)	T16	GND	V9	N/C	Y2	I/O(B)	AA17	I/O(D)
N9	VCC	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	VCCPLL(2)	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	I/O(C)	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	I/O(E)	V12	VCC	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	I/O(E)	V13	N/C	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	I/O(B)	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	VCC	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	VCC	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	VCC	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLL(2)
N17	VCCIO(E)	R10	VCC	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	I/O(D)	AB5	I/O(B)
N19	I/O(E)	R12	VDED	U5	I/O(B)	V20	I/O(E)	Y13	I/O(D)	AB6	I/O(C)
N20	I/O(E)	R13	VCC	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	VCC	U7	VCCIO(C)	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	N/C	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	I/O(B)	R16	I/O(D)	U9	VCCIO(C)	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	VCCIO(E)	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	I/O(C)
P3	I/O(B)	R18	I/O(E)	U11	VCCIO(C)	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	VCCIO(D)	W5	I/O(B)	Y20	PLL(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	I/O(D)
P6	VCCIO(B)	R21	I/O(E)	U14	VCCIO(D)	W7	N/C	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	N/C	W8	I/O(C)	AA1	TDO	AB16	IOCTRL(D)
P8	VCC	T1	I/O(B)	U16	VCCIO(D)	W9	I/O(C)	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	VCCIO(E)	W10	I/O(C)	AA3	GND	AB18	I/O(D)
P10	VCC	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	I/O(D)	AA5	I/O(C)	AB20	GND
P12	VCC	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	VCCPLL(1)
P13	VCC	T6	VCCIO(B)	U21	I/O(E)	W14	I/O(D)	AA7	I/O(C)	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	VDED	T8	I/O(C)	V1	I/O(B)	W16	N/C	AA9	I/O(C)		

Package Mechanical Drawings

100 VQFP Packaging Drawing



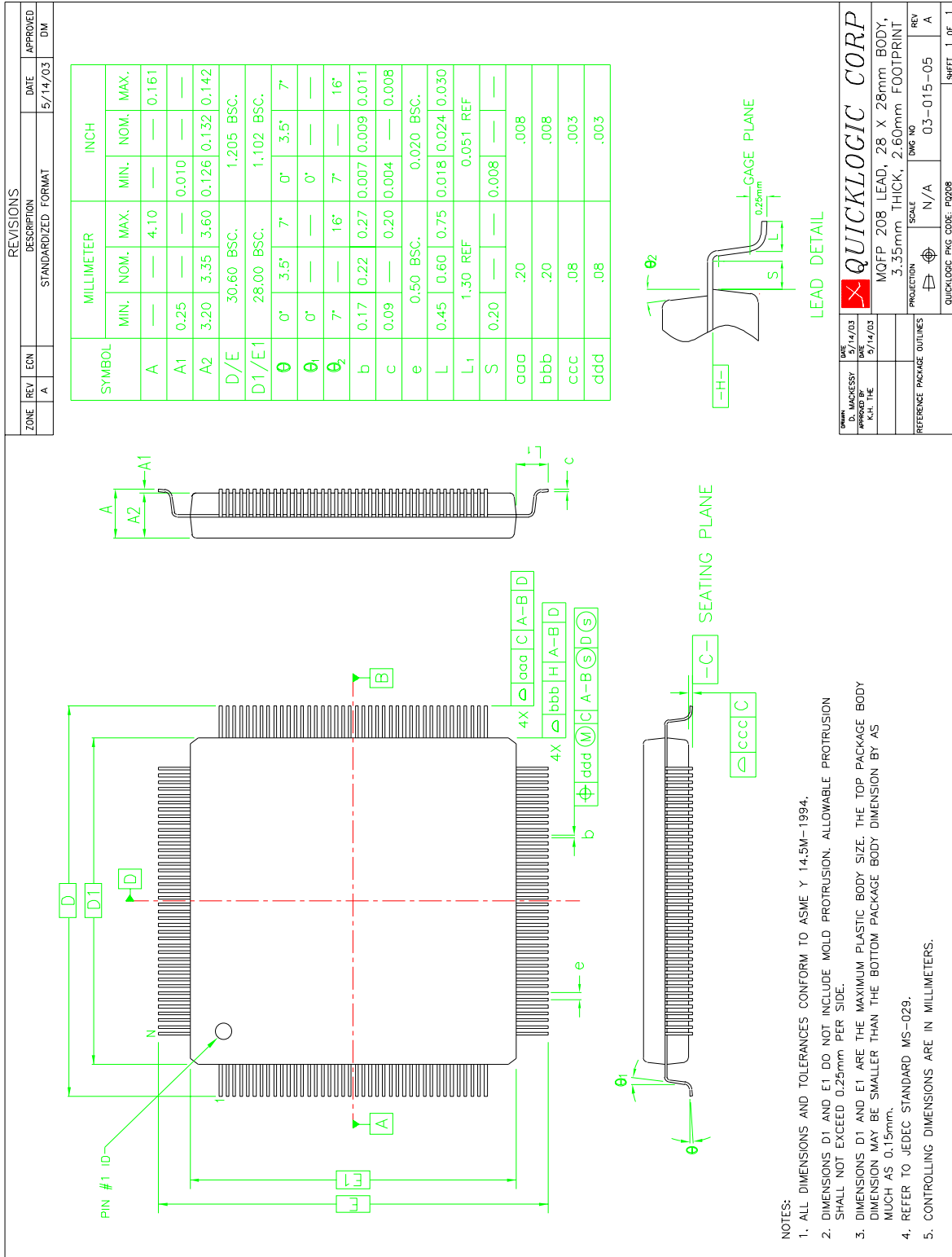
196 TF-PBGA Packaging Drawing



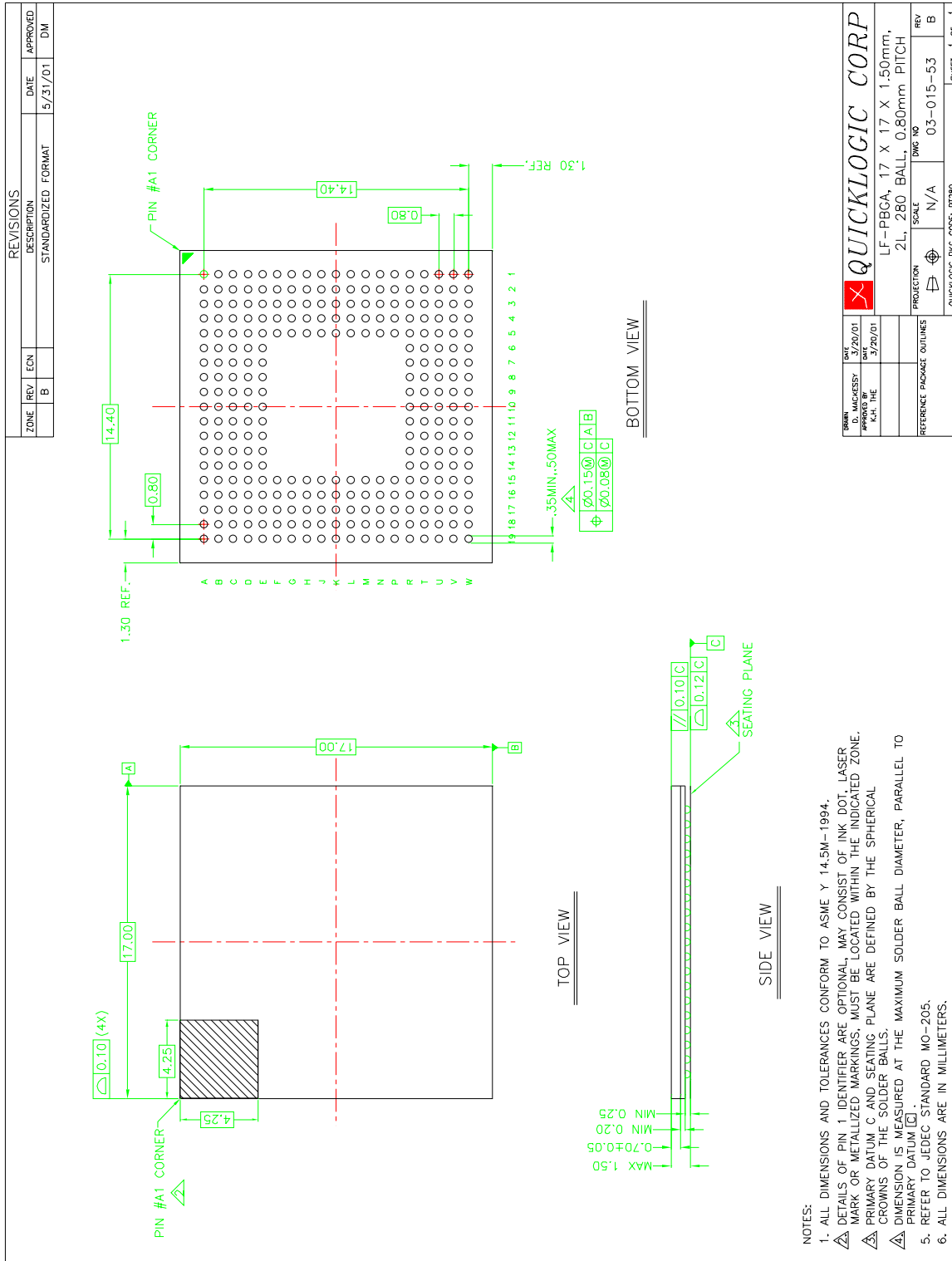
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, MAY CONSIST OF INK DOT, LASER MARK OR METALLIZED MARKINGS, MUST BE LOCATED WITHIN THE INDICATED ZONE.
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. REFER TO JEDEC STANDARD MO-216 ISSUE C.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

208 PQFP Packaging Drawing



280 LF-PBGA Packaging Drawing



- NOTES:
- ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994.
 - DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, MAY CONSIST OF INK DOT, LASER MARK OR METALLIZED MARKINGS, MUST BE LOCATED WITHIN THE INDICATED ZONE.
 - PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 - DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
 - REFER TO JEDEC STANDARD MO-205.
 - ALL DIMENSIONS ARE IN MILLIMETERS.

Packaging Information

The Eclipse-II product family packaging information is presented in **Table 41**.

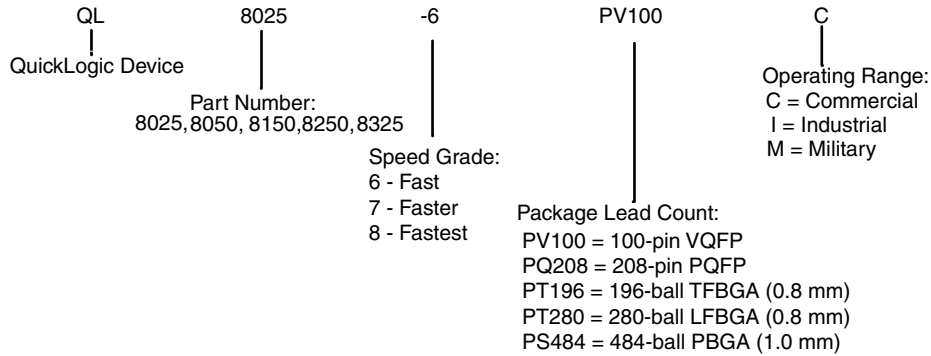
NOTE: Military temperature range plastic packages will be added as follow on products to the commercial and industrial products.

Table 41: Packaging Options

Device Information	Device									
	QL8325		QL8250		QL8150		QL8050		QL8025	
	Pin	Pitch	Pin	Pitch	Pin	Pitch	Pin	Pitch	Pin	Pitch
Package Definitions ^a	280 LFBGA	0.80 mm	280 LFBGA	0.80 mm	-	-	100 VQFP	0.50 mm	100 VQFP	0.50 mm
	484 BGA	1.0 mm	484 BGA	1.0 mm	208 PQFP	0.50 mm	196 TFBGA	0.80 mm	196 TFBGA	0.80 mm
	208 PQFP	0.50 mm	208 PQFP	0.50 mm	196 TFBGA	0.80 mm	-	-	-	-

- a. PQFP = Plastic Quad Flat Pack
 BGA = Ball Grid Array
 VQFP = Very Thin Quad Flat Pack
 TFBGA = Thin Fine Pitch Ball Grid Array
 LFBGA = Low Profile Fine Pitch Ball Grid Array

Ordering Information



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Revision History

Revision	Date	Comments
A Preliminary	August 2002	Brian Faith, Judd Heape, Andreea Rotaru
Rev A	December 2002	Brian Faith, Andreea Rotaru
Rev B	January 2003	Brian Faith, Andreea Rotaru
Rev C	May 2003	Brian Faith, Kathleen Murchek

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