DATA SHEET

PCK2002P
140 MHz PCI-X clock buffer

Product data

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File under Integrated Circuits ICL03

Philips
Semiconductors

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140 MHz PCI-X clock buffer PCK2002P

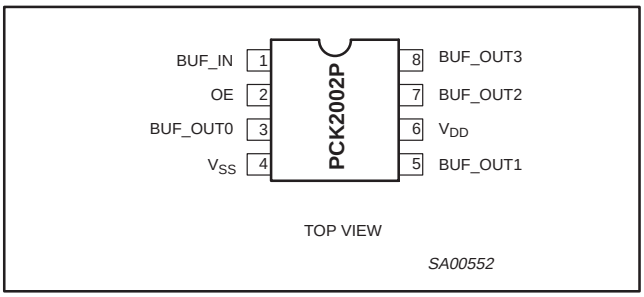
FEATURES

- General purpose and PCI-X 1:4 clock buffer
- 8-pin TSSOP package
- See PCK2001 for 48-pin 1:18 buffer part
- See PCK2001M for 28-pin 1:10 buffer part
- See PCK2001R for 16-pin 1:6 buffer part
- Operating frequency: 0 – 140 MHz
- Part-to-part skew < 500 ps
- Low output skew: <200 ps
- 3.3 V operation
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.

DESCRIPTION

The PCK2002PL is a 1–4 fanout buffer used as a high-performance, low skew, general purpose and PCI-X clock buffer. It distributes one input clock (BUF_IN) signal to four output clocks (BUF_OUT_n).

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	I/O TYPE	SYMBOL	FUNCTION
1	Input	BUF_IN	Buffered clock input
3, 5, 7, 8	Output	BUF_OUT (0–3)	Buffered clock outputs
6	Input	V_{DD}	3.3 V supply
2	Input	OE	Output Enable
4	Input	V_{SS}	Ground

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay BUF_IN to BUF_OUT_n	V_{CC} = 3.3 V, C_L = 25 pF	2.9 2.8	ns
t_r	Rise time	V_{CC} = 3.3 V, C_L = 25 pF, 0.2V_{DD} to 0.6V_{DD}	800	ps
t_f	Fall time	V_{CC} = 3.3 V, C_L = 25 pF, 0.6V_{DD} to 0.2V_{DD}	600	ps
I_{CC}	Total supply current	V_{CC} = 3.6 V	50	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
8-Pin Plastic TSSOP	–40 to +85 °C	PCK2002PDP	SOT505-1
8-Pin Plastic SO	–40 to +85 °C	PCK2002PD	SOT96-1

FUNCTION TABLE

OE	BUF_IN	BUF_OUTn
L	X	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to V_{SS} (V_{SS} = 0 V).

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC 3.3 V supply voltage		–0.5	+4.3	V
I_{IK}	DC input diode current	V_I < 0	—	–50	mA
V_I	DC input voltage	Note 2	–0.5	V_{DD} + 0.5	V
I_{OK}	DC output diode current	$V_O > V_{DD}$ or V_O < 0	—	±50	mA
V_O	DC output voltage	Note 2	–0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current	$V_O \geq 0$ to V_{DD}	—	±50	mA
T_{stg}	Storage temperature range		–65	+150	°C
P_{tot}	Power dissipation per package plastic medium-shrink SO (SSOP)	For temperature range: 0 to +70 °C above +55 °C derate linearly with 11.3 mW/K	—	850	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC 3.3V supply voltage		3.0	3.6	V
C_L	Capacitive load		20	30	pF
V_I	DC input voltage range		0	V_{DD}	V
V_O	DC output voltage range		0	V_{DD}	V
T_{amb}	Operating ambient temperature range in free air		–40	+85	°C

DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS		UNIT
					T_{amb} = –40 to +85 °C		
		V_{DD} (V)	OTHER		MIN	MAX	
V_{IH}	HIGH level input voltage	3.0 to 3.6	—	—	2.0	V_{DD} + 0.3	V
V_{IL}	LOW level input voltage	3.0 to 3.6	—	—	V_{SS} – 0.3	0.8	V
V_{OH}	Output HIGH voltage	3.0 to 3.6	I_{OH} = –1 mA	—	V_{DD} – 0.2	—	V
		3.0	I_{OH} = –24 mA	—	2.0	—	V
		3.0	I_{OH} = –12 mA	—	2.4	—	V
V_{OL}	Output LOW voltage	3.0 to 3.6	I_{OL}= 1 mA	—	—	0.2	V
		3.0	I_{OL}= 24 mA	—	—	0.8	V
		3.0	I_{OL}= 12 mA	—	—	0.55	V
I_{OH}	Output HIGH current	3.0	V_{OUT} = 1 V	—	–50	—	mA
		3.3	V_{OUT} = 1.65 V	—	—	–150	mA
I_{OL}	Output LOW current	3.0	V_{OUT} = 2.0 V	—	60	—	mA
		3.3	V_{OUT} = 1.65 V	—	—	150	mA
$\pm I_I$	Input leakage current	3.6	V_I = V_{DD} or GND	—	—	±5	µA
I_{CC}	Quiescent supply current	3.6	V_I = V_{DD} or GND	I_O = 0	—	100	µA

AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = –40 to +85 °C			UNIT
			NOTES	MIN	TYP[6]	MAX	
T_H	CLK HIGH time	66 MHz	2	6.0	—	—	ns
T_L	CLK LOW time		3	6.0	—	—	ns
T_H	CLK HIGH time	140 MHz	2	2.9	—	—	ns
T_L	CLK LOW time		3	3.0	—	—	ns
T_R	Output rise slew rate		4	1.4	1.7	4.0	V/ns
T_F	Output fall slew rate		4	1.5	2.2	4.0	V/ns
T_{PLH}	Buffer LH propagation delay		5	1.8	2.9	3.4	ns
T_{PHL}	Buffer HL propagation delay		5	1.8	2.8	3.4	ns
T_{SKW}	Bus CLK skew		1	—	—	200	ps
T_{DDSKW}	Device to device skew		1	—	—	500	ps

NOTES:
1. CLK skew is only valid for equal loading of all outputs.
2. T_H is measured at 0.5 V_{DD} as shown in Figure 2.
3. T_L is measured at 0.35 V_{DD} as shown in Figure 2.
4. T_R and T_F are measured as a transition through the threshold region 0.2 V_{DD} to 0.6 V_{DD} and 0.6 V_{DD} to 0.2 V_{DD}.
5. Input edge rate for these tests must be faster than 1 V/ns.
6. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC WAVEFORMS

V_M = 50% V_{DD}
C_L = 25 pF
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

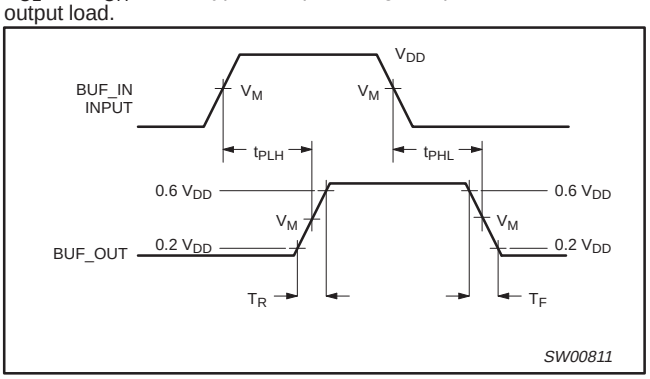


Figure 1. Load circuitry for switching times.

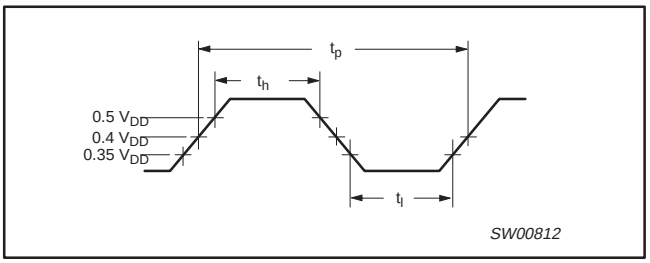


Figure 2. Buffer Output clock

TEST CIRCUIT

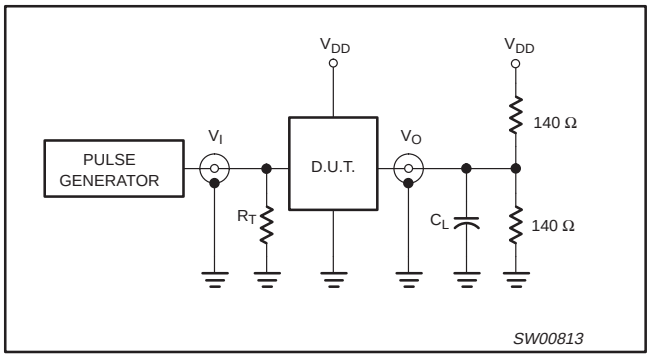
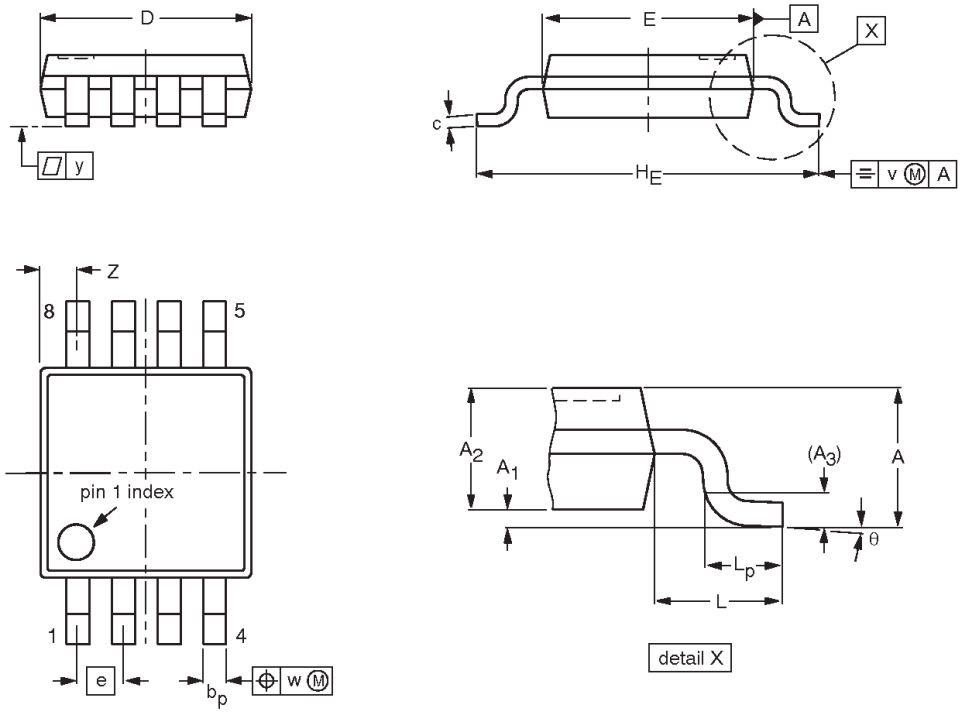
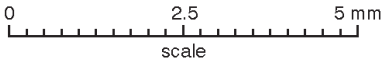


Figure 3. Load circuitry for switching times

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

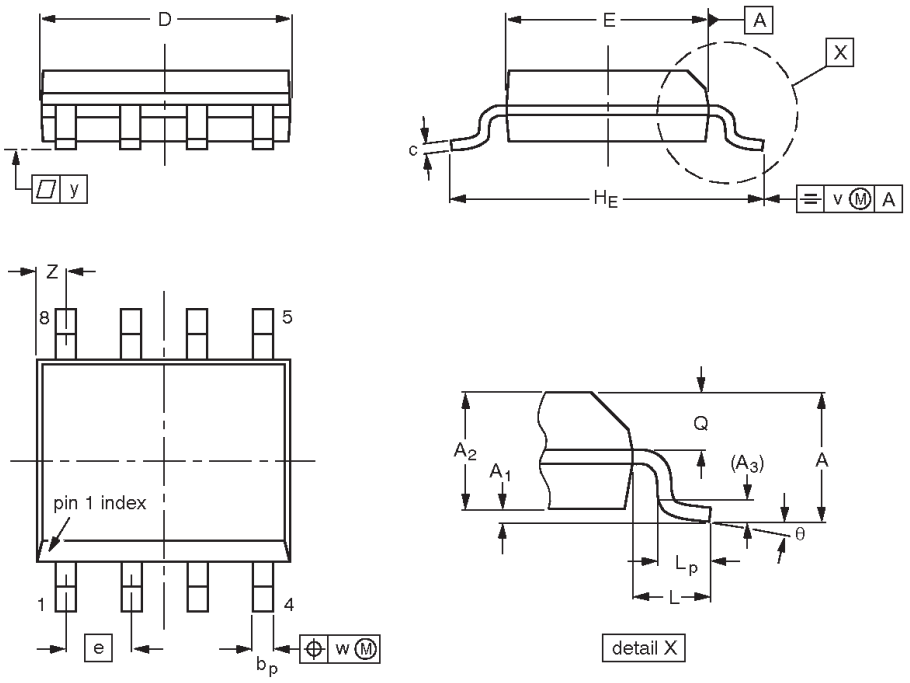
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

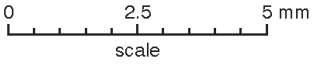
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

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2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

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Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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