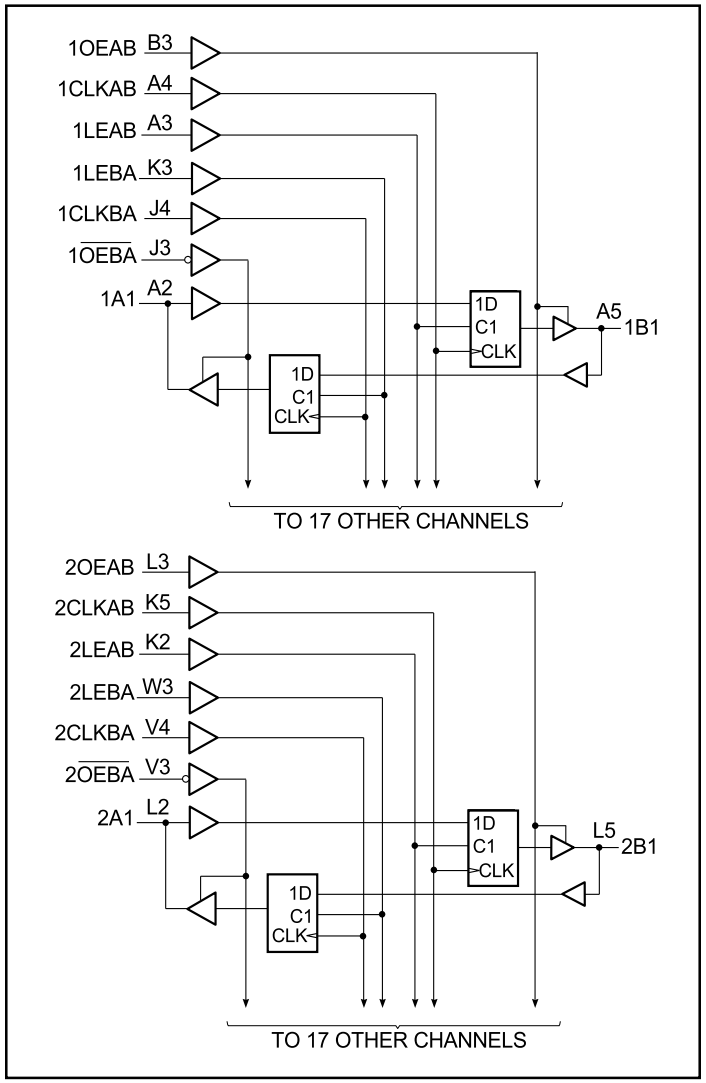
PI74ALVCH32501

36-Bit Universal Bus Transceiver with 3-State Outputs

Product Features

- PI74ALVCH32501 is designed for low voltage operation, Vcc = 1.65 to 3.6V
- Bus Hold on data inputs eliminates the need for external pullup resistors
- Industrial operation at –40ºC to 85ºC
- Packages available:
  114 Ball, 16mm x 5.5mm x 1.4mm Low Profile
  Fine Pitch Ball Grid Array,
  LFBGA (NB114)

Logic Block Diagram (Positive Logic), Two Sets



Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The 36-bit PI74ALVCH32501 universal bus transceiver is designed for 1.65V to 3.6V V_{CC} operation.

This device can be used as two 18-bit transceivers or one 36-bit transceiver. Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses OEBA, $\overline{LEBA}$, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{OEBA}$ is active low).

To ensure the high-impedance state during power up or power down, $\overline{OEBA}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a logic level.

The PI74ALVCH32501 is characterized for operation from –40°C to 85°C.

Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active HIGH)
LE	Latch Enable (Active HIGH)
CLK	Clock Input (Active HIGH)
Ax	Data I/O
Bx	Data I/O
GND	Ground
V_{CC}	Power

Truth Table(1)†

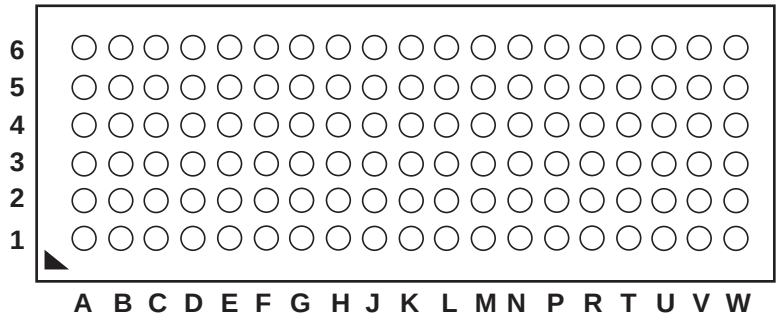
Inputs				Output
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L or H	X	B_0‡

Notes:

† A-to-B data flow is shown; B-toA flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.

‡ Output level before the indicated steady state input conditions were established, provided that CLKAB is high before LEAB goes low.

NB PACKAGE
Top View



Terminal Assignments

6	1B2	1B4	1B6	1B8	1B10	1B12	1B14	1B15	1B17	NC	2B2	2B4	2B6	2B8	2B10	2B12	2B14	2B15	2B17
5	1B1	1B3	1B5	1B7	1B9	1B11	1B13	1B16	1B18	2CLKAB	2B1	2B3	2B5	2B7	2B9	2B11	2B13	2B16	2B18
4	1CLKAB	GND	GND	V_{CC}	GND	GND	V_{CC}	GND	1CLKBA	GND	GND	GND	V_{CC}	GND	GND	V_{CC}	GND	2CLKBA	GND
3	1LEAB	1OEAB	GND	V_{CC}	GND	GND	V_{CC}	GND	$\overline{1OEBA}$	1LEBA	2OEAB	GND	V_{CC}	GND	GND	V_{CC}	GND	$\overline{2OEBA}$	2LEBA
2	1A1	1A3	1A5	1A7	1A9	1A11	1A13	1A16	1A18	2LEAB	2A1	2A3	2A5	2A7	2A9	2A11	2A13	2A16	2A18
1	1A2	1A4	1A6	1A8	1A10	1A12	1A14	1A15	1A17	NC	2A2	2A4	2A6	2A8	2A10	2A12	2A14	2A15	2A17
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**	**K**	**L**	**M**	**N**	**P**	**R**	**T**	**U**	**V**	**W**

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{CC}	–0.5V to 4.6V
Input Voltage Range, V_I: Except I/O ports (1)	–0.5V to 4.6V
I/O ports (1,2)	–0.5V to V_{CC} + 0.5V
Output Voltage Range, V_O (1,2)	–0.5V to V_{CC} +0.5V
Input Clamp Current, I_{IK} (V_I <0)	–50mA
Output Clamp Current, I_{OK} (V_O <0)	–50mA
Continuous Output Current, I_O	±50mA
Continuous Current through each V_{CC} or GND	±100mA
Package Thermal Impedance, θ_{JA} (3)	39ºC/W
Storage Temperature Range, T_{STG}	–65ºC to 150ºC

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note:
1. The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions(1)

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{CC}	Supply Voltage		1.65	3.6	V
V_{IH}	HIGH Level Input Voltage	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}		
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 2.7V to 3.6V	2		
V_{IL}	LOW Level Input Voltage	V_{CC} = 1.65V to 1.95V		0.35 x V_{CC}	
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 2.7V to 3.6V		0.8	
V_I	Input Voltage		0	V_{CC}	
V_O	Output Voltage		0	V_{CC}	
I_{OH}	High-level Output Current	V_{CC} = 1.65V		–4	mA
		V_{CC} = 2.3V		–12	
		V_{CC} = 2.7V		–12	
		V_{CC} = 3.0V		–24	
I_{OL}	Low-level Output Current	V_{CC} = 1.65V		4	
		V_{CC} = 2.3V		12	
		V_{CC} = 2.7V		12	
		V_{CC} = 3.0V		24	
$\Delta t/\Delta v$	Input Transition rise or fall time		0	10	ns/V
T_A	Operating Free-Air Temperature		-40	85	°C

Note:
1. Unused control inputs must be held at V_{CC} or G_{ND} to ensure proper device operation.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ±10%)

Parameters	Test Conditions	V_{CC}	Min.	Typ.(1)	Max.	Units
V_{OH}	I_{OH} = –100µA	1.65V to 3.6V	V_{CC} -0.2			V
	I_{OH} = –4mA	1.65V	1.2			
	I_{OH} = –6mA	2.3V	2.0			
	I_{OH} = –12mA	2.3V	1.7			
		2.7V	2.2			
		3.0V	2.4			
	I_{OH} = –24mA	3.0V	2.0			
V_{OL}	I_{OL} = 100µA	1.65V to 3.6V			0.2	
	I_{OL} = 4mA	1.65V			0.45	
	I_{OL} = 6mA	2.3V			0.4	
	I_{OL} = 12mA	2.3V			0.7	
		2.7V			0.4	
	I_{OL} = 24mA	3V			0.55	
I_I	V_I = V_{CC} or GND	3.6V			±5	µA
I_I (Hold)	V_I = 0.58V	1.65V	TBD			
	V_I = 1.07V		TBD			
	V_I = 0.7V	2.3V	45			
	V_I = 1.7V		–45			
	V_I = 0.8V	3V	75			
	V_I = 2V		–75			
	V_I = 0 to 3.6V(2)	3.6V			±500	
I_{OZ}(3)	V_O = V_{CC} or GND	3.6V			±10	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6V			20	
ΔI_{CC}	One input at V_{CC} –0.6V, Other inputs at V_{CC} or GND	3V to 3.6V			750	
C_I Control Inputs	V_I = V_{CC} or GND	3.3V		4		pF
C_{IO} A or B ports	V_O = V_{CC} or GND	3.3V		8		

Notes:

1. All typical values are at V_{CC} = 3.3V, T_A = 25ºC.

2. This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

3. For I/O ports, the I_{OZ} includes the input leakage current.

Timing Requirements over Operating Range, Figures 1,2,3

Parameters	Description	Conditions[1]	V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock frequency	C_L = 50pF R_L = 500Ω		TBD		150		150		150	MHz
t_W Pulse Duration	LE high				3.3		3.3		3.3		ns
	CLK high or low				3.3		3.3		3.3		
t_{SU} Setup time	Data before CLK ↑				2.2		2.1		1.7		
	Data before LE ↓, CLK high				1.9		1.6		1.5		
	Data before LE ↓, CLK low				1.3		1.1		1		
t_H Hold time	Data after CLK ↑				0.6		0.6		0.7		
	Data after LE ↓ CLK high or low				1.4		1.7		1.4		

Switching Characteristics Over Operating Range, Figures 1,2,3

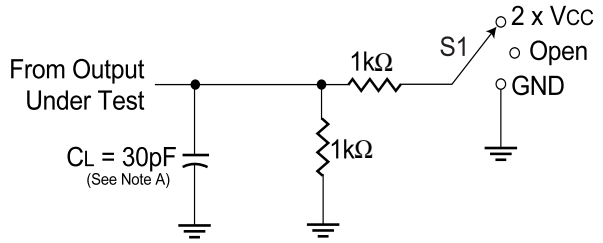
Parameters	From (Input)	To (Output)	Conditions	V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ±0.V		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}			C_L = 50pF R_L = 500Ω			150		150		150		MHz
t_{PD}	A or B	B or A			TBD	1.0	4.8		4.5	1.0	3.9	ns
	LE	A or B				1.1	5.7		5.3	1.3	4.6	
	CLK	A or B				1.2	6.1		5.6	1.4	4.9	
t_{EN}	OEAB	B				1.0	5.8		5.3	1.0	4.6	
t_{DIS}	OEAB	B				1.5	6.2		5.7	1.4	5.0	
t_{EN}	$\overline{OEBA}$	A				1.3	6.3		6.0	1.1	5.0	
t_{DIS}	$\overline{OEBA}$	A				1.3	5.3		4.6	1.3	4.2	

Operating Characteristics, T_A = 25°C

Parameter		Test Conditions	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	Units
			Typ.	Typ.	Typ.	
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 0, f = 10 MHz	TBD	44	54	pF
	Outputs Disabled			6	6	

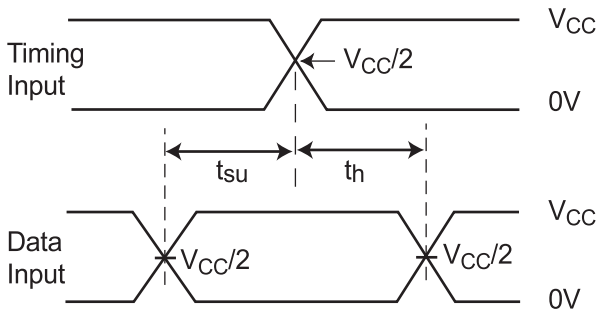
Parameter Measurement Information
V_{CC} = 1.8V ±0.15V

Load Circuit

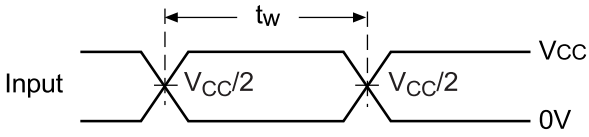


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	Open

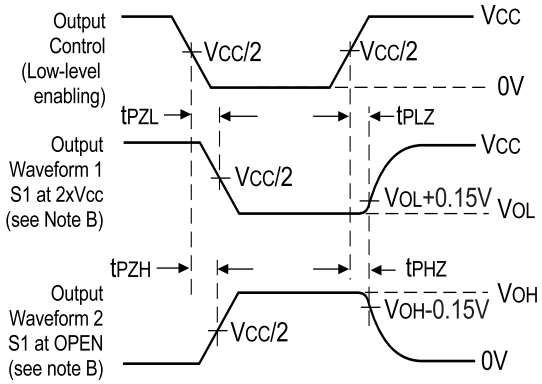
Voltage Waveforms Setup and Holdtimes



Voltage Waveforms Pulse Duration



Voltage Waveforms Enable and Disable Times



Voltage Waveforms Propagation Delay Times

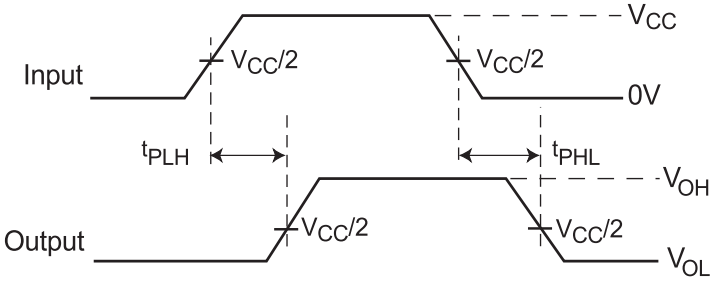


Figure 1. Load Circuit and Voltage Waveforms

Notes:

A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All inputs pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2ns, t_f ≤ 2ns.

D. The outputs are measured one at a time with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{ten}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

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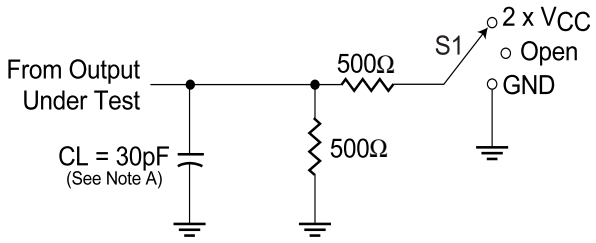
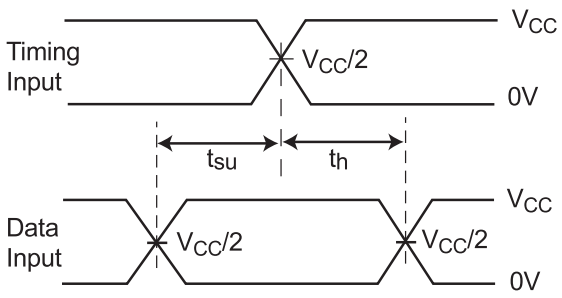
Parameter Measurement Information
V_{CC} = 2.5V ±0.2V

Load Circuit

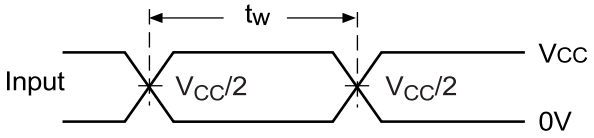


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

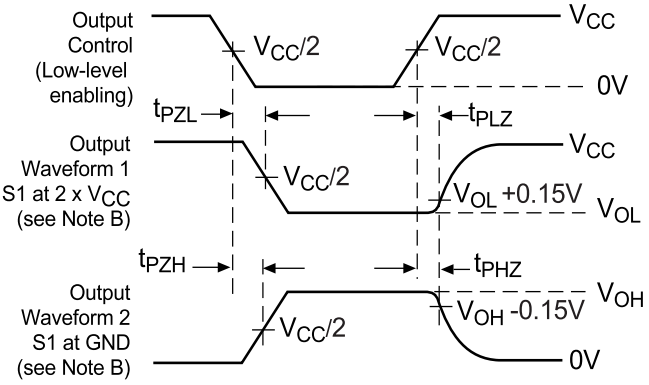
Voltage Waveforms Setup and Hold Times



Voltage Waveforms Pulse Duration



Voltage Waveforms Enable and Disable Times



Voltage Waveforms Propagation Delay Times

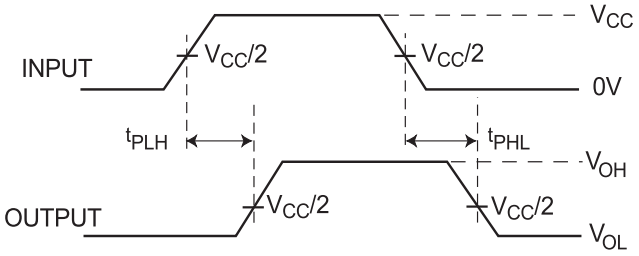


Figure 2. Load Circuit and Voltage Waveforms

Notes:

A. CL includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All inputs pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50Ω, $t_r \leq$ 2ns, $t_f \leq$ 2ns.

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F. t_{PZL} and t_{PZH} are the same as t_{ten}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

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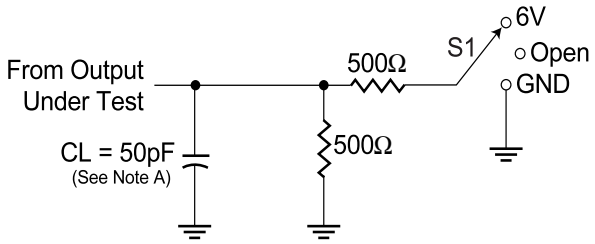
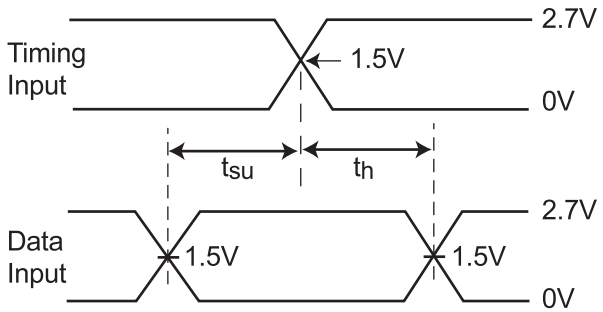
Parameter Measurement Information
V_{CC} = 2.7V and 3.3V ±0.3V

Load Circuit

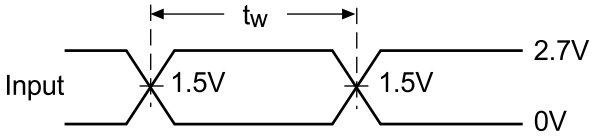


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

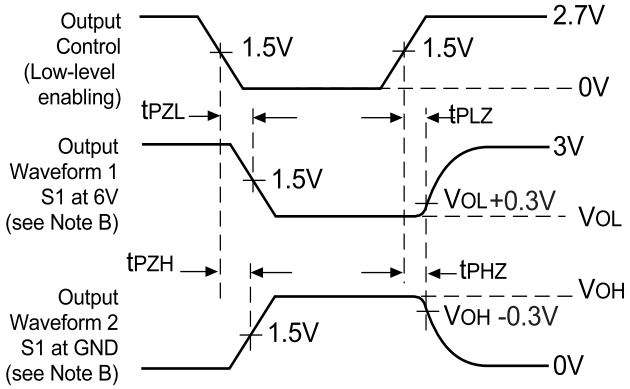
Voltage Waveforms Setup and Hold Times



Voltage Waveforms Pulse Duration



Voltage Waveforms Enable and Disable Times



Voltage Waveforms Propagation Delay Times

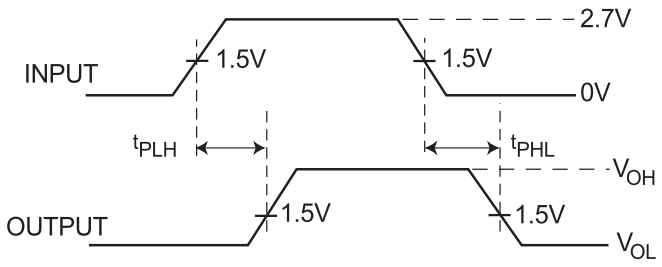


Figure 3. Load Circuit and Voltage Waveforms

Notes:

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