MC100EP16VS

3.3V / 5V ECL Differential Receiver/Driver with Variable Output Swing

The MC100EP16VS is a differential receiver with variable output amplitude. The device is functionally equivalent to the 100EP16 with an input pin that controls the amplitude of the outputs.

The V_{CTRL} input pin controls the output amplitude of the EP16VS and is referenced to V_{CC}. (See Figure 5.) The operational range of the V_{CTRL} input is from ≤ V_{BB} (max output amplitude) to V_{CC} (min output amplitude). (See Figure 4.) A variable resistor between the V_{CC} and V_{BB} pins, with the wiper driving V_{CTRL}, can control the output amplitude. Typical application circuits and a V_{CTRL} Voltage vs. Output Amplitude graph are described in this data sheet. When left open, the V_{CTRL} pin will be internally pulled down to V_{EE} and operate as a standard EP16, with 100% output amplitude.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single–ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 220 ps Propagation Delay
- Maximum Frequency > 4 GHz Typical (See Graph)
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –3.0 V to –5.5 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}

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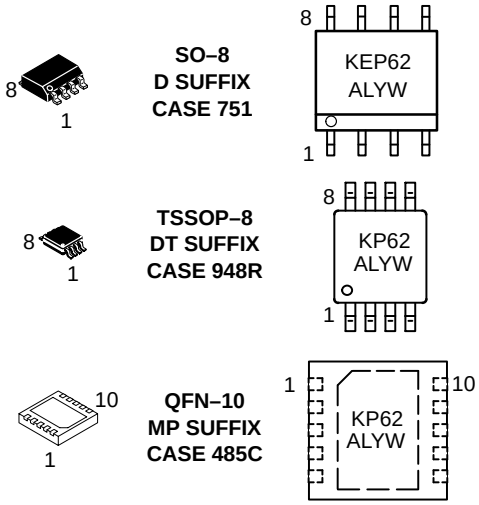
MARKING DIAGRAMS*



K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EP16VSD	SO–8	98 Units/Rail
MC100EP16VSDR2	SO–8	2500 Tape & Reel
MC100EP16VSDT	TSSOP	100 Units/Rail
MC100EP16VSDTR2	TSSOP	2500 Tape & Reel
MC100EP16VSMP	QFN	124 Units/Rail
MC100EP16VSMPR2	QFN	3000 Tape & Reel

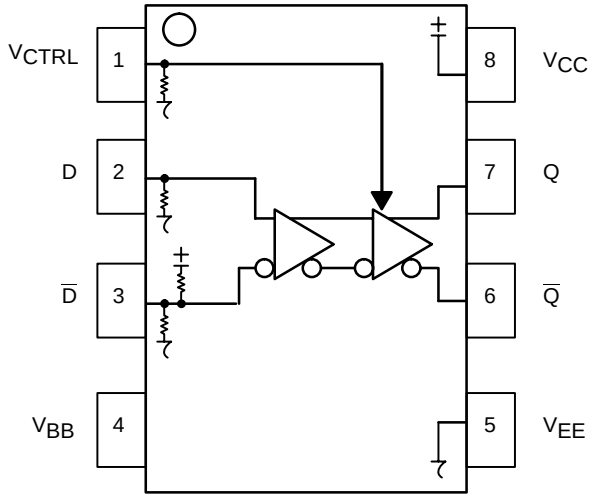


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

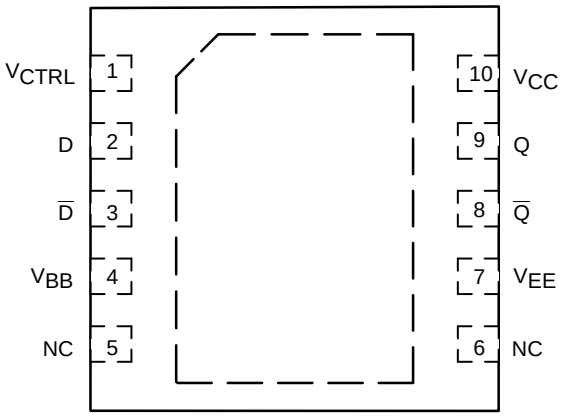


Figure 2. 10–Lead QFN Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION	8 LD	10 LD
D*, $\overline{D}$**	ECL Data Inputs	2, 3	2, 3
Q, $\overline{Q}$	ECL Data Outputs	6, 7	8, 9
V_{CTRL}*	Output Swing Control	1	1
V_{BB}	Reference Voltage Output	4	4
V_{CC}	Positive Supply	8	10
V_{EE}	Negative Supply	5	7
NC	No Connect		5, 6

* Pins will default LOW when left open.
** Pins will default to $V_{CC}/2$ when left open.

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating Oxygen Index		UL–94 code V–0 A 1/8″ 28 to 34
Transistor Count		140 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 LFPM 500 LFPM	10 QFN 10 QFN	40 20	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	std bd	10 QFN	3.3	°C/W

2. Maximum Ratings are those values beyond which device damage may occur.

DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V_{OH}	Output HIGH Voltage (Max Swing) (Note 4) $V_{CC} \ge V_{CTRL} \ge V_{EE}$	2155		2405	2155		2405	2155		2405	mV
V_{OL}	Output LOW Voltage (Max Swing) (Note 4) $V_{CTRL} \le V_{BB}$	1355	1490	1605	1355	1520	1605	1355	1520	1605	mV
	$VCC \ge V_{CTRL} > V_{BB}$		See Fig.3			See Fig.3			See Fig.3		
	$V_{CTRL} = V_{CC}$ (Min Swing)	2105	2230	2355	2095	2220	2345	2065	2190	2315	
V_{IH}	D, $\overline{D}$ Input HIGH Voltage (Single–Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	D, $\overline{D}$ Input LOW Voltage (Single–Ended)	1490		1675	1490		1675	1490		1675	mV
V_{BB}	Output Voltage Reference	1805	1905	2005	1805	1905	2005	1805	1905	2005	mV
V_{CTRL}	Input Voltage (V_{CTRL})	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V_{EE}		V_{CC}	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.0		2.9	2.0		2.9	2.0		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to –2.2 V.
4. All loading with 50 Ω to V_{CC}–2.0 volts. V_{OH} does not change with V_{CTRL}. V_{OL} changes with V_{CTRL}. V_{CTRL} is referenced to V_{CC}.
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 6)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V_{OH}	Output HIGH Voltage (Note 7) $V_{CC} > V_{CTRL} > V_{EE}$	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Max Swing) (Note 7) $V_{CTRL} \le V_{BB}$	3055	3190	3305	3055	3220	3305	3055	3220	3305	mV
	$VCC \ge V_{CTRL} > V_{BB}$		See Fig.3			See Fig.3			See Fig.3		
	$V_{CTRL} = V_{CC}$ (Min Swing)	3805	3930	4055	3795	3920	4045	3765	3890	4015	
V_{IH}	D, $\overline{D}$ Input HIGH Voltage (Single–Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	D, $\overline{D}$ Input LOW Voltage (Single–Ended)	3190		3375	3190		3375	3190		3375	mV
V_{CTRL}	Input Voltage (V_{CTRL})	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V_{EE}		V_{CC}	mV
V_{BB}	Output Voltage Reference	3505	3605	3705	3505	3605	3705	3505	3605	3705	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8)	2.0		4.6	2.0		4.6	2.0		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to –0.5 V.
7. All loading with 50 Ω to V_{CC}–2.0 volts. V_{OH} does not change with V_{CTRL}. V_{OL} changes with V_{CTRL}. V_{CTRL} is referenced to V_{CC}.
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

DC CHARACTERISTICS, NECL V_{CC} = 0 V; V_{EE} = –5.5 V to –3.0 V (Note 9)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	30	36	42	31	38	44	32	40	48	mA
V_{OH}	Output HIGH Voltage (Note 10) $V_{CC} > V_{CTRL} > V_{EE}$	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV
V_{OL}	Output LOW Voltage (Max Swing) (Note 10) $V_{CTRL} \le V_{BB}$	–1945	–1810	–1695	–1945	–1780	–1695	–1945	–1780	–1695	mV
	$VCC \ge V_{CTRL} > V_{BB}$		See Fig.3			See Fig.3			See Fig.3		
	$V_{CTRL} = V_{CC}$ (Min Swing)	–1195	–1070	–945	–1205	–1080	–955	–1235	–1110	–985	
V_{IH}	D, $\overline{D}$ Input HIGH Voltage (Single–Ended)	–1225		–880	–1225		–880	–1225		–880	mV
V_{IL}	D, $\overline{D}$ Input LOW Voltage (Single–Ended)	–1810		–1625	–1810		–1625	–1810		–1625	mV
V_{BB}	Output Voltage Reference	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{CTRL}	Input Voltage (V_{CTRL})	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V_{EE}		V_{CC}	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 11)	V_{EE}+2.0		–0.4	V_{EE}+2.0		–0.4	V_{EE}+2.0		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –150			0.5 –150			0.5 –150			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

9. Input and output parameters vary 1:1 with V_{CC}.
10. All loading with 50 Ω to V_{CC}–2.0 volts. V_{OH} does not change with V_{CTRL}. V_{OL} changes with V_{CTRL}. V_{CTRL} is referenced to V_{CC}.
11. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.0 V to –5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 12)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency (See Figure 7. F_{max}/JITTER)		> 4			> 4			> 4		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential Max Swing Min Swing	 150 90	 220 150	 280 210	 150 90	 220 150	 280 210	 160 100	 240 160	 300 220	ps
t_{SKEW}	Duty Cycle Skew (Note 13)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter (See Figure 7. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential) (Note 14)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Max Swing Q Min Swing	70 30	120 80	170 130	80 20	130 70	180 120	100 20	150 70	200 120	ps

12. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}–2.0 V.
13. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
14. V_{PP}(min) is minimum input swing for which AC parameters are guaranteed.

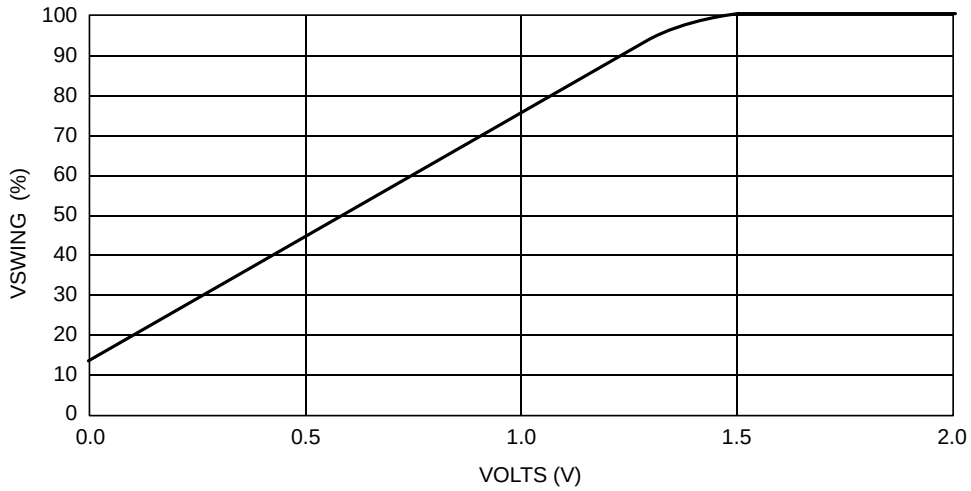


Figure 3. V_{CC} – V_{CTRL} (pin #1)

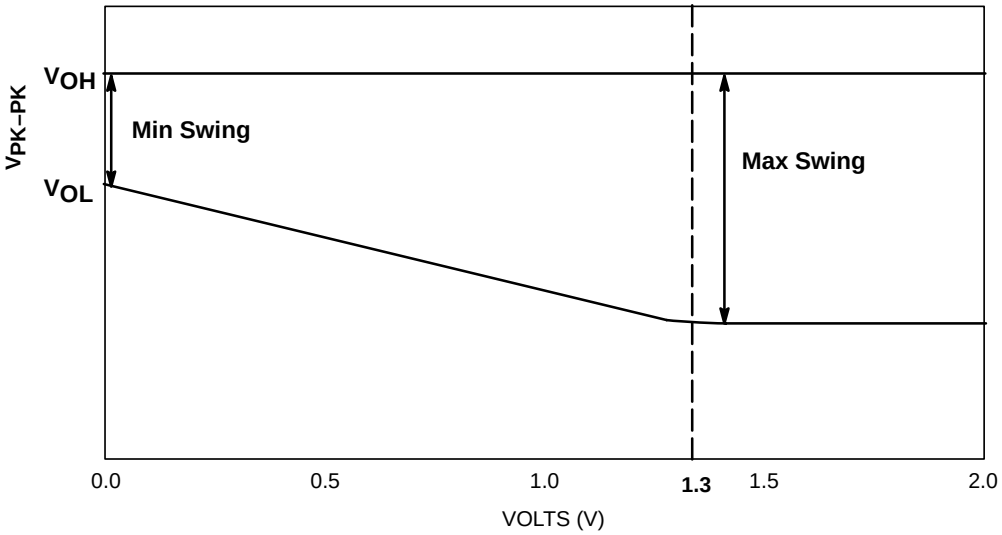


Figure 4. $V_{CC} - V_{CTRL}$

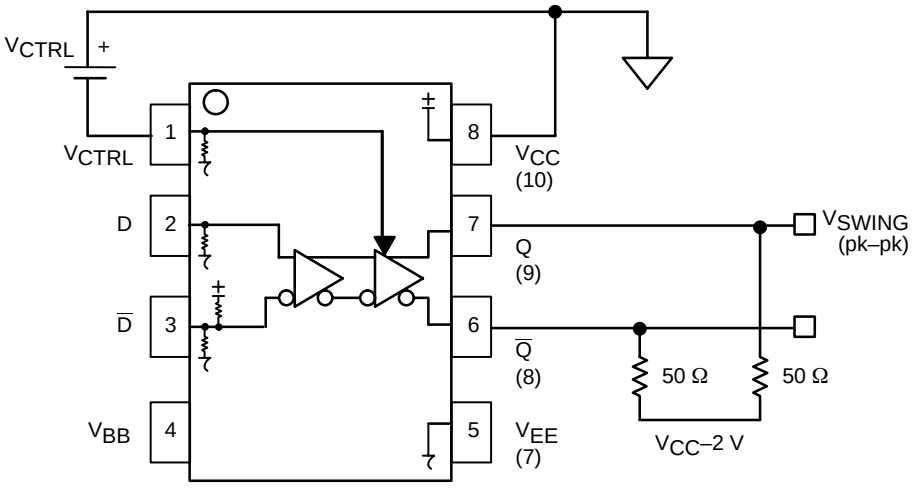


Figure 5. Voltage Source Implementation for 8 Ld Package
10 Ld Package Pins in ( )

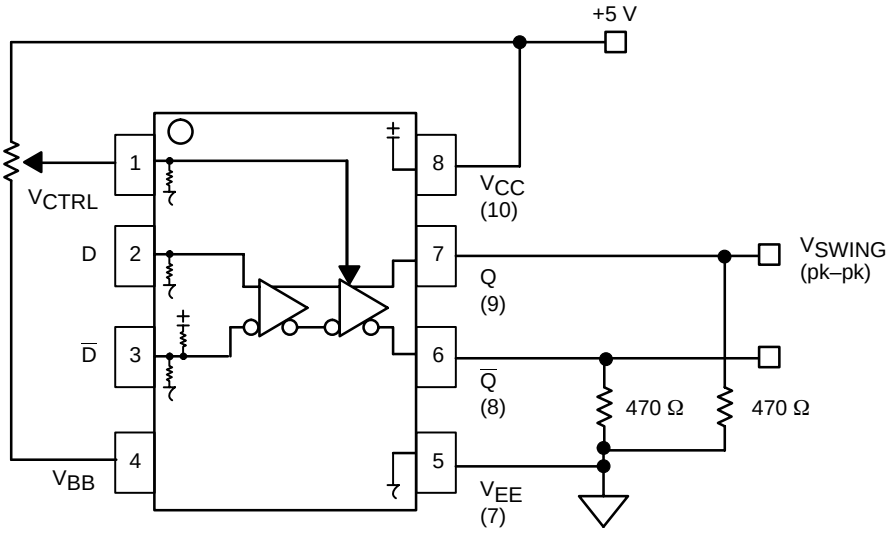


Figure 6. Alternative Implementation for 8 Ld Package
10 Ld Package Pins in ( )

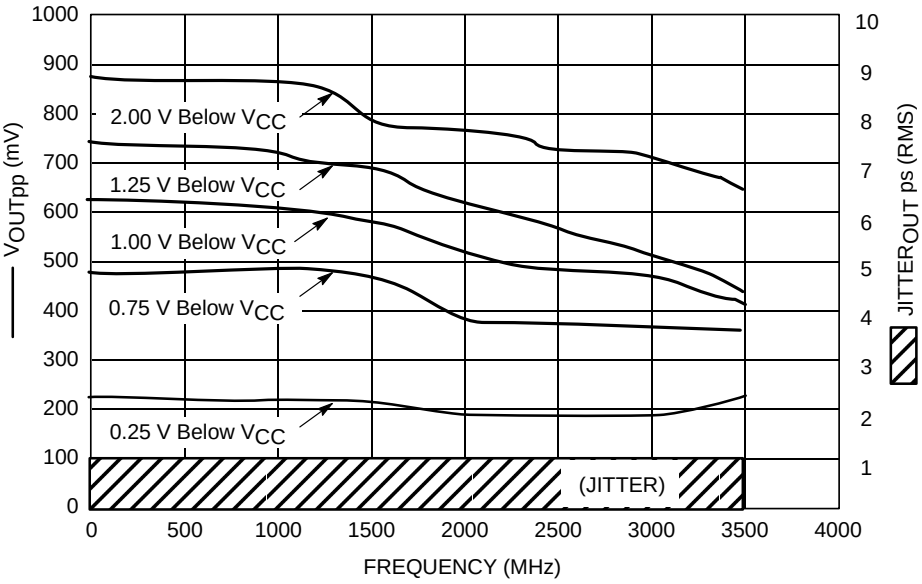


Figure 7. F_{max}/Jitter

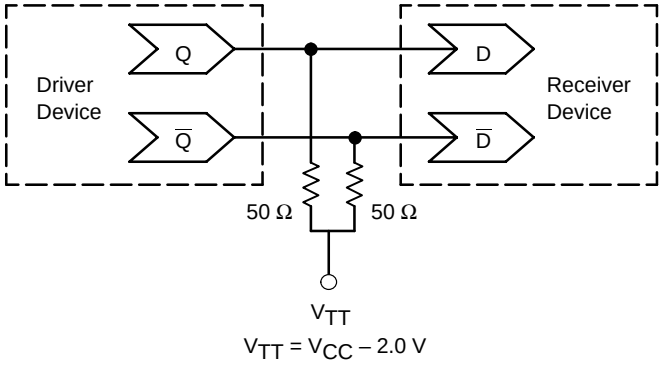


Figure 8. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

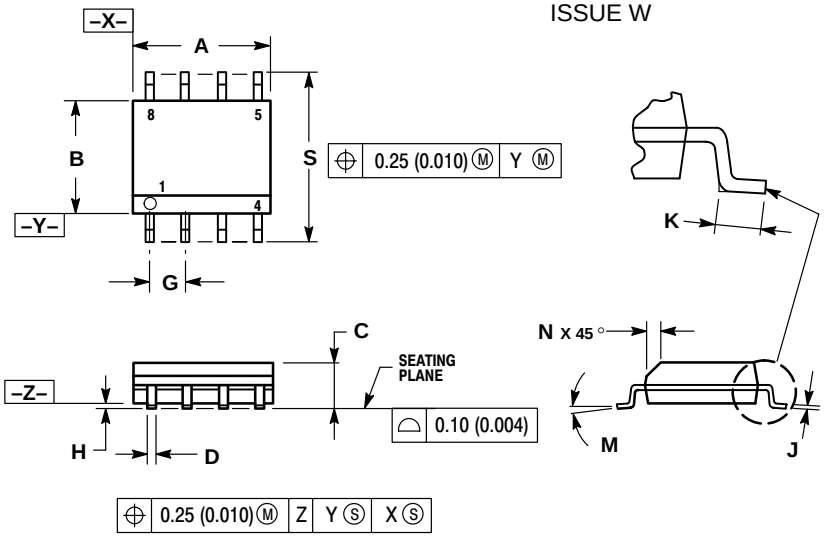
Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8009	–	ECLinPS Plus Spice I/O Model Kit
AND8020	–	Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

PACKAGE DIMENSIONS

SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–07
ISSUE W

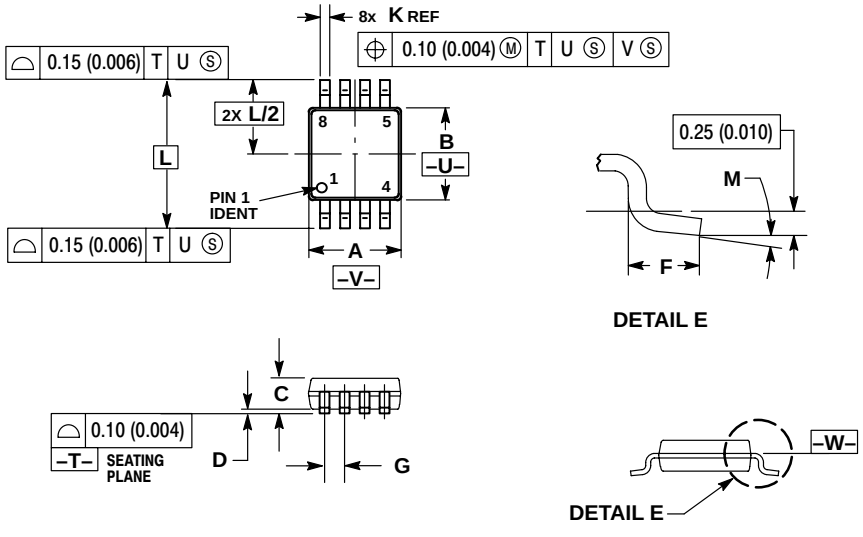


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PACKAGE DIMENSIONS

TSSOP–8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R–02
ISSUE A

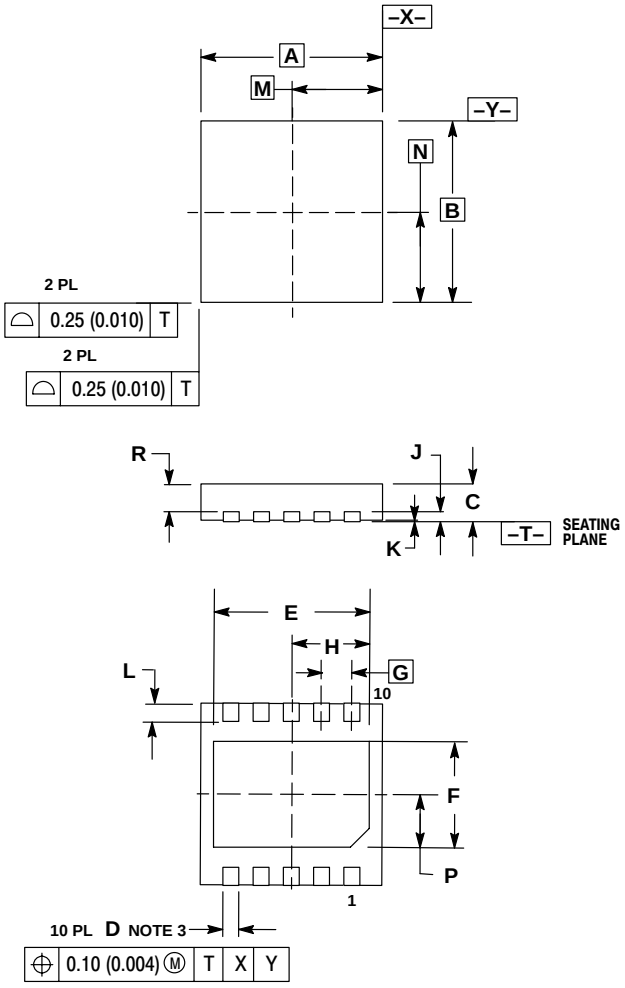


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

PACKAGE DIMENSIONS

10 QFN
MP SUFFIX
CASE 485C–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.20	0.30	0.008	0.012
E	2.45	2.55	0.096	0.100
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	1.23	1.28	0.048	0.050
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.88	0.93	0.035	0.037
R	0.60	0.80	0.024	0.031

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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