

MC100EL91

5 V Triple PECL Input to -5 V ECL Output Translator

The MC100EL91 is a triple PECL input to ECL output translator. The device receives standard voltage differential PECL signals, determined by the V_{CC} supply level, and translates them to differential -5 V ECL output signals. (For translation of LVPECL to -3.3 V ECL output, see MC100LVEL91.)

To accomplish the level translation, the EL91 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μF capacitors.

Under open input conditions, the \bar{D} input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a low, ensuring stability.

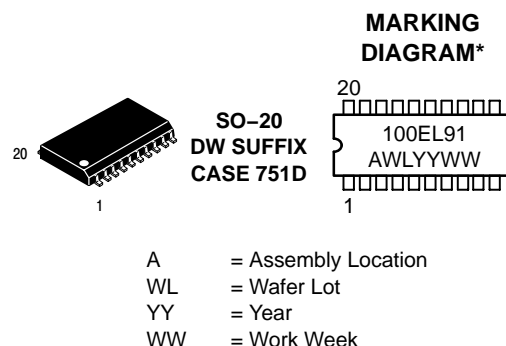
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 670 ps Typical Propagation Delay
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- Operating Range: V_{CC} = 4.75 V to 5.25 V;
 V_{EE} = -4.2 V to -5.5 V; GND= 0 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at GND
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in,
Oxygen Index: 28 to 34
- Transistor Count = 282 devices



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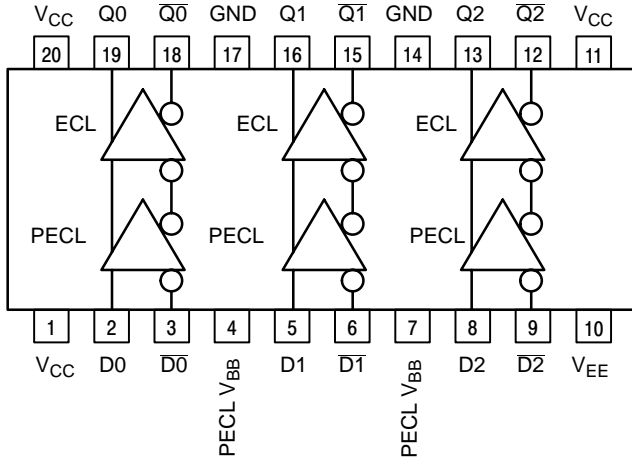
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EL91DW	SO-20	38 Units/Rail
MC100EL91DWR2	SO-20	1000 Units/Reel

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20-Lead Pinout (Top View) and Logic Diagram



PIN DESCRIPTION

PIN	FUNCTION
Dn, \overline{Dn}	PECL Inputs
Qn, \overline{Qn}	ECL Outputs
PECL V_{BB}	PECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

**All V_{CC} pins are tied together on the die.

Warning: All V_{CC} , V_{EE} , and GND pins must be externally connected to Power Supply to guarantee proper operation.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		-8 to 0	V
V_I	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	PECL V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

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PECL INPUT DC CHARACTERISTICS $V_{CC}= 5.0\text{ V}$; $V_{EE}= -5.0\text{ V}$; $GND= 0\text{ V}$ (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	V_{CC} Power Supply Current			11		6	11			11	mA
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
PECL V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$	1.3 1.5		4.8 4.8	1.2 1.4		4.8 4.8	1.2 1.4		4.8 4.8	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

- Input parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.25\text{ V}$. V_{EE} can vary -4.20 V to -5.5 V .
- V_{IHCMR} min varies 1:1 with GND . V_{IHCMR} max varies 1:1 with V_{CC} .

NECL OUTPUT DC CHARACTERISTICS $V_{CC}= 3.3\text{ V}$ to 5.0 V ; $V_{EE}= -5.0\text{ V}$; $GND= 0\text{ V}$ (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	V_{EE} Power Supply Current			28		22	28			30	mA
V_{OH}	Output HIGH Voltage (Note 5)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 5)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

- Output parameters vary 1:1 with GND . V_{EE} can vary $+0.8\text{ V}$ / -0.5 V .
- Outputs are terminated through a 50 ohm resistor to $GND=2$ volts.

AC CHARACTERISTICS $V_{CC}= 3.0\text{ V}$ to 5.5 V ; $V_{EE}= -4.2\text{ V}$ to -5.5 V ; $GND= 0\text{ V}$ (Note 9).

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		700			700			700		MHz
t_{PLH} t_{PHL}	Propagation Delay D to Q Diff S.E.	540 490	640 640	740 790	570 520	670 670	770 820	610 560	710 710	810 860	ps
t_{SKEW}	Skew Output-to-Output (Note 6) Part-to-Part (Diff) (Note 6) Duty Cycle (Diff) (Note 7)		40 25	100 200		40 25	100 200		40 25	100 200	ps
t_{JITTER}	Random Clock Jitter @ 700 MHz		1.2			1.2			1.2		pS(RMS)
V_{PP}	Input Swing (Note 8)	200		1000	200		1000	200		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	320	400	580	320	400	580	320	400	580	ps

- Skews are valid across specified voltage range, part-to-part skew is for a given temperature.
- Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
- $V_{PP}(\text{min})$ is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 .
- Outputs are terminated through a 50 Ω resistor to $GND = 2\text{ V}$.

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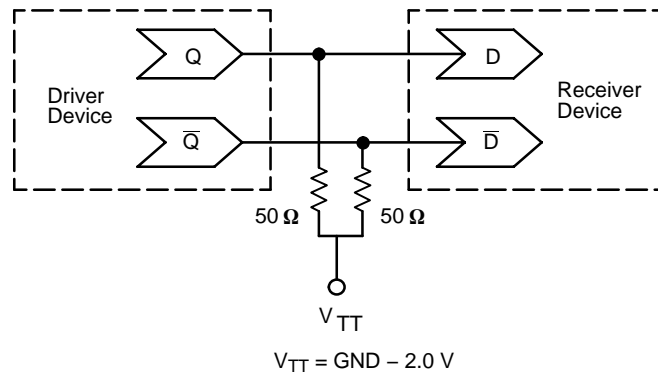


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

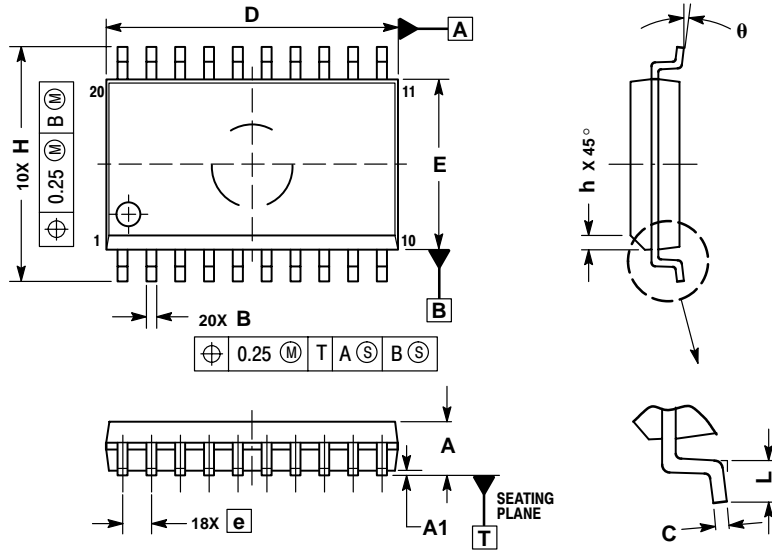
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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PACKAGE DIMENSIONS


SO-20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-05
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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