
MSM27C452CZ

262,144-Word x 16-Bit or 524,288-Word x 8-Bit

8-Word x 16-Bit or 16-Word x 8-Bit Page Mode One Time PROM

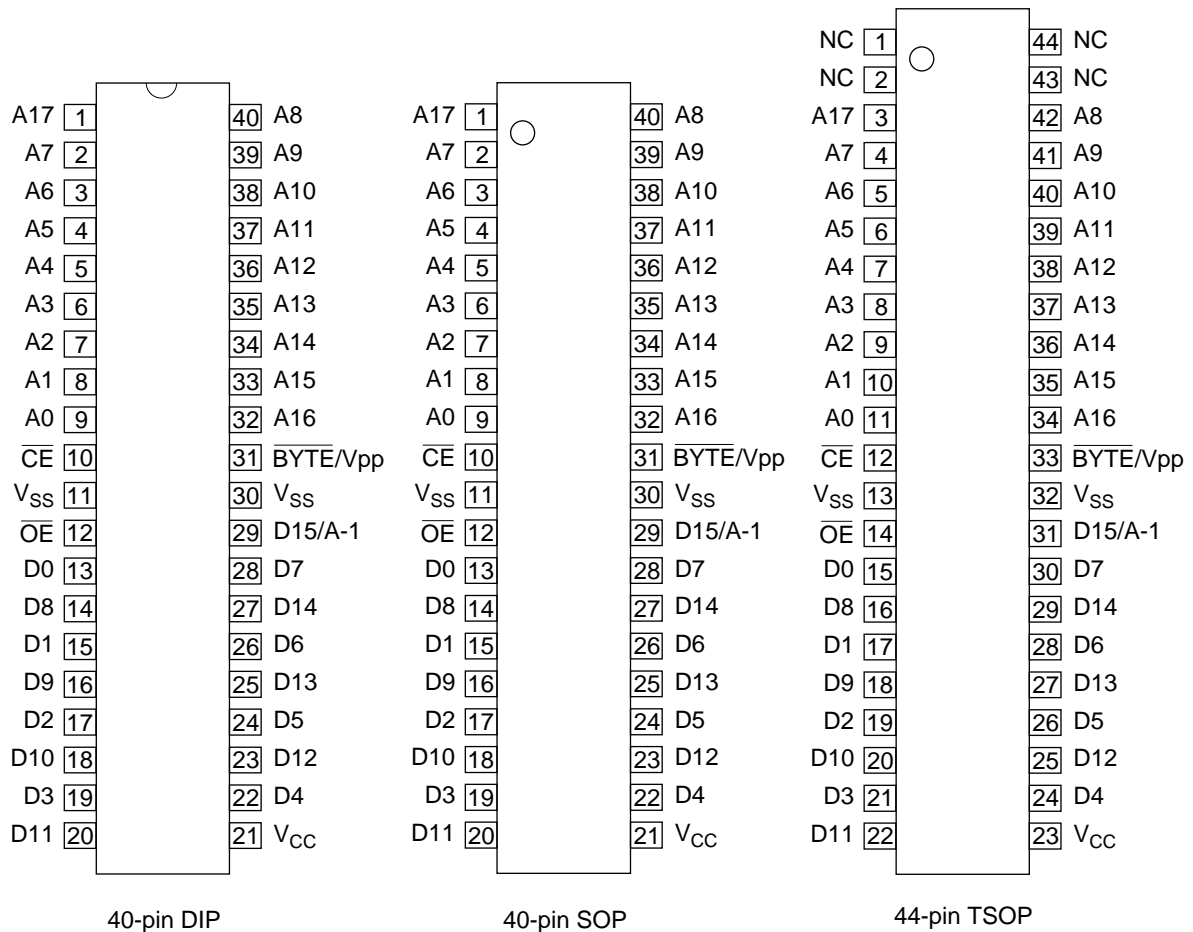
DESCRIPTION

The MSM27C452CZ is a 4Mbit electrically Programmable Read-Only Memory with page mode. Its configuration can be electrically switched between 262,144 word x 16bit and 524,288 word x 8bit. The MSM27C452CZ operates on a single +5V power supply and is TTL compatible. The MSM27C452CZ provides Page mode which can greatly reduce the read access time. Since the MSM27C452CZ operates asynchronously, external clocks are not required, making this device easy-to-use. The MSM27C452CZ is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS double silicon gate technology and is offered in 40-pin DIP, 40-pin SOP or 44-pin TSOP packages.

FEATURES

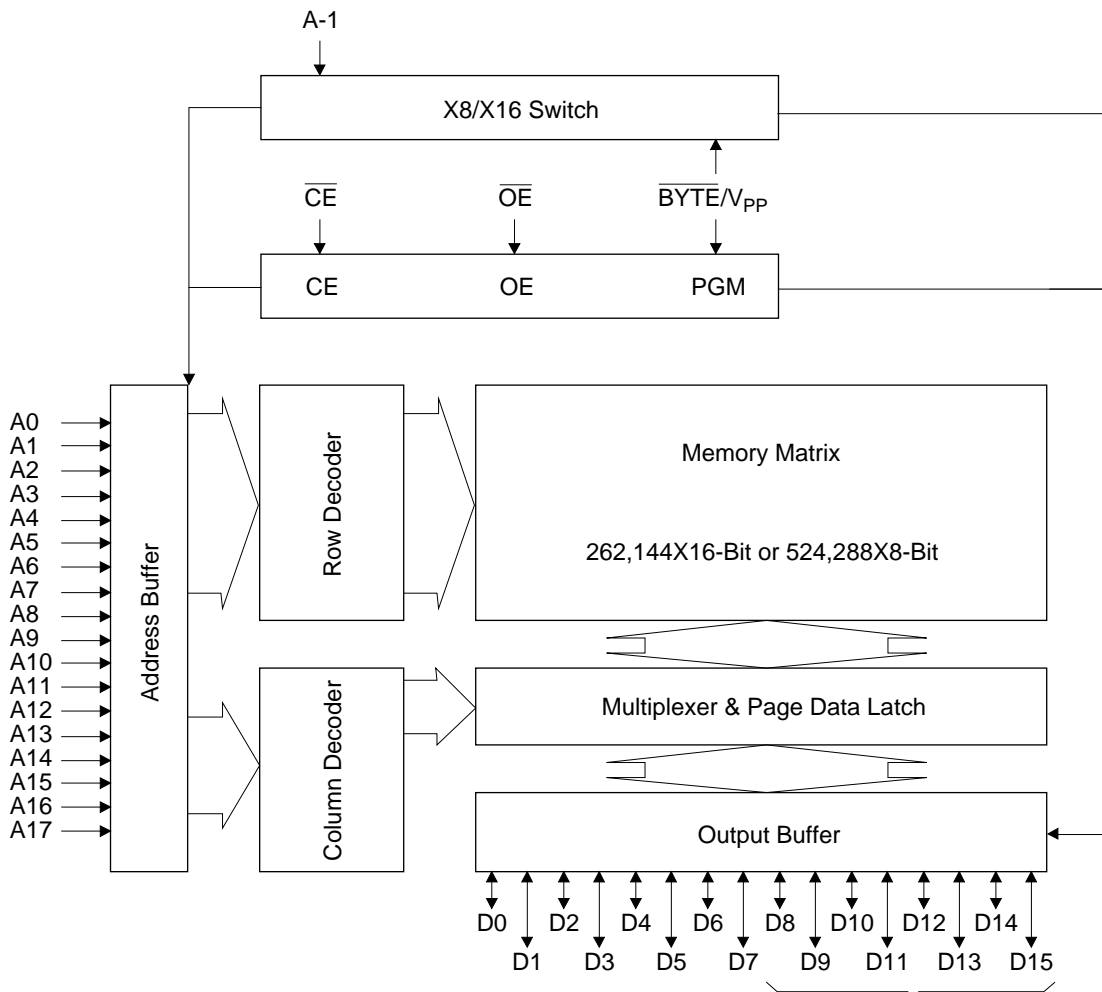
- 262,144 word x 16bit / 524,288 word x 8bit electrically switchable configuration
- Single +5V power supply
- Access time 80ns
 - Page mode access time 50ns
- Input / Output TTL compatible
- Three-state output
- Packages
 - 40-pin plastic DIP (DIP40-P-600-2.54)
 - 40-pin plastic SOP (SOP40-P-525-1.27-K)
 - 44-pin plastic TSOP (TSOP II 44-P-400-0.80-K)

PIN CONFIGURATION (TOP VIEW)



PIN NAMES	FUNCTIONS
D15/A-1	Data output / Address input
A0 - A17	Address input
D0 - D14	Data output
CE	Chip enable
OE	Output enable
V _{CC}	Power supply voltage
V _{SS}	GND
BYTE/V _{PP}	Mode switch / Program power supply voltage
NC	Non connection

BLOCK DIAGRAM



In 8-bit output mode, these pins are three-stated and pin D15 functions as the A-1 address pin.

FUNCTION TABLE

MODE	\overline{CE}	\overline{OE}	BYTE/ V_{PP}	V_{CC}	D0 - D7	D8 - D14	D15/A-1
READ (16-Bit)	L	L	H	4.5V to 5.5V	D_{OUT}		
READ (8-Bit)	L	L	L		D_{OUT}	Hi-Z	L/H
OUTPUT DISABLE	L	H	H		Hi-Z		
			L		*		
STAND-BY	H	*	H	Hi-Z			
			L	*			
PROGRAM	L	H	11.5V	6.25V	D_{IN}		
PROGRAM INHIBIT	H	H			Hi-Z		
PROGRAM VERIFY	H	L			D_{OUT}		

* : Don't Care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T_{opr}	-	0 to 70	°C
Storage temperature	T_{stg}	-	-55 to 125	°C
Input voltage	V_I	relative to V_{SS}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_O		-0.5 to $V_{CC} + 0.5$	V
Power supply voltage	V_{CC}		-0.5 to 7	V
Program power supply voltage	V_{PP}		-0.5 to 12.5	V
Power dissipation per package	P_D	-	1.0	W

RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}	$V_{CC}=4.5V - 5.5V$	4.5	-	5.5	V
V_{PP} power supply voltage	V_{PP}		-0.5	-	$V_{CC}+0.5$	V
Input "H" level	V_{IH}		2.2	-	$V_{CC}+0.5$	V
Input "L" level	V_{IL}		-0.5	-	0.8	V

Voltage is relative to V_{SS}

ELECTRICAL CHARACTERISTICS (Read operation)**DC Characteristics** $(V_{CC}=5V\pm 0.5V, T_a=0 \text{ to } 70^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	$V_I=0 \text{ to } V_{CC}$	-	-	10	μA
Output leakage current	I_{LO}	$V_O=0 \text{ to } V_{CC}$	-	-	10	μA
V_{CC} power supply current (Standby)	I_{CS1}	$\overline{CE}=V_{CC}$	-	-	50	μA
	I_{CS2}	$\overline{CE}=V_{IH}$	-	-	1	mA
V_{CC} power supply current (Read)	I_{CCA}	$\overline{CE}=V_{IL}, \overline{OE}=V_{IH}$ $t_c=80\text{ns}$	-	-	100	mA
V_{PP} power supply current	I_{PP}	$V_{PP}=V_{CC}$	-	-	50	μA
Input "H" level	V_{IH}	-	2.2	-	$V_{CC}+0.5$	V
Input "L" level	V_{IL}	-	-0.5	-	0.8	V
Output "H" level	V_{OH}	$I_{OH}=-400\mu\text{A}$	2.4	-	-	V
Output "L" level	V_{OL}	$I_{OL}=2.1\text{mA}$	-	-	0.45	V

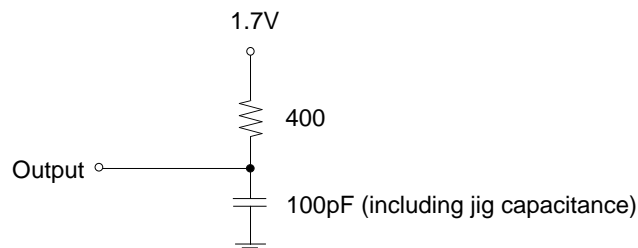
Voltage is relative to V_{SS} **AC Characteristics** $(V_{CC}=5V\pm 0.5V, T_a=0 \text{ to } 70^\circ\text{C})$

Parameter	Symbol	Condition	Min.	Max.	Unit
Random access cycle time	T_C	-	80	-	ns
Address access time	T_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	-	80	ns
Page set up time	T_{PSET}	NOTE(1)	100	-	ns
Page access cycle time	T_{PC}	-	50	-	ns
Page access time	T_{PAC}	-	-	50	ns
\overline{CE} access time	T_{CE}	$\overline{OE}=V_{IL}$	-	100	ns
\overline{OE} access time	T_{OE}	$\overline{CE}=V_{IL}$	-	50	ns
Output disable time	T_{CHZ}	$\overline{OE}=V_{IL}$	0	40	ns
	T_{OHZ}	$\overline{CE}=V_{IL}$	0	35	ns
Output hold time	T_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

NOTE(1) T_{PSET} is defined as the end of either \overline{CE} trailing edge or address transition in random access term until the first page address transition.

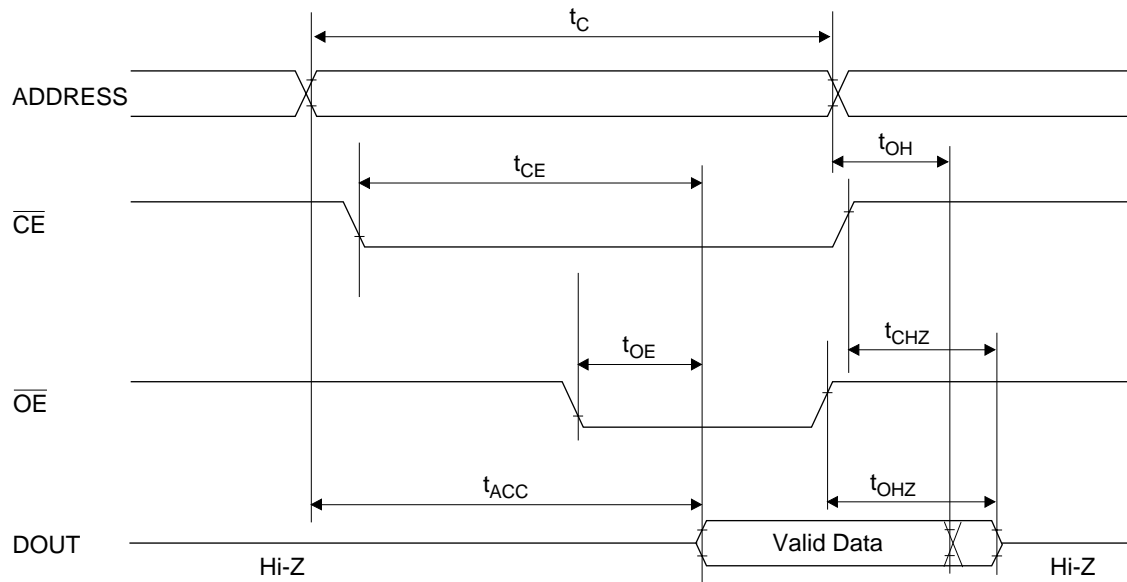
Measurement conditions

Input signal level	-----	0V/3V
Input timing reference level	-----	0.8V/2.0V
Output load	-----	1TTL gate + 100pF
Output timing reference level	-----	0.8V/2.0V

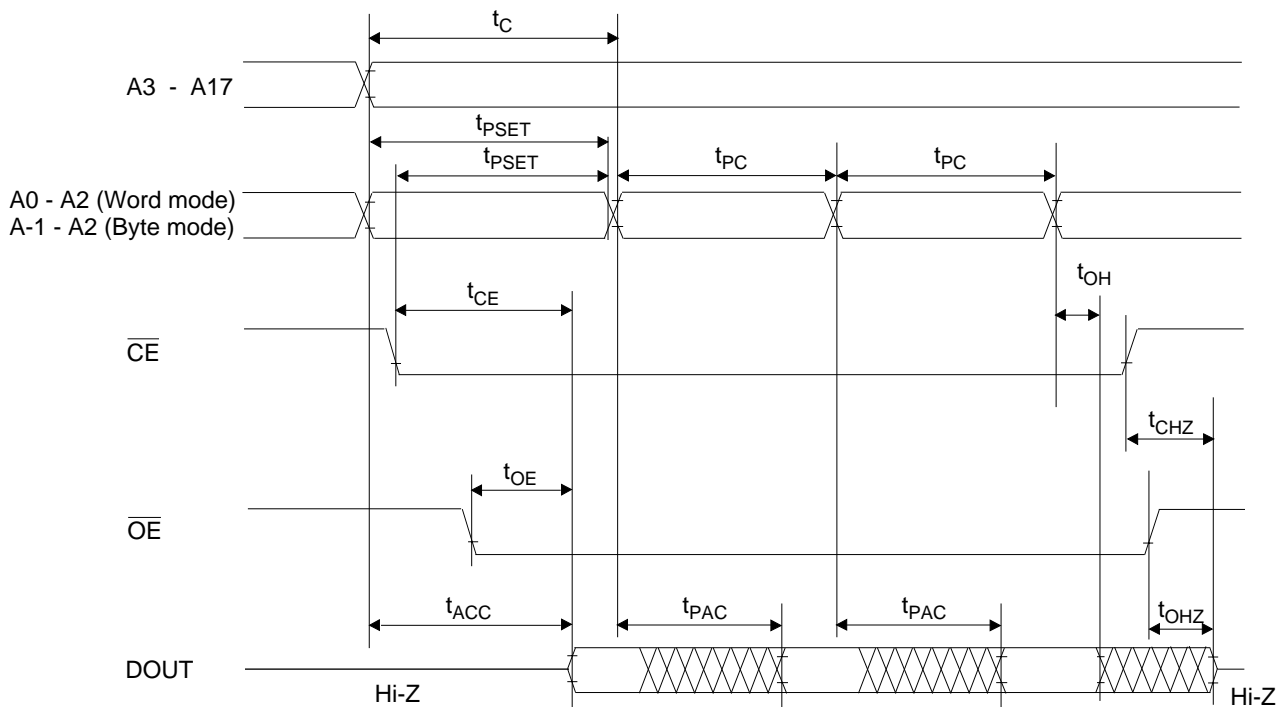


TIMING CHART

NORMAL MODE READ CYCLE



PAGE MODE READ CYCLE



ELECTRICAL CHARACTERISTICS (Programming operation)**DC Characteristics**

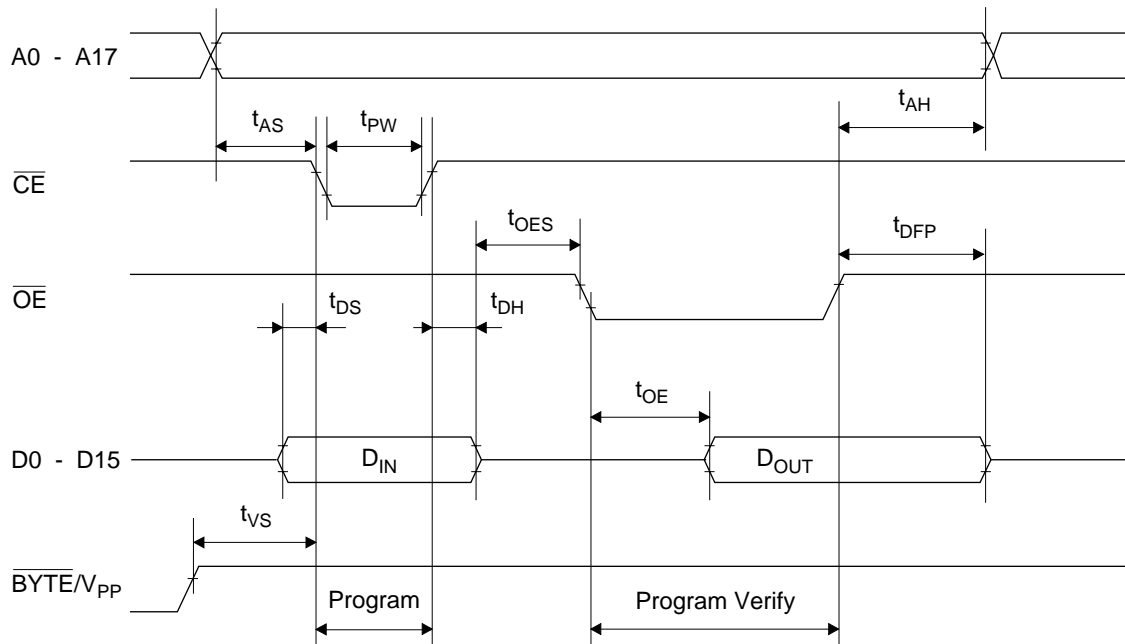
(Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I =V _{CC} +0.5V	-	-	10	μA
V _{PP} power supply current (Program)	I _{PP2}	$\overline{CE}=V_{IL}$	-	-	50	mA
V _{CC} power supply current	I _{CC}	-	-	-	80	mA
Input "H" level	V _{IH}	-	2.2	-	V _{CC} +0.5	V
Input "L" level	V _{IL}	-	-0.5	-	0.8	V
Output "H" level	V _{OH}	I _{OH} =-400μA	2.4	-	-	V
Output "L" level	V _{OL}	I _{OL} =2.1mA	-	-	0.45	V
Program voltage	V _{PP}	-	11.25	11.5	11.75	V
V _{CC} power supply voltage	V _{CC}	-	6.0	6.25	6.5	V

Voltage is relative to V_{SS}**AC Characteristics**(V_{CC}=6.25V±0.25V, V_{pp}=11.5V±0.25V, Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address set-up time	T _{AS}	-	2	-	-	μs
\overline{OE} set-up time	T _{OES}	-	2	-	-	μs
Data set-up time	T _{DS}	-	2	-	-	μs
Address hold time	T _{AH}	-	0	-	-	μs
Data hold time	T _{DH}	-	2	-	-	μs
Output float delay from \overline{OE}	T _{DFP}	-	0	-	130	ns
V _{PP} voltage set-up time	T _{VS}	-	2	-	-	μs
Program pulse width	T _{PW}	-	23	25	27	μs
Data valid from \overline{OE}	T _{OE}	-	-	-	150	ns

Programming Waveform

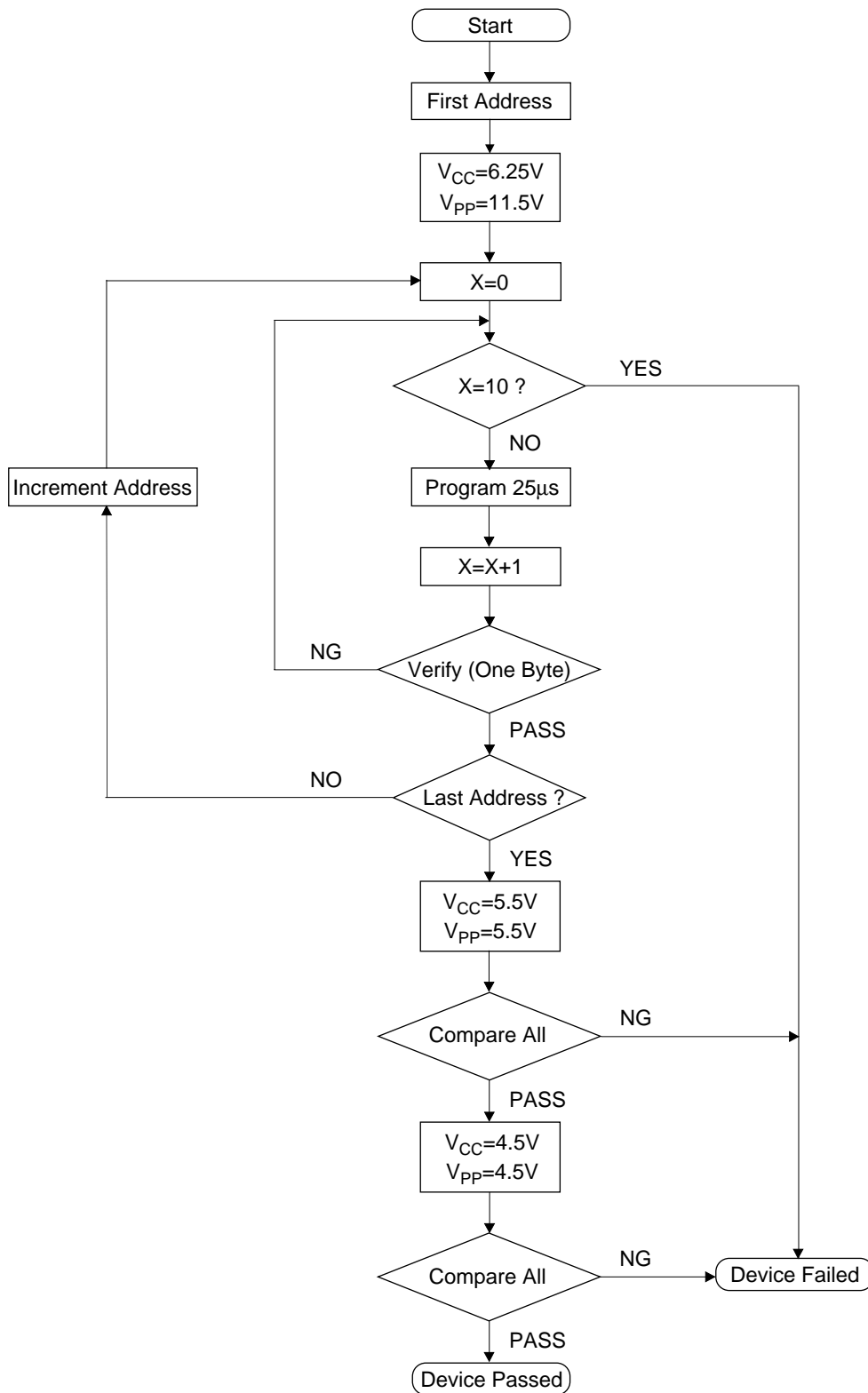


PIN Capacitance

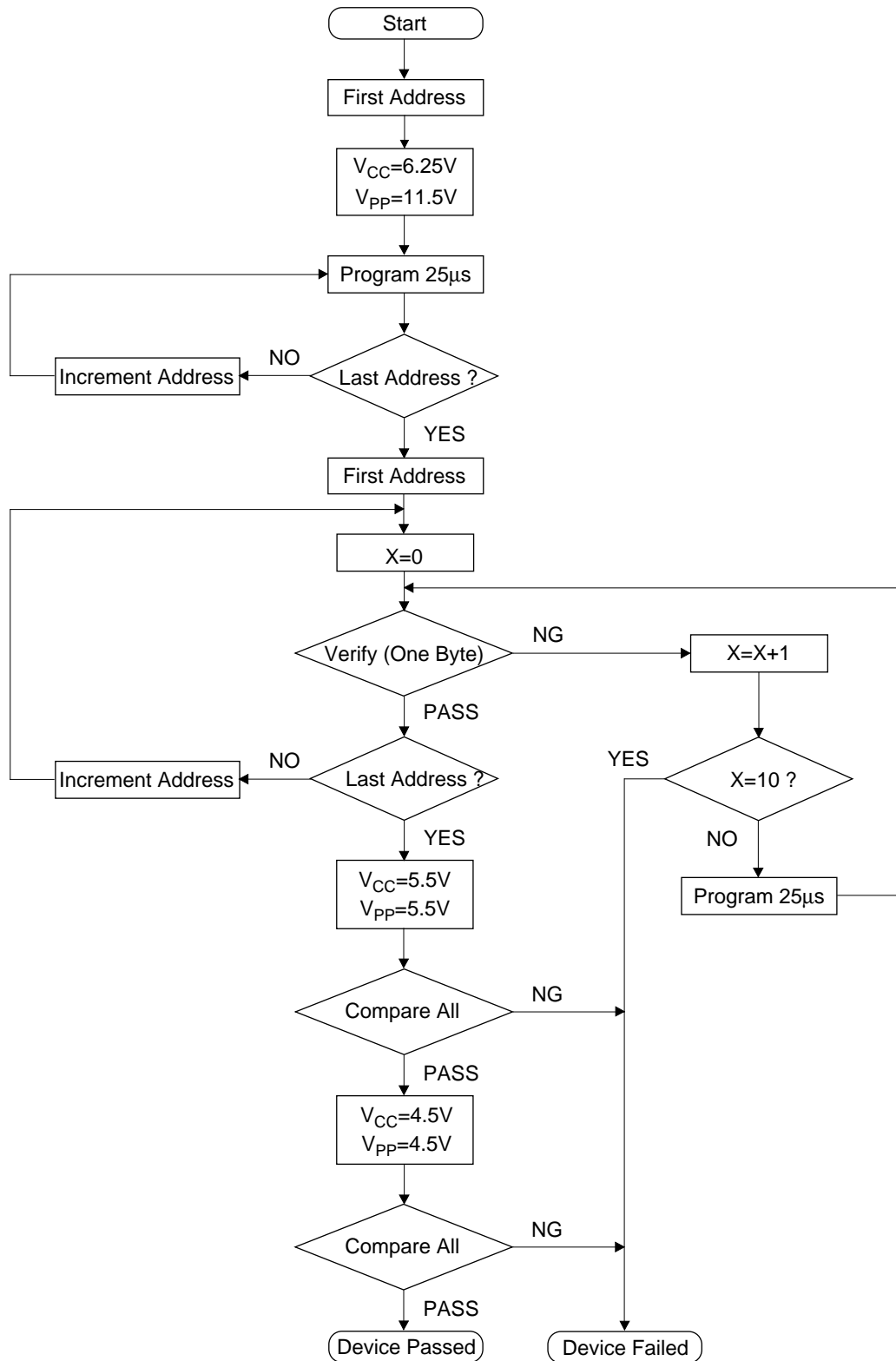
($V_{CC}=5V$, $T_a=25^{\circ}C$, $f=1MHz$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	$V_I=0V$	-	-	12	pF
BYTE/V _{PP}	C_{IN2}		-	-	60	
Output	C_{OUT}	$V_O=0V$	-	-	15	

High Speed Programming Algorithm (I)



High Speed Programming Algorithm (II)



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