National Semiconductor

PRELIMINARY
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PC87360
128-Pin LPC SuperI/O with Protection and Extensive GPIO Support

General Description

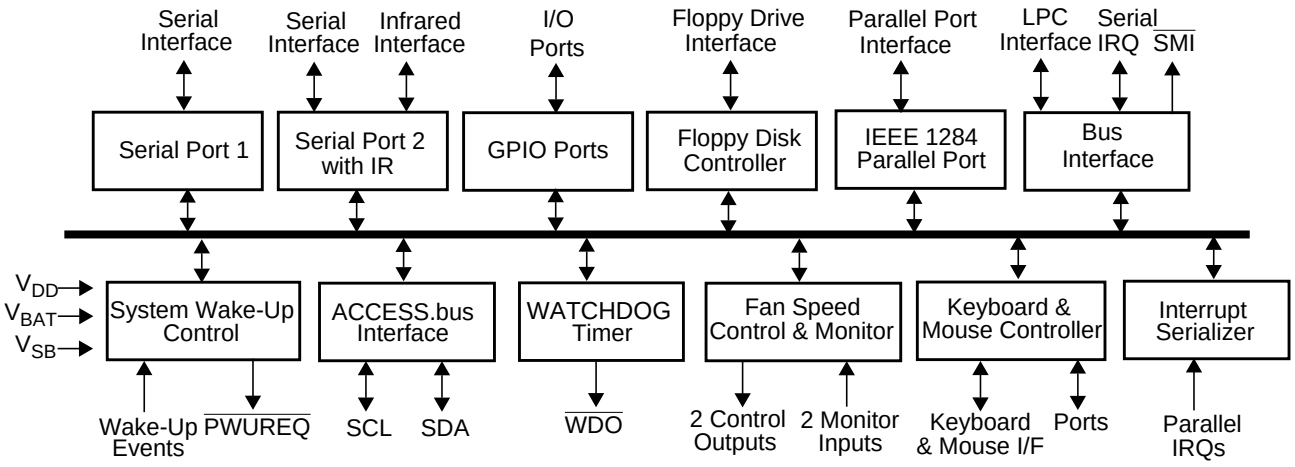
The PC87360 is the first member of National Semiconductor's 128-pin SuperI/O family to support the Low Pin Count (LPC) interface. It provides features to protect the system design, and supports 45 GPIO ports, many with Assert IRQ/$\overline{\text{SMI}}$/$\overline{\text{PWUREQ}}$ capability. The PC87360 is PC99 and ACPI compliant, and offers a single-chip solution to the most commonly used PC I/O peripherals.

The PC87360 also incorporates: Fan Speed Control and Monitoring for two fans, a Floppy Disk Controller (FDC), a Keyboard and Mouse Controller (KBC), a full IEEE 1284 Parallel Port, two enhanced Serial Ports (UARTs), one with Infrared (IR) support, an ACCESS.bus® Interface (ACB), System Wake-Up Control (SWC), Interrupt Serializer for Parallel IRQs and an enhanced WATCHDOG™ timer.

Outstanding Features

- Bus interface, based on Intel's *LPC Interface Specification* Revision 1.0, September 29th, 1997
- Protection features, including I/O access lock, GPIO lock and pin configuration lock
- 45 GPIO Ports (37 standard, including 23 with Assert IRQ/$\overline{\text{SMI}}$/$\overline{\text{PWUREQ}}$s interrupts; 8 V_{SB}-powered)
- Fan Speed Control and Monitor for two fans
- Interrupt Serializer (11 Parallel IRQs to Serial IRQ)
- Serial IRQ support (15 options)
- ACCESS.bus Interface, compatible with SMbus physical layer
- Blinking LEDs
- 128-pin PQFP Package

Block Diagram



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Features

- LPC System Interface
  - Synchronous cycles, up to 33 MHz bus clock
  - 8-bit I/O cycles
  - Up to four DMA channels
  - 8-bit DMA cycles
  - Basic read, write and DMA bus cycles are 13 clock cycles long
- Protection
  - Access lock to I/O ports ($\overline{\text{XLOCK}}$)
  - GPIO lock
  - Pin configuration lock
- 45 General-Purpose I/O (GPIO) Ports
  - 37 standard, with Assert IRQ/$\overline{\text{SMI}}$/$\overline{\text{PWUREQ}}$ for 23 ports
  - 8 V_{SB}-powered
  - Programmable drive type for each output pin (open-drain, push-pull or output disable)
  - Programmable option for internal pull-up resistor on each input pin
  - Output lock option
  - Input debounce mechanism
- PC99 and ACPI Compliant
  - PnP Configuration Register structure
  - Flexible resource allocation for all logical devices
    - Relocatable base address
    - 15 IRQ routing options
    - 4 optional 8-bit DMA channels (where applicable)
- Fan Speed Control and Fan Speed Monitor (FSCM)
  - Supports different fan types
  - Speed monitoring for two fans
    - Digital filtering of the tachometer input signal
    - Alarm for fan slower than programmable threshold speed
    - Alarm for fan stop
  - Two speed control lines with Pulse Width Modulation (PWM)
    - Output signal in the range of 6 Hz to 93.75 KHz
    - Duty cycle resolution of 1/256
- Interrupt Serializer
  - 11 Parallel IRQs to Serial IRQ
- Floppy Disk Controller (FDC)
  - Programmable write protect
  - FM and MFM mode support
  - Enhanced mode command for three-mode Floppy Disk Drive (FDD) support
  - Perpendicular recording drive support for 2.88 MB
  - Burst and non-burst modes
  - Full support for IBM Tape Drive register (TDR) implementation of AT and PS/2 drive types
  - 16-byte FIFO
  - Software compatible with the PC8477, which contains a superset of the FDC functions in the microDP8473, the NEC microPD765A and the N82077
  - High-performance, digital separator
  - Standard 5.25” and 3.5” FDD support
- Parallel Port
  - Software or hardware control
  - Enhanced Parallel Port (EPP) compatible with new version EPP 1.9 and IEEE 1284 compliant
  - EPP support for version EPP 1.7 of the Xircom specification
  - EPP support as mode 4 of the Extended Capabilities Port (ECP)
  - IEEE 1284 compliant ECP, including level 2
  - Selection of internal pull-up or pull-down resistor for Paper End (PE) pin
  - PCI bus utilization reduction by supporting a demand DMA mode mechanism and a DMA fairness mechanism
  - Protection circuit that prevents damage to the parallel port when a printer connected to it powers up or is operated at high voltages, even if the device is in power-down
  - Output buffers that can sink and source 14 mA
- Serial Port 1 (UART1)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
- Serial Port 2 with Infrared (UART2)
  - Software compatible with the 16550A and the 16450
  - Shadow register support for write-only bit monitoring
  - UART data rates up to 1.5 Mbaud
  - HP-SIR
  - ASK-IR option of SHARP-IR
  - DASK-IR option of SHARP-IR
  - Consumer Remote Control supports RC-5, RC-6, NEC, RCA and RECS 80
  - Non-standard DMA support – 1 or 2 channels
  - PnP dongle support
- Keyboard and Mouse Controller (KBC)
  - 8-bit microcontroller
  - Software compatible with the 8042AH and PC87911 microcontrollers
  - 2 KB custom-designed program ROM
  - 256 bytes RAM for data
  - Five programmable dedicated open-drain I/O lines
  - Asynchronous access to two data registers and one status register during normal operation
  - Support for both interrupt and polling
  - 93 instructions
  - 8-bit timer/counter
  - Support for binary and BCD arithmetic
  - Operation at 8 MHz,12 MHz or 16 MHz (programmable option)

Features (Continued)

— Can be customized by using the PC87323, which includes a RAM-based KBC as a development platform for KBC code

- ACCESS.bus Interface (ACB)
  - — Serial interface compatible with SMbus physical layer
  - — Compatible with Philips' I^2C®
  - — ACB master and slave
  - — Supports polling and interrupt controlled operation
  - — Optional internal pull-up on SDA and SCL pins
- WATCHDOG Timer
  - — Times out the system based on user-programmable time-out period
  - — System power-down capability for power saving
  - — User-defined trigger events to restart WATCHDOG
  - — Optional routing of WATCHDOG output on IRQ and/or SMI lines
- System Wake-Up Control (SWC)
  - — Power-up request upon detection of Keyboard, Mouse, $\overline{RI1}$, $\overline{RI2}$, $\overline{RING}$ activity and General-Purpose Input Events, as follows:
    - ❑ Preprogrammed Keyboard or Mouse sequence
    - ❑ External modem ring on serial port
    - ❑ Ring pulse or pulse train on the $\overline{RING}$ input signal
    - ❑ Preprogrammed CEIR address in a preselected standard (NEC, RCA or RC-5)
    - ❑ General-Purpose Input Events
    - ❑ IRQs of internal logical devices
  - — Optional routing of power-up request on IRQ and/or SMI lines
  - — Battery-backed event configuration
  - — Programmable VSB-powered output for blinking LEDs (LED1, LED2) control
- Clock Sources
  - — 48 MHz clock input
  - — LPC clock, up to 33 MHz
  - — On-chip low frequency clock generator for wake-up
- Power Supplies
  - — 3.3V supply operation
  - — Main (V_{DD})
  - — Standby (V_{SB})
  - — Battery backup (V_{BAT})
  - — All pins are 5V tolerant and back-drive protected, except LPC bus pins
- Strap Configuration
  - — Base Address (BADDR) strap to determine the base address of the Index-Data register pair
  - — Test strap to force the device into test mode (reserved for National Semiconductor use)

Datasheet Revision Record

Revision Date	Status	Comments
December 1998	Draft 1.0	Specifcations subject to change without notice
January 1999	Preliminary 1.0	Specification subject to change without notice; Power Supply Control and LED sections in Chapter 2 are incomplete

Item	Topic	Change/Correction	Location

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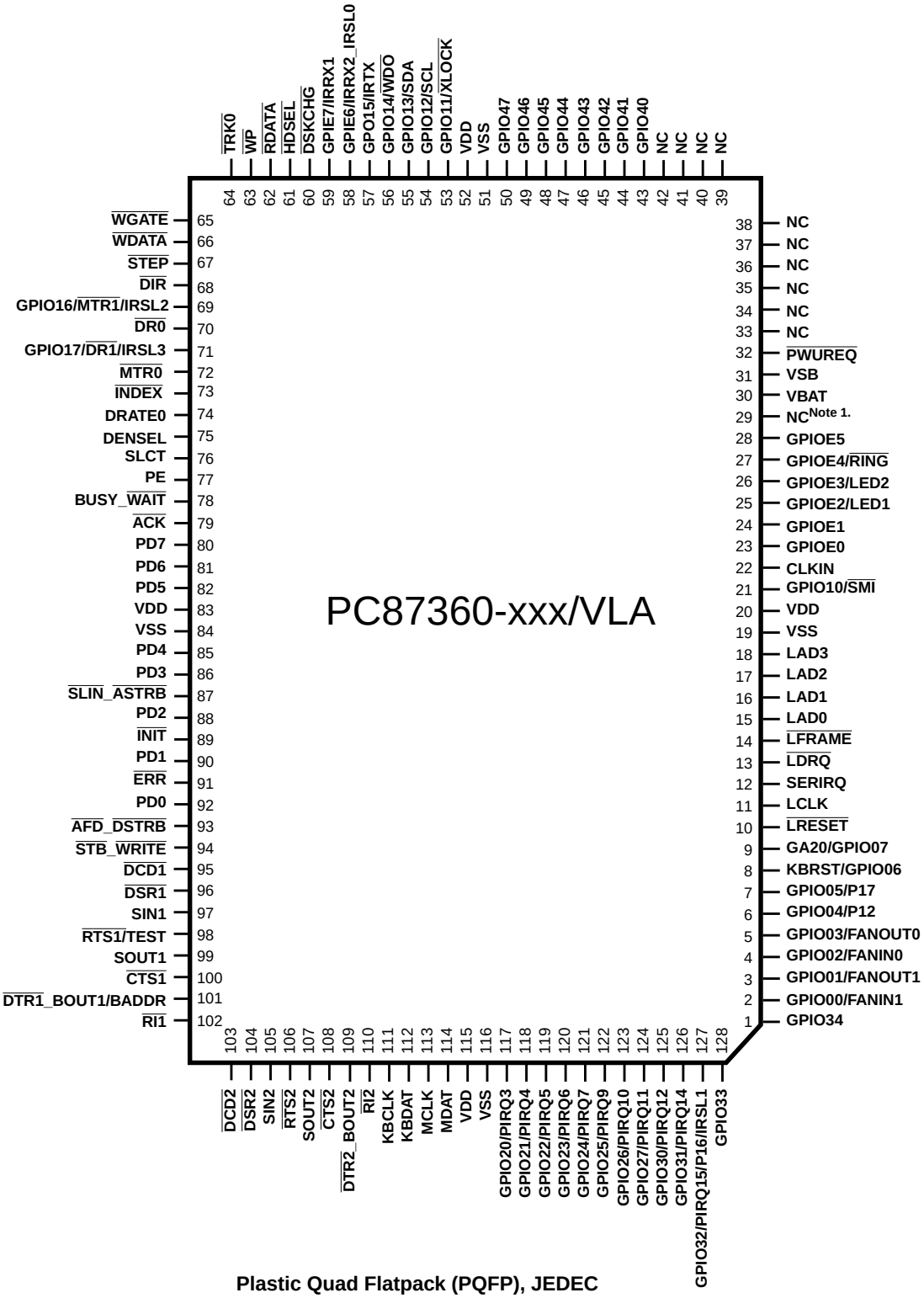
1.0 Signal/Pin Connection and Description

1.1 CONNECTION DIAGRAM



Plastic Quad Flatpack (PQFP), JEDEC
Order Number PC87360-xxx/VLA
See NS Package Number VLA128A

Note 1. For correct operation, this pin must be tied to V_{SS}.
xxx =Three character identifier for National data, and keyboard ROM and/or customer identification code

1.2 BUFFER TYPES AND SIGNAL/PIN DIRECTORY

Table 2 is an alphabetical list of all signals, cross-referenced to additional information for detailed functional descriptions, electrical DC characteristics, and pin multiplexing. The signal DC characteristics are denoted by a buffer type symbol, described briefly below and in further detail in Section 10.2. The pin multiplexing information refers to two different types of multiplexing:

- MUX - Multiplexed, denoted by a slash (/) between pins in the diagram in Section 1.1. Pins are shared between two different functions. Each function is associated with different board connectivity, and normally, the function selection is determined by the board design and cannot be changed dynamically. The multiplexing options must be configured by the BIOS upon power-up, in order to comply with the board implementation.
- MM - Multiple Mode, denoted by an underscore (_) between pins in the diagram in Section 1.1. Pins have two or more modes of operation within the same function. These modes are associated with the same external (board) connectivity. Mode selection may be controlled by the device driver, through the registers of the functional block, and do not require a special BIOS setup upon power-up. These pins are not considered multiplexed pins from the SuperI/O configuration perspective. The mode selection method (registers and bits) as well as the signal specification in each mode, are described within the functional description of the relevant functional block.

Table 1. Buffer Types

Symbol	Description
IN_C	Input, CMOS compatible
IN_{PCI}	Input, PCI 3.3V
IN_{SM}	Input, SMBus compatible
IN_{STRP}	Input, Strap pin with weak pull-down during strap time
IN_T	Input, TTL compatible
IN_{TS}	Input, TTL compatible with Schmidt Trigger
IN_{ULR}	Input, with serial UL Resistor
O_{PCI}	Output, PCI 3.3V
$O_{p/n}$	Output, push-pull buffer that is capable of sourcing *p* mA and sinking *n* mA
OD_n	Output, open-drain output buffer that is capable of sinking *n* mA
PWR	Power pin
GND	Ground pin

Table 2. SIgnal/Pin Directory

Signal	Pin(s)	Functional Group		DC Characteristics		MUX
		Name	Section	Buffer Type	Section	
$\overline{ACK}$	79	Parallel Port	1.4.9	IN_T	10.2.5	
$\overline{AFD}$_$\overline{DSTRB}$	93	Parallel Port	1.4.9	OD_{14}, $O_{14/14}$	10.2.9, 10.2.8	MM
$\overline{ASTRB}$	See $\overline{SLIN}$_$\overline{ASTRB}$					
BADDR	101	Strap Configuration	1.4.13	IN_{STRP}	10.2.4	MUX
BOUT1	See $\overline{DTR1}$_BOUT1					
BOUT2	See $\overline{DTR2}$_BOUT2					
BUSY_$\overline{WAIT}$	78	Parallel Port	1.4.9	IN_T	10.2.5	MM
CLKIN	22	Clock	1.4.3	IN_T	10.2.5	
$\overline{CTS1}$	100	Serial Port 1	1.4.12	IN_{TS}	10.2.6	

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	Functional Group		DC Characteristics		MUX
		Name	Section	Buffer Type	Section	
$\overline{CTS2}$	108	Serial Port 2	1.4.12	IN_{TS}	10.2.6	
$\overline{DCD1}$	95	Serial Port 1	1.4.12	IN_{TS}	10.2.6	
$\overline{DCD2}$	103	Serial Port 2	1.4.12	IN_{TS}	10.2.6	
DENSEL	75	FDC	1.4.5	$O_{2/12}$	10.2.8	
$\overline{DIR}$	68	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	
$\overline{DR0}$	70	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	
$\overline{DR1}$	71	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	MUX
$\overline{DRATE0}$	74	FDC	1.4.5	$O_{3/6}$	10.2.8	
$\overline{DSKCHG}$	60	FDC	1.4.5	IN_T	10.2.5	
$\overline{DSR1}$	96	Serial Port 1	1.4.12	IN_{TS}	10.2.6	
$\overline{DSR2}$	104	Serial Port 2	1.4.12	IN_{TS}	10.2.6	
$\overline{DSTRB}$	See $\overline{AFD}\_\overline{DSTRB}$					
$\overline{DTR1}$_BOUT1	101	Serial Port 1	1.4.12	$O_{3/6}$	10.2.8	MUX, MM
$\overline{DTR2}$_BOUT2	109	Serial Port 2	1.4.12	$O_{3/6}$	10.2.8	MUX, MM
$\overline{ERR}$	91	Parallel Port	1.4.9	IN_T	10.2.5	
FANIN0	4	Fan Speed	1.4.4	IN_{TS}	10.2.6	MUX
FANIN1	2	Fan Speed	1.4.4	IN_{TS}	10.2.6	MUX
FANOUT0	5	Fan Speed	1.4.4	$O_{2/14}$	10.2.8	MUX
FANOUT1	3	Fan Speed	1.4.4	$O_{2/14}$	10.2.8	MUX
GA20 (P21)	9	KBC	1.4.8	IN_T, OD_2	10.2.5, 10.2.9	MUX
GPIE6-7	58-59	System Wake-Up	1.4.14	IN_{TS}	10.2.6	MUX
GPIO00-07	2-9	GPIO Port	1.4.6	IN_{TS}, OD_6, $O_{3/6}$	10.2.6, 10.2.9, 10.2.8	MUX
GPIO10 GPIO11-14 GPO15 GPIO16-17	21 53-56 57 69, 71	GPIO Port	1.4.6	IN_{TS}, OD_6, $O_{3/6}$	10.2.6, 10.2.9, 10.2.8	MUX
GPIO20-27	117-124	GPIO Port	1.4.6	IN_{TS}, OD_6, $O_{3/6}$	10.2.6, 10.2.9, 10.2.8	MUX
GPIO30-33 GPIO34	125-128 1	GPIO Port	1.4.6	IN_{TS}, OD_6, $O_{3/6}$	10.2.6, 10.2.9, 10.2.8	MUX
GPIO40-47	43-50	GPIO Port	1.4.6	IN_{TS}, OD_6, $O_{3/6}$	10.2.6, 10.2.9, 10.2.8	
GPIOE0-5	23-28	System Wake-Up	1.4.14	IN_{TS}, OD_6, $O_{3/6}$	10.2.6, 10.2.9, 10.2.8	
$\overline{HDSEL}$	61	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	
$\overline{INDEX}$	73	FDC	1.4.5	IN_T	10.2.5	
$\overline{INIT}$	89	Parallel Port	1.4.9	OD_{14}, $O_{14/14}$	10.2.9, 10.2.8	
IRRX1	59	Infrared	1.4.7	IN_{TS}	10.2.6	MUX
IRRX2_IRSL0	58	Infrared	1.4.7	IN_{TS}, $O_{3/6}$	10.2.6, 10.2.8	MUX, MM

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	Functional Group		DC Characteristics		MUX
		Name	Section	Buffer Type	Section	
IRSL1	127	Infrared	1.4.7	IN_T, $O_{3/6}$	10.2.5, 10.2.8	MUX
IRSL2	69	Infrared	1.4.7	IN_T, $O_{3/6}$	10.2.5, 10.2.8	MUX
IRSL3	71	Infrared	1.4.7	IN_T	10.2.5	MUX
IRTX	57	Infrared	1.4.7	$O_{6/12}$	10.2.8	MUX
KBCLK	111	KBC	1.4.8	IN_{TS}, OD_{14}	10.2.6, 10.2.9	
KBDAT	112	KBC	1.4.8	IN_{TS}, OD_{14}	10.2.6, 10.2.9	
KBRST (P20)	8	KBC	1.4.8	IN_{TS}, OD_2	10.2.6, 10.2.9	MUX
LAD0-3	15-18	Bus Interface	1.4.2	IN_{PCI}, O_{PCI}	10.2.2, 10.2.7	
LED1, LED2	25, 26	System Wake-Up	1.4.14	$O_{12/12}$	10.2.8	MUX
LCLK	11	Bus Interface	1.4.2	IN_{PCI}	10.2.2	
$\overline{\text{LDRQ}}$	13	Bus Interface	1.4.2	O_{PCI}	10.2.7	
$\overline{\text{LFRAME}}$	14	Bus Interface	1.4.2	IN_{PCI}	10.2.2	
$\overline{\text{LRESET}}$	10	Bus Interface	1.4.2	IN_{PCI}	10.2.2	
MCLK	13	KBC	1.4.8	IN_{TS}, OD_{14}	10.2.6, 10.2.9	
MDAT	114	KBC	1.4.8	IN_{TS}, OD_{14}	10.2.6, 10.2.9	
$\overline{\text{MTR0}}$	72	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	
$\overline{\text{MTR1}}$	69	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	MUX
P12, P16, P17	6,127, 7	KBC	1.4.8	IN_T, OD_2	10.2.5, 10.2.9	MUX
PD7-5 PD4-3, PD2, PD1 PD0	80-82 85-86 88, 90 92	Parallel Port	1.4.9	IN_T, OD_{14}, $O_{14/14}$	10.2.5, 10.2.9, 10.2.8	
PE	77	Parallel Port	1.4.9	IN_T	10.2.5	
PIRQ3-7 PIRQ9-12 PIRQ14-15	117-121 122-125 126-127	Bus Interface	1.4.2	IN_{TS}	10.2.6	MUX
$\overline{\text{PWUREQ}}$	32	System Wake-Up	1.4.14	OD_6	10.2.9	
$\overline{\text{RDATA}}$	62	FDC	1.4.5	IN_T	10.2.5	
$\overline{\text{RI1}}$	102	Serial Port 1	1.4.12	IN_{TS}	10.2.6	
$\overline{\text{RI2}}$	110	Serial Port 2	1.4.12	IN_{TS}	10.2.6	
$\overline{\text{RING}}$	27	System Wake-Up	1.4.14	IN_{TS}	10.2.6	MUX
$\overline{\text{RTS1}}$	98	Serial Port 1	1.4.12	$O_{3/6}$	10.2.8	MUX
$\overline{\text{RTS2}}$	106	Serial Port 2	1.4.12	$O_{3/6}$	10.2.8	
SCL	54	ACB	1.4.1	IN_T, OD_6, $O_{3/6}$	10.2.5, 10.2.9, 10.2.8	MUX
SDA	55	ACB	1.4.1	IN_T, OD_6, $O_{3/6}$	10.2.5, 10.2.9, 10.2.8	MUX
SERIRQ	12	Bus Interface	1.4.2	IN_{PCI}, O_{PCI}	10.2.2, 10.2.7	

1.0 Signal/Pin Connection and Description (Continued)

Signal	Pin(s)	Functional Group		DC Characteristics		MUX
		Name	Section	Buffer Type	Section	
SIN1	97	Serial Port 1	1.4.12	IN_{TS}	10.2.6	
SIN2	105	Serial Port 2	1.4.12	IN_{TS}	10.2.6	
SLCT	76	Parallel Port	1.4.9	IN_{T}	10.2.5	
$\overline{\text{SLIN\_ASTRB}}$	87	Parallel Port	1.4.9	OD_{14}, $O_{14/14}$	10.2.9, 10.2.8	MM
$\overline{\text{SMI}}$	21	Bus Interface	1.4.2	OD_{12}	10.2.9	MUX
SOUT1	99	Serial Port 1	1.4.12	$O_{3/6}$	10.2.8	MUX
SOUT2	107	Serial Port 2	1.4.12	$O_{3/6}$	10.2.8	
$\overline{\text{STEP}}$	67	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	
$\overline{\text{STB\_WRITE}}$	94	Parallel Port	1.4.9	OD_{14}, $O_{14/14}$	10.2.9, 10.2.8	MM
TEST	98	Strap Configuration	1.4.13	IN_{STRP}	10.2.4	MUX
$\overline{\text{TRK0}}$	64	FDC	1.4.5	IN_{T}	10.2.5	
V_{BAT}	30	Power and Ground	1.4.10	IN_{ULR}	N/A	
V_{DD}	20, 52, 83, 115	Power and Ground	1.4.10	PWR	N/A	
V_{SB}	31	Power and Ground	1.4.10	PWR	N/A	
V_{SS}	19, 51, 84, 116	Power and Ground	1.4.10	GND	N/A	
$\overline{\text{WAIT}}$	See BUSY_$\overline{\text{WAIT}}$					
$\overline{\text{WDATA}}$	66	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	
$\overline{\text{WDO}}$	56	WATCHDOG	1.4.15	OD_{6}, $O_{3/6}$	10.2.9, 10.2.8	MUX
$\overline{\text{WGATE}}$	65	FDC	1.4.5	OD_{12}, $O_{2/12}$	10.2.9, 10.2.8	
$\overline{\text{WP}}$	63	FDC	1.4.5	IN_{T}	10.2.5	
$\overline{\text{WRITE}}$	See $\overline{\text{STB}}$_$\overline{\text{WRITE}}$					
$\overline{\text{XLOCK}}$	53	Protection	1.4.11	IN_{T}	10.2.5	MUX

1.3 PIN MULTIPLEXING

The multiplexing options and the associated setup configuration for all pins are described in Table 3. A multiplexing option can be chosen on one pin only per group.

Table 3. Pin Multiplexing Configuration

Pin(s)	Default			Alternate		
	Signal	I/O	Configuration	Signal	I/O	Configuration
2	GPIO00	I/O	SIOCF2, Bit 2 = 0	FANIN1	I	SIOCF2, Bit 2 = 1
3	GPIO01	I/O	SIOCF2, Bit 3 = 0	FANOUT1	O	SIOCF2, Bit 3 = 1
4	GPIO02	I/O	SIOCF2, Bit 4 = 0	FANIN0	I	SIOCF2, Bit 4 = 1
5	GPIO03	I/O	SIOCF2, Bit 5 = 0	FANOUT0	O	SIOCF2, Bit 5 = 1
6	GPIO04	I/O	SIOCF2, Bit 6 = 0	P12	I/O	SIOCF2, Bit 6 = 1
7	GPIO05	I/O	SIOCF2, Bit 7 = 0	P17	I/O	SIOCF2, Bit 7 = 1
8	KBRST (P20)		SIOCF3, Bit 0 = 1	GPIO06	I/O	SIOCF3, Bit 0 = 0
9	GA20 (P21)		SIOCF3, Bit 1 = 1	GPIO07	I/O	SIOCF3, Bit 1 = 0
21	GPIO10	I/O	SIOCF3, Bit 2 = 0	$\overline{\text{SMI}}$	O	SIOCF3, Bit 2 = 1
25	GPIOE2	I/O	SIOCFA, Bits 2-1 = 00	LED1	O	SIOCFA, Bits 2-1 = 01
26	GPIOE3	I/O	SIOCFA, Bit 3 = 0	LED2	O	SIOCFA, Bit 3 =1
27	GPIOE4	I/O	SIOCFA, Bits 5-4 = 00	$\overline{\text{RING}}$	I	SIOCFA, Bits 5-4 = 01
53	GPIO11	I/O	SIOCF3, Bit 4 = 0	$\overline{\text{XLOCK}}$	I	SIOCF3, Bit 4 = 1
54	GPIO12	I/O	SIOCF3, Bit 5 = 0	SCL	I/O	SIOCF3, Bit 5 = 1
55	GPIO13	I/O	SIOCF3, Bit 5 = 0	SDA	I/O	SIOCF3, Bit 5 = 1
56	GPIO14	I/O	SIOCF3, Bit 6 = 0	$\overline{\text{WDO}}$	O	SIOCF3, Bit 6 = 1
57	GPO15	O	SIOCF3, Bit 7 = 0	IRTX	O	SIOCF3, Bit 7 = 1
58	GPIE6	I	SIOCFB, Bit 0 = 0	IRRX2_IRSL0	I/O	SIOCFB, Bit 0 = 1
59	GPIE7	I	SIOCFB, Bit 1 = 0	IRRX1	I	SIOCFB, Bit 1 = 1
69	GPIO16	I/O	SIOCF4, Bits 1-0 = 00	$\overline{\text{MTR1}}$	O	SIOCF4, Bits 1-0 = 01
				IRSL2	I/O	SIOCF4, Bits 1-0 = 10
71	GPIO17	I/O	SIOCF4, Bits 3-2 = 00	$\overline{\text{DR1}}$	O	SIOCF4, Bits 3-2 = 01
				IRSL3	I	SIOCF4, Bits 3-2 = 10
117	GPIO20	I/O	SIOCF4, Bits 4,P[Note 1.] = 00	PIRQ3	I	SIOCF4, Bits 4,P = X1
118	GPIO21	I/O	SIOCF4, Bits 4,P[Note 1.] = 00	PIRQ4	i	SIOCF4, Bits 4,P = X1
119	GPIO22	I/O	SIOCF4, Bits 4,P[Note 1.] = 00	PIRQ5	I	SIOCF4, Bits 4,P = X1
120	GPIO23	I/O	SIOCF4, Bits 4,P[Note 1.] = 00	PIRQ6	I	SIOCF4, Bits 4,P = X1
121	GPIO24	I/O	SIOCF4, Bits 4,P[Note 1.] = 00	PIRQ7	I	SIOCF4, Bits 4,P = X1
122	GPIO25	I/O	SIOCF4, Bits 4,P[Note 1.] = 00	PIRQ9	I	SIOCF4, Bits 4,P = X1
123	GPIO26	I/O	SIOCF4, Bits 4,P[Note 1.] = 00	PIRQ10	I	SIOCF4, Bits 4,P = X1
124	GPIO27	I/O	SIOCF4, Bits 4,P[Note 1.] = 00	PIRQ11	I	SIOCF4, Bits 4,P = X1
125	GPIO30	I/O	SIOCF4, Bits 5,P[Note 1.] = 00	PIRQ12	I	SIOCF4, Bits 5,P = X1
126	GPIO31	I/O	SIOCF4, Bits 5,P[Note 1.] = 00	PIRQ14	I	SIOCF4, Bits 5,P = X1

1.0 Signal/Pin Connection and Description (Continued)

Pin(s)	Default			Alternate		
	Signal	I/O	Configuration	Signal	I/O	Configuration
127	GPIO32	I/O	SIOCF4, Bits 7,6,P[Note 1.] = 000	P16	I/O	SIOCF4, Bits 7,6,P[Note 1.] = 010
				IRSL1	I/O	SIOCF4, Bits 7,6,P[Note 1.] = 100
				PIRQ15	I	SIOCF4, Bits 7,6,P[Note 1.] = XX1

Note 1. P = SIOCF1, Bit 6 (Pins 117-127 Select PIRQ)

1.4 DETAILED SIGNAL/PIN DESCRIPTIONS

This section describes all signals, organized in functional groups.

1.4.1 ACCESS.bus Interface (ACB)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
SCL	54	I/O	IN_{SM}/OD_6	V_{DD}	**ACCESS.bus Clock Signal.** An internal pull-up is optional, depending upon the ACCESS.bus configuration register.
SDA	55	I/O	IN_{SM}/OD_6	V_{DD}	**ACCESS.bus Data Signal.** An internal pull-up is optional, depending upon the ACCESS.bus configuration register.

1.4.2 Bus Interface

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
LAD0-3	15-18	I/O	IN_{PCI}/O_{PCI}	V_{DD}	**LPC Address-Data.** Multiplexed command, address bi-directional data and cycle status.
LCLK	11	I	IN_{PCI}	V_{DD}	**LPC Clock**. Practically the PCI clock (up to 33 MHz)
$\overline{\text{LDRQ}}$	13	O	O_{PCI}	V_{DD}	**LPC DMA Request**. Encoded DMA request for LPC I/F.
$\overline{\text{LFRAME}}$	14	I	IN_{PCI}	V_{DD}	**LPC Frame**. Low pulse indicates the beginning of new LPC cycle or termination of a broken cycle.
$\overline{\text{LRESET}}$	10	I	IN_{PCI}	V_{DD}	**LPC Reset.** Practically the PCI system reset.
PIRQ3-7 PIRQ9-12 PIRQ14-15	117-121 122-125 126-127	I	IN_{TS}	V_{DD}	**Parallel Interrupt.** Converts Parallel Port interrupts into Serial Interrupts by means of the Interrupt Serializer.
SERIRQ	12	I/O	IN_{PCI}/O_{PCI}	V_{DD}	**Serial IRQ.** The interrupt requests are serialized over a single pin, where each internal IRQ signal is delivered during a designated time slot.
$\overline{\text{SMI}}$	21	OD	OD_{12}	V_{DD}	**System Management Interrupt**

1.4.3 Clock

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
CLKIN	22	I	IN_T	V_{DD}	**Clock In.** 48 MHz clock input.

1.4.4 Fan Speed Control and Monitor (FSCM)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
FANIN0 FANIN1	4 2	I	IN_{TS}	V_{DD}	**Fan Inputs.** Used to feed the fan's tachometer pulse to the Fan Speed Monitor. The rising edge indicates the completion of a half (or full) revolution of the fan.
FANOUT0 FANOUT1	5 3	O	$O_{2/14}$	V_{DD}	**Fan Outputs.** Pulse Width Modulation (PWM) signals, used to control the speed of cooling fans by controlling the voltage supplied to the fan's motor.

1.0 Signal/Pin Connection and Description (Continued)

1.4.5 Floppy Disk Controller (FDC)

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
DENSEL	75	O	$O_{2/12}$	V_{DD}	**Density Select.** Indicates that a high FDC density data rate (500 Kbps or 1 Mbps) or a low density data rate (250 or 300 Kbps) is selected. DENSEL polarity is controlled by bit 5 of the FDC Configuration Register.
$\overline{DIR}$	68	O	OD_{12}, $O_{2/12}$	V_{DD}	**Direction.** Determines the direction of the Floppy Disk Drive (FDD) head movement (active = step in, inactive = step out) during a seek operation. During reads or writes, $\overline{DIR}$ is inactive.
$\overline{DR0}$	70	O	OD_{12}, $O_{2/12}$	V_{DD}	**Drive Select 0.** Decoded drive select output signal. $\overline{DR0}$ is controlled by bit 0 of the Digital Output Register (DOR).
$\overline{DR1}$	71	O	OD_{12}, $O_{2/12}$	V_{DD}	**Drive Select 1.** Decoded drive select output signal. $\overline{DR0}$ is controlled by bit 1 of the Digital Output Register (DOR).
DRATE0	74	O	$O_{3/6}$	V_{DD}	**Data Rate 0.** Reflects the value of bit 0 of the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last. Output from the pin is push-pull buffered.
$\overline{DSKCHG}$	60	I	IN_T	V_{DD}	**Disk Change.** Indicates if the drive door has been opened. The state of this pin is stored in the Digital Input Register (DIR). This pin can also be configured as the RGATE data separator diagnostic input signal via the MODE command.
$\overline{HDSEL}$	61	O	OD_{12}, $O_{2/12}$	V_{DD}	**Head Select.** Determines which side of the FDD is accessed. Active low selects side 1, inactive selects side 0.
$\overline{INDEX}$	73	I	IN_T	V_{DD}	**Index.** Indicates the beginning of an FDD track.
$\overline{MTR0}$	72	O	OD_{12}, $O_{2/12}$	V_{DD}	**Motor Select 0.** Active low, motor enable line for drives 0, controlled by bits D7-4 of the Digital Output Register (DOR).
$\overline{MTR1}$	69	O	OD_{12}, $O_{2/12}$	V_{DD}	**Motor Select 1.** Active low, motor enable lines for drives 1, controlled by bits D7-4 of the Digital Output Register (DOR).
$\overline{RDATA}$	62	I	IN_T	V_{DD}	**Read Data.** Raw serial input data stream read from the FDD.
$\overline{STEP}$	67	O	OD_{12}, $O_{2/12}$	V_{DD}	**Step.** Issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
$\overline{TRK0}$	64	I	IN_T	V_{DD}	**Track 0.** Indicates to the controller that the head of the selected floppy disk drive is at track 0.
$\overline{WDATA}$	66	O	OD_{12}, $O_{2/12}$	V_{DD}	**Write Data**. Carries out the pre-compensated serial data that is written to the floppy disk drive. Pre-compensation is software selectable.
$\overline{WGATE}$	65	O	OD_{12}, $O_{2/12}$	V_{DD}	**Write Gate.** Enables the write circuitry of the selected disk drive. WGATE is designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.
$\overline{WP}$	63	I	IN_T	V_{DD}	**Write Protected.** Indicates that the disk in the selected drive is write protected. A software programmable configuration bit (FDC configuration at Index F0h, Logical Device 0) can force an active write-protect indication to the FDC, regardless of the status of this pin.

1.4.6 General-Purpose Input/Output (GPIO) Ports

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
GPIO00-07	2-9	I/O	IN_{TS}/ OD_6, $O_{3/6}$	V_{DD}	**General-Purpose I/O Port 0, bits 0-7.** Each pin is configured independently as input or I/O, with or without static pull-up, and with either open-drain or push-pull output type. The port support interrupt assertion and each pin can be enabled or masked as an interrupt source.
GPIO10 GPIO11-14 GPO15 GPIO16-17	21 53-56 57 69, 71	I/O	IN_{TS}/ OD_6, $O_{3/6}$	V_{DD}	**General-Purpose I/O Port 1, bits 0-7.** Same as Port 0. Bit 5 is output only with low output as default.
GPIO20-27	117-124	I/O	IN_{TS}/ OD_6, $O_{3/6}$	V_{DD}	**General-Purpose I/O Port 2, bits 0-7.** Similar to port 0, but without the interrupt assertion capability.
GPIO30-33 GPIO34	125-128 1	I/O	IN_{TS}/ OD_6, $O_{3/6}$	V_{DD}	**General-Purpose I/O Port 3, bits 0-4.** Similar to port 0, but without the interrupt assertion capability. Bits 5, 6 and 7 are not implemented.
GPIO40-47	43-50	I/O	IN_{TS}/ OD_6, $O_{3/6}$	V_{DD}	**General-Purpose I/O Port 4, bits 0-7.** Same as Port 0.

1.4.7 Infrared (IR)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
IRRX1	59	I	IN_{TS}	V_{DD}, V_{SB}	**IR Receive 1.** Primary input to receive serial data from the IR transceiver. Monitored during power-off for wake-up event detection.
IRRX2_IRSL0	58	I/O	$IN_{TS}/O_{3/6}$	V_{DD}, V_{SB}	**IRRX2 - IR Receive 2.** Auxiliary IR receiver input to support a second transceiver. Monitored during power-off for wake-up event detection.
IRSL1	127	I/O	$IN_T/O_{3/6}$	V_{DD}	
IRSL2	69	I/O	$IN_T/O_{3/6}$	V_{DD}	**IRSL3-0 IR Select**. Output are used to control the IR transceivers. Input for PnP identification of plug-in IR transceiver (dongle).
IRSL3	71	I	IN_T	V_{DD}	After reset, the dual-function IRSLX pins wake up in input mode. After the ID is read by the IR driver, they may be put into output mode. The output mode is controlled by Serial Port 2.
IRTX	57	O	$O_{6/12}$	V_{DD}	**IR Transmit.** IR serial output data.

1.4.8 Keyboard and Mouse Controller (KBC)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
GA20	9	I/O	IN_T/OD_2	V_{DD}	**Gate A20.** KBC gate A20 (P21) output.
KBCLK	111	I/O	IN_{TS}/OD_{14}	V_{DD}, V_{SB}	**Keyboard Clock.** Transfers the keyboard clock between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is driven by the internal, inverted KBC P26 signal, and is connected internally to the T0 signal of the KBC. External pull-up resistor to 5V is required (for PS/2 compliance). The pin is monitored for wake-up event detection. To enable the activity during power off, it must be pulled up to Keyboard and Mouse standby voltage.
KBDAT	112	I/O	IN_{TS}/OD_{14}	V_{DD}, V_{SB}	**Keyboard Data.** Transfers the keyboard data between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is driven by the internal, inverted KBC P27 signal, and is connected internally to KBC P10. External pull-up resistor to 5V is required (for PS/2 compliance). The pin is monitored for wake-up event detection. To enable the activity during power off, it must be pulled up to Keyboard and Mouse standby voltage.
KBRST	8	I/O	IN_T/OD_2	V_{DD}	**KBD Reset.** Keyboard Reset (P20) output.
MCLK	113	I/O	IN_{TS}/OD_{14}	V_{DD}, V_{SB}	**Mouse Clock.** Transfers the mouse clock between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is driven by the internal, inverted KBC P23 signal, and is connected internally to KBC T1. External pull-up resistor to 5V is required (for PS/2 compliance). The pin is monitored for wake-up event detection. To enable the activity during power off, it must be pulled up to Keyboard and Mouse standby voltage.
MDAT	114	I/O	IN_{TS}/OD_{14}	V_{DD}, V_{SB}	**Mouse Data.** Transfers the mouse data between the SuperI/O chip and the external keyboard using the PS/2 protocol. This pin is driven by the internal, inverted KBC P22 signal, and is connected internally to KBC P11. External pull-up resistor to 5V is required (for PS/2 compliance). The pin is monitored for wake-up event detection. To enable the activity during power off, it must be pulled up to Keyboard and Mouse standby voltage.
P12, P16, P17	6,127, 7	I/O	IN_T/OD_2	V_{DD}	**I/O Port.** KBC open-drain signal for general-purpose input and output, controlled by KBC firmware.

1.4.9 Parallel Port

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{ACK}$	79	I	IN_T	V_{DD}	**Acknowledge.** Pulsed low by the printer to indicate that it has received data from the Parallel Port.
$\overline{AFD}$_$\overline{DSTRB}$	93	O	OD_{14}, $O_{14/14}$	V_{DD}	**AFD - Automatic Feed.** When low, instructs the printer to automatically feed a line after printing each line. This pin is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be attached to this pin. **DSTRB - Data Strobe (EPP).** Active low, used in EPP mode to denote a data cycle. When the cycle is aborted, $\overline{DSTRB}$ becomes inactive (high).
BUSY_$\overline{WAIT}$	78	I	IN_T	V_{DD}	**Busy.** Set high by the printer when it cannot accept another character. **Wait.** In EPP mode, the Parallel Port device uses this active low signal to extend its access cycle.
$\overline{ERR}$	91	I	IN_T	V_{DD}	**Error.** Set active low by the printer when it detects an error.

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{INIT}$	89	O	OD_{14}, $O_{14/14}$	V_{DD}	**Initialize.** When low, initializes the printer. This signal is in TRI-STATE after a 1 is loaded into the corresponding control register bit. Use an external 4.7 KΩ pull-up resistor.
PD7-5 PD4-3, PD2, PD1 PD0	80-82 85-86 88, 90 92	I/O	IN_T/ OD_{14}, $O_{14/14}$	V_{DD}	**Parallel Port Data.** Transfer data to and from the peripheral data bus and the appropriate Parallel Port data register. These signals have a high current drive capability.
PE	77	I	IN_T	V_{DD}	**Paper End.** Set high by the printer when it is out of paper. This pin has an internal weak pull-up or pull-down resistor.
SLCT	76	I	IN_T	V_{DD}	**Select.** Set active high by the printer when the printer is selected.
$\overline{SLIN}$_$\overline{ASTRB}$	87	O	OD_{14}, $O_{14/14}$	V_{DD}	**SLIN - Select Input.** When low, selects the printer. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. Uses an external 4.7 KΩ pull-up resistor. **ASTRB - Address Strobe (EPP).** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{ASTRB}$ becomes inactive (high).
$\overline{STB}$_$\overline{WRITE}$	94	O	OD_{14}, $O_{14/14}$	V_{DD}	**STB - Data Strobe.** When low, Indicates to the printer that valid data is available at the printer port. This signal is in TRI-STATE after a 0 is loaded into the corresponding control register bit. An external 4.7 KΩ pull-up resistor should be employed. **WRITE - Write Strobe.** Active low, used in EPP mode to denote an address or data cycle. When the cycle is aborted, $\overline{WRITE}$ becomes inactive (high).

1.4.10 Power and Ground

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
V_{BAT}	30	I	IN_{ULR}	-	**Battery Power Supply.** Provides battery back-up to the System Wake-Up Control registers, when V_{SB} is lost (power-fail). The pin is connected to the internal logic through a series resistor for UL protection.
V_{DD}	20, 52, 83, 115	I	PWR	-	**Main 3.3V Power Supply**
V_{SB}	31	I	PWR	-	**Standby 3.3V Power Supply.** Provides power to the Wake-Up Control circuitry, while the main power supply is turned off.
V_{SS}	19, 51, 84, 116	I	GND	-	**Ground**

1.4.11 Protection

Signal	Pin(s)	I/O	Buffer Type	Power Well	Description
$\overline{\text{XLOCK}}$	53	I	IN_T	V_{DD}	**Access Lock.** When low, this pin blocks read/write from/to the SuperI/O Configuration 6 (SIOCF6) register to prevent accidental access.

1.4.12 Serial Port 1 and Serial Port 2

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{\text{CTS1}}$ $\overline{\text{CTS2}}$	100 108	I	IN_{TS}	V_{DD}	**Clear to Send.** When low, indicate that the modem or other data transfer device is ready to exchange data.
$\overline{\text{DCD1}}$ $\overline{\text{DCD2}}$	95 103	I	IN_{TS}	V_{DD}	**Data Carrier Detected.** When low, indicate that the modem or other data transfer device has detected the data carrier.
$\overline{\text{DSR1}}$ $\overline{\text{DSR2}}$	96 104	I	IN_{TS}	V_{DD}	**Data Set Ready.** When low, indicate that the data transfer device, e.g., modem, is ready to establish a communications link.
$\overline{\text{DTR1}}$_ BOUT1 $\overline{\text{DTR2}}$_ BOUT2	101 109	O	$O_{3/6}$	V_{DD}	**Data Terminal Ready.** When low, indicate to the modem or other data transfer device that the UART is ready to establish a communications link. After a system reset, these pins provide the $\overline{\text{DTR}}$ function and set these signals to inactive high. Loopback operation holds them inactive. **Baud Output.** Provides the associated serial channel baud rate generator output signal if test mode is selected, i.e., bit 7 of the EXCR1 Register is set. $\overline{\text{DTR1}}$_BOUT1 is used also as BADDR.
$\overline{\text{RI1}}$ $\overline{\text{RI2}}$	102 110	I	IN_{TS}	V_{DD}, V_{SB}	**Ring Indicator.** When low, indicate that a telephone ring signal has been received by the modem. They are monitored during power-off for wake-up event detection.
$\overline{\text{RTS1}}$ $\overline{\text{RTS2}}$	98 106	O	$O_{3/6}$	V_{DD}	**Request to Send.** When low, indicate to the modem or other data transfer device that the corresponding UART is ready to exchange data. A system reset sets these signals to inactive high, and loopback operation holds them inactive. $\overline{\text{RTS1}}$ is used also as TEST.
SIN1 SIN2	97 105	I	IN_{TS}	V_{DD}	**Serial Input.** Receive composite serial data from the communications link (peripheral device, modem or other data transfer device).
SOUT1 SOUT2	99 107	O	$O_{3/6}$	V_{DD}	**Serial Output.** Send composite serial data to the communications link (peripheral device, modem or other data transfer device). These signals are set active high after a system reset.

1.4.13 Strap Configuration

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
BADDR	101	I	IN_{STRP}	V_{DD}	**Base Address.** Sampled by the trailing edge of the system reset to determine the base address of the configuration Index-Data register pair. During reset, it is pulled down by internal 30Kohm resistor. If no pull-up resistor is connected, it is sampled low, setting the Index-Data pair at 2Eh-2Fh. Connecting a 10K external pull-up resistor to V_{DD} would make it sample high, setting the Index-Data pair at 4Eh-4Fh.
TEST	98	I	IN_{STRP}	V_{DD}	**Test.** If sampled high on the trailing edge of system reset, this signal forces the device into test mode. This pin is for National Semiconductor use only, and should be left unconnected.

1.4.14 System Wake-Up Control

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
LED1 LED2	25 26	O	$O_{12/12}$	V_{SB}	**LED.** V_{SB}-powered pins with programmable outputs, each of which can be used to produce a 0, 0.25, 0.5, 1, 4 Hz waveform for LED control.
GPIE6-7	58-59	I	IN_{TS}	V_{SB}	**General-Purpose Input Event**
GPIOE0-5	23-28	I/O	IN_{TS}/ OD_6, $O_{3/6}$	V_{SB}	**General-Purpose I/O Event.** V_{SB}-powered pins.
$\overline{\text{PWUREQ}}$	32	O	OD_6	V_{SB}	**Power-Up Request.** Active (low) level indicates that wake-up event has occurred, and causes the chipset to turn the power supply on, or to exit its current sleep state. The open-drain output must be pulled up to V_{SB} in order to function during power-off.
$\overline{\text{RING}}$	27	I	IN_{TS}	V_{SB}	**Telephone Line Ring.** Detection of a pulse train on the $\overline{\text{RING}}$ pin is a wake-up event that can activate the power-up request ($\overline{\text{PWUREQ}}$). The pin has a Schmidt-trigger input buffer, powered by V_{SB}.

1.4.15 WATCHDOG Timer (WDT)

Signal	Pin/s	I/O	Buffer Type	Power Well	Description
$\overline{\text{WDO}}$	56	O	OD_6, $O_{3/6}$	V_{DD}	**WATCHDOG Out.** Low level indicates that the WATCHDOG Timer has reached its time-out period without being retriggered. The output type and an optional pull-up are configurable.

1.5 INTERNAL PULL-UP AND PULL-DOWN RESISTORS

The signals listed in Table 4 can optionally support internal pull-up (PU) and/or pull-down (PD) resistors. See Section 10.3 for the values of each resistor type.

Table 4. Internal Pull-Up and Pull-Down Resistors

Signal	Pin/s	Type	Comments
ACCESS.bus (ACB)			
SCL	54	PU_{25}	Programmable
SDA	55	PU_{25}	Programmable
General-Purpose Input/Output (GPIO) Ports			
GPIO00-07	2-9	PU_{25}	Programmable
GPIO10 GPIO11-14 GPO15 GPIO16-17	21 53-56 57 69, 71	PU_{25}	Programmable
GPIO20-27	117-124	PU_{25}	Programmable
GPIO30-33 GPIO34	125-128 1	PU_{25}	Programmable
GPIO40-47	43-50	PU_{25}	Programmable
Keyboard and Mouse Controller (KBC)			
P12, P16, P17	6,127,7	PU_{25}	
Strap Configuration			
BADDR	101	PD_{30}	Strap
TEST	98	PD_{30}	Strap
Parallel Port			
$\overline{ACK}$	79	PU_{50}	
$\overline{AFD}\_\overline{DSTRB}$	93	PU_{100}	
BUSY_$\overline{WAIT}$	78	PD_{30}	
$\overline{ERR}$	91	PU_{50}	
$\overline{INIT}$	89	PU_{100}	
PE	77	PU_{50}/ PD_{30}	Programmable
SLCT	76	PD_{30}	
$\overline{SLIN}\_\overline{ASTRB}$	87	PU_{100}	
$\overline{STB}\_\overline{WRITE}$	94	PU_{100}	
System Wake-Up Control (SWC)			
GPIE6-7	58-59	PU_{25}	Programmable
GPIOE0-5	23-28	PU_{25}	Programmable

Signal	Pin/s	Type	Comments
$\overline{\text{RING}}$	27	PU_{25}	
WATCHDOG Timer (WDT)			
$\overline{\text{WDO}}$	56	PU1	Programmable

1.0 Signal/Pin Connection and Description (Continued)

2.0 Device Architecture and Configuration

The PC87360 SuperI/O device comprises a collection of generic and proprietary functional blocks. Each functional block is described in a separate chapter in this document. However, some parameters in the implementation of each functional block may vary per SuperI/O device. This chapter describes the PC87360 structure and provides all logical device specific information, including special implementation of generic blocks, system interface and device configuration.

2.1 OVERVIEW

The PC87360 consists of 11 logical devices, the host interface, and a central set of configuration registers, all built around a central, internal bus. The internal bus is similar to an 8-bit ISA bus protocol. See Figure 1, which illustrates the blocks and related logic.

The system interface serves as a bridge between the external LPC interface and the internal bus. It supports 8-bit I/O Read, 8-bit I/O Write and 8-bit DMA transactions, as defined in Intel's *LPC Interface Specification, Revision 1.0*.

The central configuration register set supports ACPI compliant PnP configuration. The configuration registers are structured as a subset of the Plug and Play Standard registers, defined in Appendix A of the *Plug and Play ISA Specification, Revision 1.0a* by Intel and Microsoft. All system resources assigned to the functional blocks (I/O address space, DMA channels and IRQ lines) are configured in, and managed by, the central configuration register set. In addition, some function-specific parameters are configurable through the configuration registers and distributed to the functional blocks through special control signals.

2.2 CONFIGURATION STRUCTURE AND ACCESS

The configuration structure is comprised of a set of banked registers which are accessed via a pair of specialized registers.

2.2.1 The Index-Data Register Pair

Access to the SuperI/O configuration registers is via an Index-Data register pair, using only two system I/O byte locations. The base address of this register pair is determined during reset, according to the state of the hardware strapping option on the BADDR pin. Table 5 shows the selected base addresses as a function of BADDR.

Table 5. BADDR Strapping Options

BADDR	I/O Address	
	Index Register	Data Register
0	2Eh	2Fh
1	4Eh	4Fh

The Index register is an 8-bit R/W register located at the selected base address (Base+0). It is used as a pointer to the configuration register file, and holds the index of the configuration register that is currently accessible via the Data register. Reading the Index register returns the last value written to it (or the default of 00h after reset).

The Data register is an 8-bit virtual register, used as a data path to any configuration register. Accessing the Data register actually accesses the configuration register that is currently pointed to by the Index register.

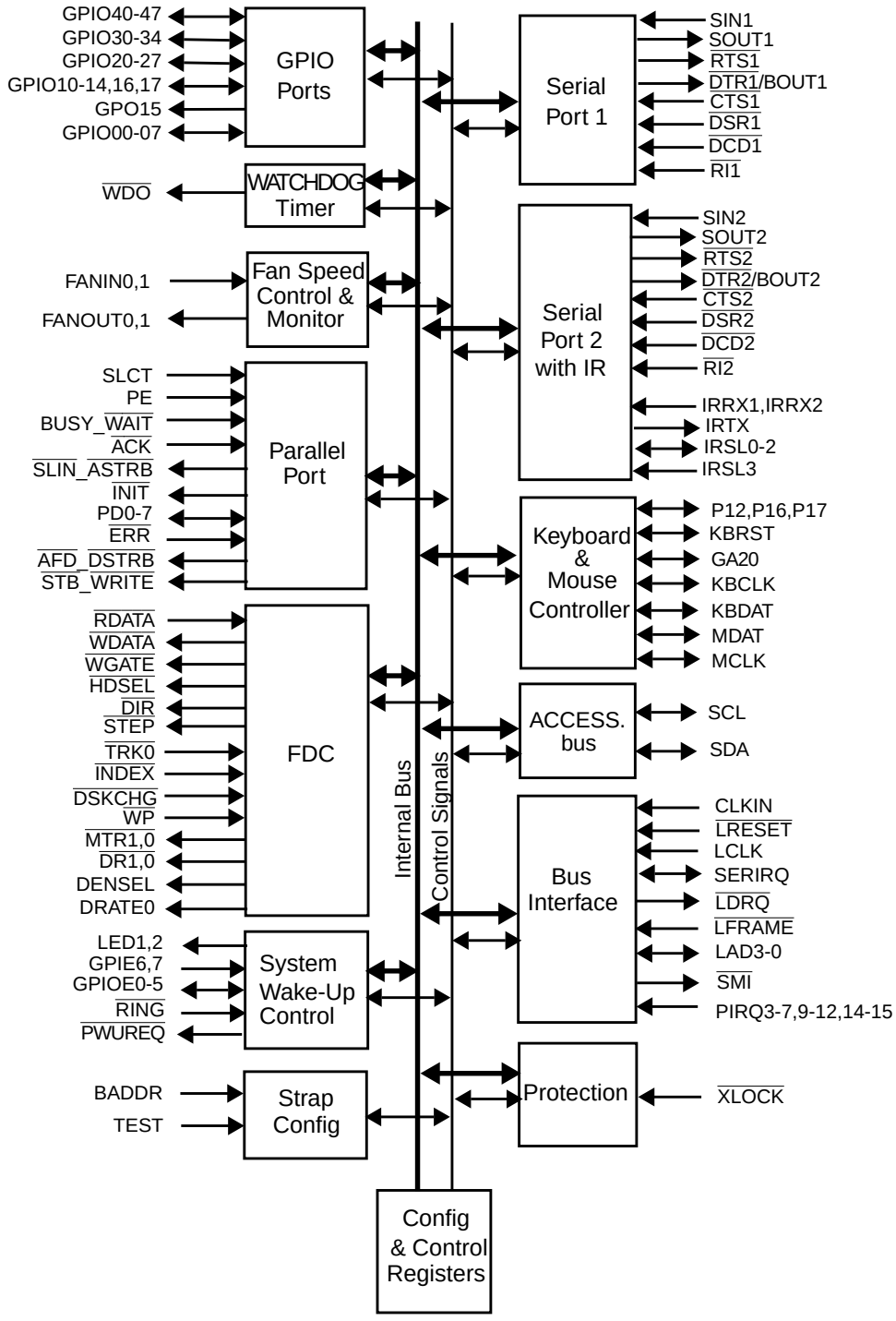


Figure 1. PC87360 Detailed Block Diagram

2.0 Device Architecture and Configuration (Continued)

2.2.2 Banked Logical Device Registers Structure

Each functional block is associated with a Logical Device Number (LDN). The configuration registers are grouped into banks, where each bank holds the standard configuration registers of the corresponding logical device. Table 6 shows the LDN values of the PC87360 functional blocks.

Figure 2 shows the structure of the standard configuration register file. The SuperI/O control and configuration registers are not banked and are accessed by the Index-Data register pair only, as described above. However, the device control and device configuration registers are duplicated over banks for logical devices. Therefore, accessing a specific register in a specific bank is performed by two dimensional indexing, where the LDN register selects the bank (or logical device) and the Index register selects the register within the bank. Accessing the Data register while the Index register holds a value of 30h or higher results in a physical access to the Logical Device Configuration registers currently pointed to by the Index register, within the logical device currently selected by the LDN register.

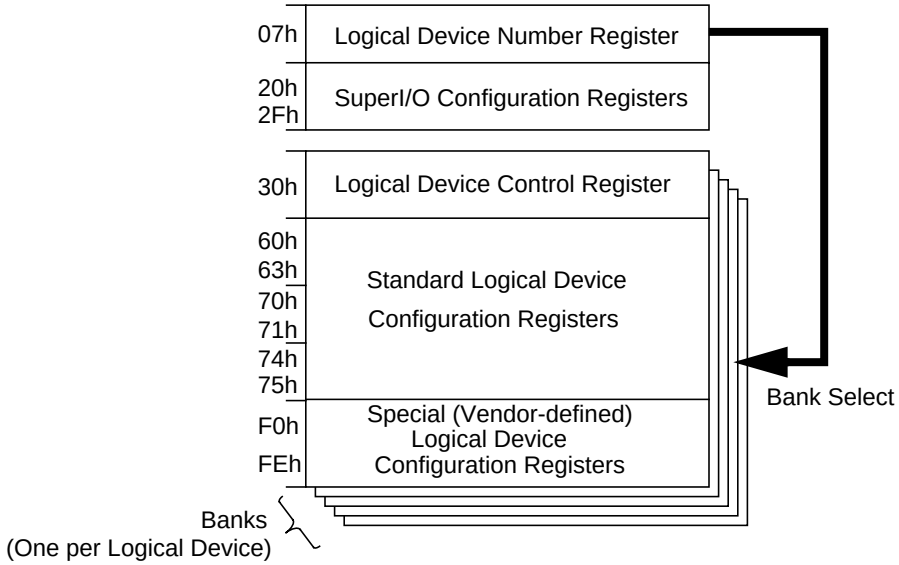


Figure 2. Structure of the Standard Configuration Register File

Table 6. Logical Device Number (LDN) Assignments

LDN	Functional Block
00h	Floppy Disk Controller (FDC)
01h	Parallel Port (PP)
02h	Serial Port 2 with IR (SP2)
03h	Serial Port 1 (SP1)
04h	System Wake-Up Control (SWC)
05h	Keyboard and Mouse Controller (KBC) - Mouse interface
06h	Keyboard and Mouse Controller (KBC) - Keyboard interface
07h	General-Purpose I/O (GPIO) Ports
08h	ACCESS.bus Interface (ACB)
09h	Fan Speed Control and Monitor (FSCM)
0Ah	WATCHDOG Timer (WDT)

Write accesses to unimplemented registers (i.e. accessing the Data register while the Index register points to a non-existing register), are ignored and read returns 00h on all addresses except for 74h and 75h (DMA configuration registers) which returns 04h (indicating no DMA channel is active). The configuration registers are accessible immediately after reset.

2.2.3 Standard Logical Device Configuration Register Definitions

Unless otherwise noted in Tables 7 through 12:

- All registers are read/write.
- All reserved bits return 0 on reads, except where noted otherwise. They must not be modified as it may cause unpredictable results. Use read-modify-write to prevent the values of reserved bits from being changed during write.
- Write only registers should not use read-modify-write during updates.

Table 7. Standard Control Registers

Index	Register Name	Description
07h	Logical Device Number	This register selects the current logical device. See Table 6 for valid numbers. All other values are reserved.
20h - 2Fh	SuperI/O Configuration	SuperI/O configuration registers and ID registers

Table 8. Logical Device Activate Register

Index	Register Name	Description
30h	Activate	Bit 0 - Logical device activation control 0: Disabled 1: Enabled Bits 7-1 - Reserved

Table 9. I/O Space Configuration Registers

Index	Register Name	Description
60h	I/O Port Base Address Bits (15-8) Descriptor 0	Indicates selected I/O lower limit address bits 15-8 for I/O Descriptor 0.
61h	I/O Port Base Address Bits (7-0) Descriptor 0	Indicates selected I/O lower limit address bits 7-0 for I/O Descriptor 0.
62h	I/O Port Base Address Bits (15-8) Descriptor 1	Indicates selected I/O lower limit address bits 15-8 for I/O Descriptor 1.
63h	I/O Port Base Address Bits (7-0) Descriptor 1	Indicates selected I/O lower limit address bits 7-0 for I/O Descriptor 1.

Table 10. Interrupt Configuration Registers

Index	Register Name	Description
70h	Interrupt Number and Wake-Up on IRQ Enable	Indicates selected interrupt number. Bit 4 - Enables wake-up on the IRQ of the logical device. When enabled, IRQ assertion triggers a wake-up event. 0: Disabled (default) 1: Enabled Bits 3-0 select the interrupt number. A value of 1 selects IRQ1, a value of 2 selects IRQ2, etc. (up to IRQ15). IRQ0 is not a valid interrupt selection.
71h	Interrupt Request Type Select	Indicates the type and level of the interrupt request number selected in the previous register. Bit 0 - Type of interrupt request selected in previous register 0: Edge 1: Level Bit 1 - Level of interrupt request selected in previous register 0: Low polarity 1: High polarity

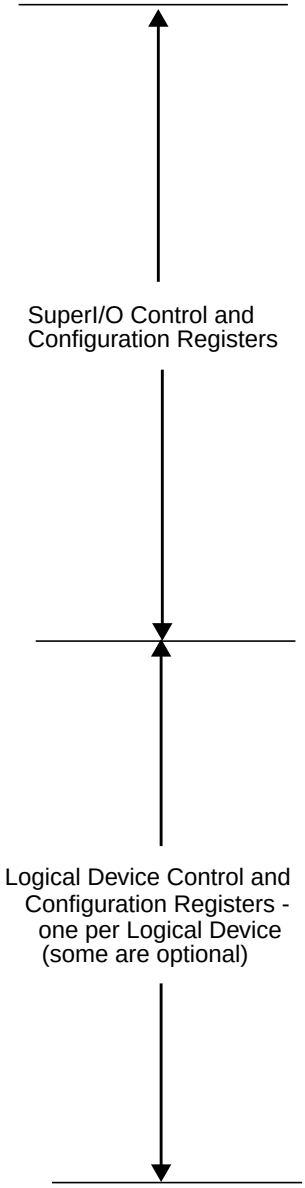
Table 11. DMA Configuration Registers

Index	Register Name	Description
74h	DMA Channel Select 0	Indicates selected DMA channel for DMA 0 of the logical device (0 - The first DMA channel in case of using more than one DMA channel). Bits 2-0 select the DMA channel for DMA 0. The valid choices are 0-3, where a value of 0 selects DMA channel 0, 1 selects channel 1, etc. A value of 4 indicates that no DMA channel is active. The values 5-7 are reserved.
75h	DMA Channel Select 1	Indicates selected DMA channel for DMA 1 of the logical device (1 - The second DMA channel in case of using more than one DMA channel). Bits 2-0 select the DMA channel for DMA 1. The valid choices are 0-3, where a value of 0 selects DMA channel 0, 1 selects channel 1, etc. A value of 4 indicates that no DMA channel is active. The values 5-7 are reserved.

Table 12. Special Logical Device Configuration Registers

Index	Register Name	Description
F0h-FEh	Logical Device Configuration	Special (vendor-defined) configuration options.

2.2.4 Standard Configuration Registers



Index	Register Name
07h	Logical Device Number
20h	SuperI/O ID
21h	SuperI/O Configuration 1
22h	SuperI/O Configuration 2
23h	SuperI/O Configuration 3
24h	SuperI/O Configuration 4
25h	SuperI/O Configuration 5
26h	SuperI/O Configuration 6
27h	SuperI/O Revision ID
28h	SuperI/O Configuration 8
2Ah	SuperI/O Configuration A
2Bh	SuperI/O Configuration B
2Ch	SuperI/O Configuration C
2Eh	Reserved exclusively for National use
30h	Logical Device Control (Activate)
60h	I/O Base Address Descriptor 0 Bits 15-8
61h	I/O Base Address Descriptor 0 Bits 7-0
62h	I/O Base Address Descriptor 1 Bits 15-8
63h	I/O Base Address Descriptor 1 Bits 7-0
70h	Interrupt Number and Wake-Up on IRQ Enable
71h	IRQ Type Select
74h	DMA Channel Select 0
75h	DMA Channel Select 1
F0h	Device Specific Logical Device Configuration 1
F1h	Device Specific Logical Device Configuration 2
F2h	Device Specific Logical Device Configuration 3

Figure 3. Configuration Register Map

SuperI/O Control and Configuration Registers

The SuperI/O Configuration registers at indexes 20h and 27h are mainly used for part identification, global power management and the selection of pin multiplexing options. For details, see Section 2.7.

Logical Device Control and Configuration Registers

A subset of these registers is implemented for each logical device. See functional block description in the following sections.

Control

The only implemented control register for each logical device is the Activate register at index 30h. Bit 0 of the Activate register controls the activation of the associated function block. Activation of the block enables access to the block's registers, and attaches its system resources, which are unused as long as the block is not activated. Other effects may apply, on a function-specific basis (such as clock enable and active pinout signaling).

Standard Configuration

The standard configuration registers are used to manage the PnP resource allocation to the functional blocks. The I/O port base address descriptor 0 is a pair of registers at Index 60-61h, holding the (first or only) 16-bit base address for the register set of the functional block. An optional 16-bit second base-address (descriptor 1) at index 62-63h is used for logical devices with more than one continuous register set. Interrupt Number and Wake-Up on IRQ Enable (index 70h) and IRQ Type Select (index 71h) allocate an IRQ line to the block and control its type. DMA Channel Select 0 (index 74h) allocates a DMA channel to the block, where applicable. DMA Channel Select 1 (index 75h) allocates a second DMA channel, where applicable.

Special Configuration

The vendor-defined registers, starting at index F0h, are used to control function-specific parameters such as operation modes, power saving modes, pin TRI-STATE, clock rate selection, and non-standard extensions to generic functions.

2.2.5 Default Configuration Setup

The default configuration setup of the PC87360 can include four reset types, described below. See specific register descriptions for the bits affected by each reset type.

- **Software Reset**
  This reset is enabled by bit 1 of the SIOCF1 register, which resets all logical devices. A software reset also resets most bits in the SuperI/O control and configuration registers (see Section 2.7 for the bits not affected). This reset does not affect register bits that are locked for write access.
- **Hardware Reset**
  This reset is activated by the assertion of the $\overline{\text{LRESET}}$ input. It resets all logical devices, with the exception of the System Wake-Up Control (SWC). It also resets all SuperI/O control and configuration registers, except for those that are battery-backed.
- **V_{PP} Power-Up Reset**
  This reset is activated when either V_{SB} or V_{BAT} is powered up after both have been off. V_{PP} is an internal voltage which is a combination of V_{SB} and V_{BAT}. V_{PP} is taken from V_{SB} if V_{SB} is greater than the minimum (Min) value defined in the *Device Characteristics* chapter; otherwise, V_{BAT} is used as the V_{PP} source. This reset resets all registers whose values are retained by V_{PP}.
- **V_{SB} Power-Up Reset**
  This is an internally generated reset that resets the SWC, excluding those SWC registers whose values are retained by V_{PP}. This reset is activated after V_{SB} is powered up.

In event of a hardware reset, the PC87360 wakes up with the following default configuration setup:

— The configuration base address is 2Eh or 4Eh, according to the BADDR strap pin value, as shown in Table 5.

— The Keyboard Controller (KBC) is active and all other logical devices are disabled, with the exception of the SWC which remains functional but whose registers cannot be accessed.

— All multiplexed GPIO pins, except for pins whose function is controlled by battery-backed registers and pins 8 and 9 (which are controlled by bits 1 and 0 of the SIOCF3 register) are configured as GPIO pins, with an internal static pull-up (default direction is input).

In event of either a hardware or a software reset, the PC87360 wakes up with the following default configuration setup:

— The legacy devices are assigned with their legacy system resource allocation.

— The National proprietary functions are not assigned with any default resources and the default values of their base addresses are all 00h.

2.2.6 Power States

The following terminology is used in this document to describe the various possible power states:

- **Power On**
  Both V_{SB} and V_{DD} are active.
- **Power Off**
  V_{SB} is active and V_{DD} is inactive.

- **Power Fail**
  Both V_{SB} and V_{DD} are inactive.

Note: The following state is illegal: V_{DD} active and V_{SB} inactive.

2.2.7 Address Decoding

A full 16-bit address decoding is applied when accessing the configuration I/O space as well as the registers of the functional blocks. However, the number of configurable bits in the base address registers varies for each logical device.

The lower 1, 2, 3, 4 or 5 address bits are decoded within the functional block to determine the offset of the accessed register, within the logical device's I/O range of 2, 4, 8, 16 or 32 bytes, respectively. The rest of the bits are matched with the base address register to decode the entire I/O range allocated to the logical device. Therefore the lower bits of the base address register are forced to 0 (read only), and the base address is forced to be 2, 4, 8, 16 or 32 byte-aligned, according to the size of the I/O range.

The base address of the FDC, Serial Port 1, Serial Port 2 with IR and KBC are limited to the I/O address range of 00h to 7FXh only (bits 11-15 are forced to 0). The Parallel Port base address is limited to the I/O address range of 00h to 3F8h. The addresses of the non-legacy logical devices are configurable within the full 16-bit address range (up to FFFXh).

In some special cases, other address bits are used for internal decoding (such as bit 2 in the KBC and bit 10 in the Parallel Port). The KBC has two I/O descriptors with some implied dependency between them. For more details, see the description of the base address register for each logical device.

2.3 INTERRUPT SERIALIZER

The Interrupt Serializer translates parallel interrupt request (PIRQ) signals received from external devices, via the PIRQn pins, into serial interrupt request data transmitted over the SERIRQ bus. This enables the integration of devices that support only parallel IRQ in a system which supports only serial IRQs. Figure 4 shows the interrupt serialization mechanism.

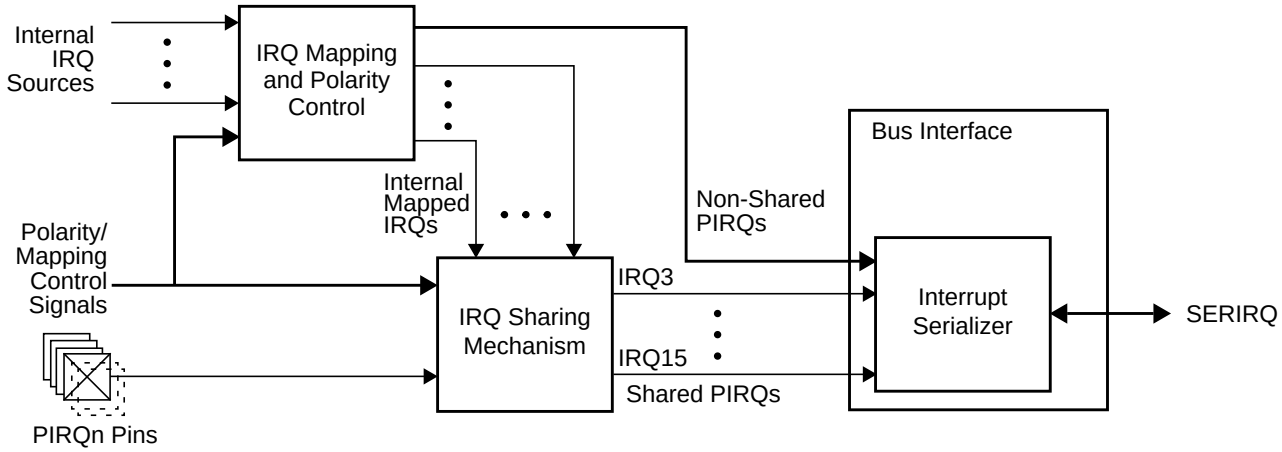


Figure 4. Interrupt Serialization Mechanism

PIRQ signals that enter the device are fed into an IRQ sharing mechanism. This mechanism combines them with internal IRQ signals that are mapped to their associated IRQ slots. The resulting internal shared IRQs are then fed into the Interrupt Serializer, where they are translated into serial data and transmitted over the SERIRQ bus.

The IRQ sharing mechanism allows an internal IRQ and an external PIRQ to share the same IRQ slot. To share an IRQ slot, all IRQ sources routed to it, including possibly a PIRQn pin, must be active low. When multiple IRQ sources are set to share an IRQ slot, the corresponding internal IRQ signal is a logic AND of all IRQ sources.

When an IRQ slot is exclusively used by a PIRQ pin, each transition sensed on this PIRQ pin is translated into a new value. This value is transmitted over the SERIRQ bus during the corresponding IRQ slot. A transition on PIRQn results in a new value that is transmitted during IRQ slot "n" of the SERIRQ bus. For example, a transition on PIRQ3 is translated into the transmission of the new value of PIRQ3 during slot 3 of the SERIRQ bus. No polarity adjustment occurs during this translation process. Therefore, when the level of a PIRQn pin goes high or low, the result is transmitted with no polarity adjustment during slot "n" of the SERIRQ bus.

The Interrupt Serializer is controlled by bit 6, Pins 117-127 Select PIRQ, of SuperI/O Configuration 1 register. When this bit is set to 0 (default), the Interrupt Serializer is disabled. When it is set to 1, the Interrupt Serializer is enabled, and each PIRQn input function is selected on its associated pin. The PIRQn input value is then routed to the Interrupt Serializer as the IRQ value to be driven onto IRQ slot "n" when at least one of the following conditions is true:

- Slot "n" is not selected by any internal IRQ source.
- Slot "n" is selected by an internal IRQ source which is set for sharing (low polarity).

Otherwise, the IRQ value driven onto IRQ slot "n" is the value of any internal IRQ that is selected.

2.4 PROTECTION

The PC87360 provides features to protect the PC at both hardware and software levels .

The device can disable I/O port access. This protects system integrity by enabling the primary operating software to prevent other unwanted I/O operations by other software.

At the software level, the device can be locked to protect configuration bits or alteration of the hardware configuration of the device, as well as internal GPIO settings and several types of configuration settings.

All protection mechanisms can optionally be used.

2.4.1 Access Lock to I/O Ports

Locking access to the I/O ports of the device is based on the SIOCF6 register (for details, see Section 2.7.7). This protection feature is implemented for the following logical devices:

- FDC (Logical Device 0)
- Parallel Port (Logical Device 1)
- Serial Port 2 (Logical Device 2)
- Serial Port 1 (Logical Device 3)
- ACB (Logical Device 8)

Each one of these logical devices has an associated bit in the SIOCF6 register. When one of these bits is set, the associated logical device is completely disabled. For example, when bit 0 of the SIOCF6 register is set to 1, the FDC is disabled.

To lock access to the I/O ports, the SIOCF6 register must be set to read only. This can be done by either software or hardware. By software, set bit 7 of the SIOCF6 register to 1. This bit can only be cleared (read/write enabled) by a hardware reset.

Alternatively, use the $\overline{\text{XLOCK}}$ input hardware-based function to set the SIOCF6 register to read only. First, select $\overline{\text{XLOCK}}$ on its pin, pin 53, by setting bit 4 of the SIOCF3 register to 1. $\overline{\text{XLOCK}}$ can then can be used to control the SIOCF6 register, as follows:

- When $\overline{\text{XLOCK}}$ is driven high, the SIOCF6 register is read/write.
- When $\overline{\text{XLOCK}}$ is driven low, the SIOCF6 register is read only.

2.4.2 Pin Configuration Lock

To lock the pin configuration of the PC87360 in order to prevent unwanted changes to hardware configuration, set bit 7 of the SIOCF1 register to 1. Setting this bit causes all function select configuration bits, including those that are battery backed, to become read only bits. This bit can only be cleared by a hardware reset.

2.4.3 GPIO Pin Function Lock

The PC87360 is capable of locking the attributes of each GPIO or Standby GPIO pin. The following attributes can be locked:

- Output enable
- Output type
- Static pull-up
- Driven data.

GPIO pins are locked per pin by setting the Lock bit in the appropriate GPIO Pin Configuration register. When the Lock bit is set, the configuration of the associated GPIO pin can only be released by a hardware reset.

Standby GPIO pins are locked in the same manner by setting the Lock bit in the appropriate Standby GPIO Pin Configuration registers. However, once a Standby GPIO pin is locked, its locked attributes can only be released with a V_{SB} power-up reset.

Table 13 summarizes the bit states that affect PSON V_{SB} power-up default state.

Table 13. PSON V_{SB} Power-Up Default State

Resume Last PSON State (SIOCFD, Bit 2)	Last PSON State	PSON V_{SB} Power-Up Default
1	0	0
1	1	1
0	X	Same as $\overline{SLPS3}$ state

2.5 LED OPERATION AND STATES

The device supports up to two LEDs, depending on Pin 25 and Pin 26 Function Select (bits 1-2 and bit 3) of the SIOCFA register. The polarity of both LEDs is determined by LED Polarity Control (bit 7) of the SIOCFD register.

, when in power-on state. The device also provides modes for hardware LED control. This enables the LEDs to support features such as power and error indication.

The LEDs may be operated in software, hardware1 or hardware 2 modes. These modes are set by LED Mode Control (bits 2 and 3) of the SIOCFB register. Each LED can be set to On, Off or to blink at different rates by means of bits 0-2 (LED1) and bits 3-5 (LED2) of the SIOCFC register. When in power-on state (both V_{DD} and V_{SB} exist), the LEDs are software-controlled. When in power fail state (no V_{SB} and no V_{DD}) the LEDs are off. Table 14 shows the effect of hardware modes 1 and 2 on LED operation that override the above rules.

Table 14. Hardware Modes 1 and 2 Effect on LED Operation

Mode	System State	LED1	LED2
Hardware 1 (SIOCFB, bits 3-2=01)	V_{SB} power-up reset	Off	1 Hz blink, 50% duty cycle
	Power off (V_{SB}, no V_{DD})	Software-controlled	1 Hz blink, 50% duty cycle

2.6 REGISTER TYPE ABBREVIATIONS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

2.7 SUPERI/O CONFIGURATION REGISTERS

This section describes the SuperI/O configuration and ID registers (those registers with first level indexes in the range of 20h - 2Eh). See Table 15 for a summary and directory of these registers.

Table 15. SuperI/O Configuration Registers

Index	Mnemonic	Register Name	Power Well	Type	Section
20h	SID	SuperI/O ID	V_{DD}	RO	2.7.1
21h	SIOCF1	SuperI/O Configuration 1	V_{DD}	R/W	2.7.2
22h	SIOCF2	SuperI/O Configuration 2	V_{DD}	R/W	2.7.3
23h	SIOCF3	SuperI/O Configuration 3	V_{DD}	R/W	2.7.4
24h	SIOCF4	SuperI/O Configuration 4	V_{DD}	R/W	2.7.5
25h	SIOCF5	SuperI/O Configuration 5	V_{DD}	R/W	2.7.6
27h	SRID	SuperI/O Revision ID	V_{DD}	RO	2.7.8

Index	Mnemonic	Register Name	Power Well	Type	Section
28h	SIOCF8	SuperI/O Configuration 8	V_{DD}	R/W	2.7.9
2Ah	SIOCFA	SuperI/O Configuration A	V_{PP}	R/W	2.7.10
2Bh	SIOCFB	SuperI/O Configuration B	V_{PP}	R/W	2.7.11
2Ch	SIOCFC	SuperI/O Configuration C	V_{PP}	R/W	2.7.12
2Eh	Reserved exclusively for National use				

2.7.1 SuperI/O ID Register (SID)

This register contains the identity number of the chip. The PC87360 is identified by the value E1h.

Location: Index 20h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Chip ID**							
Reset	1	1	1	0	0	0	0	1

2.7.2 SuperI/O Configuration 1 Register (SIOCF1)

Location: Index 21h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Pin Function Select Lock**	**Pins 117-127 Function Select**	**Number of DMA Wait States**		**Number of I/O Wait States**		**SW Reset**	**Global Device Enable**
Reset	0	0	0	1	0	0	0	1

Bit	Description
7	**Pin Function Select Lock**. This bit determines if the bits (located in the SIOCF1, 2, 3, 4, 5, A and B registers) that select pin functions are read only or read/write. When set to 1, this bit can only be cleared by a hardware reset. 0: Bits are R/W. 1: Bits are RO.
6	**Pins 117-127 Function Select.** 0: Pins 117-127 function set by SIOCF4 (default) 1: Pins 117-127 are PIRQ3-7, 9, 11-12, 14-15
5-4	**Number of DMA Wait States.** **Bits 5 4 — Number** 0 0 — Reserved 0 1 — Two (default) 1 0 — Six 1 1 — Twelve
3-2	**Number of I/O Wait States.** **Bits 3 2 — Number** 0 0 — Zero (default) 0 1 — Two 1 0 — Six 1 1 — Twelve
1	**SW Reset**. Read always returns 0. 0: Ignored (default) 1: Resets all the logical devices that are reset by hardware reset (with the exception of the lock bits), and resets the registers of the SWC
0	**Global Device Enable.** This bit controls the function enable of all the PC87360 logical devices, except System Wake-Up Control (SWC). With the exception of SWC, it allows all logical devices to be disabled simultaneously by writing to a single bit. 0: All logical devices in the PC87360 are disabled, except SWC 1: Each logical device is enabled according to its Activate register (Index 30h) (default)

2.7.3 SuperI/O Configuration 2 Register (SIOCF2)

Location: Index 22h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Pin 7 Function Select**	**Pin 6 Function Select**	**Pin 5 Function Select**	**Pin 4 Function Select**	**Pin 3 Function Select**	**Pin 2 Function Select**	**Pin 1 Function Select**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Pin 7 Function Select.** This is a R/W bit. 0: GPIO05 (default) 1: P17
6	**Pin 6 Function Select.** This is a R/W bit. 0: GPIO04 (default) 1: P12
5	**Pin 5 Function Select.** This is a R/W bit. 0: GPIO03 (default) 1: FANOUT0
4	**Pin 4 Function Select.** This is a R/W bit. 0: GPIO02 (default) 1: FANIN0
3	**Pin 3 Function Select.** This is a R/W bit. 0: GPIO01 (default) 1: FANOUT1
2	**Pin 2 Function Select.** This is a R/W bit. 0: GPIO00 (default) 1: FANIN1
1-0	**Pin 1 Function Select.** This is a RO bit. **Bits 1 0 Function** 0 0 GPIO34 (default) Others Reserved

2.7.4 SuperI/O Configuration 3 Register (SIOCF3)

Location: Index 23h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Pin 57 Function Select**	**Pin 56 Function Select**	**Pins 54, 55 Function Select**	**Pin 53 Function Select**	**Reserved**	**Pin 21 Function Select**	**Pin 9 Function Select**	**Pin 8 Function Select**
Reset	0	0	0	0	0	0	1	1

Bit	Description
7	**Pin 57 Function Select.** 0: GPO15 (default) 1: IRTX
6	**Pin 56 Function Select.** 0: GPIO14 (default) 1: $\overline{\text{WDO}}$
5	**Pins 54, 55 Function Select.** 0: GPIO12/GPIO13 (default) 1: SCL/SDA
4	**Pin 53 Function Select.** 0: GPIO11 (default) 1: $\overline{\text{XLOCK}}$
3	**Reserved**
2	**Pin 21 Function Select.** 0: GPIO10 (default) 1: $\overline{\text{SMI}}$
1	**Pin 9 Function Select.** 0: GPIO07 1: GA20 (P21) (default)
0	**Pin 8 Function Select.** 0: GPIO06 1: KBRST (P20) (default)

2.7.5 SuperI/O Configuration 4 Register (SIOCF4)

Location: Index 24h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Pin 127 Function Select**		**Pins 125,126 Function Select**	**Plns 117-124 Function Select**	**Pin 71 Function Select**		**Pin 69 Function Select**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Pin 127 Function Select.** This is a R/W bit. **Bits 7 6 P* Function** 0 0 0 GPIO32 (default) 0 1 0 P16 1 0 0 IRSL1 X X 1 PIRQ15
5	**Pins 125,126 Function Select.** This is a RO bit. **Bits 5 P* Function** 0 0 GPIO30,31 (default) 1 0 Reserved X 1 PIRQ12,14
4	**Pins 117-124 Function Select.** This is a RO bit. **Bits 4 P* Function** 0 0 GPIO20-27 (default) 1 0 Reserved X 1 PIRQ3-7,9-11
3-2	**Pin 71 Function Select.** This is a R/W bit. **Bits 3 2 Function** 0 0 GPIO17 (default) 0 1 $\overline{DR1}$ 1 0 IRSL3 1 1 Reserved
1-0	**Pin 69 Function Select.** This is a R/W bit. **Bits 1 0 Function** 0 0 GPIO16 (default) 0 1 $\overline{MTR1}$ 1 0 IRSL2 1 1 Reserved

***** Bit 6, Pins 117-127 Select PIRQ, of the SIOCF1 register

2.7.6 SuperI/O Configuration 5 Register (SIOCF5)

Location: Index 25h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**$\overline{\text{SMI}}$ to IRQ2 Enable**	**Reserved**		**Pin 128 Function Select**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved**
4	**$\overline{\text{SMI}}$ to IRQ2 Enable.** This is a R/W bit. 0: Disabled (default) 1: Enabled
3-2	**Reserved**
1-0	**Pin 128 Function Select.** This is a RO bit. **Bits 1 0 Function** 0 0 GPIO33 (default) Others Reserved

2.7.7 SuperI/O Configuration 6 Register (SIOCF6)

Write access to this register can be inhibited by either asserting $\overline{\text{XLOCK}}$ when it is selected on pin 53, or by setting bit 7 of this register. Activation of each logical device (bits 0-4) is also affected by bit 0 of the logical device Activate register, index 30h and bit 0 of the SIOCF1 register.

Location: Index 26h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SIOCF6 Software Lock**	**General-Purpose Scratch**		**ACB Disable**	**Serial Port 1 Disable**	**Serial Port 2 Disable**	**Parallel Port Disable**	**FDC Disable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**SIOCF6 Software Lock.** Once this bit is set to 1 by software, it can be cleared only by hardware reset. 0: Write access to bits 0-6 of this register is controlled by $\overline{\text{XLOCK}}$ (default) 1: Bits 0-6 of this register are RO
6-5	**General-Purpose Scratch**
4	**ACB Disable** 0: Enabled (default) 1: Disabled
3	**Serial Port 1 Disable** 0: Enabled (default) 1: Disabled
2	**Serial Port 2 Disable** 0: Enabled (default) 1: Disabled
1	**Parallel Port Disable** 0: Enabled (default) 1: Disabled
0	**FDC Disable** 0: Enabled (default) 1: Disabled

2.7.8 SuperI/O Revision ID Register (SRID)

This register contains the identity number of the chip revision. SRID is incremented on each revision.

Location: Index 27h

Type: RO

2.7.9 SuperI/O Configuration 8 Register (SIOCF8)

Location: Index 28h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**Mouse IRQ to $\overline{\text{SMI}}$ Enable**	**KBD IRQ to $\overline{\text{SMI}}$ Enable**	**KBD P12 to $\overline{\text{SMI}}$ Enable**	**GPI to $\overline{\text{SMI}}$ Enable**	**$\overline{\text{WDO}}$ to $\overline{\text{SMI}}$ Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved**
4	**Mouse IRQ to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
3	**KBD IRQ to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
2	**KBD P12 to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
1	**GPI to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
0	**$\overline{\text{WDO}}$ to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled

2.7.10 SuperI/O Configuration A Register (SIOCFA)

This is a battery-backed register.

Location: Index 2Ah

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**Pin 28 Function Select**	**Pln 27 Function Select**		**Pin 26 Function Select**	**Pin 25 Function Select**		**Reserved**
Reset	Strap	0	0	0	0	0	0	0

Bit	Description
	Reserved
6	**Pin 28 Function Select** 0: GPIOE5 (default at V_{PP} power-up reset) 1: Reserved
5-4	**Pln 27 Function Select** **Bits 5 4 Function** 0 0 GPIOE4 (default at V_{PP} power-up reset) 0 1 $\overline{\text{RING}}$ Other Reserved
3	**Pin 26 Function Select** 0: GPIOE3 (default at V_{PP} power-up reset) 1: LED2
2-1	**Pin 25 Function Select** **Bits 2 1 Function** 0 0 GPIOE2 (default at V_{PP} power-up reset) 0 1 LED1 Other Reserved
0	**Pin 24 Function Select** 0: GPIOE1 (default at V_{PP} power-up reset) 1: Reserved

2.7.11 SuperI/O Configuration B Register (SIOCFB)

This is a battery-backed register.

Location: Index 2Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**LED Mode Control**		**Pin 59 Function Select**	**Pin 58 Function Select**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3-2	**LED Mode Control** **Bits 3 2 Function** 0 0 Software mode (default at V_{PP} power-up reset) 0 1 Hardware mode 1 (default at V_{SB} power-up)1 XReserved
1	**Pin 59 Function Select** 0: GPIE7 (default at V_{PP} power-up reset) 1: IRRX1
0	**Pin 58 Function Select** 0: GPIE6 (default at V_{PP} power-up reset) 1: IRRX2_IRSL0

2.7.12 SuperI/O Configuration C Register (SIOCFC)

This is a battery-backed register.

Location: Index 2Ch

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**LED Configuration**	**Reserved**	**LED2 Blink Rate**			**LED1 Blink Rate**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**LED Configuration** 0: One dual-colored LED (default at V_{PP} power-up reset) 1: Two LEDs
6	**Reserved**
5-3	**LED2 Blink Rate** **Bits 5 4 3 — Rate (Hz) — Duty Cycle** 0 0 0 — Off — Always low 0 0 1 — 0.25 — 12.5% 0 1 0 — 0.5 — 25% 0 1 1 — 1 — 50%Note 1. 1 0 0 — 2 — 50% 1 0 1 — 3 — 50% 1 1 0 — 4 — 50% 1 1 1 — On — Always high (default at V_{PP} power-up reset)
2-0	**LED1 Blink Rate** **Bits 2 1 0 — Rate (Hz) — Duty Cycle** 0 0 0 — Off — Always low (default at V_{PP} power-up reset) 0 0 1 — 0.25 — 12.5% 0 1 0 — 0.5 — 25% 0 1 1 — 1 — 50% 1 0 0 — 2 — 50% 1 0 1 — 3 — 50% 1 1 0 — 4 — 50% 1 1 1 — On — Always high

Note 1. When hardware mode 1 is selected, this rate will be set when V_{SB} is powered up or when V_{DD} becomes inactive while VSB is active.

2.7.13 SuperI/O Configuration D Register (SIOCFD)

This is a battery-backed register.

Location: Index 2Dh

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**LED Polarity Control**	**Reserved**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**LED Polarity Control.** This is a R/W bit. It determines if the LED outputs are active high or active low when they are lit. 0: Active high (default at V_{SB} power-up reset) 1: Active low
6-0	**Reserved**

2.8 FLOPPY DISK CONTROLLER (FDC) CONFIGURATION

2.8.1 General Description

The generic FDC is a standard FDC with a digital data separator, and is DP8473 and N82077 software compatible. The PC87360 FDC supports 14 of the 17 standard FDC signals described in the generic Floppy Disk Controller (FDC) chapter, including:

- FM and MFM modes are supported. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  0 = FM mode
  1 = MFM mode
- A logic 1 is returned for all floating (TRI-STATE) FDC register bits upon LPC I/O read cycles.

Exceptions to standard FDC support include:

- Automatic media sense is not supported (MSEN0-1 pins are not implemented)
- DRATE1 is not supported.

Table 16 lists the FDC functional block registers.

Table 16. FDC Registers

Offset[Note 1.]	Mnemonic	Register Name	Type
00h	SRA	Status A	RO
01h	SRB	Status B	RO
02h	DOR	Digital Output	R/W
03h	TDR	Tape Drive	R/W
04h	MSR	Main Status	R
	DSR	Data Rate Select	W
05h	FIFO	Data (FIFO)	R/W
06h		N/A	X
07h	DIR	Digital Input	R
	CCR	Configuration Control	W

Note 1. This is the 8-byte aligned FDC base address.

2.8.2 Logical Device 0 (FDC) Configuration

Table 17 lists the Configuration registers which affect the FDC. Only the last two registers (F0h and F1h) are described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 17. FDC Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register and bit 0 of the SIOCF6 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	03h
61h	Base Address LSB register. Bits 2 and 0 (for A2 and A0) are read only, 00b.	R/W	F2h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	06h
71h	Interrupt Type. Bit 1 is read/write; other bits are read only.	R/W	03h
74h	DMA Channel Select	R/W	02h
75h	Report no second DMA assignment	RO	04h
F0h	FDC Configuration register	R/W	24h
F1h	Drive ID register	R/W	00h

2.8.3 FDC Configuration Register

This register is reset by hardware to 24h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**TDR Register Mode**	**DENSEL Polarity Control**	**Reserved**	**Write Protect**	**PC-AT or PS/2 Drive Mode Select**	**Reserved**	**TRI-STATE Control**
Reset	0	0	1	0	0	1	0	0
Required	0			0				

Bit	Description
7	**Reserved**. Must be 0.
6	**TDR Register Mode** 0: PC-AT compatible drive mode; i.e., bits 7-2 of the TDR are 111111b (default) 1: Enhanced drive mode
5	**DENSEL Polarity Control** 0: Active low for 500 Kbps or 1 Mbps data rates 1: Active high for 500 Kbps or 1 Mbps data rates (default)
4	**Reserved.** Must be 0.
3	**Write Protect.** This bit allows forcing of write protect functionality by software. When set, writes to the floppy disk drive are disabled. This effect is identical to $\overline{WP}$ when it is active. 0: Write protected according to $\overline{WP}$ signal (default) 1: Write protected regardless of value of $\overline{WP}$ signal
2	**PC-AT or PS/2 Drive Mode Select** 0: PS/2 drive mode 1: PC-AT drive mode (default)
1	**Reserved**
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.8.4 Drive ID Register

This read/write register is reset by hardware to 00h. This register controls bits 5 and 4 of the TDR register in the Enhanced mode.

Location: Index F1h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Drive 1 ID**		**Drive 0 ID**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3-2	**Drive 1 ID.** When drive 1 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.
1-0	**Drive 0 ID.** When drive 0 is accessed, these bits are reflected on bits 5-4 of the TDR register, respectively.

Usage Hints: Some BIOS implementations support automatic media sense FDDs, in which case bit 5 of the TDR register in the Enhanced mode is interpreted as valid media sense when it is cleared to 0. If drive 0 and/or drive 1 do not support automatic media sense, bits 1 and/or 3 of the Drive ID register should be set to 1 respectively (to indicate non-valid media sense) when the corresponding drive is selected and the Drive ID bit is reflected on bit 5 of the TDR register in the Enhanced mode.

2.9 PARALLEL PORT CONFIGURATION

2.9.1 General Description

The PC87360 Parallel Port supports all IEEE1284 standard communication modes: Compatibility (known also as Standard or SPP), Bidirectional (known also as PS/2), FIFO, EPP (known also as Mode 4) and ECP (with an optional Extended ECP mode).

The Parallel Port includes two groups of runtime registers, as follows:

- A group of 21 registers at first level offset, sharing 14 entries. Three of this registers (at offsets 403h, 404h and 405h) are used only in the Extended ECP mode.
- A group of four registers, used only in the Extended ECP mode, accessed by a second level offset.

The desired mode is selected by the ECR runtime register (offset 402h). The selected mode determines which runtime registers are used and which address bits are used for the base address. See Tables 18 and 19 for a listing of all registers, their offset addresses, and the associated modes.

Table 18. Parallel Port Registers at First Level Offset

Offset	Mnemonic	Mode(s)	Type	Register Name
00h	DATAR	0,1	R/W	Data
	AFIFO	3	W	ECP FIFO (Address)
	DTR	4	R/W	Data (for EPP)
01h	DSR	0,1,2,3	RO	Status
	STR	4	RO	Status (for EPP)
02h	DCR	0,1,2,3	R/W	Control
	CTR	4	R/W	Control (for EPP)
03h	ADDR	4	R/W	EPP Address
04h	DATA0	4	R/W	EPP Data Port 0
05h	DATA1	4	R/W	EPP Data Port 1
06h	DATA2	4	R/W	EPP Data Port 2
07h	DATA3	4	R/W	EPP Data Port 3
400h	CFIFO DFIFO TFIFO CNFGA	2 3 6 7	W R/W R/W RO	PP Data FIFO ECP Data FIFO Test FIFO Configuration A
401h	CNFGB	7	RO	Configuration B
402h	ECR	0,1,2,3	R/W	Extended Control
403h	EIR[Note 1.]	0,1,2,3	R/W	Extended Index
404h	EDR[1]	0,1,2,3	R/W	Extended Data
405h	EAR[1]	0,1,2,3	R/W	Extended Auxiliary Status

Note 1. These registers are extended to the standard IEEE1284 registers. They are accessible only when enabled by bit 4 of the Parallel Port Configuration register (see Section 2.9.3).

Table 19. Parallel Port Registers at Second Level Offset

Offset	Mnemonic	Type	Register Name
00h	Control0	R/W	Extended Control 0
02h	Control2	R/W	Extended Control 1
04h	Control4	R/W	Extended Control 4
05h	PP Confg0	R/W	Configuration 0

2.9.2 Logical Device 1 (PP) Configuration

Table 20 lists the configuration registers which affect the Parallel Port. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 20. Parallel Port Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b. Bit 2 (for A10) should be 0b.	R/W	02h
61h	Base Address LSB register. Bits 1 and 0 (A1 and A0) are read only, 00b. For ECP Mode 4 (EPP) or when using the Extended registers, bit 2 (A2) should also be 0b.	R/W	78h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	07h
71h	Interrupt Type Bits 7-2 are read only. Bit 1 is a read/write bit. Bit 0 is read only. It reflects the interrupt type dictated by the Parallel Port operation mode. This bit is set to 1 (level interrupt) in Extended Mode and cleared (edge interrupt) in all other modes.	R/W	02h
74h	DMA Channel Select	R/W	04h
75h	Report no second DMA assignment	RO	04h
F0h	Parallel Port Configuration register	R/W	F2h

2.9.3 Parallel Port Configuration Register

This register is reset by hardware to F2h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**Extended Register Access**	**Reserved**		**Power Mode Control**	**TRI-STATE Control**
Reset	1	1	1	1	0	0	1	0
Required	1	1	1					

Bit	Description
7-5	**Reserved.** Must be 11.
4	**Extended Register Access** 0: Registers at base (address) + 403h, base + 404h and base + 405h are not accessible (reads and writes are ignored). 1: Registers at base (address) + 403h, base + 404h and base + 405h are accessible. This option supports run-time configuration within the Parallel Port address space.
3-2	**Reserved**
1	**Power Mode Control.** When the logical device is active: 0: Parallel port clock disabled. ECP modes and EPP time-out are not functional when the logical device is active. Registers are maintained. 1: Parallel port clock enabled. All operation modes are functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.10 SERIAL PORT 2 CONFIGURATION

2.10.1 General Description

Serial Port 2 includes IR functionality as described in the Serial Port 2 with IR chapter.

2.10.2 Logical Device 2 (SP2) Configuration

Table 21 lists the configuration registers which affect the Serial Port 2. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 21. Serial Port 2 Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register and bit 2 of the SIOCF6 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	02h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	03h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	03h
74h	DMA Channel Select 0 (RX_DMA)	R/W	04h
75h	DMA Channel Select 1 (TX_DMA)	R/W	04h
F0h	Serial Port 2 Configuration register	R/W	02h

2.10.3 Serial Port 2 Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 2. 0: All attempts to access the extended registers in Serial Port 2 are ignored (default). 1: Enables bank switching for Serial Port 2.
6-3	**Reserved**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 2 logical device. 0: No transfer in progress (default). 1: Transfer in progress.
1	**Power Mode Control.** When the logical device is active in: 0: Low power mode Serial Port 2 Clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained. (Unlike Active bit in Index 30 that also prevents access to Serial Port 2 registers.) 1: Normal power mode Serial Port 2 clock enabled. Serial Port 2 is functional when the logical device is active (default).
0	**TRI-STATE Control**. When enabled and the device is inactive, the logical device output pins are in TRI-STATE. One exception is the IRTX pin, which is driven to 0 when Serial Port 2 is inactive and is not affected by this bit. 0: Disabled (default) 1: Enabled

2.11 SERIAL PORT 1 CONFIGURATION

2.11.1 Logical Device 3 (SP1) Configuration

Table 22 lists the configuration registers which affect the Serial Port 2. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 22. Serial Port 1 Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register and bit 3 of the SIOCF6 register.	R/W	00h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	03h
61h	Base Address LSB register. Bit 2-0 (for A2-0) are read only, 000b.	R/W	F8h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	04h
71h	Interrupt Type. Bit 1 is R/W; other bits are read only.	R/W	03h
74h	Report no DMA Assignment	RO	04h
75h	Report no DMA Assignment	RO	04h
F0h	Serial Port 1 Configuration register	R/W	02h

2.11.2 Serial Port 1 Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Bank Select Enable**	**Reserved**				**Busy Indicator**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7	**Bank Select Enable**. Enables bank switching for Serial Port 1. 0: Disabled (default). 1: Enabled
6-3	**Reserved**
2	**Busy Indicator.** This read only bit can be used by power management software to decide when to power-down the Serial Port 1 logical device. 0: No transfer in progress (default). 1: Transfer in progress.
1	**Power Mode Control.** When the logical device is active in: 0: Low power mode Serial Port 1 Clock disabled. The output signals are set to their default states. The $\overline{RI}$ input signal can be programmed to generate an interrupt. Registers are maintained. (Unlike Active bit in Index 30 that also prevents access to Serial Port 1 registers.) 1: Normal power mode Serial Port 1 clock enabled. Serial Port 1 is functional when the logical device is active (default).
0	**TRI-STATE Control**. When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.12 SYSTEM WAKE-UP CONTROL (SWC) CONFIGURATION

2.12.1 Logical Device 4 (SWC) Configuration

Table 23 lists the configuration registers which affect the SWC. See Sections 2.2.3 and 2.2.4 for a detailed description of these registers.

Table 23. System Wake-Up Control (SWC) Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. When bit 0 is cleared, the registers of this logical device are not accessible. Note 1.	R/W	00h
60h	Base Address MSB register	R/W	00h
61h	Base Address LSB register. Bits 4-0 (for A4-0) are read only, 00000b.	R/W	00h
70h	Interrupt Number	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h

Note 1. The logical device registers are maintained, and all wake-up detection mechanisms are functional.

2.13 KEYBOARD AND MOUSE CONTROLLER (KBC) CONFIGURATION

2.13.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a Mouse controller (Logical Device 5) and a Keyboard controller (Logical Device 6).

The hardware KBC module is integrated to provide the following pin functions: P12, P16, P17, KBRST (P20), GA20 (P21), KBDAT, KBCLK, MDAT, and MCLK. KBRST and GA20 are implemented as bi-directional, open-drain pins. The Keyboard and Mouse interfaces are implemented as bi-directional, open-drain pins. Their internal connections are shown in Figure 5.

P10, P11, P13-P15, P22-P27 of the KBC core are not available on dedicated pins; neither are T0 and T1. P10, P11, P22, P23, P26, P27, T0 and T1 are used to implement the Keyboard and Mouse interface.

Internal pull-ups are implemented only on P12, P16 and P17.

The KBC executes a program fetched from an on-chip 2Kbyte ROM. The code programmed in this ROM is user-customizable. The KBC has two interrupt request signals: one for the Keyboard and one for the Mouse. The interrupt requests are implemented using ports P24 and P25 of the KBC core. The interrupt requests are controlled exclusively by the KBC firmware, except for the type and number, which are affected by configuration registers (see Section 2.13.2 24).

The interrupt requests are implemented as bi-directional signals. When an I/O port is read, all unused bits return the value latched in the output registers of the ports.

For KBC firmware that implements interrupt-on-OBF schemes, it is recommended to implement it as follows:

1. Put the data in DBBOUT.
2. Set the appropriate port bit to issue an interrupt request.

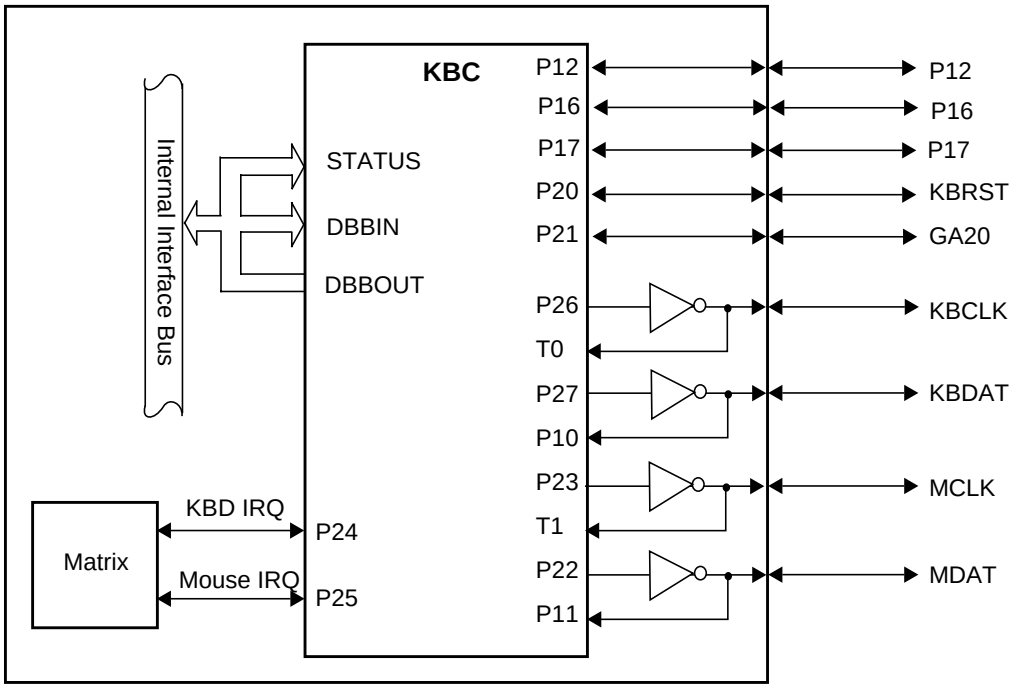


Figure 5. Keyboard and Mouse Interfaces

2.13.2 Logical Devices 5 and 6 (Mouse and Keyboard) Configuration

Tables 24 and 25 list the configuration registers which affect the Mouse and the Keyboard respectively. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for descriptions of the others.

Table 24. Mouse Configuration Registers

Index	Mouse Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1. When the Mouse of the KBC is inactive, the IRQ selected by the Mouse Interrupt Number and Wake-Up on IRQ Enable register (index 70h) is not asserted. This register has no effect on host KBC commands handling the PS/2 Mouse.	R/W	00h
70h	Mouse Interrupt Number and Wake-Up on IRQ Enable register	R/W	0Ch
71h	Mouse Interrupt Type. Bits 1,0 are read/write; other bits are read only.	R/W	02h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h

Table 25. Keyboard Configuration Registers

Index	Keyboard Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1.	R/W	01h
60h	Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	00h
61h	Base Address LSB register. Bits 2-0 are read only 000b.	R/W	60h
62h	Command Base Address MSB register. Bits 7-3 (for A15-11) are read only, 00000b.	R/W	00h
63h	Command Base Address LSB. Bits 2-0 are read only 100b.	R/W	64h
70h	KBD Interrupt Number and Wake-Up on IRQ Enable register	R/W	01h
71h	KBD Interrupt Type. Bits 1,0 are read/write; others are read only.	R/W	02h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	KBC Configuration register	R/W	40h

2.13.3 KBC Configuration Register

This register is reset by hardware to 40h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**KBC Clock Source**		**Reserved**					**TRI-STATE Control**
Reset	0	1	0	0	0	0	0	0
Required						0		

Bit	Description
7-6	**KBC Clock Source.** The clock source can be changed only when the KBC is inactive (disabled). **Bits 7 6 Source** 0 0 8 MHz 0 1 12 MHz (default) 1 0 16 MHz 1 1 Reserved
5-1	**Reserved**
0	**TRI-STATE Control**. If KBD is inactive (disabled) when this bit is set, the KBD pins (KBCLK and KBDAT) are in TRI-STATE. If Mouse is inactive (disabled) when this bit is set, the Mouse pins (MCLK and MDAT) are in TRI-STATE. 0: Disabled (default) 1: Enabled

Usage Hints:

1. To change the clock frequency of the KBC, perform the following:
   a. Disable the KBC logical devices.
   b. Change the frequency setting.
   c. Enable the KBC logical devices.

2.14 GENERAL-PURPOSE INPUT/OUTPUT (GPIO) PORTS CONFIGURATION

2.14.1 General Description

The GPIO functional block includes 37 pins, arranged in four 8-bit ports (ports 0, 1, 2 and 4) and one 5-bit port (port 3). All pins in port 0 are I/O, and have full event detection capability, enabling them to trigger the assertion of IRQ, SMI and PWUREQ signals. With the exception of bit 5 which is output only, port 1 pins are also I/O with full event detection capability. All pins in ports 2 and 3 are I/O, but none of them has event detection capability. The sixteen runtime registers associated with the five ports are arranged in the GPIO address space as shown in Table 26. The GPIO base address is 16-byte aligned. Address bits 3-0 are used to indicate the register offset.

Table 26. Runtime Registers in GPIO Address Space

Offset	Mnemonic	Register Name	Port	Type
00h	GPDO0	GPIO Data Out 0	0	R/W
01h	GPDI0	GPIO Data In 0		RO
02h	GPEVEN0	GPIO Event Enable 0		R/W
03h	GPEVST0	GPIO Event Status 0		R/W1C
04h	GPDO1	GPIO Data Out 1	1	R/W
05h	GPDI1	GPIO Data In 1		RO
06h	GPEVEN1	GPIO Event Enable 1		R/W
07h	GPEVST1	GPIO Event Status 1		R/W1C
08h	GPDO2	Data Out 2	2	R/W
09h	GPDI2	Data In 2		RO
0Ah	GPDO3	Data Out 3	3	R/W
0Bh	GPDI3	Data In 3		RO
0Ch	GPDO4	GPIO Data Out 4	4	R/W
0Dh	GPDI4	GPIO Data In 4		RO
0Eh	GPEVEN4	GPIO Event Enable 4		R/W
0Fh	GPEVST4	GPIO Event Status 4		R/W1C

2.14.2 Implementation

The standard GPIO port with event detection capability (such as ports 0, 1 and 4) has four runtime registers. Each pin is associated with a GPIO Pin Configuration register that includes seven configuration bits. Ports 2 and 3 are non-standard ports that do not support event detection, and therefore differ from the generic model as follows:

- They each have two runtime registers for basic functionality: GPDO2/3 and GPDI2/3. Event detection registers GPEVEN2/3 and GPEVST2/3 are not available.
- Only bits 3-0 are implemented in the GPIO Pin Configuration registers of ports 2 and 3. Bits 6-4, associated with the event detection functionality, are reserved.

2.14.3 Logical Device 7 (GPIO) Configuration

Table 27 lists the configuration registers which affect the GPIO. Only the last three registers (F0h - F2h) are described here. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 27. GPIO Configuration Register

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 7 of the SIOCF1 register.	R/W	00h
60h	Base Address MSB register	R/W	00h
61h	Base Address LSB register. Bits 3-0 (for A3-0) are read only, 0000b.	R/W	00h
70h	Interrupt Number	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	GPIO Pin Select register	R/W	00h
F1h	GPIO Pin Configuration register	R/W	00h
F2h	GPIO Pin Event Routing register	R/W	00h

Figure shows the organization of these registers.

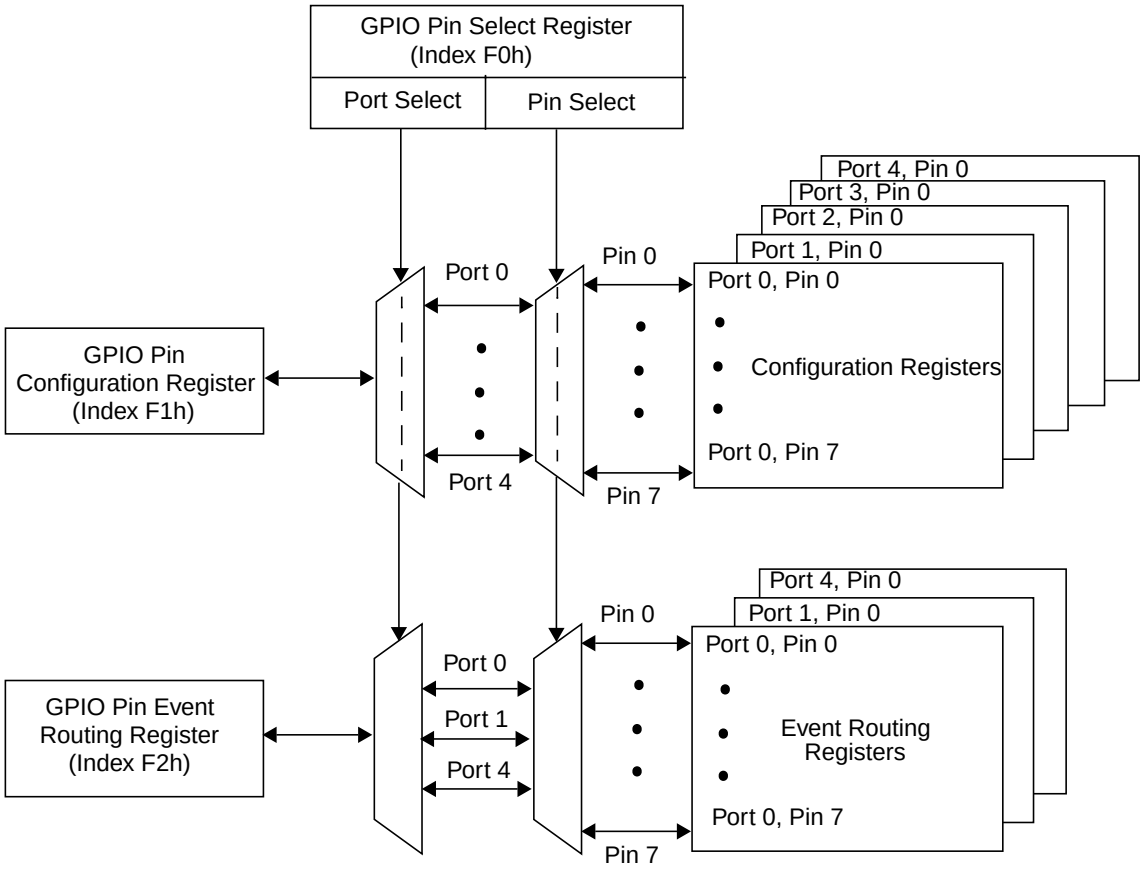


Figure 6. Organization of GPIO Pin Registers

2.14.4 GPIO Pin Select Register

This register selects the GPIO pin (port number and bit number) to be configured (i.e., which register is accessed via the GPIO Pin Configuration register). It is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**Port Select**			**Reserved**	**Pin Select**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved**
6-4	**Port Select.** These bits select the GPIO port to be configured: 000: Port 0 (default) 001, 010, 011,100: Binary value of port numbers 1-4 respectively. All other values are reserved.
3	**Reserved**
2-0	**Pin Select.** These bits select the GPIO pin to be configured in the selected port: 000, 001, ... 111: Binary value of the pin number, 0, 1, ... 7 respectively (default=0)

2.14.5 GPIO Pin Configuration Register

This register reflects, for both read and write, the register currently selected by the GPIO Pin Select register. All the GPIO Pin registers that are accessed via this register have a common bit structure, as shown below. This register is reset by hardware to 44h, except for ports 2 and 3, that are reset to 04h.

Location: Index F1h

Type: R/W

Ports: 0,1 and 4 (with event detection capability)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**Event Debounce Enable**	**Event Polarity**	**Event Type**	**Lock**	**Pull-Up Control**	**Output Type**	**Output Enable**
Reset	0	1	0	0	0	1	0	0

Ports 2 and 3 (without event detection capability)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Lock**	**Pull-Up Control**	**Output Type**	**Output Enable**
Reset	0	0	0	0	0	1	0	0

Bit	Description
7	**Reserved**
6	**Event Debounce Enable.** (Ports 0,1 and 4 with event detection capability). Enables transferring the signal only after a predetermined debouncing period of time. 0: Disabled 1: Enabled (default) **Reserved.** (Ports 2 and 3). Always 0.
5	**Event Polarity.** (Ports 0,1 and 4 with event detection capability). This bit defines the polarity of the signal that issues an interrupt from the corresponding GPIO pin (falling/low or rising/high). 0: Falling edge or low level input (default) 1: Rising edge or high level input **Reserved.** (Ports 2 and 3). Always 0.
4	**Event Type.** (Ports 0,1 and 4 with event detection capability). This bit defines the type of the signal that issues an interrupt from the corresponding GPIO pin (edge or level). 0: Edge input (default) 1: Level input **Reserved.** (Ports 2 and 3). Always 0.
3	**Lock**. This bit locks the corresponding GPIO pin. Once this bit is set to 1 by software, it can only be cleared to 0 by system reset or power-off. Pin multiplexing is functional until the Multiplexing Lock bit is 1 (bit 7 of SuperI/O Configuration 3 register, SIOCF3). 0: No effect (default) 1: Direction, output type, pull-up and output value locked
2	**Pull-Up Control**. This bit is used to enable/disable the internal pull-up capability of the corresponding GPIO pin. It supports open-drain output signals with internal pull-ups and TTL input signals 0: Disabled 1: Enabled (default)
1	**Output Type.** This bit controls the output buffer type (open-drain or push-pull) of the corresponding GPIO pin. 0: Open-drain (default) 1: Push-pull
0	**Output Enable.** This bit indicates the GPIO pin output state. It has no effect on the input path. 0: TRI-STATE (default) 1: Output enabled

2.14.6 GPIO Event Routing Register

This register enables the routing of the GPIO event to IRQ, $\overline{SMI}$ and/or $\overline{PWUREQ}$ signals. It is implemented only for ports 0,1 and 4 which have event detection capability. This register is reset by hardware to 00h.

Location: Index F2h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**Enable $\overline{PWUREQ}$ Routing**	**Enable $\overline{SMI}$ Routing**	**Enable IRQ Routing**
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-3	**Reserved**
2	**Enable $\overline{PWUREQ}$ Routing** 0: Disabled (default) 1: Enabled
1	**Enable $\overline{SMI}$ Routing** 0: Disabled (default) 1: Enabled
0	**Enable IRQ Routing** 0: Disabled 1: Enabled (default)

2.15 ACCESS.BUS INTERFACE (ACB) CONFIGURATION

2.15.1 General Description

The ACB is a two-wire synchronous serial interface compatible with the ACCESS.bus physical layer. The ACB uses a 24 MHz internal clock.

The six runtime registers are shown below.

Table 28. ACB Runtime Registers

Offset	Mnemonic	Register Name	Type
00h	ACBSDA	ACB Serial Data	R/W
01h	ACBST	ACB Status	Varies per bit
02h	ACBCST	ACB Control Status	Varies per bit
03h	ACBCTL1	ACB Control 1	R/W
04h	ACBADDR	ACB Own Address	R/W
05h	ACBCTL2	ACB Control 2	R/W

2.15.2 Logical Device 8 (ACB) Configuration

Table 29 lists the configuration registers which affect the ACB. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 29. ACB Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register.	R/W	00h
60h	Base Address MSB register	R/W	00h
61h	Base Address LSB register. Bits 2-0 (for A2-0) are read only, 000b.	R/W	00h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	ACB Configuration register	R/W	00h

2.15.3 ACB Configuration Register

This register is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**Internal Pull-Up Enable**	**Reserved**	
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-3	**Reserved**
2	**Internal Pull-Up Enable** 0: No internal pull-up resistors on SCL and SDA (default) 1: Internal pull-up resistors on SCL and SDA
1-0	**Reserved**

2.16 FAN SPEED CONTROL AND MONITOR (FSCM) CONFIGURATION

2.16.1 General Description

This module includes two Fan Speed Control units and two Fan Speed Monitor units. The 10 runtime registers of the four functional blocks are arranged in the address space shown in Table 30. The base address is 16-byte aligned. Address bits 0-3 are used to indicate the register offset.

Table 30. Runtime Registers in FSCM Address Space

Offset	Mnemonic	Register Name	Function
00h	FCPSR0	Fan Control 0 Pre-Scale	Fan Speed Control 0
01h	FCDCR0	Fan Control 0 Duty Cycle	
02h	FCPSR1	Fan Control 1 Pre-Scale	Fan Speed Control 1
03h	FCDCR1	Fan Control 1 Duty Cycle	
04h-05h	Reserved		
06h	FMTHR0	Fan Monitor 0 Threshold	Fan Speed Monitor 0
07h	FMSPR0	Fan Monitor 0 Speed	
08h	FMCSR0	Fan Monitor 0 Control & Status	
09h	FMTHR1	Fan Monitor 1 Threshold	Fan Speed Monitor 1
0Ah	FMSPR1	Fan Monitor 1 Speed	
0Bh	FMCSR1	Fan Monitor 1 Control & Status	
0Ch-0Fh	Reserved		

2.16.2 Logical Device 9 (FSCM) Configuration

Table 31 lists the configuration registers which affect the Fan Speed Controls and the Fan Speed Monitors. Only the last one (F0h) is described here. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 31. FSCM Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. See also bit 0 of the SIOCF1 register.	R/W	00h
60h	Base Address MSB register	R/W	00h
61h	Base Address LSB register. Bit 3-0 (for A3-0) are read only, 0000b.	R/W	00h
70h	Interrupt Number and Wake-Up on IRQ Enable register	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	Fan Speed Control and Monitor Configuration 1 register	R/W	00h

2.16.3 Fan Speed Control and Monitor Configuration 1 Register

This register is reset by hardware to 00h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Fan Speed Invert 1 Enable**	**Fan Speed Control 1 Enable**	**Fan Speed Monitor 1 Enable**	**Fan Speed Invert 0 Enable**	**Fan Speed Control 0 Enable**	**Fan Speed Monitor 0 Enable**	**Reserved**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Fan Speed Invert 1 Enable** 0: Disabled (default) 1: Enabled
6	**Fan Speed Control 1 Enable** 0: Disabled (default) 1: Enabled
5	**Fan Speed Monitor 1 Enable** 0: Disabled (default) 1: Enabled
4	**Fan Speed Invert 0 Enable** 0: Disabled (default) 1: Enabled
3	**Fan Speed Control 0 Enable** 0: Disabled (default) 1: Enabled
2	**Fan Speed Monitor 0 Enable** 0: Disabled (default) 1: Enabled
1	**Reserved**
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

2.17 WATCHDOG TIMER (WDT) CONFIGURATION

2.17.1 Logical Device 10 (WDT) Configuration

Table 32 lists the configuration registers which affect the WATCHDOG Timer. Only the last register (F0h) is described here. See Sections 2.2.3 and 2.2.4 for a detailed description of the others.

Table 32. WDT Configuration Registers

Index	Configuration Register or Action	Type	Reset
30h	Activate. When bit 0 is cleared, the registers of this logical device are not accessible.	R/W	00h
60h	Base Address MSB register	R/W	00h
61h	Base Address LSB register. Bits 1 and 0 (for A1 and A0) are read only, 00b.	R/W	00h
70h	Interrupt Number (for routing the $\overline{WDO}$ signal) and Wake-Up on IRQ Enable register.	R/W	00h
71h	Interrupt Type. Bit 1 is read/write. Other bits are read only.	R/W	03h
74h	Report no DMA assignment	RO	04h
75h	Report no DMA assignment	RO	04h
F0h	WATCHDOG Timer Configuration register	R/W	02h

2.17.2 WATCHDOG Timer Configuration Register

This register is reset by hardware to 02h.

Location: Index F0h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Output Type**	**Internal Pull-Up Enable**	**Power Mode Control**	**TRI-STATE Control**
Reset	0	0	0	0	0	0	1	0

Bit	Description
7-4	**Reserved**
3	**Output Type.** This bit controls the buffer type (open-drain or push-pull) of the $\overline{WDO}$ pin. 0: Open-drain (default) 1: Push-pull
2	**Internal Pull-Up Enable.** This bit controls the internal pull-up resistor on the $\overline{WDO}$ pin. 0: Disabled (default) 1: Enabled
1	**Power Mode Control** 0: Low power mode: WATCHDOG Timer clock disabled. $\overline{WDO}$ output signal is set to 1. Registers are accessible and maintained (unlike Active bit in Index 30h that also prevents access to WATCHDOG Timer registers). 1: Normal power mode: WATCHDOG Timer clock enabled. WATCHDOG Timer is functional when the logical device is active (default).
0	**TRI-STATE Control.** When enabled and the device is inactive, the logical device output pins are in TRI-STATE. 0: Disabled (default) 1: Enabled

3.0 System Wake-Up Control (SWC)

3.1 OVERVIEW

The SWC recognizes the following maskable system events:

- Modem ring ($\overline{RI1}$ and $\overline{RI2}$ pins)
- Telephone ring ($\overline{RING}$ input pin)
- Keyboard activity or specific programmable key sequence
- Mouse activity or specific programmable sequence of clicks and movements
- Programmable Consumer Electronics IR (CEIR) address
- Wake-up on module IRQs for FDC, Parallel Port, Serial Ports 1 and 2, Mouse, KBC, ACB, Fan Speed Control and Monitor (FSCM) and WATCHDOG Timer (WDT)
- Eight V_{SB}-powered, general-purpose input events (via GPIOE0-5 and GPIE6-7)
- 23 V_{DD}-powered, GPIO-triggered events (via GPIO00-07, GPIO10-14, GPIO16-17 and GPIO40-47)
- Software event.

The SWC notifies the device when any of these events occur by asserting one or more of the following output pins:

- Power-Up Request ($\overline{PWUREQ}$)
- System Management Interrupt ($\overline{SMI}$)
- Interrupt Request (via SERIRQ)

Figure 7 shows the block diagram of the SWC.

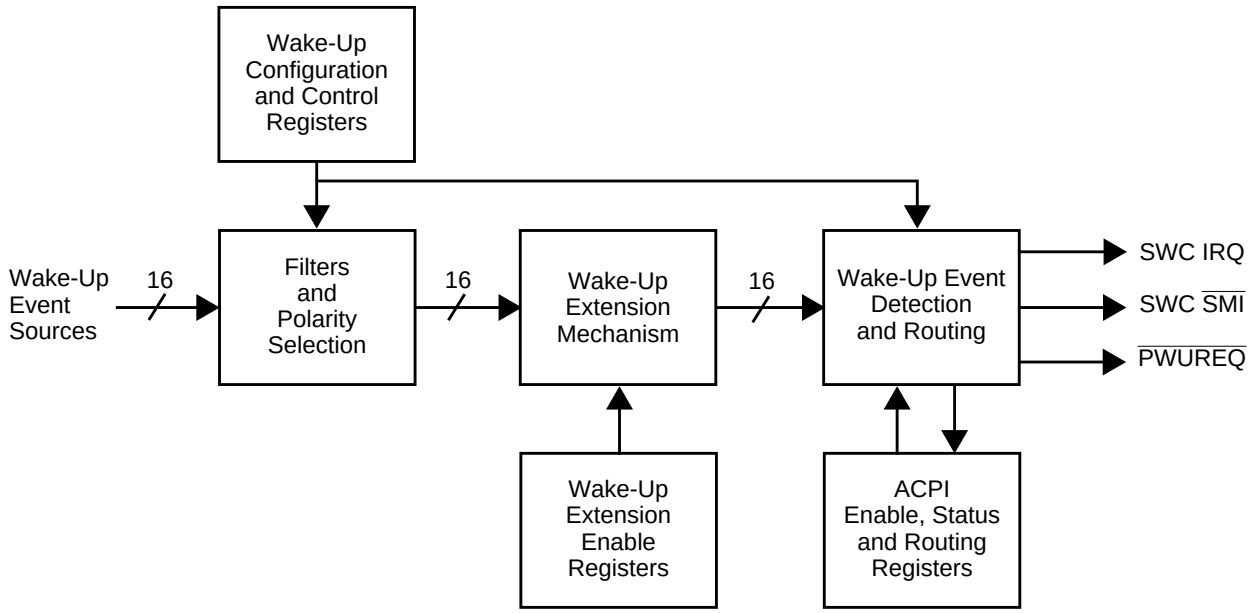


Figure 7. SWC Block Diagram

In addition to the event detection and system notification capabilities, the SWC operates several general-purpose I/O pins powered by V_{SB}. These pins can be used to perform various tasks while V_{SB} is present and V_{DD} is not.

3.2 FUNCTIONAL DESCRIPTION

The SWC monitors 16 system events or activities. Upon entering the SWC, the events pass through a filter (where applicable) and polarity adjustment logic. After filtering and polarity adjustment, each event enters the Wake-Up Mode Control (Extension) Logic which determines its effect during the various system power states. See Figure 7 for an illustration of this mechanism.

3.0 System Wake-Up Control (SWC) (Continued)

After the wake-up mode is determined for all events, each one of them is fed into a dedicated detector that determines when this event is active, according to predetermined (either fixed or programmable) criteria. A set of dedicated registers is used to determine the wake-up criteria, including the CEIR address and the keyboard sequence.

Two Wake-Up Events Status registers (WK_STSn) hold a Status bit for each of the 16 events.

Six Wake-Up Events Routing Control register s (WK_ENn WK_SMIENn and WK_IRQENn) hold three Routing Enable bits for each of the 16 events, to allow selective routing of these events to $\overline{\text{PWUREQ}}$, $\overline{\text{SMI}}$ and/or the assigned SWC interrupt request (IRQ) channel.

Upon detection of any active event, the corresponding Status bit is set to 1, regardless of any Routing Enable bit. If both the Status bit and a Routing Enable bit corresponding to a specific event are set to 1 (no matter in what order), the output pin corresponding to that Routing Enable bit is asserted. The Status bit is deasserted by writing 1 to it. Writing 0 to a Routing Enable bit of an event prevents it from issuing the corresponding system notification, but does not affect the Status bit. Figure 8 show the routing scheme of detected wake-up events to the various means of system notification.

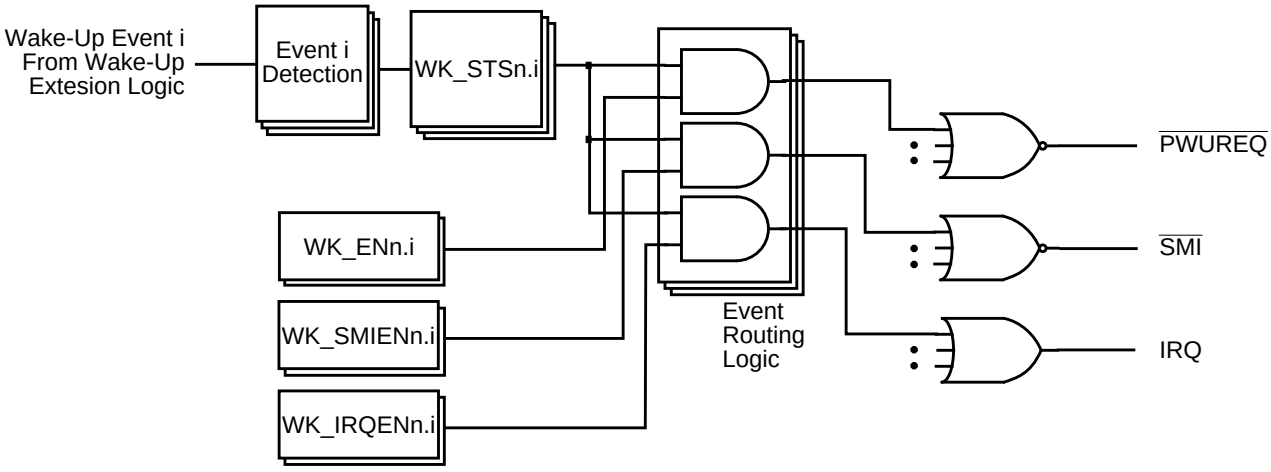


Figure 8. Wake-Up Events Routing Scheme

To enable the assertion of $\overline{\text{SMI}}$ by detected wake-up events, it is necessary to either select the $\overline{\text{SMI}}$ function on a device pin or route it to an interrupt request channel via the device's configuration registers.

Four Wake-Up Extension Enable registers (WK_X1EN0, 1 and WK_X2EN0, 1) hold two configuration bits for each of the 16 events to control the wake-up mode for each one of them. Figure 9 illustrates the Wake-Up Mode Control (Extension) mechanism.

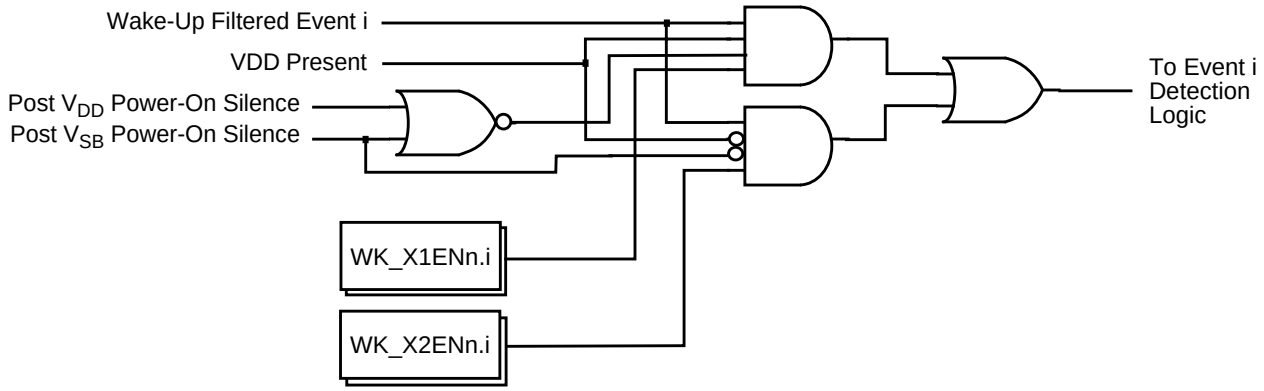


Figure 9. Wake-Up Mode Control (Extension) Mechanism

In addition to monitoring various system events, the SWC operates several general-purpose I/O (GPIO) pins powered by V_{SB}. Two runtime data registers (SB_GPDO0 and SBGPDI0) hold a Data Out bit and a Data In bit for each V_{SB} powered GPIO pin. In addition, each GPIO pin has a dedicated configuration register that controls its characteristics. These configuration registers are accessed via a set of Standby GPIO Pin Select and Pin Configuration registers (SBGPSEL and SBGPCFG). For a detailed description of the V_{SB} powered GPIO pins, see Section 3.4.28.

The SWC logic is powered by V_{SB}. The SWC control and configuration registers are battery backed, powered by V_{PP}. The setup of the wake-up events, including programmable sequences, is retained throughout power failures (no V_{SB}) as long as the battery is connected. V_{PP} is taken from V_{SB} if V_{SB} is greater than the minimum (Min) value defined in the *Device Characteristics* chapter; otherwise, V_{BAT} is used as the V_{PP} source.

Hardware reset does not affect these registers. They are reset only by software reset or power-up of V_{PP}.

3.3 EVENT DETECTION

3.3.1 Modem Ring

High to low transitions on $\overline{RI1}$ or $\overline{RI2}$ indicate the detection of ring in external modem connected to Serial Port 1 or Serial Port 2, respectively, and can be used as wake-up events.

3.3.2 Telephone Ring

A telephone ring is detected by the SWC by processing the raw signal coming directly from the telephone line into the $\overline{RING}$ input pin. Detection of a pulse-train with a frequency higher than 16 Hz that lasts at least 0.19 sec, is used as a wake-up event.

The $\overline{RING}$ pulse-train detection is achieved by monitoring the falling edges on $\overline{RING}$ in time slots of 62.5 msec (a 16 Hz cycle). A positive detection occurs if falling edges of $\overline{RING}$ are detected in three consecutive time slots, following a time slot in which no $\overline{RING}$ falling edge is detected. This detection method guarantees the detection of a $\overline{RING}$ pulse-train with frequencies higher than 16 Hz. It filters out (does not detect) pulses of less than 10 Hz, and may detect pulses between 10 Hz to 16 Hz.

3.3.3 Keyboard and Mouse Activity

The detection of either any activity or a specific predetermined keyboard or mouse activity can be used as a wake-up event.

The keyboard wake-up detection can be programmed to detect:

- Any keystroke
- A specific programmable sequence of up to eight alphanumeric keystrokes
- Any programmable sequence of up to 8 bytes of data received from the keyboard.

The mouse wake-up detection can be programmed to detect either any mouse click or movement, or a specific programmable click (left or right) or double-clicks.

The keyboard or mouse event detection operates independently of the KBC (which is powered down with the rest of the system).

3.3.4 CEIR Address

A CEIR transmission received on an IRRX pin in a pre-selected standard (NEC, RCA or RC-5) is matched against a programmable CEIR address. Detection of matching can be used as a wake-up event.

Whenever an IR signal is detected, the receiver immediately enters the active state. When this happens, the receiver keeps sampling the IR input signal and generates a bit string where a logic 1 indicates an idle condition and a logic 0 indicates the presence of IR energy. The received bit string is de-serialized and assembled into 8-bit characters.

The expected CEIR protocol of the received signal should be configured through bits 5,4 at the CEIR Wake-Up Control register (see Section 3.4.20).

The CEIR Wake-Up Address register (IRWAD) holds the unique address to be compared with the address contained in the incoming CEIR message. If CEIR is enabled (bit 0 of the IRWCR register is 1) and an address match occurs, then the CEIR Event Status bit of the WK_STS0 register is set to 1 (see Section 3.4.2).

The CEIR Address Shift register holds the received address which is compared with the address contained in the IRWAD. The comparison is affected also by the CEIR Wake-Up Address Mask register (IRWAM) in which each bit determines whether to ignore the corresponding bit in the IRWAD.

If CEIR routing to interrupt request is enabled, the assigned SWC interrupt request may be used to indicate that a complete address has been received. To get this interrupt when the address is completely received, the IRWAM should be written with FFh. Once the interrupt is received, the value of the address can be read from the ADSR register.

Another parameter that is used to determine whether a CEIR signal is to be considered valid is the bit cell time width. There are four time ranges for the different protocols and carrier frequencies. Four pairs of registers define the low and high limits of each time range. (See Sections 3.4.27 through for more details regarding the recommended values for each protocol.)

The CEIR address detection operates independently of the serial port with the IR (which is powered down with the rest of the system).

3.3.5 Standby General-Purpose Input Events

A general-purpose event is defined as the detection of falling edge, rising edge, low level or high level on a specific signal. Each signal's event is configurable via software. GPIOE0-5 and GPIE6-7 may trigger a system notification by any of the means mentioned in Section 3.1.

A debouncer of 16 ms is enabled (default) on each event. It may be disabled by software.

3.3.6 GPIO-Triggered Events

A GPIO-triggered event is defined as the detection of falling edge, rising edge, low level or high level on a specific GPIO signal whose status bit is routed to $\overline{\text{PWUREQ}}$. Each signal's event is configurable via software in the GPIO logical device configuration registers. GPIO00-07, GPIO10-14, GPIO16-17 and GPIO40-47 may trigger a system notification only by $\overline{\text{PWUREQ}}$. Other means of system notification triggered by GPIOs are available via the GPIO logical device configuration registers.

A debouncer of 16 ms is enabled (default) on each event. It may be disabled by software.

All GPIO pins are powered by V_{DD}, and therefore can cause an assertion of $\overline{\text{PWUREQ}}$ only when V_{DD} is present.

3.3.7 Software Event

A software event is defined as writing 1 to the Software Event Status bit of the WK_STS0 register. Once this bit is set to 1, it has the same effect as any other Event Status bit.

Since WK_STS0 is accessible only when V_{DD} is present, the Software Event can be activated only when V_{DD} is present.

3.3.8 Module IRQ Wake-Up Event

A module IRQ wake-up event is defined as the leading edge of the IRQ assertion of any of the following logical devices: FDC, Parallel Port, Serial Ports 1 and 2, Mouse, KBC, ACB and Fan Speed Control and Monitor (FSCM).

To enable the IRQ of a specific logical device to trigger a wake-up event, the associated Enable bit must be set to 1. This is bit 4 of the Interrupt Number and Wake-Up on IRQ Enable register, located at index 70h in the configuration space of the logical device (see Table 10 in *Device Architecture and Configuration* chapter). When this bit is set, any IRQ assertion of the corresponding logical device activates the module IRQ wake-up event. Therefore, the module IRQ wake-up event is a combination of all IRQ signals of the logical devices for which wake-up on IRQ is enabled.

When the event is detected as active, its associated Status bit (bit 7 of the WK0_STS register) is set to 1. If the associated Enable bit (bit 7 of the WK_EN0 register) is also set to 1, the $\overline{\text{PWUREQ}}$ output is asserted. It remains asserted until the Status bit is cleared.

Since all the logical devices listed above are powered by V_{DD}, a module IRQ event can be activated only when V_{DD} is present.

3.4 SWC REGISTERS

The SWC registers are organized in four banks, all of which are battery-backed. The offsets are related to a base address that is determined by the SWC Base Address register in the device configuration registers. The lower 19 offsets are common to the four banks, while the upper offsets (13-1fh) are divided as follows:

- Bank 0 holds the Keyboard/Mouse Control registers.
- Bank 1 holds the CEIR Control registers.
- Bank 2 holds the Event Routing Configuration and Wake-Up Extension Control registers.
- Bank 3 holds the Standby General-Purpose I/O (GPIO) Pins Configuration registers.

The active bank is selected through the Configuration Bank Select field (bits 1-0) in the Wake-Up Configuration register (WK_CFG). See Section 3.4.6.

As a programming aid, the registers are described in this chapter according to the following functional groupings:

- General status, enable, configuration and routing registers
- Extension enable registers
- PS/2 event configuration registers
- CEIR event configuration registers
- Standby GPIO configuration and control registers

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

3.4.1 SWC Register Map

The following tables list the SWC registers. For the SWC register bitmap, see Section 3.5.

Table 33. Banks 0, 1, 2 and 3 - The Common Control and Status Register Map

Offset	Mnemonic	Register Name	Type	Section
00h	WK_STS0	Wake-Up Events Status 0	R/W1C	3.4.2
01h	WK_STS1	Wake-Up Events Status 1	R/W1C	3.4.3
02h	WK_EN0	Wake-Up Enable 0	R/W	3.4.4
03h	WK_EN1	Wake-Up Enable 1	R/W	3.4.5
04h	WK_CFG	Wake-Up Configuration	R/W	3.4.6
05h-07h	Reserved			
08h	SB_GPDO0	Standby GPIOE/GPIE Data Out 0	R/W	3.4.31
09h	SB_GPDI0	Standby GPIOE/GPIE Data In 0	RO	3.4.32
0Ah-12h	Reserved			

Table 34. Bank 0 - PS/2 Keyboard/Mouse Wake-Up Configuration and Control Register Map

Offset	Mnemonic	Register Name	Type	Section
13h	PS2CTL	PS/2 Protocol Control	R/W	3.4.16
14h-15h	Reserved			
16h	KDSR	Keyboard Data Shift	RO	3.4.17
17h	MDSR	Mouse Data Shift	RO	3.4.18
08h-1Fh	PS2KEY0-PS2KEY7	PS/2 Keyboard Key Data	R/W	3.4.19

Table 35. Bank 1 - CEIR Wake-Up Configuration and Control Register Map

Offset	Mnemonic	Register Name	Type	Section
13h	IRWCR	CEIR Wake-Up Control	R/W	3.4.20
14h	Reserved			
15h	IRWAD	CEIR Wake-Up Address	R/W	3.4.21
16h	IRWAM	CEIR Wake-Up Address Mask	R/W	3.4.22
17h	ADSR	CEIR Address Shift	R/O	3.4.23
18h	IRWTR0L	CEIR Wake-Up, Range 0, Low Limit	R/W	3.4.24
19h	IRWTR0H	CEIR Wake-Up, Range 0, High Limit	R/W	3.4.24
1Ah	IRWTR1L	CEIR Wake-Up, Range 1, Low Limit	R/W	3.4.25
1Bh	IRWTR1H	CEIR Wake-Up, Range 1, High Limit	R/W	3.4.25
1Ch	IRWTR2L	CEIR Wake-Up, Range 2, Low Limit	R/W	3.4.26
1Dh	IRWTR2H	CEIR Wake-Up, Range 2, High Limit	R/W	3.4.26
1Eh	IRWTR3L	CEIR Wake-Up, Range 3, Low Limit	R/W	3.4.27
1Fh	IRWTR3H	CEIR Wake-Up, Range 3, High Limit	R/W	3.4.27

Table 36. Bank 2 - Event Routing Configuration Register Map

Offset	Mnemonic	Register Name	Type	Section
13h	WK_SMIEN0	Wake-Up SMI Enable 0	R/W	3.4.7
14h	WK_SMIEN1	Wake-Up SMI Enable 1	R/W	3.4.8
15h	WK_IRQEN0	Wake-Up Interrupt Request Enable 0	R/W	3.4.9
16h	WK_IRQEN1	Wake-Up Interrupt Request Enable 1	R/W	3.4.10
17h	WK_X1EN0	Wake-Up Extension 1 Enable 0	R/W	3.4.11
18h	WK_X1EN1	Wake-Up Extension 1 Enable 1	R/W	3.4.12
19h	WK_X2EN0	Wake-Up Extension 2 Enable 0	R/W	3.4.13
1Ah	WK_X2EN1	Wake-Up Extension 2 Enable 1	R/W	3.4.14
1Bh-1Fh	Reserved			

Table 37. Bank 3 - Standby GPIO Pin Configuration Register Map

Offset	Mnemonic	Register Name	Type	Section
13h	SBGPSEL	Standby GPIO Pin Select	R/W	3.4.29
14h	SBGPCFG	Standby GPIO Pin Configuration	R/W	3.4.30
15h-1Fh	Reserved			

3.4.2 Wake-Up Events Status Register 0 (WK_STS0)

This register is set to 00h on power-up of V_{PP}, V_{SB} or software reset. It indicates which of the corresponding eight wake-up events have occurred. Writing 1 to a bit clears it to 0. Writing 0 has no effect. Bit 6 of this register has a special type, as described in the table below.

Location: Offset 00h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Module IRQ Event Status**	**Software Event Status**	**GPIO Event Status**	**CEIR Event Status**	**Mouse Event Status**	**KBD Event Status**	**$\overline{\text{RI2}}$ Event Status**	**$\overline{\text{RI1}}$ Event Status**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Module IRQ Event Status.** This sticky bit shows the status of the module IRQ event detection. 0: Event not active (default) 1: Event active
6	**Software Event Status**. Writing 1 to this bit inverts its value. 0: Event not active (default) 1: Event active
5	**GPIO Event Status.** This sticky bit shows the status of the V_{DD} GPIO event detection. 0: Event not detected (default) 1: Event detected
4	**CEIR Event Status** 0: Event not detected (default) 1: Event detected
3	**Mouse Event Status** 0: Event not detected (default) 1: Event detected
2	**KBD Event Status** 0: Event not detected (default) 1: Event detected
1	**$\overline{\text{RI2}}$ Event Status** 0: Event not detected (default) 1: Event detected
0	**$\overline{\text{RI1}}$ Event Status** 0: Event not detected (default) 1: Event detected

3.4.3 Wake-Up Events Status Register (WK_STS1)

This register is set to 00h on power-up of V_{PP}, V_{SB} or software reset. It indicates which of the corresponding eight wake-up events have occurred. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

Location: Offset 01h

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**GPIE7 Event Status**	**GPIE6 Event Status**	**GPIE5 Event Status**	**GPIE4/ $\overline{\text{RING}}$ Event Status**	**GPIE3 Event Status**	**GPIE2 Event Status**	**GPIE1 Event Status**	**GPIE0 Event Status**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIE7 Event Status** 0: Event not detected (default) 1: Event detected
6	**GPIE6 Event Status** 0: Event not detected (default) 1: Event detected
5	**GPIE5 Event Status** 0: Event not detected (default) 1: Event detected
4	**GPIE4/$\overline{\text{RING}}$ Event Status.** This sticky bit shows the status of either GPIE4 or $\overline{\text{RING}}$ event detection, according to the function currently selected on pin 27. 0: Event not detected (default) 1: Event detected
3	**GPIE3 Event Status** 0: Event not detected (default) 1: Event detected
2	**GPIE2 Event Status** 0: Event not detected (default) 1: Event detected
1	**GPIE1 Event Status** 0: Event not detected (default) 1: Event detected
0	**GPIE0 Event Status** 0: Event not detected (default) 1: Event detected

3.4.4 Wake-Up Events Enable Register (WK_EN0)

This register is set to 00h on power-up of V_{PP} or software reset. Detected wake-up events that are enabled activate the $\overline{\text{PWUREQ}}$ signal.

Location: Offset 02h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Module IRQ Event Enable**	**Software Event Enable**	**GPIO Event Enable**	**CEIR Event Enable**	**Mouse Event Enable**	**KBD Event Enable**	**$\overline{\text{RI2}}$ Event Enable**	**$\overline{\text{RI1}}$ Event Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Module IRQ Event Enable** 0: Disabled (default) 1: Enabled
6	**Software Event Enable** 0: Disabled (default) 1: Enabled
5	**GPIO Event Enable** 0: Disabled (default) 1: Enabled
4	**CEIR Event Enable** 0: Disabled (default) 1: Enabled
3	**Mouse Event Enable** 0: Disabled (default) 1: Enabled
2	**KBD Event Enable** 0: Disabled (default) 1: Enabled
1	**$\overline{\text{RI2}}$ Event Enable** 0: Disabled (default) 1: Enabled
0	**$\overline{\text{RI1}}$ Event Enable** 0: Disabled (default) 1: Enabled

3.4.5 Wake-Up Events Enable Register 1 (WK_EN1)

This register is set to 00h on power-up of V_{PP} or software reset. Detected wake-up events that are enabled activate the $\overline{\text{PWUREQ}}$ signal.

Location: Offset 03h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIE7 Event Enable**	**GPIE6 Event Enable**	**GPIE5 Event Enable**	**GPIE4/ $\overline{\text{RING}}$ Event Enable**	**GPIE3 Event Enable**	**GPIE2 Event Enable**	**GPIE1 Event Enable**	**GPIE0 Event Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIE7 Event Enable** 0: Disabled (default) 1: Enabled
6	**GPIE6 Event Enable** 0: Disabled (default) 1: Enabled
5	**GPIE5 Event Enable** 0: Disabled (default) 1: Enabled
4	**GPIE4/$\overline{\text{RING}}$ Event Enable** 0: Disabled (default) 1: Enabled
3	**GPIE3 Event Enable** 0: Disabled (default) 1: Enabled.
2	**GPIE2 Event Enable** 0: Disabled (default) 1: Enabled
1	**GPIE1 Event Enable** 0: Disabled (default) 1: Enabled
0	**GPIE0 Event Enable** 0: Disabled (default) 1: Enabled

3.4.6 Wake-Up Configuration Register (WK_CFG)

This register is set to 00h on power-up of V_{PP} or software reset. It enables access to CEIR registers, keyboard/mouse registers, Event Routing Control registers or Standby GPIO registers.

Location: Offset 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**Swap KBC Inputs**	**Configuration Bank Select**	
Reset	0	0	0	0	0	0	0	0
Required	0	0						

Bit	Description
7-3	**Reserved**
2	**Swap KBC Inputs** 0: No swapping (default) 1: KBD (KBCLK, KBDAT) and Mouse (MCLK, MDAT) inputs swapped
1-0	**Configuration Bank Select** **Bits 1 0 — Bank — Register** 0 0 — 0 — Keyboard/Mouse 0 1 — 1 — CEIR 1 0 — 2 — Event Routing, Wake-Up Extension 1 1 — 3 — Standby GPIO

3.4.7 Wake-Up Events Routing to $\overline{\text{SMI}}$ Enable Register 0 (WK_SMIEN0)

This register is set to 00h on power-up of V_{PP} or software reset. It controls the routing of detected wake-up events to the $\overline{\text{SMI}}$ signal. Detected wake-up events that are enabled activate the $\overline{\text{SMI}}$ signal regardless of the value of the WK_EN0 register.

Location: Bank 2, Offset 13h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**Software Event to $\overline{\text{SMI}}$ Enable**	**Reserved**	**CEIR Event to $\overline{\text{SMI}}$ Enable**	**Mouse Event to SMI Enable**	**KBD Event to $\overline{\text{SMI}}$ Enable**	**$\overline{\text{RI2}}$ Event to $\overline{\text{SMI}}$ Enable**	**$\overline{\text{RI1}}$ Event to $\overline{\text{SMI}}$ Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved**
6	**Software Event to SMI Enable** 0: Disabled (default) 1: Enabled
5	**Reserved**
4	**CEIR Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
3	**Mouse Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
2	**KBD Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
1	**$\overline{\text{RI2}}$ Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
0	**$\overline{\text{RI1}}$ Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled

3.4.8 Wake-Up Events Routing to $\overline{\text{SMI}}$ Enable Register 1 (WK_SMIEN1)

This register is set to 00h on power-up of V_{PP} or software reset. It controls the routing of detected wake-up events to the $\overline{\text{SMI}}$ signal. Detected wake-up events that are enabled activate the $\overline{\text{SMI}}$ signal regardless of the value of the WK_EN1 register.

Location: Bank 2, Offset 14h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIE7 Event to $\overline{\text{SMI}}$ Enable**	**GPIE6 Event to $\overline{\text{SMI}}$ Enable**	**GPIE5 Event to $\overline{\text{SMI}}$ Enable**	**GPIE4/ $\overline{\text{RING}}$ Event to $\overline{\text{SMI}}$ Enable**	**GPIE3 Event to $\overline{\text{SMI}}$ Enable**	**GPIE2 Event to $\overline{\text{SMI}}$ Enable**	**GPIE1 Event to $\overline{\text{SMI}}$ Enable**	**GPIE0 Event to $\overline{\text{SMI}}$ Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIE7 Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
6	**GPIE6 Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
5	**GPIE5 Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
4	**GPIE4/$\overline{\text{RING}}$ Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
3	**GPIE3 Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled.
2	**GPIE2 Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
1	**GPIE1 Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled
0	**GPIE0 Event to $\overline{\text{SMI}}$ Enable** 0: Disabled (default) 1: Enabled

3.4.9 Wake-Up Events Routing to IRQ Enable Register 0 (WK_IRQEN0)

This register is set to 00h on power-up of V_{PP} or software reset. It controls the routing of detected wake-up events to the assigned SWC interrupt request (IRQ) channel. Detected wake-up events that are enabled activate the assigned IRQ channel regardless of the value of the WK_EN0 register.

Location: Bank 2, Offset 15h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**Software Event to IRQ Enable**	**Reserved**	**CEIR Event to IRQ Enable**	**Mouse Event to IRQ Enable**	**KBD Event to IRQ Enable**	**$\overline{\text{RI2}}$ Event to IRQ Enable**	**$\overline{\text{RI1}}$ Event to IRQ Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Reserved**
6	**Software Event to IRQ Enable** 0: Disabled (default) 1: Enabled
5	**Reserved**
4	**CEIR Event to IRQ Enable** 0: Disabled (default) 1: Enabled
3	**Mouse Event to IRQ Enable** 0: Disabled (default) 1: Enabled
2	**KBD Event to IRQ Enable** 0: Disabled (default) 1: Enabled.
1	**$\overline{\text{RI2}}$ Event to IRQ Enable** 0: Disabled (default) 1: Enabled
0	**$\overline{\text{RI1}}$ Event to IRQ Enable** 0: Disabled (default) 1: Enabled

3.4.10 Wake-Up Events Routing to IRQ Enable Register 1 (WK_IRQEN1)

This register is set to 00h on power-up of V_{PP} or software reset. It controls the routing of detected wake-up events to the assigned SWC IRQ channel. Detected wake-up events that are enabled activate the IRQ signal regardless of the value of the WK_EN1 register.

Location: Bank 2, Offset 16h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIE7 Event to IRQ Enable**	**GPIE6 Event to IRQ Enable**	**GPIE5 Event to IRQ Enable**	**GPIE4/ $\overline{\text{RING}}$ Event to IRQ Enable**	**GPIE3 Event to IRQ Enable**	**GPIE2 Event to IRQ Enable**	**GPIE1 Event to IRQ Enable**	**GPIE0 Event to IRQ Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**GPIE7 Event to IRQ Enable** 0: Disabled (default) 1: Enabled
6	**GPIE6 Event to IRQ Enable** 0: Disabled (default) 1: Enabled
5	**GPIOE5 Event to IRQ Enable** 0: Disabled (default) 1: Enabled
4	**GPIE4/$\overline{\text{RING}}$ Event to IRQ Enable** 0: Disabled (default) 1: Enabled
3	**GPIE3 Event to IRQ Enable** 0: Disabled (default) 1: Enabled.
2	**GPIE2 Event to IRQ Enable** 0: Disabled (default) 1: Enabled
1	**GPIE1 Event to IRQ Enable** 0: Disabled (default) 1: Enabled
0	**GPIE0 Event to IRQ Enable** 0: Disabled (default) 1: Enabled

3.4.11 Wake-Up Extension 1 Enable Register 0 (WK_X1EN0)

This register is set to 1Fh on power-up of V_{PP} or software reset. It controls the routing of raw wake-up events to event detectors while V_{DD} is present. Wake-up events that are enabled are routed to their event detectors while V_{DD} is present.

Location: Bank 2, Offset 17h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**CEIR Event Ex. 1 Enable**	**Mouse Event Ex. 1 Enable**	**KBD Event Ex. 1 Enable**	**$\overline{\text{RI2}}$ Event Ex. 1 Enable**	**$\overline{\text{RI1}}$ Event Ex.1 Enable**
Reset	0	0	0	1	1	1	1	1

Bit	Description
7-5	**Reserved**
4	**CEIR Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
3	**Mouse Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
2	**KBD Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
1	**$\overline{\text{RI2}}$ Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
0	**$\overline{\text{RI1}}$ Event Extension 1 Enable** 0: Disabled 1: Enabled (default)

3.4.12 Wake-Up Extension 1 Enable Register 1 (WK_X1EN1)

This register is set to FFh on power-up of V_{PP} or software reset. It controls the routing of raw wake-up events to event detectors while V_{DD} is present. Wake-up events that are enabled are routed to their event detectors while V_{DD} is present.

Location: Bank 2, Offset 18h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIE7 Event Ex. 1 Enable**	**GPIE6 Event Ex. 1 Enable**	**GPIE5 Event Ex. 1 Enable**	**GPIE4/ $\overline{\text{RING}}$ Event Ex. 1 Enable**	**GPIE3 Event Ex. 1 Enable**	**GPIE2 Event Ex. 1 Enable**	**GPIE1 Event Ex. 1 Enable**	**GPIE0 Event Ex. 1 Enable**
Reset	1	1	1	1	1	1	1	1

Bit	Description
7	**GPIE7 Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
6	**GPIE6 Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
5	**GPIE5 Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
4	**GPIE4/$\overline{\text{RING}}$ Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
3	**GPIE3 Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
2	**GPIE2 Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
1	**GPIE1 Event Extension 1 Enable** 0: Disabled 1: Enabled (default)
0	**GPIE0 Event Extension 1 Enable** 0: Disabled 1: Enabled (default)

3.4.13 Wake-Up Extension 2 Enable Register 0 (WK_X2EN0)

This register is set to 1Fh on power-up of V_{PP} or software reset. It controls the routing of raw wake-up events to event detectors while V_{DD} is not present. Wake-up events that are enabled are routed to their event detectors while V_{DD} is not present.

Location: Bank 2, Offset 19h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**CEIR Event Ex. 2 Enable**	**Mouse Event Ex. 2 Enable**	**KBD Event Ex. 2 Enable**	**$\overline{\text{RI2}}$ Event Ex. 2 Enable**	**$\overline{\text{RI1}}$ Event Ex. 2 Enable**
Reset	0	0	0	1	1	1	1	1

Bit	Description
7-5	**Reserved**
4	**CEIR Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
3	**Mouse Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
2	**KBD Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
1	**$\overline{\text{RI2}}$ Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
0	**$\overline{\text{RI1}}$ Event Extension 2 Enable** 0: Disabled 1: Enabled (default)

3.4.14 Wake-Up Extension 2 Enable Register 1 (WK_X2EN1)

This register is set to FFh on power-up of V_{PP} or software reset. It controls the routing of raw wake-up events to event detectors while V_{DD} is not present. Wake-up events that are enabled are routed to their event detectors while V_{DD} is not present.

Location: Bank 2, Offset 1Ah

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**GPIE7 Event Ex. 2 Enable**	**GPIE6 Event Ex. 2 Enable**	**GPIE5 Event Ex. 2 Enable**	**GPIE4/ $\overline{\text{RING}}$ Event Ex. 2 Enable**	**GPIE3 Event Ex. 2 Enable**	**GPIE2 Event Ex. 2 Enable**	**GPIE1 Event Ex. 2 Enable**	**GPIE0 Event Ex. 2 Enable**
Reset	1	1	1	1	1	1	1	1

Bit	Description
7	**GPIE7 Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
6	**GPIE6 Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
5	**GPIE5 Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
4	**GPIE4/$\overline{\text{RING}}$ Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
3	**GPIE3 Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
2	**GPIE2 Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
1	**GPIE1 Event Extension 2 Enable** 0: Disabled 1: Enabled (default)
0	**GPIE0 Event Extension 2 Enable** 0: Disabled 1: Enabled (default)

3.4.15 PS/2 Keyboard and Mouse Wake-Up Events

The SWC can be configured to detect any predetermined PS/2 keyboard or mouse activity.

The detection mechanisms for keyboard and mouse events are independent. Therefore, they can be operated simultaneously with no interference. Since both mechanisms are implemented by hardware which is independent of the device's keyboard controller, the keyboard controller itself need not be activated to detect either keyboard or mouse events.

Keyboard Wake-Up Events

The keyboard wake-up detection mechanism can be programmed to detect:

- Any keystroke
- A specific programmable sequence of up to eight alphanumeric keystrokes (Password mode)
- Any programmable sequence of up to 8 bytes of data received from the keyboard (Special Key Sequence mode).

To program the keyboard wake-up detection mechanism to wake-up on any keystroke, perform the following sequence:

1. Put the wake-up mechansim in Special Key Sequence mode by setting bits 3-0 of the PS2CTL register to 0001b.
2. Set the PS2KEY0 and PS2KEY1 registers to 00h. This forces the wake-up detection mechanism to ignore the values of incoming data, thus causing it to wake-up on any keystroke.

In Password mode, the Make and Break bytes transmitted by the keyboard are discarded, and only the scan codes are compared against those programmed in the PS2KEYn registers. To simplify the detection mechanism, only keys with a scan code of 1 byte can be included in the sequence to be detected. To program the keyboard wake-up detection mechanism to operate in Password mode, proceed as follows:

1. Set bits 3-0 of the PS2CTL register with a value that indicates the desired number of keystrokes in the sequence. The programmed value should be the number of keystrokes + 7. For example, to wake-up on a sequence of two keys, set bits 3-0 to 9h.
2. Program the appropriate subset of the PS2KEY0-PS2KEY7 registers, in sequential order, with the scan codes of the keys in the sequence. For example, if there are three keys in the sequence and the scan codes of these keys are 05h (first), 50h (second) and 44h (third), program PS2KEY0 to 05h, PS2KEY1 to 50h and PS2KEY2 to 44h (the scan codes are only examples).

In Special Key Sequence mode, all the bytes transmitted by the keyboard are compared against the ones programmed in the PS2KEYn registers. These include also the Make and Break bytes. This mode enables the detection of any sequence of keystrokes, including also keys such as Shift and Alt. To program the keyboard wake-up detection mechanism to operate in Special Key Sequence mode, proceed as follows:

1. Set bits 3-0 of the PS2CTL register to a value that indicates the desired number of keystrokes in the sequence. The programmed value should be the number of keystrokes + 1. For example, to wake-up on a sequence of three received bytes, set bits 3-0 of PS2CTL to 2h.
2. Program the appropriate subset of the PS2KEY0-PS2KEY7 registers, in sequential order, with the values of the data bytes that comprise the sequence. For example, if the number of bytes in the sequence is four, and the values of these bytes are E0h (first), 5Bh (second), E0h (third) and DBh (fourth), program PS2KEY0 to E0h, PS2KEY1 to 5Bh, PS2KEY2 to E0h and PS2KEY3 to DBh (the byte values are only examples).

Mouse Wake-Up Events

The mouse wake-up detection mechanism can be programmed to detect either any mouse click or movement, or a specific programmable click (left or right) or double-click.

To program this mechanism to wake-up on a specific event, set bits 6-4 of the PS2CTL register to the required value, according to the description of these bits in Section 3.4.16.

3.4.16 PS/2 Protocol Control Register (PS2CTL)

This register is set to 00h on power-up of V_{PP} or software reset. It configures the PS/2 keyboard and mouse wake-up features. Before changing bits 6-4 or 3-0, clear them to 0 and then write the new value.

Location: Bank 0, Offset 13h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Disable Parity Check**	**Mouse Wake-Up Configuration**			**Keyboard Wake-Up Configuration**			
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Disable Parity Check** 0: Enabled (default) 1: Disabled
6-4	**Mouse Wake-Up Configuration** **Bits 6 5 4 — Configuration** 0 0 0 Disable mouse wake-up detection 0 0 1 Wake-up on any mouse movement or button click 0 1 0 Wake-up on left button click 0 1 1 Wake-up on left button double-click 1 0 0 Wake-up on right button click 1 0 1 Wake-up on right button double-click 1 1 0 Wake-up on any button single-click (left, right or middle) 1 1 1 Wake-up on any button double-click (left, right or middle)
3-0	**Keyboard Wake-Up Configuration** **Bits 3 2 1 0 — Configuration** 0 0 0 0 Disable keyboard wake-up detection 0 0 0 1 to 0 1 1 1 } Special key sequence 2-8 PS/2 scan codes, “Make” and “Break” (including Shift and Alt keys) 1 0 0 0 to 1 1 1 1 } Password enabled with 1-8 keys “Make” code (excluding Shift and Alt keys)

3.4.17 Keyboard Data Shift Register (KDSR)

This register is set to 00h on power-up of V_{PP} or software reset. It stores the keyboard data shifted in from the keyboard during transmission, only when keyboard wake-up detection is enabled.

Location: Bank 0, Offset 16h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Keyboard Data**							
Reset	0	0	0	0	0	0	0	0

3.4.18 Mouse Data Shift Register (MDSR)

This register is set to 00h on power-up of V_{SB} or software reset. It stores the mouse data shifted in from the mouse during transmission, only when mouse wake-up detection is enabled.

Location: Bank 0, Offset 17h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**Mouse Data**		
Reset	0	0	0	0	0	0	0	0

3.4.19 PS/2 Keyboard Key Data Registers (PS2KEY0 - PS2KEY7)

Eight registers (PS2KEY0-PS2KEY7) store the scan codes for the password or key sequence of the keyboard wake-up feature, as follows:

- PS2KEY0 register stores the scan code for the first key in the password/key sequence.
- PS2KEY1 register stores the scan code for the second key in the password/key sequence.
- PS2KEY2 - PS2KEY7 registers store the scan codes for the third to eighth keys in the password/key sequence.

When one of these registers is set to 00h, it indicates that the value of the corresponding scan code byte is ignored (not compared). These registers are set to 00h on power-up of V_{PP} or software reset.

Location: Bank 0, Offset 18h-1Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Scan Code of Keys 0-7**							
Reset	0	0	0	0	0	0	0	0

3.4.20 CEIR Wake-Up Control Register (IRWCR)

This register is set to 00h on power-up of V_{PP} or software reset.

Location: Bank 1, Offset 13h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**CEIR Protocol Select**		**Select IRRX2 Input**	**Invert IRRXn Input**	**Reserved**	**CEIR Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-6	**Reserved**
5-4	**CEIR Protocol Select** **Bits 5 4 Protocol** 0 0 RC5 (default) 0 1 NEC/RCA 1 X Reserved
3	**Select IRRX2 Input.** Selects the IRRX input. 0: IRRX1 (default) 1: IRRX2
2	**Invert IRRXn Input** 0: Not inverted (default) 1: Inverted
1	**Reserved.**
0	**CEIR Enable** 0: CEIR is disabled. Registers are maintained, but CEIR Event Status bit (of WK0_STS) does not reflect CEIR events. (Unlike the CEIR Event Enable bit of WK0_EN that does not affect the CEIR Event Status bit.) (default) 1: CEIR is enabled

3.4.21 CEIR Wake-Up Address Register (IRWAD)

This register holds the unique address to be compared with the address contained in the incoming CEIR message. If CEIR is enabled (bit 0 of the IRWCR register is 1) and an address match occurs, then bit 5 of the WK0_STS register is set to 1 (see Section 3.4.2).

This register is set to 00h on power-up of V_{PP} or software reset.

Location: Bank 1, Offset 15h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**CEIR Wake-Up Address**							
Reset	0	0	0	0	0	0	0	0

3.4.22 CEIR Wake-Up Address Mask Register (IRWAM)

Each bit in this register determines whether the corresponding bit in the IRWAD register is enabled in the address comparison. Bits 5, 6 and 7 must be set to 1 if the RC-5 protocol is selected.

This register is set to E0h on power-up of V_{PP} or software reset.

Location: Bank 1, Offset 16h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**CEIR Wake-Up Address Mask**							
Reset	1	1	1	0	0	0	0	0

Bit	Description
7-0	**CEIR Wake-Up Address Mask.** If the corresponding bit is 0, the address bit is not masked (enabled for compare). If the corresponding bit is 1, the address bit is masked (ignored during compare).

3.4.23 CEIR Address Shift Register (ADSR)

This register holds the received address to be compared with the address contained in the IRWAD register.

This register is set to 00h on power-up of V_{PP} or software reset.

Location: Bank 1, Offset 17h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**CEIR Address**							
Reset	0	0	0	0	0	0	0	0

3.4.24 CEIR Wake-Up Range 0 Registers

These registers define the low and high limits of time range 0. The values are represented in units of 0.1 msec.

For the RC-5 protocol, the bit cell width must fall within this range for the cell to be considered valid. The nominal cell width is 1.778 msec for a 36 KHz carrier. IRWTR0L and IRWTR0H should be set to 10h and 14h respectively (default).

For the NEC protocol, the time distance between two consecutive CEIR pulses that encodes a bit value of 0 must fall within this range. The nominal distance for a 0 is 1.125 msec for a 38 KHz carrier. IRWTR0L and IRWTR0H should be set to 09h and 0Dh respectively.

IRWTR0L Register

This register is set to 10h on power-up of V_{PP} or software reset.

Location: Bank 1, Offset 18h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**CEIR Pulse Change, Range 0, Low Limit**				
Reset	0	0	0	1	0	0	0	0

IRWTR0H Register

This register is set to 14h on power-up of V_{PP} or software reset.

Location: Bank 1, Offset 19h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**CEIR Pulse Change, Range 0, High Limit**				
Reset	0	0	0	1	0	1	0	0

3.4.25 CEIR Wake-Up Range 1 Registers

These registers define the low and high limits of time range 1. The values are represented in units of 0.1 msec.

For the RC-5 protocol, the pulse width defining a half-bit cell must fall within this range in order for the cell to be considered valid. The nominal pulse width is 0.889 for a 38 KHz carrier. IRWTR1L and IRWTR1H should be set to 07h and 0Bh respectively (default).

For the NEC protocol, the time between two consecutive CEIR pulses that encodes a bit value of 1 must fall within this range. The nominal time for a 1 is 2.25 msec for a 36 KHz carrier. IRWTR1L and IRWTR1H should be set to 14h and 19h respectively.

IRWTR1L Register

This register is set to 07h on power-up of V_{PP} or software reset.

Location: Bank 1, Offset 1Ah

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**CEIR Pulse Change, Range 1, Low Limit**				
Reset	0	0	0	0	0	1	1	1

IRWTR1H Register

This register is set to 0Bh on power-up of V_{PP} or software reset.

Location: Bank 1, Offset 1Bh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**CEIR Pulse Change, Range 1, High Limit**				
Reset	0	0	0	0	1	0	1	1

3.4.26 CEIR Wake-Up Range 2 Registers

These registers define the low and high limits of time range 2. The values are represented in units of 0.1 msec. These registers are not used when the RC-5 protocol is selected.

For the NEC protocol, the header pulse width must fall within this range in order for the header to be considered valid. The nominal value is 9 msec for a 38 KHz carrier. IRWTR2L and IRWTR2H should be set to 50h and 64h respectively (default).

IRWTR2L Register

This register is set to 50h on power-up of V_{pp} or software reset.

Location: Bank 1, Offset 1Ch

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**CEIR Pulse Change, Range 2, Low Limit**							
Reset	0	1	0	1	0	0	0	0

IRWTR2H Register

This register is set to 64h on power-up of V_{pp} or software reset.

Location: Bank 1, Offset 1Dh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**CEIR Pulse Change, Range 2, High Limit**							
Reset	0	1	1	0	0	1	0	0

3.4.27 CEIR Wake-Up Range 3 Registers

These registers define the low and high limits of time range 3. The values are represented in units of 0.1 msec. These registers are not used when the RC-5 protocol is selected.

For the NEC protocol, the post header gap width must fall within this range in order for the gap to be considered valid. The nominal value is 4.5 msec for a 36 KHz carrier. IRWTR3L and IRWTR3H should be set to 28h and 32h respectively (default).

IRWTR3L Register

This register is set to 28h on power-up of V_{pp} or software reset.

Location: Bank1, Offset 1Eh

Type: R/WS

Bit	7	6	5	4	3	2	1	0
Name	**CEIR Pulse Change, Range 3, Low Limit**							
Reset	0	0	1	0	1	0	0	0

IRWTR3H Register

This register is set to 32h on power-up of V_{pp} or software reset.

Location: Bank 1, Offset 1Fh

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**CEIR Pulse Change, Range 3, High Limit**							
Reset	0	0	1	1	0	0	1	0

CEIR Recommended Values

Table 38 lists the recommended time ranges limits for the different protocols and their four applicable ranges. The values are represented in hexadecimal code where the units are of 0.1 msec.

Table 38. Time Range Limits for CEIR Protocols

Range	RC-5		NEC		RCA	
	Low Limit	High Limit	Low Limit	High Limit	Low Limit	High Limit
0	10h	14h	09h	0Dh	0Ch	12h
1	07h	0Bh	14h	19h	16h	1Ch
2	–	–	50h	64h	B4h	DCh
3	–	–	28h	32h	23h	2Dh

3.4.28 Standby General-Purpose I/O (SBGPIO) Register Overview

The SWC can be used to operate up to 8 V_{SB}-powered general-purpose input/output (GPIO), input (GPI) pins, all of which support event detection. These are as follows:

- GPIOE0-5 are GPIO pins.
- GPIE6,7 are GPI pins.

For programming convenience, these pins are associated with an SBGPIO port. Specifically, GPIE0-5 and GPIE6,7 are associated with bits 0 to 7 of SBGPIO port 0, respectively.

Table 39 provides a summary of the SBGPIO pin-to-port assignment and pin types.

Table 39. SBGPIO Pin Types and Associated Port

Pin(s)	Port	Type	Event Detection
GPIOE0-5	0	I/O	Yes
GPIE6,7	0	I	Yes

An SBGPIO port is structured as an 8-bit port, based on eight pins. It features:

- Software capability to manipulate and read pin levels
- Controllable system notification by several means based on the pin level or level transition
- Ability to capture and manipulate events and their associated status
- Back-drive protected pins.

SBGPIO port operation is associated with two sets of registers:

- Pin configuration registers, mapped in the SWC register bank 3. These registers are used to statically set up the logical behavior of each pin. There is one 8-bit register for each SBGPIO pin.
- Two 8-bit runtime registers: SBGPIO Data Out (SBGPDO) and SBGPIO Data In (SBGPDI). These registers are mapped in the SWC device I/O space (determined by the base address registers in the SWC Device Configuration). They are used to manipulate and/or read the pin values. Each runtime register corresponds to the 8-pin port described above (see Table 39).

Each SBGPIO pin is associated with up to six configuration bits and the corresponding bit slice of the two runtime registers, as shown in Figure 10.

The SBGPIO port has basic as well as enhanced functionality. Basic functionality includes the manipulation and reading of the SBGPIO pins, as described in Section . Enhanced functionality includes event detection, as described in *Event Detection*.

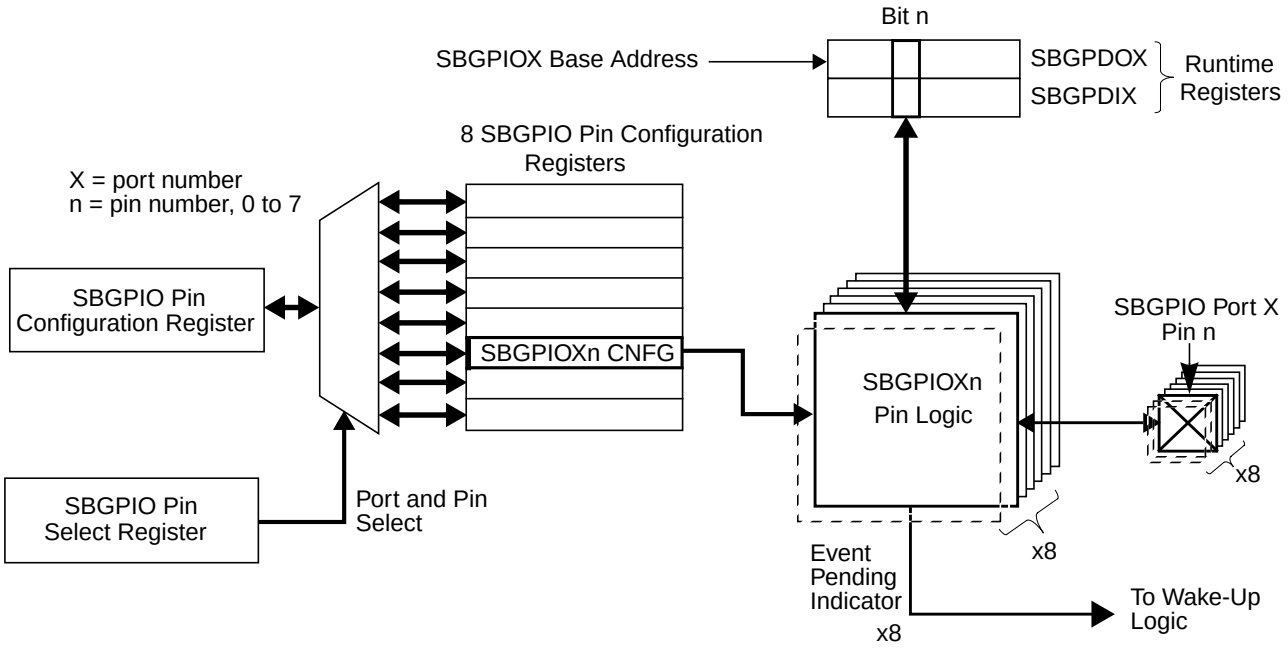


Figure 10. SBGPIO Port Architecture

Basic Functionality

The basic functionality of each SBGPIO pin is based on four configuration bits and a bit slice of runtime registers SBGPDO and SBGPDI. The configuration and operation of a single pin (pin n in port X) is shown in Figure 11.

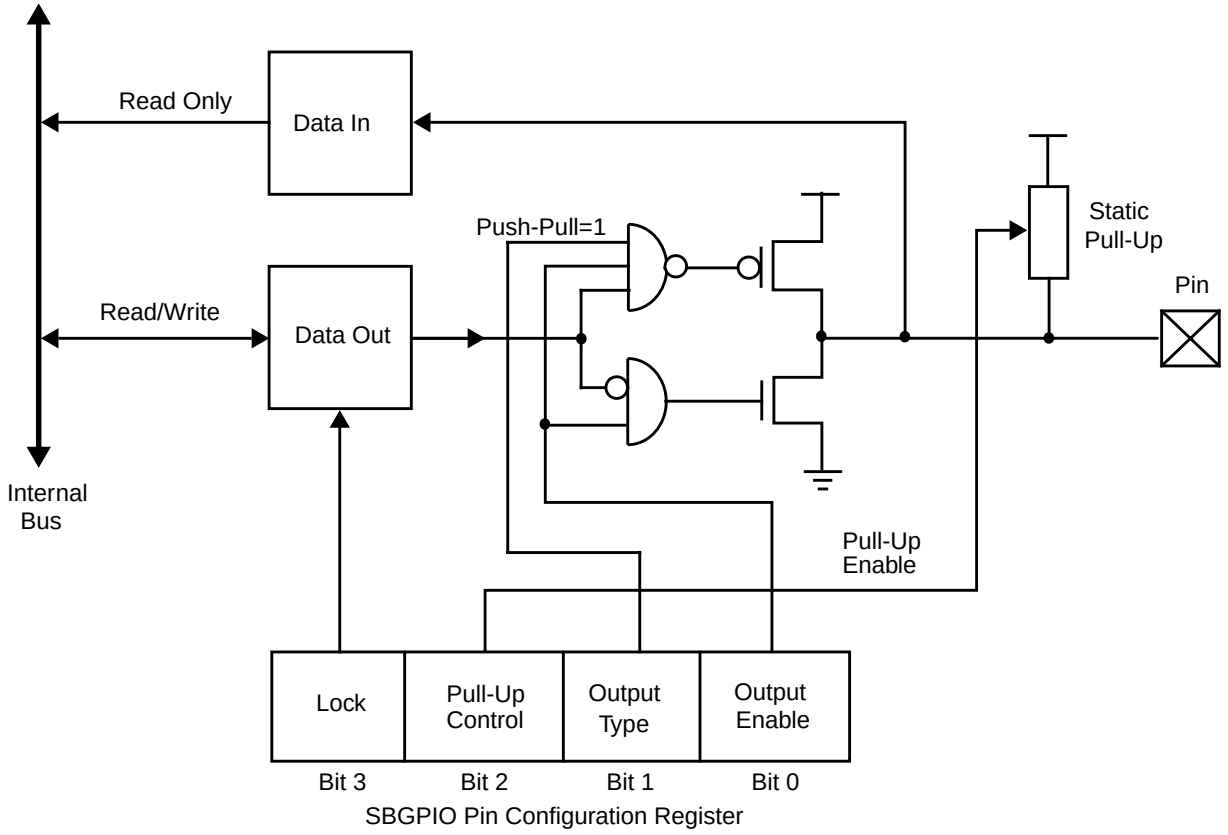


Figure 11. SBGPIO Basic Functionality

Configuration Options

The SBGPIO Pin Configuration register controls the following basic configuration options:

- Pin Direction - Controlled by Output Enable (bit 0)
- Output Type - Push-pull vs. open-drain. It is controlled by Output Type (bit 1) by enabling/disabling the pull-up portion of the output buffer.
- Weak Static Pull-up - May be added to any type of port (input, open-drain or totem pole). It is controlled by Pull-Up Control (bit 2).
- Pin Lock - A GPIO pin may be locked to prevent any changes in the output value and/or the output characteristics. The lock is controlled by Lock (bit 3). It disables writes to the SBGPDO register bits, and to bits 0-3 of the Standby GPIO Pin Configuration register (Including the Lock bit itself). Once locked, it can be released by hardware reset only.

Operation

The value that is written to the SBGPDO register is driven to the pin, if the output is enabled. Reading from the SBGPDO register returns its contents, regardless of the pin value or the port configuration. The SBGPDI register is a read-only register. Reading from the SBGPDI register returns the pin value, regardless of what is driving it (the port itself, configured as an output port, or the external device when the port is configured as an input port). Writing to this register is ignored.

Activation of the SBGPIO port is controlled by the same external, device-specific configuration bit (or a combination of bits) that control the activation of the SWC. When the SWC logical device is inactive, access to both the SBGPDI and SBGPDO registers is disabled. However, there is no change in the port configuration and in the SBGPDO value, and hence there is no effect on the outputs of the pins.

Event Detection

The enhanced SBGPIO port supports input event detection. This functionality is based on three configuration bits. The configuration and operation of the event detection capability is shown in Figure 12. An SWC status register reflects the status of each input event. SWC configuration registers determine the effect of each input event on the various means of system notification available in the SWC.

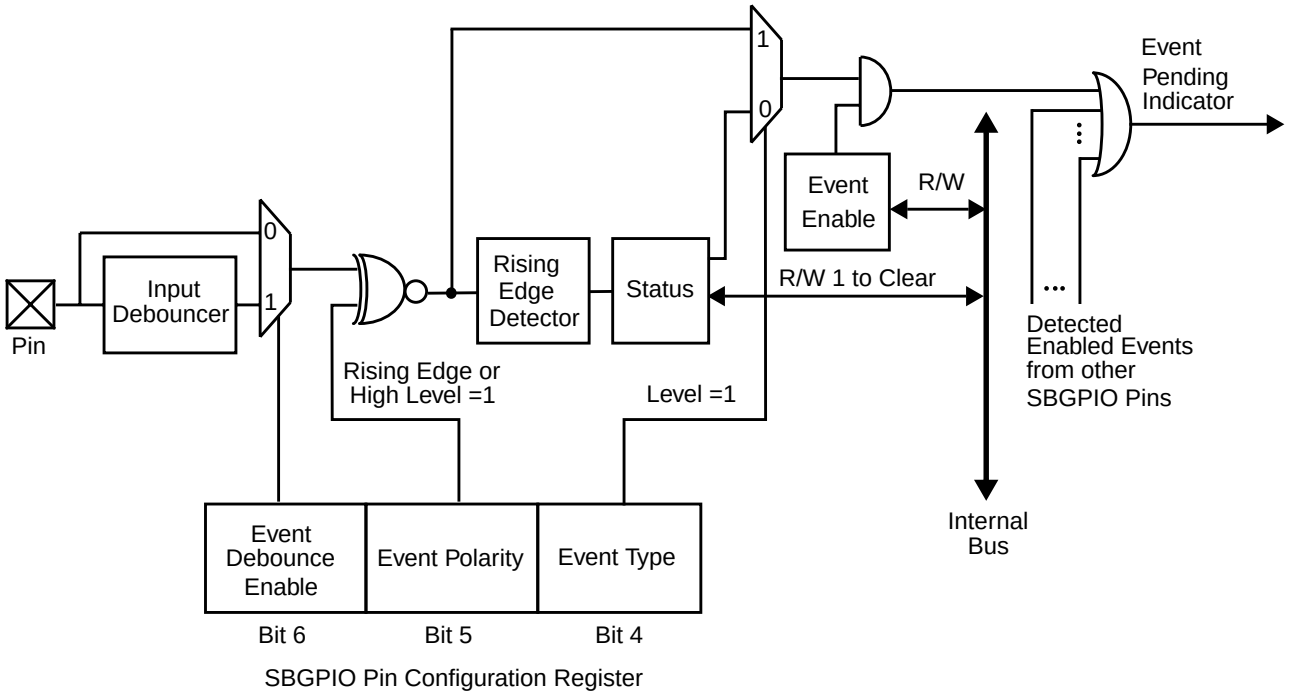


Figure 12. Event Detection

Event Configuration

Each pin in the SBGPIO port is a potential input event source. The event detection can trigger a system notification upon predetermined behavior of the source pin. The SBGPIO Pin Configuration register determines the event detection trigger type for the system notification.

- Event Type and Polarity - Two trigger types of event detection are supported: edge and level. An edge event may be detected upon a source pin transition either from high to low or low to high. A level event may be detected when the source pin is in active level. The trigger type is determined by Event Type (bit 4). The direction of the transition (for edge) or the polarity of the active level (for level) is determined by Event Polarity (bit 5).
- Event Debounce Enable - The input signal can be debounced for about 15 msec before entering the detector. The signal state is transferred to the detector only after a debouncing period during which the signal has no transitions, to ensure that the signal is stable. The debouncer adds 15 msec delay to both assertion and de-assertion of the event pending indicator. Therefore, when working with a level event and system notification by either $\overline{SMI}$ or IRQ, it is recommended to disable the debounce if the delay in the $\overline{SMI}$/IRQ de-assertion is not acceptable. The debounce is controlled by Event Debounce Enable (bit 6 of the SBGPIO Pin Configuration register).

3.4.29 Standby GPIO Pin Select Register (SBGPSEL)

This register selects the GPIOE/GPIE pin (port number and pin number) to be configured (the register accessed by the Standby GPIO Pin Configuration register). This register is reset to 00h on V_{PP} power-up or software reset.

When port 0 is selected, bits 2-0 select between pins GPIE7,6 and GPIOE5-0.

Location: Bank 3, Offset 13h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**Port Select**	**Reserved**	**Pin Select**		
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-5	**Reserved**
4	**Port Select.** This bit selects the GPIO port to be configured. 0: Port 0 (default) 1: Reserved
3	**Reserved**
2-0	**Pin Select**. These bits select the GPIO pin to be configured in the selected port. 000, 001, ... 111:The binary value of the pin number, 0, 1, ... 7 respectively (default=0)

3.4.30 Standby GPIO Pin Configuration Register (SBGPCFG)

This is a group of eight identical configuration registers, each of which is associated with one GPIOE/GPIE pin. The entire set is mapped to the same address. The mapping scheme is based on the Standby GPIO Pin Select (SBGPSEL) register that functions as an index register, and the specific Standby GPIO Pin Configuration register that reflects the configuration of the currently selected pin.

Bits 0-3 are applicable only for pins GPIOE0-5. Bits 4-6 are applicable for all GPIOE/GPIE pins.

Location: Bank 3, Offset 14h

Type: R/W (bit 3 is set only)

For GPIOE and GPIE:

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**Event Debounce Enable**	**Event Polarity**	**Event Type**	**Lock**	**Pull-Up Control**	**Output Type**	**Output Enable**
Reset	0	1	0	0	0	1	0	0

Bit	Description
7	**Reserved**
6	**Event Debounce Enable** 0: Disabled 1: Enabled (default)
5	**Event Polarity.** This bit defines the polarity of the signal that causes a detection of an event from the corresponding GPIO pin. 0: Falling edge or low level input (default) 1: Rising edge or high level input
4	**Event Type.** This bit defines the signal type that causes a detection of an event from the corresponding GPIO pin. 0: Edge input (default) 1: Level input
3	**Lock**. This bit locks bits 2-0 of this register. These bits are associated with the GPIO pin currently selected by the SBGPSEL register. Once this bit is set to 1 by software, it can only be cleared to 0 by V_{SB} power-up reset. 0: No effect (default at V_{SB} power-up reset) 1: Direction, output type, pull-up and output value locked
2	**Pull-Up Control.** This bit is used to enable/disable the internal pull-up capability of the corresponding GPIO pin. It supports open-drain output signals with internal pull-ups and TTL input signals. 0: Disabled 1: Enabled (default)
1	**Output Type.** This bit controls the output buffer type (open-drain or totem pole) of the corresponding GPIO pin. 0: Open-drain (default) 1: Push-pull
0	**Output Enable.** For GPIOE and GPIE, this bit indicates the GPIO pin output state. It has no effect on input. 0: TRI-STATE (default for GPIOE/GPIE) 1: Output enabled

3.4.31 Standby GPIOE/GPIE Data Out Register 0 (SB_GPDO0)

This register is set to 3Fh on V_{PP} power-up or software reset, only when the Lock bit of the SBGPCFG register is set to 0. It determines the value to be driven on the GPIOE pins when configured as outputs.

Location: Offset 08h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**Data Out**					
Reset	0	0	1	1	1	1	1	1

Bit	Description
7-6	**Reserved**
5	**Data Out.** Bits 5-0 correspond to pins GPIOE5-0 respectively. The value of each bit determines the value driven on the corresponding GPIOE pin when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the corresponding GPIOE Configuration Lock bit. Reading the bit returns its value, regardless of the pin value and configuration. 0: Corresponding pin level low when output enabled 1: Corresponding pin level high (according to buffer type and static pull-up selection) when output enabled
4	
3	
2	
1	
0	

3.4.32 Standby GPIOE/GPIE Data In Register 0 (SB_GPDI0)

This register reflects the values of the GPIE7-6 and GPIOE5-0 pins. Write to this register is ignored.

Location: Offset 09h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Data In**							
Reset	X	X	X	X	X	X	X	X

Bit	Description
7	**Data In.** Bits 7-0 correspond to pins GPIE7-6 and GPIOE5-0 respectively. Reading each bit returns the value of the corresponding GPIE/GPIOE pin regardless of the pin configuration and the SB0_GPDO register value. 0: Corresponding pin level low 1: Corresponding pin level high
6	
5	
4	
3	
2	
1	
0	

3.5 SWC REGISTER BITMAP

Table 40. Banks 0 and 1 - The Common Register Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	WK_STS0	Module IRQ Event Status	Software Event Status	GPIO Event Status	CEIR Event Status	Mouse Event Status	KBD Event Status	$\overline{RI2}$ Event Status	$\overline{RI1}$ Event Status
01h	WK_STS1	GPIE7 Event Status	GPIE6 Event Status	GPIE5 Event Status	GPIE4/$\overline{RING}$ Event Status	GPIE3 Event Status	GPIE2 Event Status	GPIE1 Event Status	GPIE0 Event Status
02h	WK_EN0	Module IRQ Event Enable	Software Event Enable	GPIO Event Enable	CEIR Event Enable	Mouse Event Enable	KBD Event Enable	$\overline{RI2}$ Event Enable	$\overline{RI1}$ Event Enable
03h	WK_EN1	GPIE7 Event Enable	GPIE6 Event Enable	GPIE5 Event Enable	GPIE4/$\overline{RING}$ Event Enable	GPIE3 Event Enable	GPIE2 Event Enable	GPIE1 Event Enable	GPIE0 Event Enable
04h	WK_CFG	Reserved					Swap KBC Inputs	Configuration Bank Select	
05h-07h	Reserved								
08h	SB_GPDO0	Reserved		Data Out					
09h	SB_GPDI0	Data In							
0Ah-12h	Reserved								

Table 41. Bank 0 - PS/2 Keyboard/Mouse Wake-Up Configuration and Control Registers Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
13h	PS2CTL	Disable Parity	Mouse Wake-Up Configuration			Keyboard Wake-Up Configuration			
16h	KDSR	Keyboard Data							
17h	MDSR	Reserved					Mouse Data		
18h-1Fh	PS2KEY0-PS2KEY7	Scan Code of Keys 0-7							

Table 42. Bank 1 - CEIR Wake-Up Configuration and Control Registers Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
13h	IRWCR	Reserved		CEIR Protocol Select		Select IRRX2 Input	Invert IRRXn Input	Reserved	CEIR Enable
14h	Reserved								
15h	IRWAD	CEIR Wake-Up Address							
16h	IRWAM	CEIR Wake-Up Address Mask							
17h	ADSR	CEIR Address							

18h	IRWTR0L	Reserved	CEIR Pulse Change, Range 0, Low Limit
19h	IRWTR0H	Reserved	CEIR Pulse Change, Range 0, High Limit
1Ah	IRWTR1L	Reserved	CEIR Pulse Change, Range 1, Low Limit
1Bh	IRWTR1H	Reserved	CEIR Pulse Change, Range 1, High Limit
1Ch	IRWTR2L	CEIR Pulse Change, Range 2, Low Limit	
1Dh	IRWTR2H	CEIR Pulse Change, Range 2, High Limit	
1Eh	IRWTR3L	CEIR Pulse Change, Range 3, Low Limit	
1Fh	IRWTR3H	CEIR Pulse Change, Range 3, High Limit	

Table 43. Bank 2 - Event Routing Control Registers Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
13h	WK_SMIEN0	Reserved	Software Event to SMI Enable	Reserved	CEIR Event to SMI Enable	Mouse Event to SMI Enable	KBD Event to SMI Enable	$\overline{RI2}$ Event to SMI Enable	$\overline{RI1}$ Event to SMI Enable
14h	WK_SMIEN1	GPIE7 Event to SMI Enable	GPIE6 Event to SMI Enable	GPIE5 Event to SMI Enable	GPIE4/ $\overline{RING}$ Event to SMI Enable	GPIE3 Event to SMI Enable	GPIE2 Event to SMI Enable	GPIE1 Event to SMI Enable	GPIE0 Event to SMI Enable
15h	WK_IRQEN0	Reserved	Software Event to IRQ Enable	Reserved	CEIR Event to IRQ Enable	Mouse Event to IRQ Enable	KBD Event to IRQ Enable	$\overline{RI2}$ Event to IRQ Enable	$\overline{RI1}$ Event to IRQ Enable
16h	WK_IRQEN1	GPIE7 Event to IRQ Enable	GPIE6 Event to IRQ Enable	GPIE5 Event to IRQ Enable	GPIE4/ $\overline{RING}$ Event to IRQ Enable	GPIE3 Event to IRQ Enable	GPIE2 Event to IRQ Enable	GPIE1 Event to IRQ Enable	GPIE0 Event to IRQ Enable
17h	WK_X1EN0	Reserved			CEIR Event Ex. 1 Enable	Mouse Event Ex. 1 Enable	KBD Event Ex. 1 Enable	$\overline{RI2}$ Event Ex. 1 Enable	$\overline{RI1}$ Event Ex. 1 Enable
18h	WK_X1EN1	GPIE7 Event Ex. 1 Enable	GPIE6 Event Ex. 1 Enable	GPIE5 Event Ex. 1 Enable	GPIE4/ $\overline{RING}$ Event Ex. 1 Enable	GPIE3 Event Ex. 1 Enable	GPIE2 Event Ex. 1 Enable	GPIE1 Event Ex. 1 Enable	GPIE0 Event Ex. 1 Enable
19h	WK_X2EN0	Reserved			CEIR Event Ex. 2 Enable	Mouse Event Ex. 2 Enable	KBD Event Ex. 2 Enable	$\overline{RI2}$ Event Ex. 2 Enable	$\overline{RI1}$ Event Ex. 2 Enable
1Ah	WK_X2EN1	GPIE7 Event Ex. 2 Enable	GPIE6 Event Ex. 2 Enable	GPIE5 Event Ex. 2 Enable	GPIE4/ $\overline{RING}$ Event Ex. 2 Enable	GPIE3 Event Ex. 2 Enable	GPIE2 Event Ex. 2 Enable	GPIE1 Event Ex. 2 Enable	GPIE0 Event Ex. 2 Enable
1Bh-1Fh	Reserved								

Bank 3 - Standby General-Purpose I/O Configuration Registers Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
13h	SBGPSEL	Reserved			Port Select	Reserved	Pin Select		
14h	SBGPCFG	Reserved	Event Debounce Enable	Event Polarity	Event Type	Lock	Pull-Up Control	Output Type	Output Enable
15h-1Fh	Reserved								

4.0 Fan Speed Control

4.1 OVERVIEW

This chapter describes a generic Fan Speed Control module. For the implementation used in this device, see the *Device Architecture and Configuration* chapter.

The Fan Speed Control is a programmable Pulse Width Modulation (PWM) generator. The PWM generator output is used to control the fan's power voltage, which is correlated to the fan's speed. Converting a 0 to 100% duty cycle PWM signal to an analog voltage range is achieved by an external circuit, as shown in Figure 13. Some newer fans accept direct PWM input without any external circuitry.

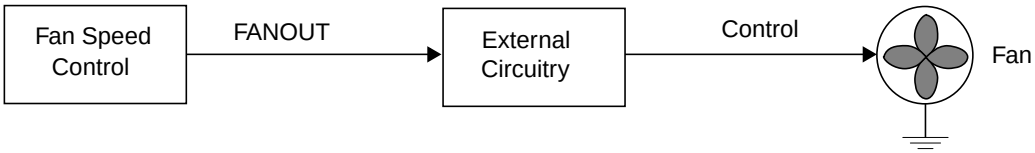


Figure 13. Fan Speed Control - System Configuration

4.2 FUNCTIONAL DESCRIPTION

The PWM generator operation is based on a PWM counter and two registers: the Fan Speed Control Pre-Scale register (FCPSR), used to determine the overall cycle time (or the frequency) of the FANOUT output, and the Fan Speed Control Duty Cycle register (FCDCR), used to determine the duty cycle of the FANOUT between 0 to 100%.

The PWM counter is an 8-bit, free-running counter that runs continuously in a cyclic manner, i.e its cycle equals 256 clock periods. The PWM output is high as long as the count is lower than the FCDCR value, and flips to low as the counter exceeds that value. The duty cycle (expressed as a percentage) is therefore (FCDCR/256)*100. In particular, the PWM output is continuously low when FCDCR=0 and continuously high when FCDCR=FFh. The FANOUT output may be inverted by an external configuration bit, in which case the FANOUT duty cycle is ([256-FCDCR]/256)*100.

The PWM counter clock is generated by dividing the input clock, either 24 MHz or 200 KHz, using a clock divider. The division factor, which must be between 1 and 124, is defined as Pre-Scale Value+1, where Pre-Scale is the binary value stored in bits 6 to 0 of the FCPSR register. The resulting PWM output frequency is therefore:

(24 MHz or 200 kHz/([Pre-Scale Value+1]*****256).

The default selection of 24 MHz input clock allows a programmable FANOUT frequency in the range of 756 Hz to 93.75 KHz. For lower frequencies, selecting the 200 KHz input clock allows a frequency range of 6 Hz to 781 Hz. See Figure 14.

The FANOUT frequency must be pre-selected according to the fan type's specific requirements prior to enabling the Fan Speed Control. The only run-time change that is required to dynamically control the fan speed is the value of the FCDCR register.

Warning! The contents of the FCPSR register must not be changed when the Fan Speed Control is enabled.

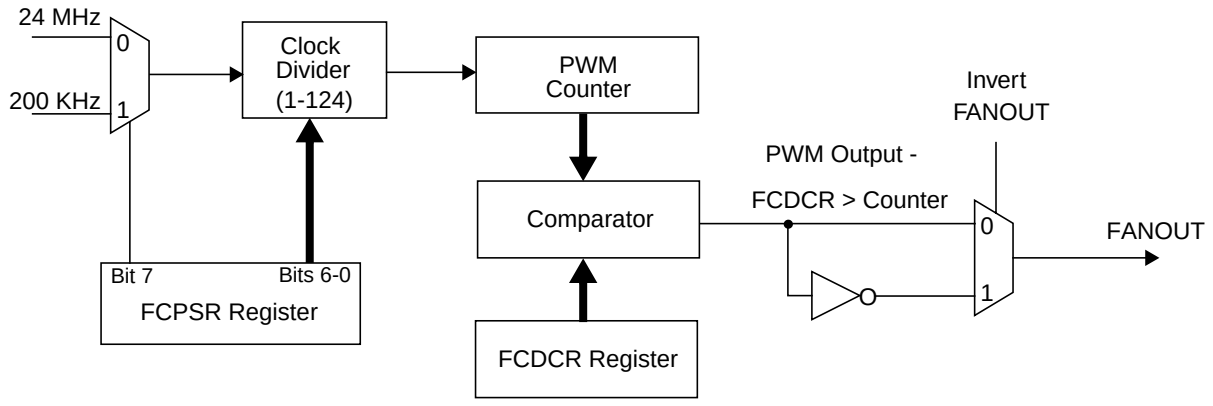


Figure 14. PWM Generator (FANOUT)

4.3 FAN SPEED CONTROL REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

4.3.1 Fan Speed Control Register Map

Offset	Mnemonic	Register Name	Type	Section
Device specific[Note 1.]	FCPSR	Fan Speed Control Pre-Scale	R/W	4.3.2
Device specific[Note 1.]	FCDCR	Fan Speed Control Duty Cycle	R/W	4.3.3

Note 1. The location of this register is defined in the *Device Architecture and Configuration* chapter.

4.3.2 Fan Speed Control Pre-Scale Register (FCPSR)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Clock Select**	**Pre-Scale Value**						
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Clock Select.** This bit selects the input clock for the clock divider. 0: 24 MHz 1: 200 KHz
6-0	**Pre-Scale Value.** The clock divider for the input clock (24 MHz or 200 KHz) is Pre-Scale Value + 1. Writing 0000000b to these bits transfers the input clock directly to the counter. The maximum clock divider is 124 (7Bh +1). These bits must not be programmed with the values 7Ch, 7Dh, 7Eh and 7Fh as this may produce unpredictable results. The contents of this register should not be changed when the corresponding Fan Speed Control Enable bit of the Fan Speed Control Configuration register is 1 (see *Device Architecture and Configuration* chapter) as this may produce unpredictable results.

4.3.3 Fan Speed Control Duty Cycle Register (FCDCR)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Duty Cycle Value**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7-0	**Duty Cycle.** The binary value of this 8-bit field determines the number of clock cycles, out of a 256-cycle period, during which the PWM output is high (while FANOUT is either equal to or the inverse of the PWM output, depending on the Inverse FANOUT configuration bit). 00h: PWM output is continuously low 01h - FEh: PWM output is high for [Duty Cycle Value] clock cycles and low for [256-Duty Cycle Value] clock cycles FFh: PWM output is continuously high

4.4 FAN SPEED CONTROL BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
Device specific Note 1.	FCPSR	Clock Select	Pre-Scale Value						
Device specific Note 1.	FCDCR	Duty Cycle Value							

Note 1. The location of this register is defined in the *Device Architecture and Configuration* chapter.

5.0 Fan Speed Monitor

5.1 OVERVIEW

This chapter describes a generic Fan Speed Monitor module. For the implementation used in this device, see the *Device Architecture and Configuration* chapter.

The Fan Speed Monitor determines the fan's speed by measuring the time between consecutive tachometer pulses, emitted by the fan once or twice per revolution (depending on the fan type). It may provide the system with a current speed reading and/or alert the system, by interrupt, whenever the speed drops below a programmable threshold. The Fan Speed Monitor indicates whether the speed is just below the threshold or inefficiently low to consider the fan stopped.

Figure 15 shows the basic system configuration of the Fan Speed Monitor.

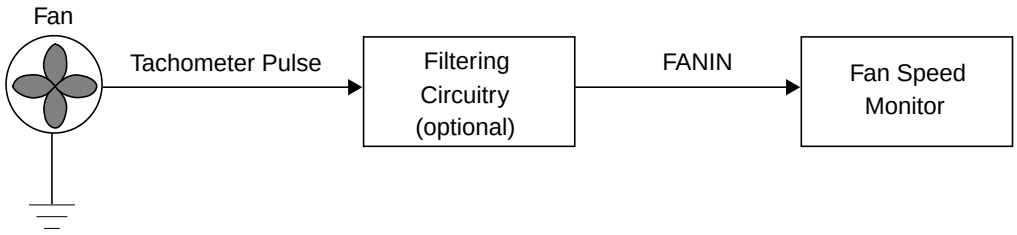


Figure 15. Fan Speed Monitor - System Configuration

5.2 FUNCTIONAL DESCRIPTION

The fan emits a tachometer pulse every half or full revolution (depending on the fan type). These pulses are fed into the Fan Speed Monitor through the FANIN input pin. Measuring the time between these pulses is the basis for speed monitoring.

NCBTP is defined as the Number of Clock-cycles Between consecutive Tachometer Pulses. For a known clock rate (f Hz) and number of pulses per revolution (n=1,2), the Fan Speed is calculated according to the following relationship:

$$\text{Fan Speed (in RPM)} = 60 \bullet \frac{f}{NCBTP \bullet n}$$

The Fan Speed Monitor consists of an 8-bit counter to measure the NCBTP and three 8-bit registers: Fan Monitor Speed register (FMSPR), Fan Monitor Threshold register (FMTHR) and Fan Monitor Control and Status register (FMCSR). Figure 16 is a general block diagram of the Fan Speed Monitor.

The Up Counter and the FMSPR register are cleared to 0 while the Fan Speed Monitor is disabled (and in particular upon system reset).

When the Fan Speed Monitor is enabled and there was no counter overflow, the counter runs (up-counts), clocked by the selected clock rate. Starting from the second FANIN pulse (after activation) and upon every rising edge of FANIN when the Over Threshold bit is 0, the FMSPR register is loaded with the contents of the counter, the counter is cleared to 0, and the Speed Ready bit is set to 1.

Upon reading FMSPR, the Speed Ready bit of the FMCSR is cleared to 0.

The above operation continually repeats itself, providing the host with the current speed reading, as long as the FMSPR register value is lower than the threshold.

Once the loaded FMSPR register value exceeds the threshold, the Over Threshold bit is set to 1. Interrupt is asserted if enabled. The FMSPR register is not loaded with any new values when the Over Threshold bit is set. A new value is loaded only after clearing the Over Threshold bit (by writing 1) and reading the FMSPR register. This guarantees that the same NCBTP value that generated the interrupt remains available for the interrupt handler.

If the counter passes FFh, the Overflow bit is set to 1, the FMSPR register is cleared, and the interrupt is asserted, if enabled. The Overflow bit is cleared to 0 when it is written with 1, after which speed measurement resumes.

The input buffer of the FANIN signal is a hysteresis buffer (Schmitt trigger). This signal passes through a digital filter when the Filter Disable bit (bit 4 of the FMCSR register) is 0**.** The digital filter uses a 32 KHz clock to filter out any pulses shorter than 750 µsec. This filter can be by-passed when setting bit 4 of the FMCSR register to 1.

.

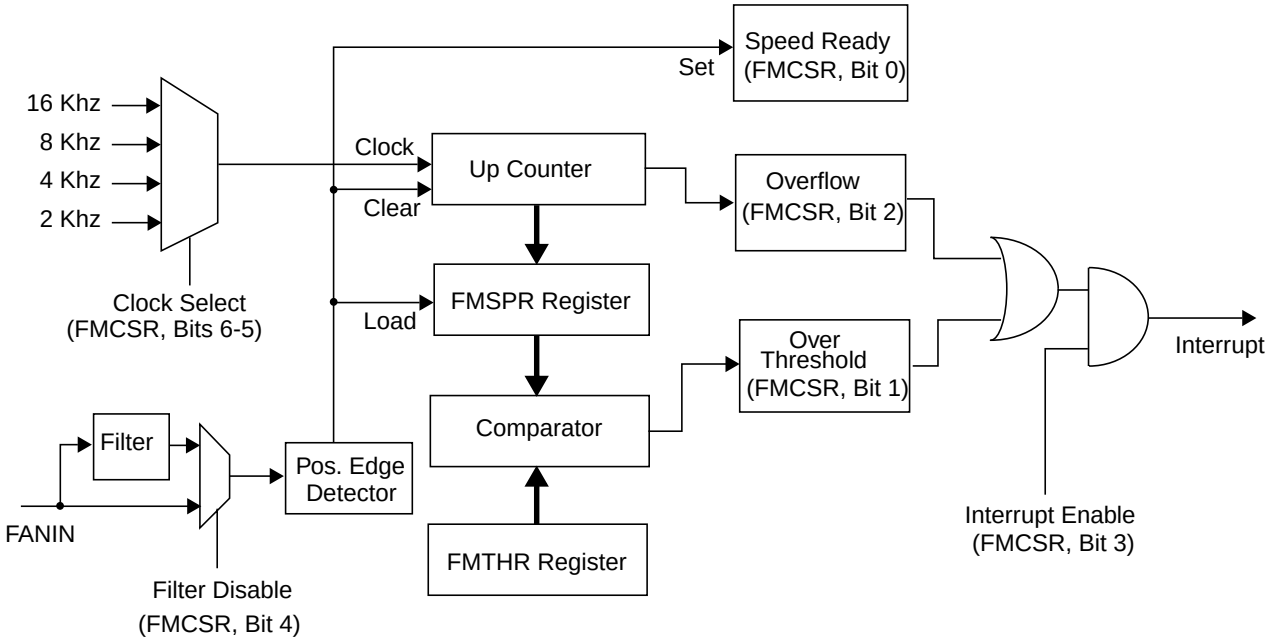


Figure 16. Fan Speed Monitor

5.3 FAN SPEED MONITOR REGISTERS

The FMSPR register is used to hold the current speed reading (which is represented by the latest NCBTP and refreshed upon every FANIN pulse).

The FMTHR register holds the maximum allowed NCBTP value (representing the slowest speed at which the fan is allowed to operate) without causing system alert.

Additional control and status bits are available through the FMCSR register. These include:

- Over Threshold. A status bit that indicates that the NCBTP has exceeded the threshold (the speed has dropped below the allowed minimum).
- Overflow. A status bit that indicates that the NCBTP is higher than FFh. With a proper input clock selection, this means that the speed is inefficiently low and is considered stopped.
- Speed Ready. A status bit that indicates that new, valid data has been loaded into the FMSPR register.
- Clock Select. A 2-bit control field that selects the counter clock rate as either 2 KHz, 4 KHz, 8 KHz or 16 KHz.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

5.3.1 Fan Speed Monitor Register Map

Offset	Mnemonic	Register Name	Type	Section
Device specific[Note 1.]	FMTHR	Fan Monitor Threshold	R/W	5.3.2
Device specific[Note 1.]	FMSPR	Fan Monitor Speed	RO	5.3.3
Device specific[Note 1.]	FMCSR	Fan Monitor Control and Status	Varies per bit	5.3.4

Note 1. The location of this register is defined in the *Device Architecture and Configuration* chapter.

5.3.2 Fan Monitor Threshold Register (FMTHR)

This 8-bit register contains the programmable threshold for the fan. This threshold is the maximum number of clock cycles between consecutive tachometer pulses (frequencies of 16, 8, 4 or 2 KHz). It represents the minimum fan speed permitted in the system. If the period between consecutive tachometer pulses is greater than the threshold, an interrupt (if enabled) is issued. After reset, the value of FMTHR is FFh.

This register should not be changed when the corresponding Fan Monitor Enable bit is set to 1 (enabled), since this may cause unpredictable results.

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Threshold Value**							
Reset	1	1	1	1	1	1	1	1

5.3.3 Fan Monitor Speed Register (FMSPR)

This read-only 8-bit register holds the speed reading, represented by number of clock cycles between consecutive tachometer pulses. For details, refer to Section 5.2. When the Speed Ready bit of the FMCSR register is 1, FMSPR holds valid data that has not yet been read.

It is cleared to 00h upon any of the following conditions:

- System reset
- Fan Monitor Enable bit is set to 0
- Overflow bit is set to 1.

Location: Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Fan Speed Reading**							
Reset	0	0	0	0	0	0	0	0

5.3.4 Fan Monitor Control and Status Register (FMCSR)

Location: Device specific

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**Clock Select**		**Filter Disable**	**Interrupt Enable**	**Overflow**	**Over Threshold**	**Speed Ready**
Reset	0	0	1	0	0	0	0	0

Bit	Type	Description
7		**Reserved**
6-5	R/W	**Clock Select.** Selects the clock source provided to the counter. These bits must not be changed when the corresponding Fan Monitor Enable bit is 1 (enabled). 00: 16 KHz 01: 8 KHz (default) 10: 4 KHz 11: 2 KHz
4	R/W	**Filter Disable**. When this bit is set to 1, the digital filter is disabled. When it is cleared, the filter is enabled. This bit should not be changed when the corresponding Fan Monitor Enable bit is 1 (enabled) to avoid unpredictable results. 0: Digital filter enabled (default) 1: Digital filter disabled
3	R/W	**Interrupt Enable**. This bit controls the assertion of overflow interrupt and Over Threshold interrupt. 0: Interrupt disabled (default) 1: Interrupt enabled. Interrupt is asserted when an Over Threshold bit, Overflow bit or both are set to 1.
2	R/W1C	**Overflow**. Indicates that the counter has passed FFh, and the fan speed is inefficiently slow; i.e., slower than 60 * f/(256 * n). Writing 1 to this bit clears it to 0. 0: No overflow occurred since the last time this bit was cleared (by reset or by writing 1) 1: Counter passed FFh
1	R/W1C	**Over Threshold**. Indicates that the value loaded into the FMSPR register upon detection of the rising edge of the FANIN pulse exceeded the threshold value. 0: FMSPR register value did not exceed the threshold since the last time this bit was cleared (by reset or by writing 1) 1: FMSPR register value exceeded the threshold
0	RO	**Speed Ready**. This bit indicates that the speed register holds new (not yet read) and valid data. It is set to 1 on each rising edge of the FANIN input (starting from the second one) if the Over Threshold bit is 0. It is cleared to 0 whenever the speed register is read, or when the Overflow bit is set. 0: No new valid data in the FMSPR register (data is either invalid or has already been read) 1: FMSPR register loaded with new and valid data

5.4 FAN SPEED MONITOR BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
Device specific Note 1.	FMTHR	Threshold Value							
Device specific Note 1.	FMSPR	Fan Speed Reading							
Device specific Note 1.	FMCSR	Reserved	Clock Select		Filter Disable	Interrupt Enable	Overflow	Over Threshold	Speed Ready

Note 1. The location of this register is defined in the *Device Architecture and Configuration* chapter.

6.0 General-Purpose Input/Output (GPIO) Port

This chapter describes one 8-bit port. A device may include a combination of several ports with different implementations. For the device specific implementation, see the *Device Architecture and Configuration* chapter.

6.1 OVERVIEW

The GPIO port is an 8-bit port, which is based on eight pins. It features:

- Software capability to manipulate and read pin levels
- Controllable system notification by several means based on the pin level or level transition
- Ability to capture and manipulate events and their associated status
- Back-drive protected pins.

GPIO port operation is associated with two sets of registers:

- Pin Configuration registers, mapped in the Device Configuration space. These registers are used to statically set up the logical behavior of each pin. There are two 8-bit register for each GPIO pin.
- Four 8-bit runtime registers: GPIO Data Out (GPDO), GPIO Data In (GPDI), GPIO Event Enable (GPEVEN) and GPIO Event Status (GPEVST). These registers are mapped in the GPIO device IO space (which is determined by the base address registers in the GPIO Device Configuration). They are used to manipulate and/or read the pin values, and to control and handle system notification. Each runtime register corresponds to the 8-pin port, such that bit n in each one of the four registers is associated with GPIOXn pin, where X is the port number.

Each GPIO pin is associated with ten configuration bits and the corresponding bit slice of the four runtime registers, as shown in Figure 17.

The functionality of the GPIO port is divided into basic functionality that includes the manipulation and reading of the GPIO pins, and enhanced functionality. The basic functionality is described in Section 6.2. The enhanced functionality which includes the event detection and system notification is described in Section 6.3.

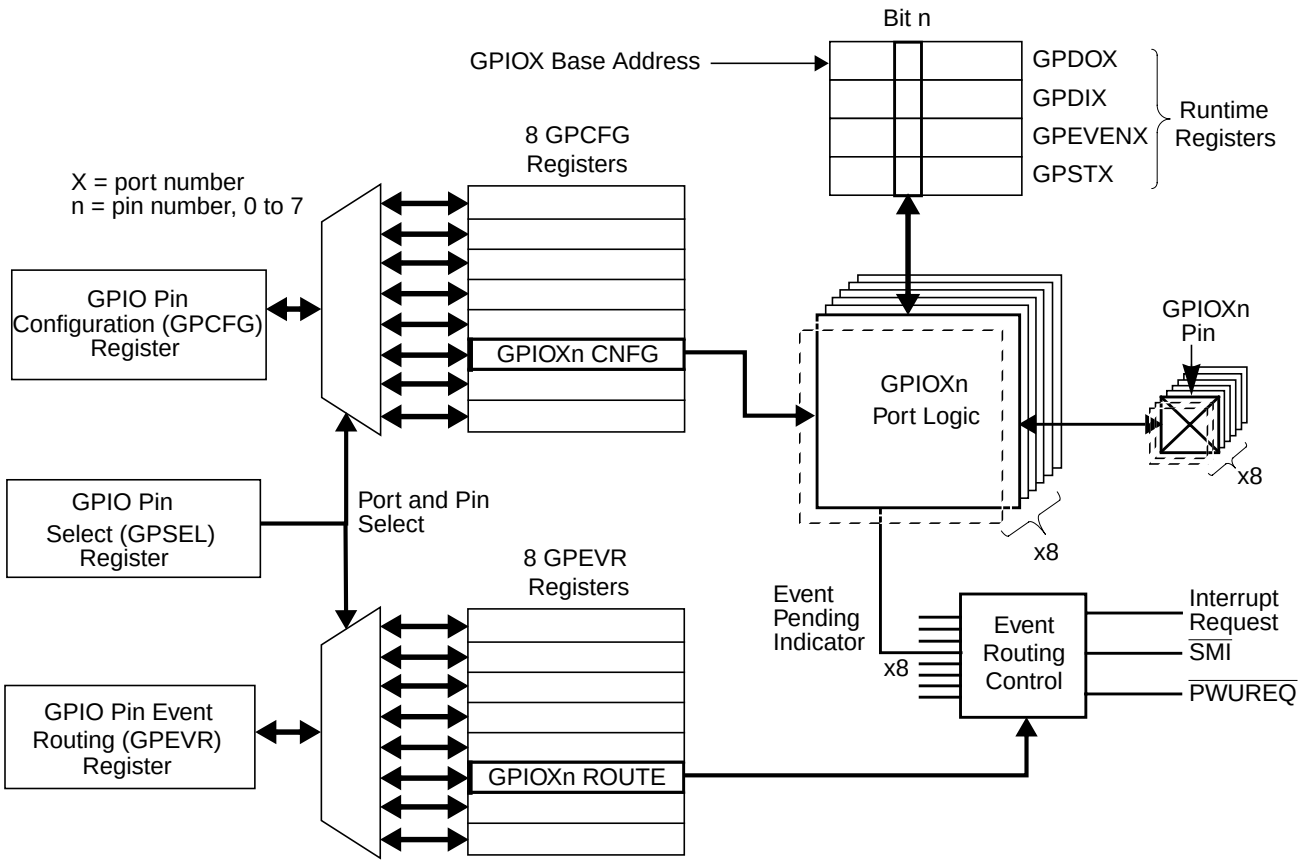


Figure 17. GPIO Port Architecture

6.2 BASIC FUNCTIONALITY

The basic functionality of each GPIO pin is based on four configuration bits and a bit slice of runtime registers GPDO and GPDI. The configuration and operation of a single pin GPIOXn (pin n in port X) is shown in Figure 18.

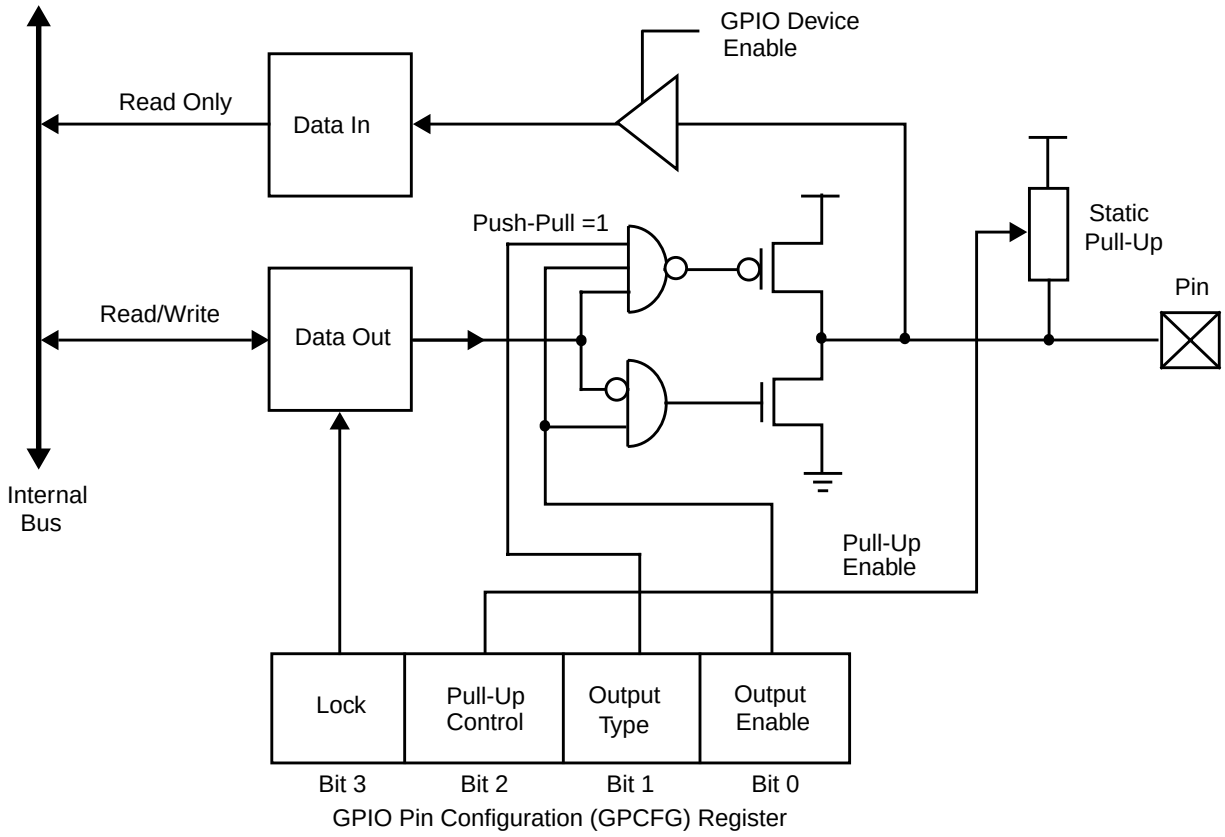


Figure 18. GPIO Basic Functionality

6.2.1 Configuration Options

The GPCFG register controls the following basic configuration options:

- Port Direction - Controlled by the Output Enable bit (bit 0)
- Output Type - Push-pull vs. open-drain. It is controlled by Output Buffer Type (bit 1) by enabling/disabling the pull-up portion of the output buffer.
- Weak Static Pull-up - May be added to any type of port (input, open-drain or push-pull). It is controlled by Pull-Up Control (bit 2).
- Pin Lock - GPIO pin may be locked to prevent any changes in the output value and/or the output characteristics. The lock is controlled by Lock (bit 3). It disables writes to the GPDO register bits, and to bits 0-3 of the GPCFG register (Including the Lock bit itself). Once locked, it can be released by hardware reset only.

6.2.2 Operation

The value that is written to the GPDO register is driven to the pin, if the output is enabled. Reading from the GPDO register returns its contents, regardless of the pin value or the port configuration. The GPDI register is a read-only register. Reading from the GPDI register returns the pin value, regardless of what is driving it (the port itself, configured as an output port, or the external device when the port is configured as an input port). Writing to this register is ignored.

Activation of the GPIO port is controlled by external device specific configuration bit (or a combination of bits). When the port is inactive, access to GPDI and GPDO registers is disabled, and the inputs are blocked. However, there is no change in the port configuration and in the GPDO value, and hence there is no effect on the outputs of the pins.

6.3 EVENT HANDLING AND SYSTEM NOTIFICATION

The enhanced GPIO port supports system notification based on event detection. This functionality is based on six configuration bits and a bit slice of runtime registers GPEVEN and GPST. The configuration and operation of the event detection capability is shown in Figure 19. The operation of system notification is illustrated in Figure 20.

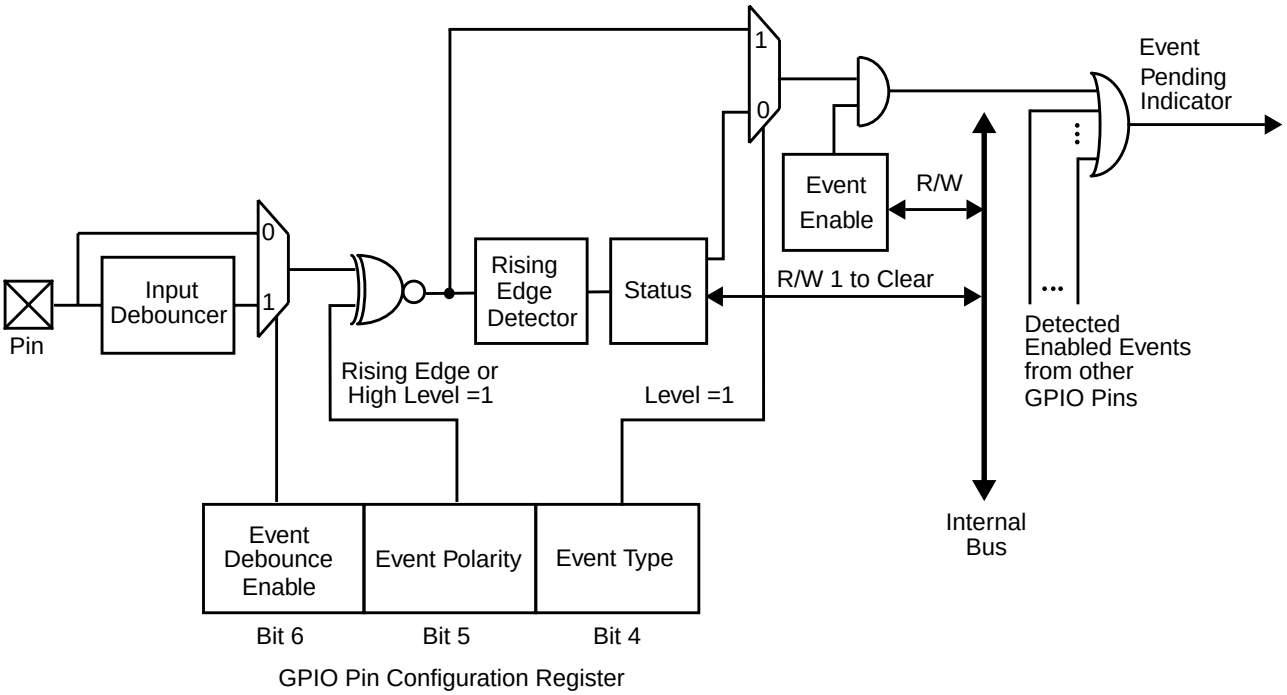


Figure 19. Event Detection

6.3.1 Event Configuration

Each pin in the GPIO port is a potential input event source. The event detection can trigger a system notification upon predetermined behavior of the source pin. The GPCFG register determines the event detection trigger type for the system notification.

Event Type and Polarity

Two trigger types of event detection are supported: edge and level. An edge event may be detected upon a source pin transition either from high to low or low to high. A level event may be detected when the source pin is in active level. The trigger type is determined by Event Type (bit 4 of the GPCFG register). The direction of the transition (for edge) or the polarity of the active level (for level) is determined by Event Polarity (bit 5 of the GPCFG register).

Event Debounce Enable

The input signal can be debounced for about 15 msec before entering the detector. The signal state is transferred to the detector only after a debouncing period during which the signal has no transitions, to ensure that the signal is stable. The debouncer adds 15 msec delay to both assertion and de-assertion of the event pending indicator. Therefore, when working with a level event and system notification by either $\overline{\text{SMI}}$ or IRQ, it is recommended to disable the debounce if the delay in the $\overline{\text{SMI}}$/IRQ de-assertion is not acceptable. The debounce is controlled by Event Debounce Enable (bit 6 of the GPCFG register).

6.3.2 System Notification

System notification on GPIO-triggered events is by means of assertion of one or more of the following output pins:

- Interrupt Request (via the device's Bus Interface)
- System Management Interrupt ($\overline{\text{SMI}}$, via the device's Bus Interface)
- Power-Up Request ($\overline{\text{PWUREQ}}$, via the System Wake-Up Control)

The system notification for each GPIO pin is controlled by the corresponding bits in the GPEVEN and GPEVR registers. System notification by a GPIO pin is enabled if the corresponding bit of the GPEVEN register is set to 1. The corresponding bits in the GPEVR register select which means of system notification the detected event is routed to. The event routing mechanism is described in Figure 20.

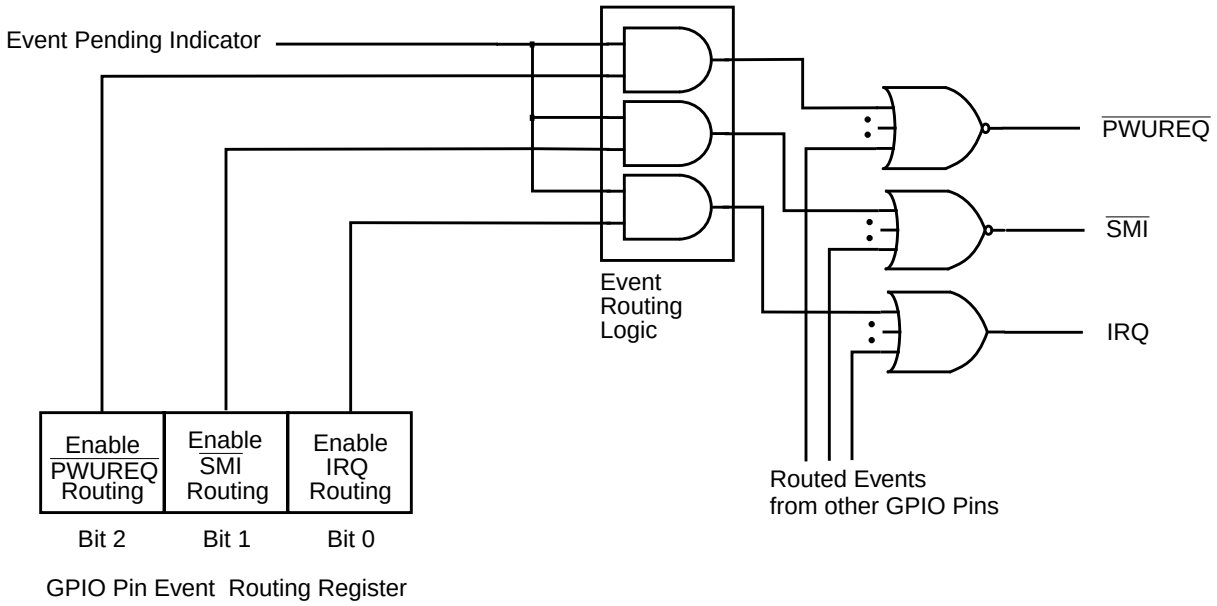


Figure 20. GPIO Event Routing Mechanism

The GPST register is a general-purpose edge detector which may be used to reflect the event source pending status for edge-triggered events.

The term *active edge* refers to a change in a GPIO pin level that matches the Event Polarity bit (1 for rising edge and 0 for falling edge). *Active level* refers to the GPIO pin level that matches the Event Polarity bit (1 for high level and 0 for low level). The corresponding bit of the GPST register is set by hardware whenever an active edge is detected, regardless of any other bit settings. Writing 1 to the Status bit clears it to 0. Writing 0 is ignored.

A GPIO pin is in event pending state if the corresponding bit of the GPEVEN register is set and either:

- The Event Type is level and the pin is in active level, or
- The Event Type is edge and the corresponding bit of the GPST register is set.

The target means of system notification is asserted if at least one GPIO pin is in event pending state.

The selection of the target means of system notification is determined by the GPEVR register. If IRQ is selected as one of the means for the system notification, the specific IRQ line is determined by the IRQ selection procedure of the device configuration. The assertion of any means of system notification is blocked when the GPIO functional block is deactivated.

If the output of a GPIO pin is enabled, it may be put in event pending state by the software when writing to the GPDO register.

An pending edge event may be cleared by clearing the corresponding GPST bit. However, a level event source may not be released by software (except for disabling the source), as long as the pin is in active level. When level event is used, it is recommended to disable the input debouncer.

Upon de-activation of the GPIO port, the GPST register is cleared and access to both the GPST and GPEVEN registers is disabled. All system notification means including the target IRQ line are detached from the GPIO and de-asserted.

Before enabling any system notification, it is recommended to set the desired event configuration, and then verify that the status registers are cleared.

6.4 GPIO PORT REGISTERS

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

6.4.1 GPIO Pin Configuration (GPCFG) Register

This is a group of eight identical configuration registers, each of which is associated with one GPIO pin. The entire set is mapped to the PnP configuration space. The mapping scheme is based on the GPSEL register that functions as an index register, and the specific GPCFG register that reflects the configuration of the currently selected pin. For details on the GPSEL register, refer to the *Device Architecture and Configuration* chapter.

Bits 4-6 are applicable only for the enhanced GPIO port with event detection support. In the basic port. these bits are reserved, return 0 on read and have no effect on port functionality.

Location: Device specific

Type: R/W (bit 3 is set only)

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**	**Event Debounce Enable**	**Event Polarity**	**Event Type**	**Lock**	**Pull-Up Control**	**Output Type**	**Output Enable**
Reset	0	1	0	0	0	1	0	0

Bit	Description
7	**Reserved**
6	**Event Debounce Enable** 0: Disabled 1: Enabled (default)
5	**Event Polarity.** This bit defines the polarity of the signal that causes a detection of an event from the corresponding GPIO pin (falling/low or rising/high). 0: Falling edge or low level input (default) 1: Rising edge or high level input
4	**Event Type.** This bit defines the signal type that causes a detection of an event from the corresponding GPIO pin. 0: Edge input (default) 1: Level input
3	**Lock**. This bit locks the corresponding GPIO pin. Once this bit is set to 1 by software, it can only be cleared to 0 by system reset or power-off. Pin multiplexing is functional until the Multiplexing Lock bit is 1. (Refer to the *Device Architecture and Configuration* chapter.) 0: No effect (default) 1: Direction, output type, pull-up and output value locked
2	**Pull-Up Control**. This bit is used to enable/disable the internal pull-up capability of the corresponding GPIO pin. It supports open-drain output signals with internal pull-ups and TTL input signals 0: Disabled 1: Enabled (default)
1	**Output Type.** This bit controls the output buffer type (open-drain or push-pull) of the corresponding GPIO pin. 0: Open-drain (default) 1: Push-pull
0	**Output Enable.** This bit indicates the GPIO pin output state. It has no effect on input. 0: TRI-STATE (default) 1: Output enabled

6.4.2 GPIO Pin Event Routing (GPEVR) Register

This is a group of eight identical configuration registers, each of which is associated with one GPIO pin. The entire set is mapped to the PnP configuration space. The mapping scheme is based on the GPSEL register that functions as an index register, and the specific GPER register that reflects the routing configuration of the currently selected pin. For details on the GPSEL register, refer to the *Device Architecture and Configuration* chapter.

This set of registers is applicable only for the enhanced GPIO port with event detection support. In the basic port this register set is reserved, returns 0 on read and has no effect on port functionality.

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**					**GPIO Event to $\overline{\text{PWUREQ}}$ Enable**	**GPIO Event to $\overline{\text{SMI}}$ Enable**	**GPIO Event to IRQ Enable**
Reset	0	0	0	0	0	0	0	1

Bit	Description
7-3	**Reserved**
2	**GPIO Event to $\overline{\text{PWUREQ}}$ Enable**. This bit is used to enable/disable the routing of the corresponding GPIO detected event to $\overline{\text{PWUREQ}}$. 0: Disabled (default) 1: Enabled
1	**GPIO Event to $\overline{\text{SMI}}$ Enable.** This bit is used to enable/disable the routing of the corresponding GPIO detected event to $\overline{\text{SMI}}$. 0: Disabled (default) 1: Enabled
0	**GPIO Event to IRQ Enable.** This bit is used to enable/disable the routing of the corresponding GPIO detected event to IRQ. 0: Disabled 1: Enabled (default)

6.4.3 GPIO Port Runtime Register Map

Offset	Mnemonic	Register Name	Type	Section
Device specific Note 1.	GPDO	GPIO Data Out	R/W	6.4.4
Device specific Note 1.	GPDI	GPIO Data In	RO	6.4.5
Device specific Note 1.	GPEVEN	GPIO Event Enable	R/W	6.4.6
Device specific Note 1.	GPEVST	GPIO Event Status	R/W1C	6.4.7

Note 1. The location of this register is defined in the *Device Architecture and Configuration* chapter in Section 2.14.1.

6.4.4 GPIO Data Out Register (GPDO)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Data Out**							
Reset	1	1	1	1	1	1	1	1

Bit	Description
7	**Data Out.** Bits 7-0 correspond to pins 7-0 respectively. The value of each bit determines the value driven on the corresponding GPIO pin when its output buffer is enabled. Writing to the bit latches the written data unless the bit is locked by the GPCFG register Lock bit. Reading the bit returns its value, regardless of the pin value and configuration. 0: Corresponding pin driven to low when output enabled 1: Corresponding pin driven or released to high (according to buffer type and static pull-up selection) when output enabled
6	
5	
4	
3	
2	
1	
0	

6.4.5 GPIO Data In Register (GPDI)

Location: Device specific

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Data In**							
Reset	X	X	X	X	X	X	X	X

Bit	Description
7	**Data In.** Bits 7-0 correspond to pins 7-0 respectively. Reading each bit returns the value of the corresponding GPIO pin, regardless of the pin configuration and the GPDO register value. Write is ignored. 0: Corresponding pin level low 1: Corresponding pin level high
6	
5	
4	
3	
2	
1	
0	

6.4.6 GPIO Event Enable Register (GPEVEN)

Location: Device specific

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Event Enable**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Event Enable.** Bits 7-0 correspond to pins 7-0 respectively. Each bit enables system notification triggering by the corresponding GPIO pin. The bit has no effect on the corresponding Status bit in the GPST register. 0: IRQ generation by corresponding GPIO pin masked 1: IRQ generation by corresponding GPIO pin enabled
6	
5	
4	
3	
2	
1	
0	

6.4.7 GPIO Event Status Register (GPEVST)

Location: Device specific

Type: R/W1C

Bit	7	6	5	4	3	2	1	0
Name	**Status**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**Status.** Bits 7-0 correspond to pins 7-0 respectively. Each bit is an edge detector that is set to 1 by the hardware upon detection of an active edge (i.e. edge that matches the IRQ Polarity bit) on the corresponding GPIO pin. This edge detection is independent of the Event Type or the Event Enable bit in the GPEVEN register. However, the bit may reflect the event status for enabled, edge-trigger event sources. Writing 1 to the Status bit clears it to 0. 0: No active edge detected since last cleared 1: Active edge detected
6	
5	
4	
3	
2	
1	
0	

7.0 WATCHDOG Timer (WDT)

7.1 OVERVIEW

The WATCHDOG Timer prompts the system via SMI or interrupt when no system activity is detected on a predefined selection of system events for a predefined period of time (1 to 255 minutes).

The WATCHDOG Timer monitors four maskable system events: the interrupt request lines of the Keyboard, Mouse and the two serial ports (UART1 and UART2). The system prompt is performed by asserting a special-purpose output pin ($\overline{WDO}$), which can be attached to external SMI. Alternatively, this indication can be routed to any arbitrary IRQ line and is also available on a status bit that can be read by the host.

This chapter describes the generic WATCHDOG Timer functional block. A device may include a different implementation. For device specific implementation, see the *Device Architecture and Configuration* chapter.

7.2 FUNCTIONAL DESCRIPTION

The WATCHDOG Timer consists of an 8-bit counter and three registers: Timeout register (WDTO), Mask register (WDMSK) and Status register (WDST). The counter is an 8-bit down counter that is clocked every minute and is used for the timeout period countdown. The WDTO register holds the programmable timeout, which is the period of inactivity after which the WATCHDOG Timer prompts the system (1 to 255 minutes). The WDMSK register determines which system events are enabled as WATCHDOG Timer trigger events to restart the countdown. The WDST register holds the WATCHDOG Timer status bit that reflects the value of the $\overline{WDO}$ pin and indicates that the timeout period has expired.

Figure 21 shows the functionality of the WATCHDOG Timer.

Upon reset, the Timeout register (WDTO) is initialized to zero, the timer is deactivated, the $\overline{WDO}$ is inactive (high) and all trigger events are masked.

Upon writing to the WDTO register, the timer is activated while the counter is loaded with the timeout value and starts counting down every minute. If a trigger event (unmasked system event) occurs before the counter has expired (reached zero), the counter is reloaded with the timeout period (from WDTO register) and restarts the countdown. If no trigger event occurs before the timeout period expires, the counter reaches zero and stops counting. Consequently, the $\overline{WDO}$ pin is asserted (pulled low) and the $\overline{WDO}$ Status bit is cleared to 0.

Writing to the WDTO register de-asserts the $\overline{WDO}$ output (released high) and sets the $\overline{WDO}$ Status bit to 1. If a non-zero value is written, a new countdown starts as described above. If 00h is written, the timer is deactivated.

To summarize, the $\overline{WDO}$ output is de-asserted (high) and the Status bit is set to 1 (inactive) upon:

- Reset,
- Activating the WATCHDOG Timer or
- Writing to the WDTO register.

The $\overline{WDO}$ output is asserted (low) and the $\overline{WDO}$ status is set to zero (active) when the counter reaches zero.

When an IRQ is assigned to the WATCHDOG Timer (through the WATCHDOG Timer device configuration), the selected IRQ level is active as long as the $\overline{WDO}$ status bit is low (active).

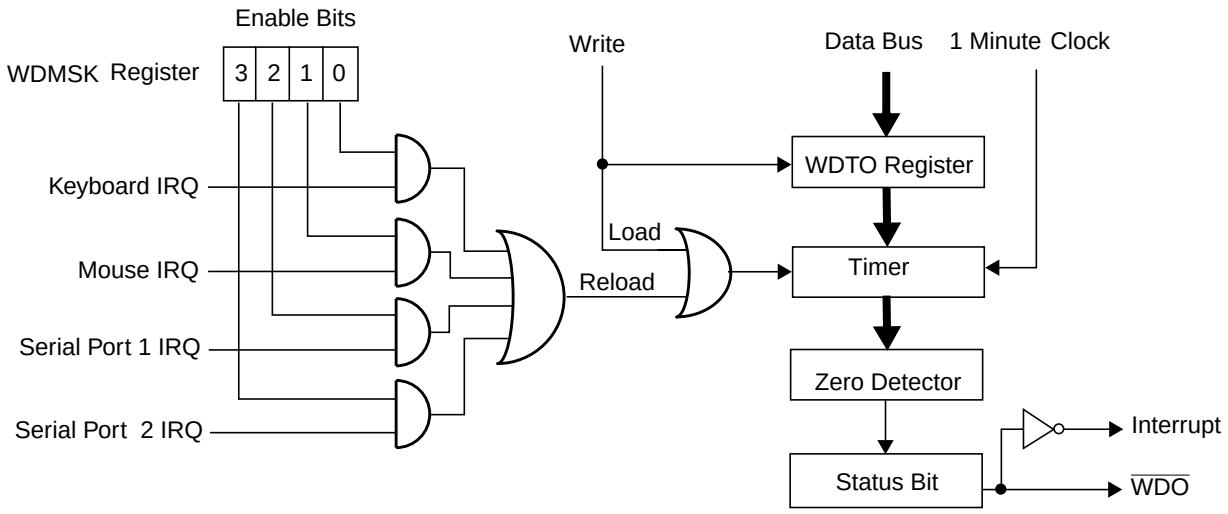


Figure 21. WATCHDOG Timer Functional Diagram

7.3 WATCHDOG TIMER REGISTERS

The WATCHDOG Timer registers at offsets 00h-02h relative to the WATCHDOG base address, are shown in the following register map. The base address is defined by designated registers in the WATCHDOG Timer device configuration register set.

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

7.3.1 WATCHDOG Timer Register Map

Offset	Mnemonic	Register Name	Type	Section
00h	WDTO	WATCHDOG Timeout	R/W	7.3.2
01h	WDMSK	WATCHDOG Mask	R/W	7.3.3
02h	WDST	WATCHDOG Status	RO	7.3.4
03h		Reserved		

7.3.2 WATCHDOG Timeout Register (WDTO)

This register holds the programmable timeout period, between 1 and 255 minutes. Writing to this register de-asserts the $\overline{\text{WDO}}$ output and sets the $\overline{\text{WDO}}$ status bit to 1 (inactive). Additionally, writing to this register is interpreted as a command for starting or stopping the WATCHDOG Timer, according to the data written. If a non-zero value is written, the timer is activated (countdown starts). If a non-zero value is written when the counter is running, the timer is immediately reloaded with the new value and starts counting down from the new value. If 00h is written, the timer and its outputs are de-activated.

Location: Offset 00h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Programmed Timeout Period**							
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-0	**Programmed Timeout Period.** These bits hold the binary value of the timeout period in minutes (1 to 255). A value of 00h halts the counter and forces the outputs to inactive levels. A device reset clears the register to 00h. 00h: Timer and $\overline{\text{WDO}}$ outputs inactive 01h-FFh: Programmed timeout period (in minutes)

7.3.3 WATCHDOG Mask Register (WDMSK)

This register is used to determine which system events (IRQ) are enabled as WATCHDOG Timer trigger events. An enabled IRQ event becomes a trigger event that causes the timer to reload the WDTO and restart the countdown.

This register enables or masks the trigger events that restart the WATCHDOG timer.

Location: Offset 01h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**Serial Port 2 IRQ Trigger Enable**	**Serial Port 1 IRQ Trigger Enable**	**Mouse IRQ Trigger Enable**	**KBD IRQ Trigger Enable**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-4	**Reserved**
3	**Serial Port 2 IRQ Trigger Enable.** This bit enables the IRQ assigned to Serial Port 2 to trigger WATCHDOG Timer reloading. 0: Serial Port 2 IRQ not a trigger event 1: An active Serial Port 2 IRQ enabled as a trigger event
2	**Serial Port 1 IRQ Trigger Enable.** This bit enables the IRQ assigned to Serial Port 1 to trigger WATCHDOG Timer reloading. 0: Serial Port 1 IRQ not a trigger event 1: An active Serial Port 1 IRQ enabled as a trigger event
1	**Mouse IRQ Trigger Enable.** This bit enables the IRQ assigned to the Mouse to trigger WATCHDOG Timer reloading. 0: Mouse IRQ not a trigger event 1: An active Mouse IRQ enabled as a trigger event
0	**KBD IRQ Trigger Enable.** This bit enables the IRQ assigned to the Keyboard to trigger reloading of the WATCHDOG timer. 0: Keyboard IRQ not a trigger event 1: An active Keyboard IRQ enabled as a trigger event

7.3.4 WATCHDOG Status Register (WDST)

This register holds the WATCHDOG Timer status, which reflects the value of the $\overline{WDO}$ pin and indicates that the timeout period has expired.

On reset or on WATCHDOG Timer activation, this register is initialized to 01h.

Location: Offset 02h

Type: RO

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**							**$\overline{WDO}$ Value**
Reset	0	0	0	0	0	0	0	1
Required	0							

Bit	Description
7-1	**Reserved**
0	**$\overline{WDO}$ Value.** This bit reflects the value of the $\overline{WDO}$ signal (even if $\overline{WDO}$ is not configured for output). 0: $\overline{WDO}$ active 1: $\overline{WDO}$ inactive (default)

7.4 WATCHDOG TIMER REGISTER BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	WDTO	Programmed Timeout Period							
01h	WDMSK	Reserved				Serial Port 2 IRQ Trigger Enable	Serial Port 1 IRQ Trigger Enable	Mouse IRQ Trigger Enable	KBD IRQ Trigger Enable
02h	WDST	Reserved							$\overline{WDO}$ Value

8.0 ACCESS.bus Interface (ACB)

The ACB is a two-wire synchronous serial interface compatible with the ACCESS.bus physical layer. The ACB is also compatible with Intel's SMBus and Philips' I^2C. The ACB can be configured as a bus master or slave, and can maintain bi-directional communication with both multiple master and slave devices. As a slave device, the ACB may issue a request to become the bus master.

The ACB allows easy interfacing to a wide range of low-cost memories and I/O devices, including EEPROMs, SRAMs, timers, ADC, DAC, clock chips and peripheral drivers.

This chapter describes the general ACB functional block. A device may include a different implementation. For device specific implementation, see the *Device Architecture and Configuration* chapter.

8.1 OVERVIEW

The ACCESS.bus protocol uses a two-wire interface for bi-directional communication between the devices connected to the bus. The two interface lines are the Serial Data Line (SDL) and the Serial Clock Line (SCL). These lines should be connected to a positive supply via an internal or external pull-up resistor, and remain high even when the bus is idle.

Each IC has a unique address and can operate as a transmitter or a receiver (though some peripherals are only receivers).

During data transactions, the master device initiates the transaction, generates the clock signal and terminates the transaction. For example, when the ACB initiates a data transaction with an attached ACCESS.bus compliant peripheral, the ACB becomes the master. When the peripheral responds and transmits data to the ACB, their master/slave (data transaction initiator and clock generator) relationship is unchanged, even though their transmitter/receiver functions are reversed.

8.2 FUNCTIONAL DESCRIPTION

8.2.1 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable (see Figure 22). Any changes on the SDA line during the high state of the SCL and in the middle of a transaction aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data, using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Each byte is transferred with the most significant bit first, and after each byte (8 bits), an Acknowledge signal must follow. The following sections provide further details of this process.

During each clock cycle, the slave can stall the master while it handles the received data or prepares new data. This can be done for each bit transferred, or on a byte boundary, by the slave holding SCL low to extend the clock-low period. Typically, slaves extend the first clock cycle of a transfer if a byte read has not yet been stored, or if the next byte to be transmitted is not yet ready. Some microcontrollers, with limited hardware support for ACCESS.bus, extend the access after each bit, thus allowing the software to handle this bit.

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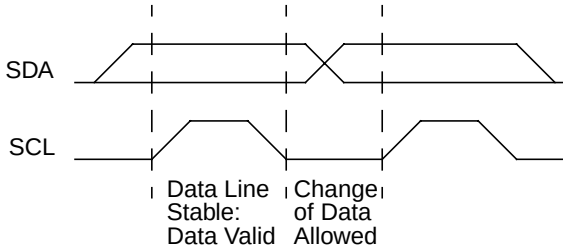

Figure 22. Bit Transfer

8.2.2 Start and Stop Conditions

The ACCESS.bus master generates Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and retains this status for a certain time after a Stop Condition is generated. A high to low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low to high transition of the SDA line while the SCL is high indicates a Stop Condition (Figure 23). After a Stop Condition is issued, the data in the received buffer is not valid.

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a change in the direction of data transfer.

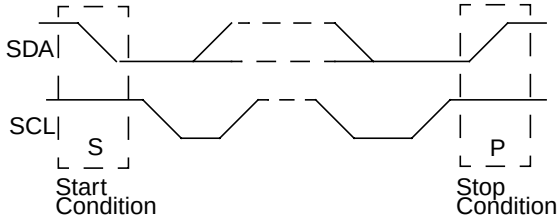

Figure 23. Start and Stop Conditions

8.2.3 Acknowledge (ACK) Cycle

The ACK cycle consists of two signals: the ACK clock pulse sent by the master with each byte transferred, and the ACK signal sent by the receiving device (see Figure 24).

The master generates the ACK clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the ACK signal. The receiver must pull down the SDA line during the ACK clock pulse, signalling that it has correctly received the last data byte and is ready to receive the next byte. Figure 25 illustrates the ACK cycle.

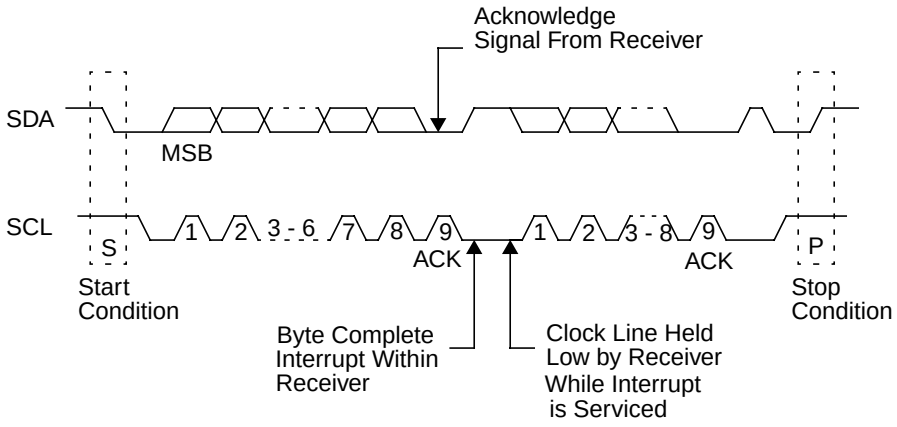

Figure 24. ACCESS.bus Data Transaction

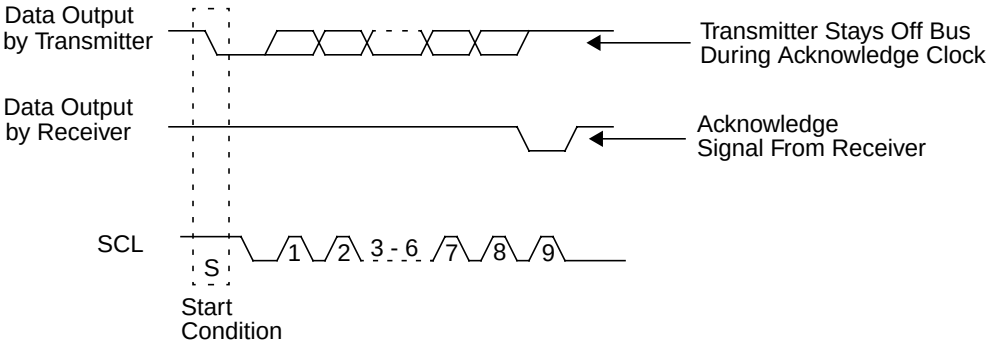

Figure 25. ACCESS.bus Acknowledge Cycle

8.2.4 Acknowledge after Every Byte Rule

According to this rule, the master generates an acknowledge clock pulse after each byte transfer, and the receiver sends an acknowledge signal after every byte received. There are two exceptions to this rule:

1. When the master is the receiver, it must indicate to the transmitter the end of data by not acknowledging (negative acknowledge) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.
2. When the receiver is full, otherwise occupied, or a problem has occurred, it sends a negative acknowledge to indicate that it cannot accept additional data bytes.

8.2.5 Addressing Transfer Formats

Each device on the bus has a unique address. Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line once it recognizes its address.

The address consists of the first 7 bits after a Start Condition. The direction of the data transfer (R/$\overline{W}$) depends on the bit sent after the address, the eighth bit. A low to high transition during a SCL high period indicates the Stop Condition, and ends the transaction of SDA (see Figure 26).

When the address is sent, each device in the system compares this address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending on the state of the R/$\overline{W}$ bit (1=read, 0=write), the device acts either as a transmitter or a receiver.

The I^2C bus protocol allows a general call address to be sent to all slaves connected to the bus. The first byte sent specifies the general call address (00h) and the second byte specifies the meaning of the general call (for example, write slave address by software only). Those slaves that require data acknowledge the call, and become slave receivers; other slaves ignore the call.

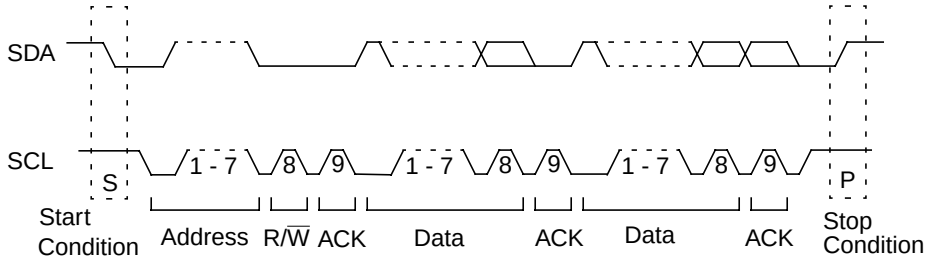

Figure 26. A Complete ACCESS.bus Data Transaction

8.2.6 Arbitration on the Bus

Multiple master devices on the bus require arbitration between their conflicting bus access demands. Control of the bus is initially determined according to address bits and clock cycle. If the masters are trying to address the same slave, data comparisons determine the outcome of this arbitration. In master mode, the device immediately aborts a transaction if the value sampled on the SDA line differs from the value driven by the device. (An exception to this rule is SDA while receiving data. The lines may be driven low by the slave without causing an abort.)

The SCL signal is monitored for clock synchronization and to allow the slave to stall the bus. The actual clock period is set by the master with the longest clock period, or by the slave stall period. The clock high period is determined by the master with the shortest clock high period.

When an abort occurs during the address transmission, a master that identifies the conflict should give up the bus, switch to slave mode and continue to sample SDA to check if it is being addressed by the winning master on the bus.

8.2.7 Master Mode

Requesting Bus Mastership

An ACCESS.bus transaction starts with a master device requesting bus mastership. It asserts a Start Condition, followed by the address of the device it wants to access. If this transaction is successfully completed, the software may assume that the device has become the bus master.

For the device to become the bus master, the software should perform the following steps:

1. Configure the INTEN bit of the ACBCTL1 register to the desired operation mode (Polling or Interrupt) and set the START bit of this register. This causes the ACB to issue a Start Condition on the ACCESS.bus when the ACCESS.bus becomes free (BB bit of the ACBCST register is cleared, or other conditions that can delay start). It then stalls the bus by holding SCL low.
2. If a bus conflict is detected (i.e., another device pulls down the SCL signal), the BER bit of the ACBST register is set.
3. If there is no bus conflict, the MASTER bit of the ACBST register and the SCAST of the ACBST register are set.
4. If the INTEN bit of the ACBCTL1 register is set and either the BER or SDAST bit of the ACBST register is set, an interrupt is issued.

Sending the Address Byte

When the device is the active master of the ACCESS.bus (the MASTER bit of the ACBST register is set), it can send the address on the bus.

The address sent should not be the device's own address, as defined by the ADDR bit of the ACBADDR register if the SAEN bit of this register is set, nor should it be the global call address if the GCMTCH bit of the ACBCST register is set.

To send the address byte, use the following sequence:

1. For a receive transaction where the software wants only one byte of data, it should set the ACB bit of the ACBCTL1 Registe. If only an address needs to be sent or if the device requires stall for some other reason, set the STASTRE bit of the ACBCTL1 register.
2. Write the address byte (7-bit target device address) and the direction bit to the ACBSDA register. This causes the ACB to generate a transaction. At the end of this transaction, the acknowledge bit received is copied to the NEGACK bit of the ACBST register. During the transaction, the SDA and SCL lines are continuously checked for conflict with other devices. If a conflict is detected, the transaction is aborted, the BER bit of the ACBST register is set and the MASTER bit of this register is cleared.
3. If the STASTRE bit of the ACBCTL1 register is set and the transaction was successfully completed (i.e., both the BER and NEGACK bits of the ACBST register are cleared), the STASTR bit is set. In this case, the ACB stalls any further ACCESS.bus operations (i.e., holds SCL low). If the INTEN bit of the ACBCTL1 register is set, it also sends an interrupt request to the host.
4. If the requested direction is transmit and the start transaction was completed successfully (i.e., neither the NEGACK nor the BER bit of the ACBST register is set, and no other master has accessed the device), the SDAST bit of the ACBST register is set to indicate that the ACB awaits attention.
5. If the requested direction is receive, the start transaction was completed successfully and the STASTRE bit of the ACBCTL1 register is cleared, the ACB starts receiving the first byte automatically.
6. Check that both the BER and NEGACK bits of the ACBST register are cleared. If the INTEN bit of the ACBCTL1 register is set, an interrupt is generated when either the BER or NEGACK bit of the ACBST register is set.

Master Transmit

After becoming the bus master, the device can start transmitting data on the ACCESS.bus.

To transmit a byte in an interrupt or polling controlled operation, the software should:

1. Check that both the BER and NEGACK bits of the ACBST register are cleared, and that the SDAST bit of the ACBST register is set. If the STASTRE bit of the ACBCTL1 register is set, also check that the STASTR bit of the ACBST register is cleared (and clear it if required).
2. Write the data byte to be transmitted to the ACBSDA register.

When either the NEGACK or BER bit of the ACBST register is set, an interrupt is generated. When the slave responds with a negative acknowledge, the NEGACK bit of the ACBST register is set and the SDAST bit of the ACBST register remains cleared. In this case, if the INTEN bit of the ACBCTL1 register is set, an interrupt is issued.

Master Receive

After becoming the bus master, the device can start receiving data on the ACCESS.bus.

To receive a byte in an interrupt or polling operation, the software should:

1. Check that the SDAST bit of the ACBST register is set and that the BER bit is cleared. If the STASTRE bit of the ACBCTL1 register is set, also check that the STASTRE bit of the ACBST register is cleared (and clear it if required).
2. Set the ACK bit of the ACBCTL1 register to 1, if the next byte is the last byte that should be read. This causes a negative acknowledge to be sent.
3. Read the data byte from the ACBSDA register.

Before receiving the last byte of data, set the ACK bit of the ACBCTL1 register.

Master Stop

To end a transaction, set the STOP bit of the ACBCTL1 register before clearing the current stall flag (i.e., the SDAST, NEGACK or STASTR bit of the ACBST register). This causes the ACB to send a Stop Condition immediately, and to clear the STOP bit of the ACBCTL1 register. A Stop Condition may be issued only when the device is the active bus master (the MASTER bit of the ACBST register is set).

Master Bus Stall

The ACB can stall the ACCESS.bus between transfers while waiting for the host response. The ACCESS.bus is stalled by holding the SCL signal low after the acknowledge cycle. Note that this is interpreted as the beginning of the following bus operation. The user must make sure that the next operation is prepared before the flag that causes the bus stall is cleared.

The flags that can cause a bus stall in master mode are:

- Negative acknowledge after sending a byte (NEGACK bit of the ACBST register =1).
- SDAST bit of the ACBST register =1.
- STASTRE bit of the ACBCTL1 register =1, after a successful start (STASTR bit of the ACBST register =1).

Repeated Start

A repeated start is performed when the device is already the bus master (MASTER bit of the ACBST register is set). In this case, the ACCESS.bus is stalled and the ACB awaits host handling due to the following states in the ACBST register: negative acknowledge (NEGACK bit =1), empty buffer (SDAST bit =1) and/or a stall after start (STASTR bit =1).

For a repeated start:

1. Set the START bit of the ACBCTL1 register =1.
2. In master receive mode, read the last data item from ACBSDA.
3. Follow the address send sequence, as described in “Sending the Address Byte”.
4. If the ACB was awaiting handling (STASTR bit of the ACBST register =1), clear it only after writing the requested address and direction to ACBSDA.

Master Error Detection

The ACB detects illegal Start or Stop Conditions (i.e., a Start or Stop Condition within the data transfer, or the acknowledge cycle) and a conflict on the data lines of the ACCESS.bus. If an illegal condition is detected, BER is set, and master mode is exited (MASTER bit of the ACBST. register is cleared).

Bus Idle Error Recovery

When a request to become the active bus master or a restart operation fails, the BER bit of the ACBST register is set to indicate the error. In some cases, both the device and the other device may identify the failure and leave the bus idle. In this case, the start sequence may be incomplete and the ACCESS.bus may remain deadlocked.

To recover from deadlock, use the following sequence:

1. Clear the BER and BB bits of the ACBCST register.
2. Wait for a timeout period to check that there is no other active master on the bus (the BB bit remains cleared).
3. Disable, and re-enable the ACB to put it in the non-addressed slave mode. This completely resets the functional block.

At this point, some of the slaves may not identify the bus error. To recover, the ACB becomes the bus master: it asserts a Start Condition, sends an address byte, then asserts a Stop Condition which synchronizes all the slaves.

8.2.8 Slave Mode

A slave device waits in idle mode for a master to initiate a bus transaction. Whenever the ACB is enabled and it is not acting as a master (the MASTER bit of the ACBST register is cleared), it acts as a slave device.

Once a Start Condition on the bus is detected, the device checks whether the address sent by the current master matches either:

- The ADDR bit value of the ACBADDR register, if the SAEN bit =1, or
- The general call address if the GCMEN bit of the ACBCTL1 register =1.

This match is checked even when the MASTER bit is set. If a bus conflict (on SDA or SCL) is detected, the BER bit of the ACBST register is set, the MASTER bit is cleared and the device continues to search the received message for a match.

If an address match or a global match is detected:

1. The device asserts its SDA pin during the acknowledge cycle.
2. The MATCH bit of the ACBCST register and the NMATCH bit of the ACBST register are set. If the XMIT bit of the ACBST register is set (slave transmit mode), the SDAST bit of the ACBST register is set to indicate that the buffer is empty.
3. If the INTEN bit of the ACBCTL1 register is set, an interrupt is generated the NMINTE bit is also set.
4. The software then reads the XMIT bit of the ACBST register to identify the direction requested by the master device. It clears the NMATCH bit of the ACBST Registe so future byte transfers are identified as data bytes.

Slave Receive and Transmit

Slave receive and transmit are performed after a match is detected and the data transfer direction is identified. After a byte transfer, the ACB extends the acknowledge clock until the software reads or writes the ACBSDA register. The receive and transmit sequences are identical to those used in the master routine.

Slave Bus Stall

When operating as a slave, the device stalls the ACCESS.bus by extending the first clock cycle of a transaction in the following cases:

- SDAST bit of the ACBST register is set.
- NMATCH bit of the ACBST register and NMINTE bit of the ACBCTL1 register are set.

Slave Error Detection

The ACB detects illegal Start and Stop Conditions on the ACCESS.bus (i.e., a Start or Stop Condition within the data transfer or the acknowledge cycle). When this occurs, the BER bit is set and MATCH and GMATCH are cleared, setting the ACB as an unaddressed slave.

8.2.9 Configuration

SDA and SCL Signals

The SDA and SCL are open-drain signals. The device permits the user to define whether to enable or disable the internal pull-up of each of these signals.

ACB Clock Frequency

The ACB permits the user to set the clock frequency for the ACCESS.bus clock. The clock is set by the the SCLFRQ field of the ACBCTL2 register, which determines the SCL clock period used by the device. This clock low period may be extended by stall periods initiated by the ACB or by another ACCESS.bus device. In case of a conflict with another bus master, a shorter clock high period may be forced by the other bus master until the conflict is resolved.

8.3 ACB REGISTERS

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

8.3.1 ACB Register Map

Offset	Mnemonic	Register Name	Type	Section
00h	ACBSDA	ACB Serial Data	R/W	8.3.2
01h	ACBST	ACB Status	Varies per bit	8.3.3
02h	ACBCST	ACB Control Status	Varies per bit	8.3.4
03h	ACBCTL1	ACB Control 1	R/W	8.3.5
04h	ACBADDR	ACB Own Address	R/W	8.3.6
05h	ACBCTL2	ACB Control 2	R/W	8.3.7

8.3.2 ACB Serial Data Register (ACBSDA)

This shift register is used to transmit and receive data. The most significant bit is transmitted (received) first, and the least significant bit is transmitted (received) last. Reading or writing to the ACBSDA register is allowed only when the SDAST bit of the ACBST register is set, or for repeated starts after setting the START bit. An attempt to access this register under other conditions may produce unpredictable results.

Location: Offset 00h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**ACB Serial Data**							
Reset								

8.3.3 ACB Status Register (ACBST)

This register maintains the current ACB status. On reset, and when the ACB is disabled, ACBST is cleared (00h).

Location: Offset 01h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**SLVSTP**	**SDAST**	**BER**	**NEGACK**	**STASTR**	**NMATCH**	**MASTER**	**XMIT**
Reset	0	0	0	0	0	0	0	0

Bit	Type	Description
7	R/W1C	**SLVSTP (Slave Stop)**. Writing 0 to SLVSTP is ignored. 0: Writing 1 or ACB disabled 1: Stop Condition detected after a slave transfer in which MATCH or GCMATCH was set
6	RO	**SDAST (SDA Status)** 0: Reading from the ACBSDA register during a receive, or when writing to it during a transmit. When ACBCTL1.START is set, reading the ACBSDA register does not clear SDAST. This enables ACB to send a repeated start in master receive mode. 1: SDA Data register awaiting data (transmit - master or slave) or holds data that should be read (receive - master or slave).
5	R/W1C	**BER (Bus Error)**. Writing 0 to BER is ignored. 0: Writing 1 or ACB disabled 1: Start or Stop Condition detected during data transfer (i.e., Start or Stop Condition during the transfer of bits 2 through 8 and acknowledge cycle), or when an arbitration problem is detected.
4	R/W1C	**NEGACK (Negative Acknowledge)**. Writing 0 to NEGACK is ignored. 0: Writing 1 or ACB disabled 1: Transmission not acknowledged on the ninth clock (In this case, SDAST is not set)
3	R/W1C	**STASTR (Stall After Start)**. Writing 0 to STASTR is ignored. 0: Writing 1 or ACB disabled 1: Address sent successfully (i.e., a Start Condition sent without a bus error, or Negative Acknowledge), if ACBCTL1.STASTRE is set. This bit is ignored in slave mode. When STASTR is set, it stalls the ACCESS.bus by pulling down the SCL line, and suspends any further action on the bus (e.g., receive of first byte in master receive mode). In addition, if ACBCTL1.INTEN is set, it also causes the ACB to send an interrupt.
2	R/W1C	**NMATCH (New Match**). Writing 0 to NMATCH is ignored. If ACBCTL1.INTEN is set, an interrupt is sent when this bit is set. 0: Software writes 1 to this bit 1: Address byte follows a Start Condition or a repeated start, causing a match or a global-call match.
1	RO	**Master** 0: Arbitration loss (BER is set) or recognition of a Stop Condition 1: Bus master request succeeded and master mode active
0	RO	**XMIT (Transmit**). Direction bit. 0: Master/slave transmit mode not active 1: Master/slave transmit mode active

8.3.4 ACB Control Status Register (ACBCST)

This register configures and controls the ACB functional block. It maintains the current ACB status and controls several ACB functions. On reset and when the ACB is disabled, the non-reserved bits of ACBCST are cleared.

Location: Offset 02h

Type: Varies per bit

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**TGSCL**	**TSDA**	**GCMTCH**	**MATCH**	**BB**	**BUSY**
Reset	0	0	0	X	0	0	0	0

Bit	Type	Description
7-6		**Reserved**
5	R/W	**TGSCL (Toggle SCL Line**). Enables toggling the SCL line during error recovery. 0: Clock toggle completed 1: When the SDA line is low, writing 1 to this bit toggles the SCL line for one cycle. Writing 1 to TGSCL while SDA is high is ignored.
4	RO	**TSDA (Test SDA Line**). This bit reads the current value of the SDA line. It can be used while recovering from an error condition in which the SDA line is constantly pulled low by an out-of-sync slave. Data written to this bit is ignored.
3	RO	**GCMTCH (Global Call Match)** 0: Start Condition or repeated Start and a Stop Condition (including illegal Start or Stop Condition) 1: In slave mode, ACBCTL1.GCMEN is set and the address byte (the first byte transferred after a Start Condition) is 00h.
2	RO	**MATCH (Address Match**) 0: Start Condition or repeated Start and a Stop Condition (including illegal Start or Stop Condition) 1: ACBADDR.SAEN is set and the first 7 bits of the address byte (the first byte transferred after a Start Condition) match the 7-bit address in the ACBADDR register.
1	R/W1C	**BB (Bus Busy)** 0: Writing 1, ACB disabled, or Stop Condition detected 1: Bus active (a low level on either SDA or SCL), or Start Condition
0	RO	**Busy**. This bit should always be written 0. This bit indicates the period between detecting a Start Condition and completing receipt of the address byte. After this, the ACB is either free or enters slave mode. 0: Completion of any state below or ACB disabled 1: ACB is in one of the following states: — Generating a Start Condition — Master mode (ACBST.MASTER is set) — Slave mode (ACBCST.MATCH or ACBCST.GCMTCH set).

8.3.5 ACB Control Register 1 (ACBCTL1)

Location: Offset 03h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**STASTRE**	**NMINTE**	**GCMEN**	**ACK**	**Reserved**	**INTEN**	**STOP**	**START**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7	**STASTRE (Stall After Start Enable**) 0: When cleared, ACBST.STASTR can not be set. However, if ACBST.STASTR is set, clearing STASTRE will not clear ACBST.STASTR. 1: Stall after start mechanism enabled, and ACB stalls the bus after the address byte
6	**NMINTE (New Match Interrupt Enable)** 0: No interrupt issued on a new match 1: Interrupt issued on a new match only if ACBCTL1.INTEN set
5	**GCMEN (Global Call Match Enable)** 0: ACB not responding to global call 1: Global call match enabled
4	**Receive Acknowledge**. This bit is ignored in transmit mode. When the device acts as a receiver (slave or master), this bit holds the stop transmitting instruction that is transmitted during the next acknowledge cycle. 0: Cleared after acknowledge cycle 1: Negative acknowledge issued on next received byte
3	**Reserved**
2	**Interrupt Enable** 0: ACB interrupt disabled 1: ACB interrupt enabled. An interrupt is generated in response to one of the following events: — Detection of an address match (ACBST.NMATCH=1) and NMINTE=1 — Receipt of Bus Error (ACBST.BER=1) — Receipt of Negative Acknowledge after sending a byte (ACBST.NEGACK=1) — Acknowledge of each transaction (same as the hardware set of the ACBST.SDAST bit) — In master mode if ACBCTL1.STASTRE=1, after a successful start (ACBST.STASTR=1) — Detection of a Stop Condition while in slave mode (ACBST.SLVSTP=1).
1	**Stop** 0: Automatically cleared after STOP issued 1: Setting this bit in master mode generates a Stop Condition to complete or abort current message transfer
0	**Start**. Set this bit only when in master mode or when requesting master mode. 0: Cleared after Start Condition sent or Bus Error (ACBST.BER=1) detected 1: Single or repeated Start Condition generated on the ACCESS.bus. If the device is not the active master of the bus (ACBST.MASTER=0), setting START generates a Start Condition when the ACCESS.bus becomes free (ACBCST.BB=0). An address transmission sequence should then be performed. If the device is the active master of the bus (ACBST.MASTER=1), setting START and then writing to the ACBSDA register generates a Start Condition. If a transmission is already in progress, a repeated Start Condition is generated. This condition can be used to switch the direction of the data flow between the master and the slave, or to choose another slave device without separating them with a Stop Condition.

8.3.6 ACB Own Address Register (ACBADDR)

This is a byte-wide register that holds the ACB ACCESS.bus address. The reset value of this register is undefined.

Location: Offset 04h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SAEN**	**ADDR**						
Reset								

Bit	Description
7	**SAEN (Slave Address Enable)** 0: ACB does not check for an address match with ADDR field 1: ADDR field holds a valid address and enables the match of ADDR to an incoming address byte
6-0	**ADDR (Own Address).** These bits hold the 7-bit device address. When in slave mode, the first 7 bits received after a Start Condition are compared with this field (first bit received is compared with bit 6, and the last bit with bit 0). If the address field matches the received data and SAEN (bit 7) is 1, a match is declared.

8.3.7 ACB Control Register 2 (ACBCTL2)

This register enables/disables the functional block and determines the ACB clock rate.

Location: Offset 05h

Type: R/W

Bit	7	6	5	4	3	2	1	0
Name	**SCLFRQ**							**ENABLE**
Reset	0	0	0	0	0	0	0	0

Bit	Description
7-1	**SCLFRQ (SCL Frequency**). This field defines the SCL period (low and high time) when the device serves as a bus master. The clock low and high times are defined as follows: $t_{SCLl} = t_{SCLh} = 2*SCLFRQ*t_{CLK}$ where t_{CLK} is the module input clock cycle, as defined in the *Device Architecture and Configuration* chapter. SCLFRQ can be programmed to values in the range of 0001000_2 (8_{10}) through 1111111_2 (127_{10}). Using any other value has unpredictable results.
0	**Enable** 0: ACB disabled, ACBCTL1, ACBST and ACBCST cleared, and clocks halted 1: ACB enabled

8.4 ACB REGISTER BITMAP

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	ACBSDA	ACB Serial Data							
01h	ACBST	SLVSTP	SDAST	BER	NEGACK	STASTR	NMATCH	MASTER	XMIT
02h	ACBCST	Reserved		TGSCL	TSDA	GCMTCH	MATCH	BB	BUSY
03h	ACBCTL1	STASTRE	NMINTE	GCMEN	ACK	Reserved	INTEN	STOP	START
04h	ACBADDR	SAEN	ADDR						
05h	ACBCTL2	SCLFRQ							ENABLE

9.0 Legacy Functional Blocks

This chapter briefly describes the following blocks that provide legacy device functions:

- Keyboard and Mouse Controller (KBC)
- Floppy Disk Controller (FDC)
- Parallel Port
- Serial Port 1 (SP1), UART Functionality for both Serial Port 1 and Serial Port 2
- Serial Port 2 (SP2), Infrared Functionality

The description of each Legacy block includes the sections listed below. For more information about legacy blocks, contact your National representative.

- General Description
- Register Map table(s)
- Bitmap table(s).

The register maps in this chapter use the following abbreviations for Type:

- R/W = Read/Write
- R = Read from a specific address returns the value of a specific register. Write to the same address is to a different register.
- W = Write
- RO = Read Only
- R/W1C = Read/Write 1 to Clear. Writing 1 to a bit clears it to 0. Writing 0 has no effect.

9.1 KEYBOARD AND MOUSE CONTROLLER (KBC)

9.1.1 General Description

The KBC is implemented physically as a single hardware module and houses two separate logical devices: a Mouse controller and a Keyboard controller.

The KBC is functionally equivalent to the industry standard 8042A Keyboard controller, which may serve as a detailed technical reference for the KBC.

9.1.2 KBC Register Map

Offset	Mnemonic	Register Name	Type
00h	DBBOUT	Read KBC Data	R
	DBBIN	Write KBC Data	W
04h	STATUS	Read Status	R
	DBBIN	Write KBC Command	W

9.1.3 KBC Bitmap Summary

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	DBBOUT	KBC Data Bits (For Read cycles)							
	DBBIN	KBC Data Bits (For Write cycles)							
04h	STATUS	General Purpose Flags				F1	F0	IBF	OBF
	DBBIN	KBC Command Bits (For Write cycles)							

9.2 FLOPPY DISK CONTROLLER (FDC)

9.2.1 General Description

The generic FDC is a standard FDC with a digital data separator, and is DP8473 and N82077 software compatible.

The FDC is implemented in this device as follows:

- FM and MFM modes are supported. To select either mode, set bit 6 of the first command byte when writing to/reading from a diskette, where:
  0 = FM mode
  1 = MFM mode
- Automatic media sense is not supported (MSEN0-1 pins are not implemented).
- DRATE1 is not supported.
- A logic 1 is returned for all floating (TRI-STATE) FDC register bits upon LPC I/O read cycles.

9.2.2 FDC Register Map

Offset	Mnemonic	Register Name	Type
00h	SRA	Status A	RO
01h	SRB	Status B	RO
02h	DOR	Digital Output	R/W
03h	TDR	Tape Drive	R/W
04h	MSR	Main Status	R
	DSR	Data Rate Select	W
05h	FIFO	Data (FIFO)	R/W
06h	Reserved		
07h	DIR	Digital Input	R
	CCR	Configuration Control	W

9.2.3 FDC Bitmap Summary

The FDC supports two system operation modes: PC-AT mode and PS/2 mode (MicroChannel systems). Unless specifically indicated otherwise, all fields in all registers are valid in both drive modes.

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	SRA[Note 1.]	IRQ Pending	Reserved	Step	$\overline{\text{TRK0}}$	Head Select	$\overline{\text{INDEX}}$	$\overline{\text{WP}}$	Head Direction
01h	SRB[Note 1.]	Reserved		Drive Select 0 Status	$\overline{\text{WDATA}}$	$\overline{\text{RDATA}}$	$\overline{\text{WGATE}}$	$\overline{\text{MTR1}}$	$\overline{\text{MTR0}}$
02h	DOR	Motor Enable 3	Motor Enable 2	Motor Enable 1	Motor Enable 0	DMAEN	Reset Controller	Drive Select	
03h	TDR	Reserved						Tape Drive Select 1,0	
	TDR[Note 2.]	Reserved		Drive ID Information		Logical Drive Exchange		Tape Drive Select 1,0	
04h	MSR	RQM	Data I/O Direction	Non-DMA Execution	Command in Progress	Drive 3 Busy	Drive 2 Busy	Drive 1 Busy	Drive 0 Busy
	DSR	Software Reset	Low Power	Reserved	Precompensation Delay Select			Data Transfer Rate Select	
05h	FIFO	Data Bits							
07h	DIR[Note 3.]	$\overline{\text{DSKCHG}}$	Reserved						
	DIR[Note 1.]	$\overline{\text{DSKCHG}}$	Reserved				DRATE 1,0 Status		High Density
07h	CCR	Reserved						DRATE1,0	

Note 1. Applicable only in PS/2 Mode
Note 2. Applicable only in Enhanced TDR Mode
Note 3. Applicable only in PC-AT Compatible Mode

9.3 PARALLEL PORT

9.3.1 General Description

The Parallel Port supports all IEEE1284 standard communication modes: Compatibility (known also as Standard or SPP), Bidirectional (known also as PS/2), FIFO, EPP (known also as Mode 4) and ECP (with an optional Extended ECP mode).

9.3.2 Parallel Port Register Map

The Parallel Port functional block register maps are grouped according to first and second level offsets. EPP and second level offset registers are available only when base address is 8-byte aligned.

Table 44. Parallel Port Register Map for First Level Offset

First Level Offset	Mnemonic	Register Name	Modes (ECR Bits) 7 6 5	Type
000h	DATAR	PP Data	0 0 0 0 0 1	R/W
000h	AFIFO	ECP Address FIFO	0 1 1	W
001h	DSR	Status	All Modes	RO
002h	DCR	Control	All Modes	R/W
003h	ADDR	EPP Address	1 0 0	R/W
004h	DATA0	EPP Data Port 0	1 0 0	R/W
005h	DATA1	EPP Data Port 1	1 0 0	R/W
006h	DATA2	EPP Data Port 2	1 0 0	R/W
007h	DATA3	EPP Data Port 3	1 0 0	R/W
400h	CFIFO	PP Data FIFO	0 1 0	W
400h	DFIFO	ECP Data FIFO	0 1 1	R/W
400h	TFIFO	Test FIFO	1 1 0	R/W
400h	CNFGA	Configuration A	1 1 1	RO
401h	CNFGB	Configuration B	1 1 1	RO
402h	ECR	Extended Control	All Modes	R/W
403h	EIR	Extended Index	All Modes	R/W
404h	EDR	Extended Data	All Modes	R/W
405h	EAR	Extended Auxiliary Status	All Modes	R/W

Table 45. Parallel Port Register Map for Second Level Offset

Second Level Offset	Register Name	Type
00h	Control0	R/W
02h	Control2	R/W
04h	Control4	R/W
05h	PP Confg0	R/W

9.3.3 Parallel Port Bitmap Summary

The Parallel Port functional block bitmaps are grouped according to first and second level offsets.

Table 46. Parallel Port Bitmap Summary for First Level Offset

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
000h	DATAR	Data Bits							
	AFIFO	Address Bits							
001h	DSR	Printer Status	$\overline{\text{ACK}}$ Status	PE Status	SLCT Status	$\overline{\text{ERR}}$ Status	Reserved		EPP Time-out Status
002h	DCR	Reserved		Direction Control	Interrupt Enable	PP Input Control	Printer Initialization Control	Automatic Line Feed Control	Data Strobe Control
003h	ADDR	EPP Device or Register Selection Address Bits							
004h	DATA0	EPP Device or R/W Data							
005h	DATA1	EPP Device or R/W Data							
006h	DATA2	EPP Device or R/W Data							
007h	DATA3	EPP Device or R/W Data							
400h	CFIFO	Data Bits							
400h	DFIFO	Data Bits							
400h	TFIFO	Data Bits							
400h	CNFGA	Reserved				Bit 7 of PP Confg0	Reserved		
401h	CNFGB	Reserved	Interrupt Request Value	Interrupt Select			Reserved	DMA Channel Select	
402h	ECR	ECP Mode Control			ECP Interrupt Mask	ECP DMA Enable	ECP Interrupt Service	FIFO Full	FIFO Empty
403h	EIR	Reserved					Second Level Offset		
404h	EDR	Data Bits							
405h	EAR	FIFO Tag	Reserved						

Table 47. Parallel Port Bitmap Summary for Second Level Offset

Register		Bits							
Second Level Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	Control0	Reserved		DCR Register Live	Freeze Bit	Reserved			EPP Time-out Interrupt Mask
02h	Control2	SPP Compatibility	Channel Address Enable	Reserved	Revision 1.7 or 1.9 Select	Reserved			
04h	Control4	Reserved	PP DMA Request Inactive Time			Reserved	PP DMA Request Active Time		
05h	PP Confg0	Bit 3 of CNFGA	Demand DMA Enable	ECP IRQ Channel Number			PE Internal Pull-up or Pull-down	ECP DMA Channel Number	

9.4 UART FUNCTIONALITY (SP1 AND SP2)

9.4.1 General Description

Both SP1 and SP2 provide UART functionality. The generic SP1 and SP2 support serial data communication with remote peripheral device or modem using a wired interface. The functional blocks can function as a standard 16450, 16550, or as an Extended UART.

9.4.2 UART Mode Register Bank Overview

Four register banks, each containing eight registers, control UART operation. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The BSR register selects the active bank and is common to all banks. See Figure 27.

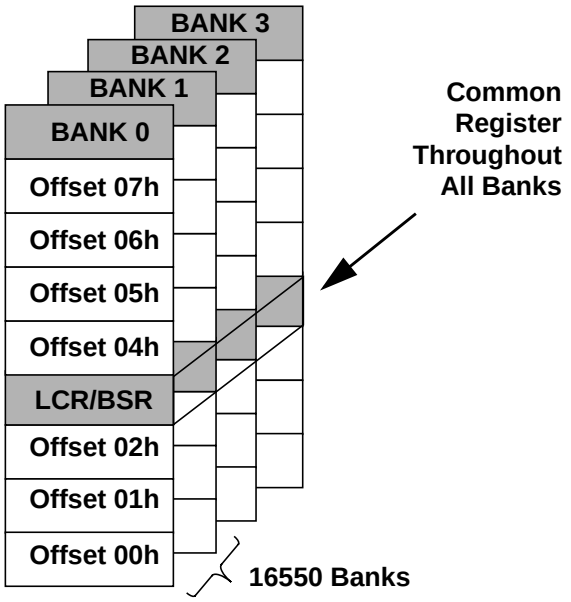

Figure 27. UART Mode Register Bank Architecture

9.4.3 SP1 and SP2 Register Maps for UART Functionality

.

Table 48. Bank 0 Register Map

Offset	Mnemonic	Register Name	Type
00h	RXD	Receiver Data Port	RO
00h	TXD	Transmitter Data Port	W
01h	IER	Interrupt Enable	R/W
02h	EIR	Event Identification (Read Cycles)	RO
	FCR	FIFO Control (Write Cycles)	W
03h	LCR[Note 1.]	Line Control	R/W
	BSR[Note 1.]	Bank Select	
04h	MCR	Modem/Mode Control	R/W
05h	LSR	Link Status	RO
06h	MSR	Modem Status	RO
07h	SPR/ASCR	Scratchpad/Auxiliary Status and Control	R/W

Note 1. When bit 7 of this Register is set to 1, bits 6-0 of BSR select the bank, as shown in Table 49.

Table 49. Bank Selection Encoding

BSR Bits								Bank Selected	Functionality
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	0	UART + IR (SP1 + SP2)
1	0	x	x	x	x	x	x	1	
1	1	x	x	x	x	1	x	1	
1	1	x	x	x	x	x	1	1	
1	1	1	0	0	0	0	0	2	
1	1	1	0	0	1	0	0	3	
1	1	1	0	1	0	0	0	4	IR Only (SP2)
1	1	1	0	1	1	0	0	5	
1	1	1	1	0	0	0	0	6	
1	1	1	1	0	1	0	0	7	

Table 50. Bank 1 Register Map

Offset	Mnemonic	Register Name	Type
00h	LBGD(L)	Legacy Baud Generator Divisor Port (Low Byte)	R/W
01h	LBGD(H)	Legacy Baud Generator Divisor Port (High Byte)	R/W
02h	Reserved		
03h	LCR/BSR	Line Control/Bank Select	R/W
04h - 07h	Reserved		

Table 51. Bank 2 Register Map

Offset	Mnemonic	Register Name	Type
00h	BGD(L)	Baud Generator Divisor Port (Low Byte)	R/W
01h	BGD(H)	Baud Generator Divisor Port (High Byte)	R/W
02h	EXCR1	Extended Control1	R/W
03h	LCR/BSR	Line Control/Bank Select	R/W
04h	EXCR2	Extended Control 2	R/W
05h	Reserved		
06h	TXFLV	TX_FIFO Level	R/W
07h	RXFLV	RX_FIFO Level	R/W

Table 52. Bank 3 Register Map

Offset	Mnemonic	Register Name	Type
00h	MRID	Module Revision ID	RO
01h	SH_LCR	Shadow of LCR (Read Only)	RO
02h	SH_FCR	Shadow of FIFO Control (Read Only)	RO
03h	LCR/BSR	Line Control/Bank Select	R/W
04h-07h	Reserved		

9.4.4 SP1 and SP2 Bitmap Summary for UART Functionality

Table 53. Bank 0 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	RXD	Receiver Data Bits							
	TXD	Transmitter Data Bits							
01h	IER Note 1.	Reserved				MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
	IER Note 2.	Reserved		TXEMP_IE	Reserved Note 3./ DMA_IE Note 4.	MS_IE	LS_IE	TXLDL_IE	RXHDL_IE
02h	EIR Note 1.	FEN1	FEN0	Reserved		RXFT	IPR1	IPR0	IPF
	EIR Note 2.	Reserved		TXEMP_EV	Reserved Note 3./ DMA_EV Note 4.	MS_EV	LS_EV or TXHLT_EV	TXLDL_EV	RXHDL_EV
	FCR	RXFTH1	RXFTH0	TXFTH1	TXFTH0	Reserved	TXSR	RXSR	FIFO_EN
03h	LCR Note 5.	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1	WLS0
	BSR Note 5.	BKSE	Bank Select						
04h	MCR Note 1.	Reserved			LOOP	ISEN or DCDLP	RILP	RTS	DTR
	MCR Note 2.	Reserved				TX_DFR	Reserved	RTS	DTR
05h	LSR	ER_INF	TXEMP	TXRDY	BRK	FE	PE	OE	RXDA
06h	MSR	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS
07h	SPR Note 1.	Scratch Data							
	ASCR Note 2.	Reserved	TXUR Note 4.	RXACT Note 4.	RXWDG Note 4.	Reserved	S_OET Note 4.	Reserved	RXF_TOUT

Note 1. Non-Extended Mode
Note 2. Extended Mode
Note 3. In SP1 only
Note 4. In SP2 only
Note 5. When bit 7 of this register is set to 1, bits 6-0 of BSR select the bank, as shown in Table 49.

Table 54. Bank 1 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	LBGD(L)	Legacy Baud Generator Divisor (Least Significant Bits)							
01h	LBGD(H)	Legacy Baud Generator Divisor (Most Significant Bits)							
02h	Reserved								
03h	LCR/BSR	Same as Bank 0							
04h-07h	Reserved								

Table 55. Bank 2 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	BGD(L)	Baud Generator Divisor Low (Least Significant Bits)							
01h	BGD(H)	Baud Generator Divisor High (Most Significant Bits)							
02h	EXCR1	BTEST	Reserved	ETDLBK	LOOP	Reserved			EXT_SL
03h	LCR/BSR	Same as Bank 0							
04h	EXCR2	LOCK	Reserved	PRESL1	PRESL0	Reserved			
05h	Reserved								
06h	TXFLV	Reserved			TFL4	TFL3	TFL2	TFL1	TFL0
07h	RXFLV	Reserved			RFL4	RFL3	RFL2	RFL1	RFL0

Table 56. Bank 3 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	MRID	Module ID (MID 7-4)				Revision ID(RID 3-0)			
01h	SH_LCR	BKSE	SBRK	STKP	EPS	PEN	STB	WLS1	WLS0
02h	SH_FCR	RXFTH1	RXFTH0	TXFHT1	TXFTH0	Reserved	TXSR	RXSR	FIFO_EN
03h	LCR/BSR	Same as Bank 0							
04h-07h	Reserved								

9.5 IR FUNCTIONALITY (SP2)

9.5.1 General Description

This section describes the IR support registers of Serial Port 2 (SP2). The UART support registers for both SP1 and SP2 are described in Section 9.4.

The IR functional block provides advanced, versatile serial communications features with IR capabilities.

SP2 supports also two DMA channels; the functional block can use either one or both of them. One channel is required for IR-based applications, since IR communication works in half duplex fashion. Two channels would normally be needed to handle high-speed full duplex UART based applications.

9.5.2 IR Mode Register Bank Overview

Eight register banks, each containing eight registers, control SP2 operation. Banks 0-3 are used to control both UART and IR modes of operation; banks 4-7 are used to control and configure the IR modes of operation only. All registers use the same 8-byte address space to indicate offsets 00h through 07h. The BSR register selects the active bank and is common to all banks. See Figure 28.

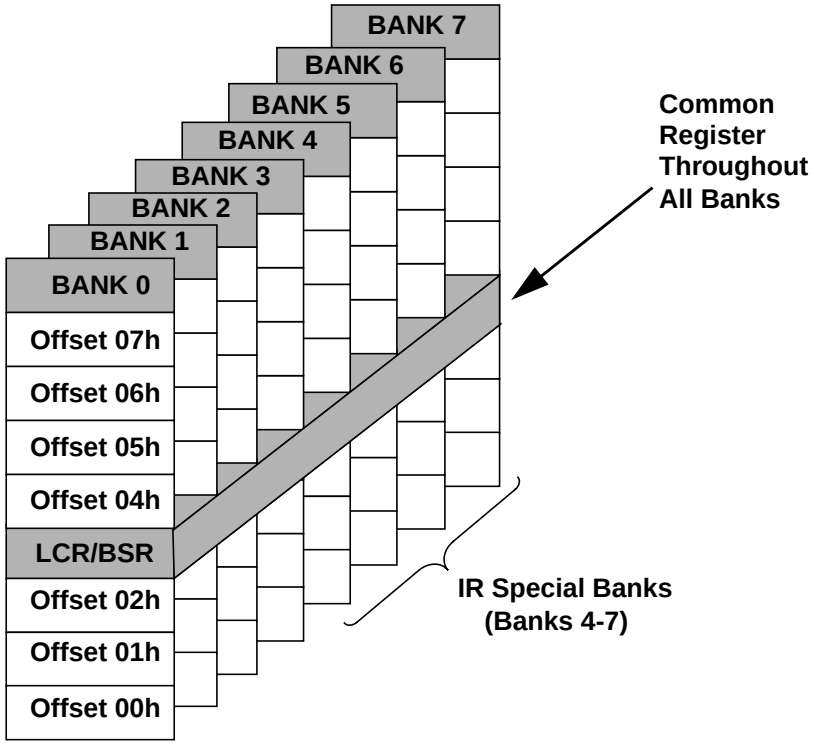

Figure 28. SP2 Register Bank Architecture

9.5.3 SP2 Register Map for IR Functionality

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Table 57. Bank 4 Register Map

Offset	Mnemonic	Register Name	Type
00h-01h	Reserved		
02h	IRCR1	IR Control 1	R/W
03h	LCR/BSR	Line Control/Bank Select	R/W
04h - 07h	Reserved		

Table 58. Bank 5 Register Map

Offset	Mnemonic	Register Name	Type
00h-02h	Reserved		
03h	LCR/BSR	Line Control/Bank Select	R/W
04h	IRCR2	IR Control 2	R/W
05h - 07h	Reserved		

Table 59. Bank 6 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRCR3	IR Control 3	R/W
01h	Reserved		
02h	SIR_PW	SIR Pulse Width Control (≤ 115 Kbps)	R/W
03h	LCR/BSR	Line Control/Bank Select	R/W
04h-07h	Reserved		

Table 60. Bank 7 Register Map

Offset	Mnemonic	Register Name	Type
00h	IRRXDC	IR Receiver Demodulator Control	RO
01h	IRTXMC	IR Transmitter Modulator Control	RO
02h	RCCFG	CEIR Configuration	RO
03h	LCR/BSR	Line Control/Bank Select	R/W
04h	IRCFG1	IR Interface Configuration 1	R/W
05h	Reserved		
06h	IRCFG3	IR Interface Configuration 3	R/W
07h	IRCFG4	IR Interface Configuration 4	R/W

9.5.4 SP2 Bitmap Summary for IR Functionality

Table 61. Bank 4 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h-01h	Reserved								
02h	EIR	Reserved				IR_SL1	IR_SL0	Reserved	
03h	LCR/BSR	Same as Bank 0							
04h-07h	Reserved								

Table 62. Bank 5 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h-02h	Reserved								
03h	LCR/BSR	Same as Bank 0							
04h	IRCR2	Reserved			AUX_IRRX	Reserved		IRMSSL	IR_FDPLX
05h-07h	Reserved								

Table 63. Bank 6 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	IRCR3	SHDM_DS	SHMD_DS	Reserved					
01h	Reserved								
02h	SIR_PW	Reserved				SPW (3-0)			
03h	LCR/BSR	Same as Bank 0							
04h-07h	Reserved								

Table 64. Bank 7 Bitmap

Register		Bits							
Offset	Mnemonic	7	6	5	4	3	2	1	0
00h	IRRXDC	DBW (2-0)			DFR (4-0)				
01h	IRTXMC	MCPW (2-0)			MCFR (4-0)				
02h	RCCFG	R_LEN	T_OV	RXHSC	RCDM_DS	Reserved	TXHSC	RC_MND1	RC_MMD0
03h	LCR/BSR	Same as Bank 0							
04h	IRCFG1	STRV_MS	SIRC (2-0)			IRID3	IRIC (2-0)		
05h	Reserved								
06h	IRCFG3	Reserved	RCH (2-0)			Reserved	RCLC (2-0)		
07h	IRCFG4	AMCFG	Reserved	IRSL0_DS	RXINV	IRSL21_DS	Reserved		

10.0 Device Characteristics

10.1 GENERAL DC ELECTRICAL CHARACTERISTICS

10.1.1 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
V_{SB}	Standby Voltage	3.0	3.3	3.6	V
V_{BAT}	Battery Backup Supply Voltage	2.4	3.0	3.6	V
T_A	Operating Temperature	0		+70	°C

10.1.2 Absolute Maximum Ratings

Absolute maximum ratings are values beyond which damage to the device may occur. Unless otherwise specified, all voltages are relative to ground.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	+6.5	V
V_I	Input Voltage		–0.5	V_{DD} + 0.5	V
V_O	Output Voltage		–0.5	V_{DD} + 0.5	V
T_{STG}	Storage Temperature		–65	+165	°C
P_D	Power Dissipation			1	W
T_L	Lead Temperature Soldering (10 s)			+260	°C
	ESD Tolerance	C_{ZAP} = 100 pF R_{ZAP} = 1.5 KΩ[Note 1.]	2000		V

Note 1. Value based on test complying with RAI-5-048-RA human body model ESD testing.

10.1.3 Capacitance

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Input Pin Capacitance		5	7	pF
C_{IN1}	Clock Input Capacitance	5	8	12	pF
C_{IO}	I/O Pin Capacitance		10	12	pF
C_O	Output Pin Capacitance		6	8	pF

T_A = 25°C, f = 1 MHz

10.1.4 Power Consumption under Recommended Operating Conditions

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{CC}	V_{DD} Average Main Supply Current	V_{IL} = 0.5 V, V_{IH} = 2.4 V No Load	32	50	mA
I_{CCLP}	V_{DD} Quiescent Main Supply Current in Low Power Mode	V_{IL} = V_{SS}, V_{IH} = V_{DD} No Load	1.3	1.7	mA
I_{SB}	V_{SB} Average Main Supply Current	V_{IL} = 0.5 V, V_{IH} = 2.4 V No Load		15	mA
I_{SBLP}	V_{SB} Quiescent Main Supply Current in Low Power Mode	V_{IL} = V_{SS}, V_{IH} = V_{SB} V No Load		3	mA
I_{BAT}	V_{BAT} Battery Supply Current	V_{DD}, V_{SB} = 0 V, V_{BAT} = 3 V		250	nA

10.2 DC CHARACTERISTICS OF PINS, BY I/O BUFFER TYPES

The following tables summarize the DC characteristics of all device pins described in the *Signal/Pin Connection and Description* chapter. The characteristics describe the general I/O buffer types defined in Table 1. For exceptions, refer to Section 10.2.10. The DC characteristics of the system interface meet the PCI2.1 3.3V DC signaling.

10.2.1 Input, CMOS Compatible

Symbol: IN_C

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.7 V_{DD}	5.5 Note 1.	V
V_{IL}	Input Low Voltage		–0.5 Note 1.	0.3 V_{DD}	V
I_{IL}	Input Leakage Current	V_{IN} = V_{DD}		50	nA
		V_{IN} = V_{SS}		–50	nA

Note 1. Not tested. Guaranteed by design.

10.2.2 Input, PCI 3.3V

Symbol: IN_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		0.5V_{DD}	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage		-0.5	0.3V_{DD}	V
I_{IL} Note 1.	Input Leakage Current	0 < V_{in} < V_{DD}		±10	µA

Note 1. Input leakage currents include hi-Z output leakage for all bidirectional buffers with TRI-STATE outputs.

10.2.3 Input, SMBus Compatible

Symbol: IN_{SM}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		1.4	5.5 Note 1.	V
V_{IL}	Input Low Voltage		–0.5 Note 1.	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		10	µA
		$V_{IN} = V_{SS}$		–10	µA

Note 1. Not tested. Guaranteed by design.

10.2.4 Input, Strap Pin

Symbol: IN_{STRP}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		$0.6V_{DD}$ Note 1.	5.5 Note 1.	V
I_{IL}	Input Leakage Current	During Reset: $V_{IN} = V_{DD}$		150	µA
		$V_{IN} = V_{SS}$		–10	µA

Note 1. Not tested. Guaranteed by design.

10.2.5 Input, TTL Compatible

Symbol: IN_{T}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5 Note 1.	V
V_{IL}	Input Low Voltage		–0.5 Note 1.	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		10	µA
		$V_{IN} = V_{SS}$		–10	µA

Note 1. Not tested. Guaranteed by design.

10.2.6 Input, TTL Compatible with Schmitt Trigger

Symbol: IN_{TS}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input High Voltage		2.0	5.5 Note 1.	V
V_{IL}	Input Low Voltage		–0.5 Note 1.	0.8	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$		10	µA
		$V_{IN} = V_{SS}$		–10	µA
V_{H}	Input Hysteresis		250		mV

Note 1. Not tested. Guaranteed by design.

10.2.7 Output, PCI 3.3V

Symbol: O_{PCI}

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{out} = -500 µA	$0.9V_{DD}$		V
V_{OL}	Output Low Voltage	I_{out} =1500 µA		$0.1\ V_{DD}$	V

10.2.8 Output, Totem-Pole Buffer

Symbol: $O_{p/n}$

Output, Totem-Pole buffer that is capable of sourcing *p* mA and sinking *n* mA

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -p$ mA	2.4		V
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V

10.2.9 Output, Open-Drain Buffer

Symbol: OD_n

Output, Open-Drain output buffer, capable of sinking *n* mA. Output from these signals is open-drain and cannot be forced high.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	$I_{OL} = n$ mA		0.4	V

10.2.10 Exceptions

1. All pins are back-drive protected, except for the output pins with PCI Buffer Type.
2. The following pins have a static pull-up resistor and therefore may have input leakage current (when $V_{IN} = V_{SS}$) of about (-)160µA: $\overline{ACK}$, $\overline{AFD}$_$\overline{DSTRB}$, $\overline{ERR}$, GPIO40-47, GPIO30-34, GPIO20-27, GPIO16-17, GPIO10-14, GPIO00-07, $\overline{INIT}$, P12, P16, P17, PE, $\overline{SLIN}$_ASTRB, $\overline{STB}$_WRITE
3. The following pins have a static pull-down resistor and therefore may have input leakage current (when $V_{IN} = V_{DD}$) of about 130µA: BUSY_$\overline{WAIT}$, PE, SLCT
4. Output from SLCT, BUSY_$\overline{WAIT}$ (and PE if bit 2 of PP Confg0 Register is “0”) is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is level 2. External 4.7 KW pull-up resistors should be used.
5. Output from $\overline{ACK}$, $\overline{ERR}$ (and PE if bit 2 of PP Confg0 Register is set to 1) is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based FIFO and bit 4 of the Control2 parallel port register is set to 1. Otherwise, output from these signals is level 2. External 4.7 KW pull-up resistors should be used.
6. Output from $\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$ is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based (FIFO). Otherwise, output from these signals is level 2. External 4.7 KΩ pull-up resistors should be used.
7. Output from PD7-0 is open-drain in all SPP modes, except in SPP Compatible mode when the setup mode is ECP-based (FIFO) and bit 4 of the Control2 parallel port register is 1. Otherwise, output from these signals is Level 2. External 4.7 KΩ pull-up resistors should be used.
8. I_{OH} is valid for a GPIO pin only when it is not configured as open-drain.
9. P12, P16 and P17 are driven high for about 100 ns after a low-to-high transition, during which it is capable of sourcing 2 mA.

10.3 INTERNAL RESISTORS

10.3.1 Pull-Up Resistor

Symbol: PU_{nn}.

Symbol	Parameter	Conditions	Typical	Min	Max	Unit
R_{PU}	Pull-up equivalent resistance	V_{DD} = 3.3V	*nn*	*nn*-30%	*nn*+30%	KΩ

10.3.2 Pull-Down Resistor

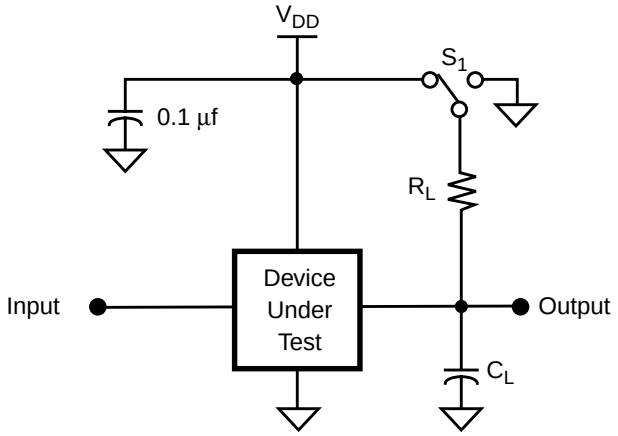
Symbol: PD_{nn}.

Symbol	Parameter	Conditions	Typical	Min	Max	Unit
R_{PD}	Pull-down equivalent resistance	V_{DD} = 3.3V	*nn*	*nn*-30%	*nn*+30%	KΩ

10.4 AC ELECTRICAL CHARACTERISTICS

10.4.1 AC Test Conditions

Load Circuit (Notes 1, 2, 3)



AC Testing Input, Output Waveform

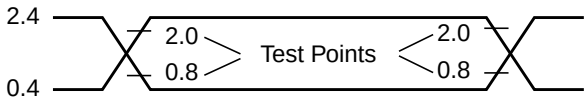


Figure 29. AC Test Conditions, T_A = 0 °C to 70 °C, V_{DD} = 5.0 V ±10%

Notes:

1. C_L = 100 pF for all output except O_{PCI}, and CL= 50pF for outputs of type O_{PCI}, this includes jig and scope capacitance.
2. S_1 = Open for push-pull output pins.
   S_1 = V_{DD} for high impedance to active low and active low to high impedance measurements.
   S_1 = GND for high impedance to active high and active high to high impedance measurements.
   R_L = 1.0KΩ for µP interface pins.
3. For the FDC open-drive interface pins, S_1 = V_{DD} and R_L = 150Ω.

10.4.2 Clock Timing

Symbol	Parameter	48 MHz		
		Min	Max	Unit
t_{CH}	Clock High Pulse Width Note 1.	8.4		ns
t_{CL}	Clock Low Pulse Width Note 1.	8.4		ns
t_{CP}	Clock Period Note 1.	20	21.5	ns

Note 1. Not tested. Guaranteed by design.

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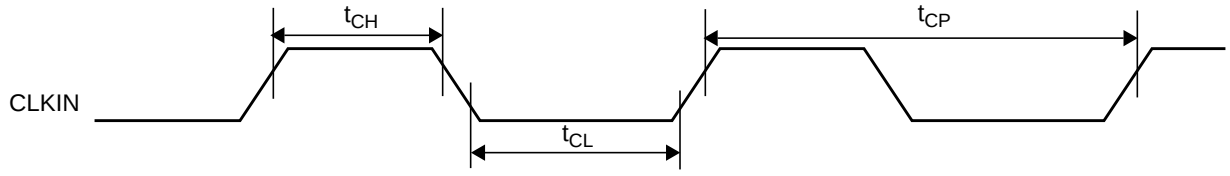


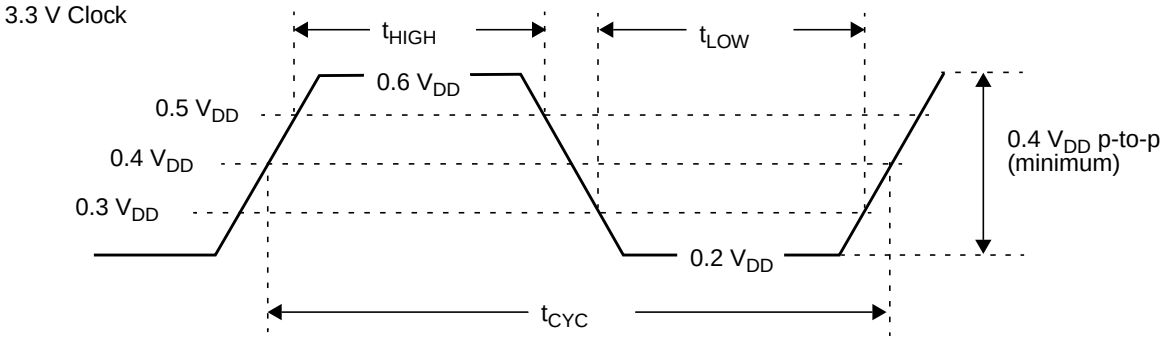
10.4.3 LCLK and $\overline{\text{LRESET}}$

Symbol	Parameter	Min	Max	Units
t_{CYC} Note 1.	LCLK Cycle Time	30		ns
t_{HIGH}	LCLK High Time	11		ns
t_{LOW}	LCLK Low Time	11		ns
-	LCLK Slew Rate Note 2.	1	4	V/ns
-	$\overline{\text{LRESET}}$ Slew Rate Note 3.	50		mV/ns

Note 1. The PCI may have any clock frequency between nominal DC and 33 MHz. Device operational parameters at frequencies under 16 MHz may be guaranteed by design rather than by testing. The clock frequency may be changed at any time during the operation of the system as long as the clock edges remain “clean” (monotonic) and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state.

Note 2. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock wavering as shown below.

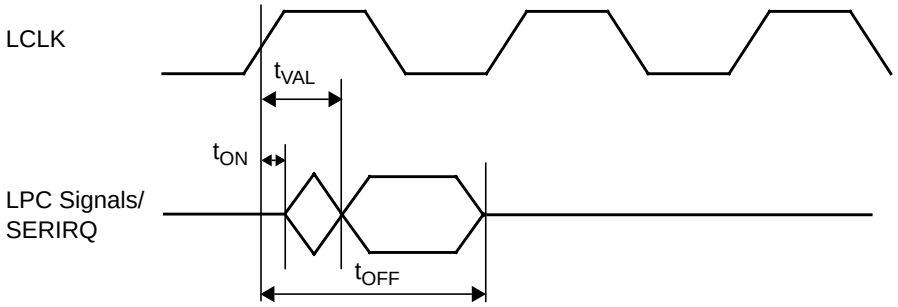
Note 3. The minimum $\overline{\text{LRESET}}$ slew rate applies only to the rising (de-assertion) edge of the reset signal, and ensures that system noise cannot render an otherwise a monotonic signal to appear to bounce in the switching range.



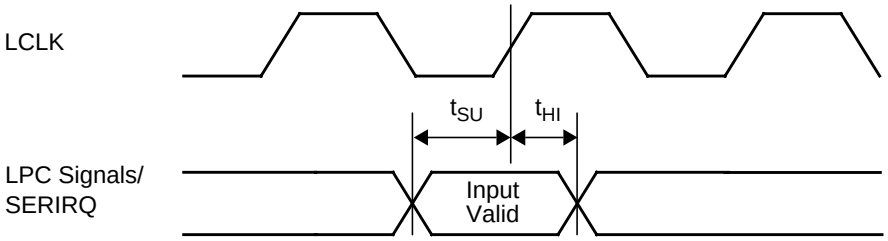
10.4.4 LPC and SERIRQ Signals

Symbol	Figure	Description	Reference Conditions	Min	Max	Unit
t_{VAL}	Output	Output Valid Delay	After RE CLK		11	ns
t_{ON}	Output	Float to Active Delay	After RE CLK	2		ns
t_{OFF}	Output	Active to Float Delay	After RE CLK		28	ns
t_{SU}	Input	Input Setup Time	Before RE CLK	7		ns
t_{HI}	Input	Input Hold Time	After RE CLK	0		ns

Output



Input



10.4.5 Serial Port, Sharp-IR, SIR and Consumer Remote Control Timing

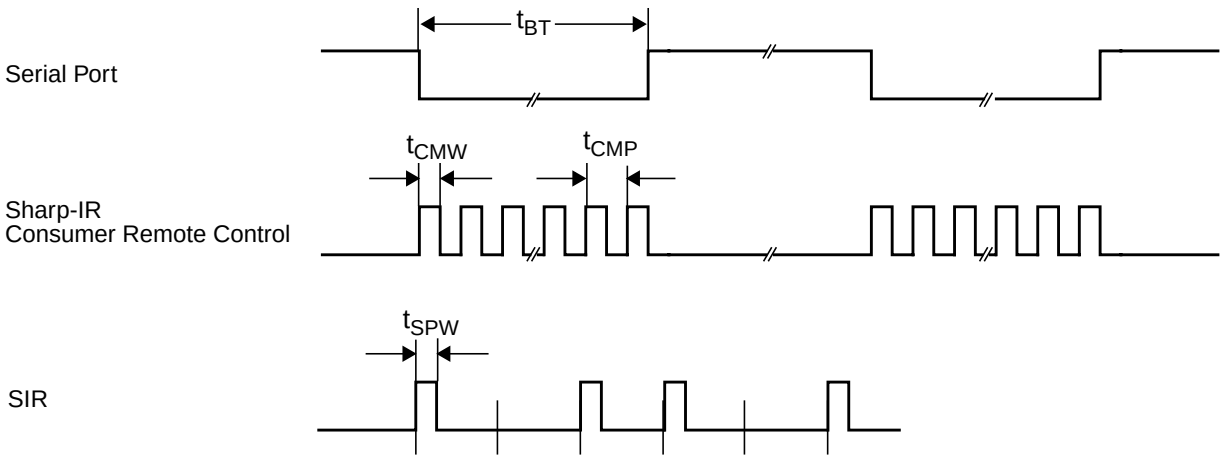
Symbol	Parameter	Conditions	Min	Max	Unit
t_{BT}	Single Bit Time in Serial Port and Sharp-IR	Transmitter	$t_{BTN} - 25$ Note 1.	$t_{BTN} + 25$	ns
		Receiver	$t_{BTN} - 2\%$	$t_{BTN} + 2\%$	ns
t_{CMW}	Modulation Signal Pulse Width in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CWN} - 25$ Note 2.	$t_{CWN} + 25$	ns
		Receiver	500		ns
t_{CMP}	Modulation Signal Period in Sharp-IR and Consumer Remote Control	Transmitter	$t_{CPN} - 25$ Note 3.	$t_{CPN} + 25$	ns
		Receiver	t_{MMIN} Note 4.	t_{MMAX} Note 4.	ns
t_{SPW}	SIR Signal Pulse Width	Transmitter, Variable	$(3/16) \times t_{BTN} - 15$ Note 1.	$(3/16) \times t_{BTN} + 15$ Note 1.	ns
		Transmitter, Fixed	1.48	1.78	µs
		Receiver	1		µs
S_{DRT}	SIR Data Rate Tolerance. % of Nominal Data Rate.	Transmitter		± 0.87%	
		Receiver		± 2.0%	
t_{SJT}	SIR Leading Edge Jitter. % of Nominal Bit Duration.	Transmitter		± 2.5%	
		Receiver		± 6.5%	

Note 1. t_{BTN} is the nominal bit time in Serial Port, Sharp-IR, SIR and Consumer Remote Control modes. It is determined by the setting of the Baud Generator Divisor registers

Note 2. t_{CWN} is the nominal pulse width of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCPW field (bits 7-5) of the IRTXMC registerand the TXHSC bit (bit 2) of the RCCFG register

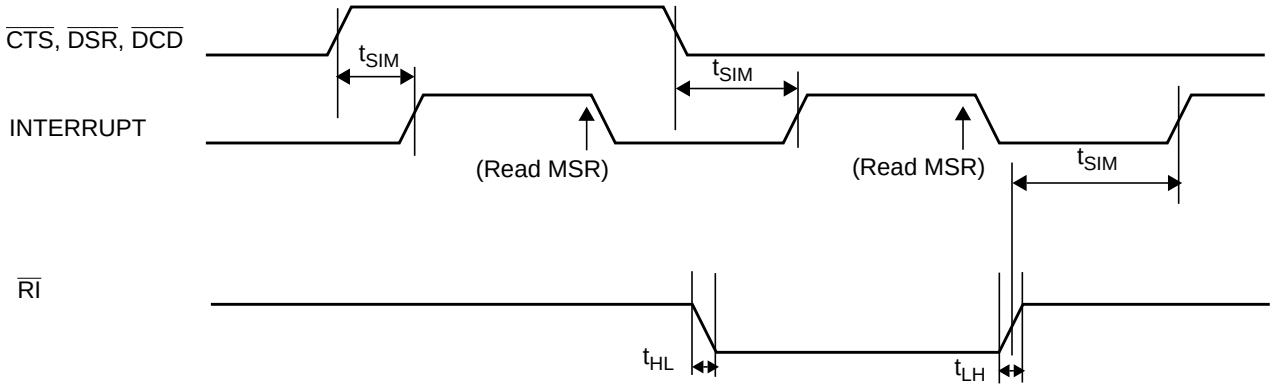
Note 3. t_{CPN} is the nominal period of the modulation signal for Sharp-IR and Consumer Remote Control modes. It is determined by the MCFR field (bits 4-0) of the IRTXMC registerand the TXHSC bit (bit 2) of the RCCFG register.

Note 4. t_{MMIN} and t_{MMAX} define the time range within which the period of the incoming subcarrier signal has to fall in order for the signal to be accepted by the receiver. These time values are determined by the contents of the IRRXDC register and the setting of the RXHSC bit (bit 5) of the RCCFG register



10.4.6 Modem Control Timing

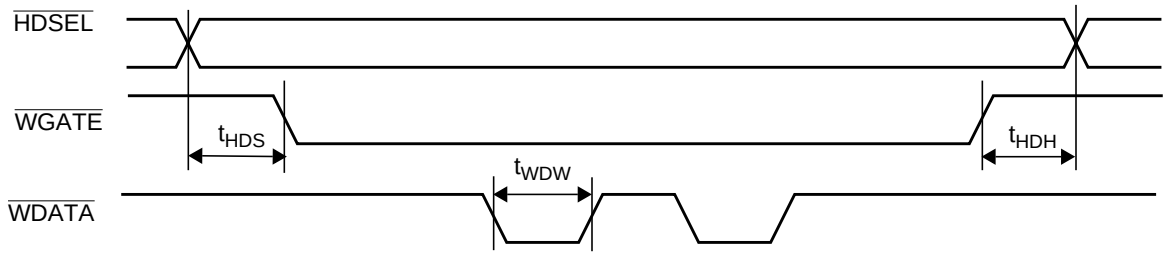
Symbol	Parameter	Min	Max	Unit
t_{HL}	$\overline{RI2,1}$ High to Low Transition	10		ns
t_{LH}	$\overline{RI2,1}$ Low to High Transition	10		ns
t_{SIM}	Delay to Set IRQ from Modem Input		40	ns



10.4.7 FDC Write Data Timing

Symbol	Parameter	Min	Max	Unit
t_{HDH}	$\overline{HDSEL}$ Hold from $\overline{WGATE}$ Inactive[Note 1.]	100		µs
t_{HDS}	$\overline{HDSEL}$ Setup to $\overline{WGATE}$ Active[Note 1.]	100		µs
t_{WDW}	Write Data Pulse Width	See t_{DRP}, t_{ICP} and t_{WDW} values in table below		

Note 1. Not tested. Guaranteed by design.



t_{DRP} t_{ICP} t_{WDW} Values

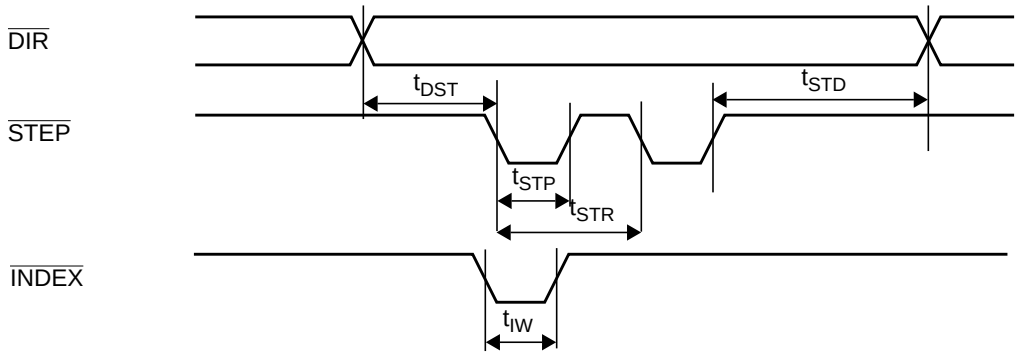
Data Rate	t_{DRP}	t_{ICP}	t_{ICP} Nominal	t_{WDW}	t_{WDW} Minimum	Unit
1 Mbps	1000	6 x t_{CP}[Note 1.]	125	2 x t_{ICP}	250	ns
500 Kbps	2000	6 x t_{CP}[Note 1.]	125	2 x t_{ICP}	250	ns
300 Kbps	3333	10 x t_{CP}[Note 1.]	208	2 x t_{ICP}	375	ns
250 Kbps	4000	12 x t_{CP}[Note 1.]	250	2 x t_{ICP}	500	ns

Note 1. t_{CP} is the clock period defined in the *LCLK and LRESET* section of this chapter.

10.4.8 FDC Drive Control Timing

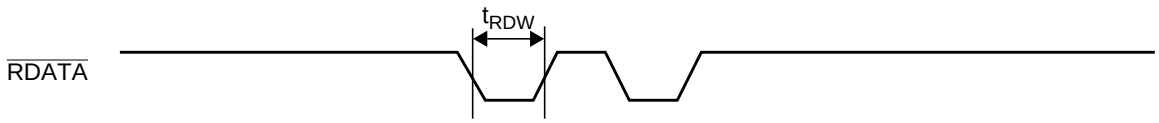
Symbol	Parameter	Min	Max	Unit
t_{DST}	$\overline{DIR}$ Setup to $\overline{STEP}$ Active[Note 1.]	6		µs
t_{IW}	Index Pulse Width	100		ns
t_{STD}	$\overline{DIR}$ Hold from $\overline{STEP}$ Inactive	t_{STR}		ms
t_{STP}	$\overline{STEP}$ Active High Pulse Width[Note 1.]	8		µs
t_{STR}	$\overline{STEP}$ Rate Time[Note 1.]	0.5		ms

Note 1. Not tested. Guaranteed by design.



10.4.9 FDC Read Data Timing

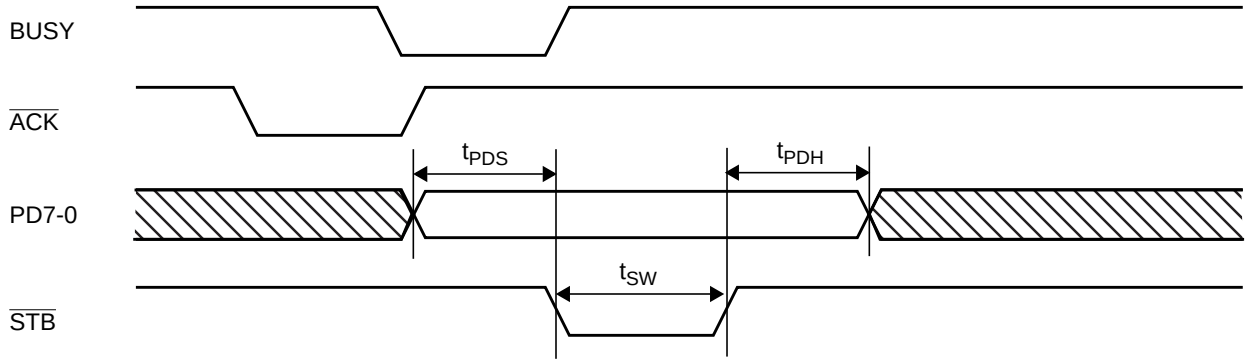
Symbol	Parameter	Min	Max	Unit
t_{RDW}	Read Data Pulse Width	50		ns



10.4.10 Standard Parallel Port Timing

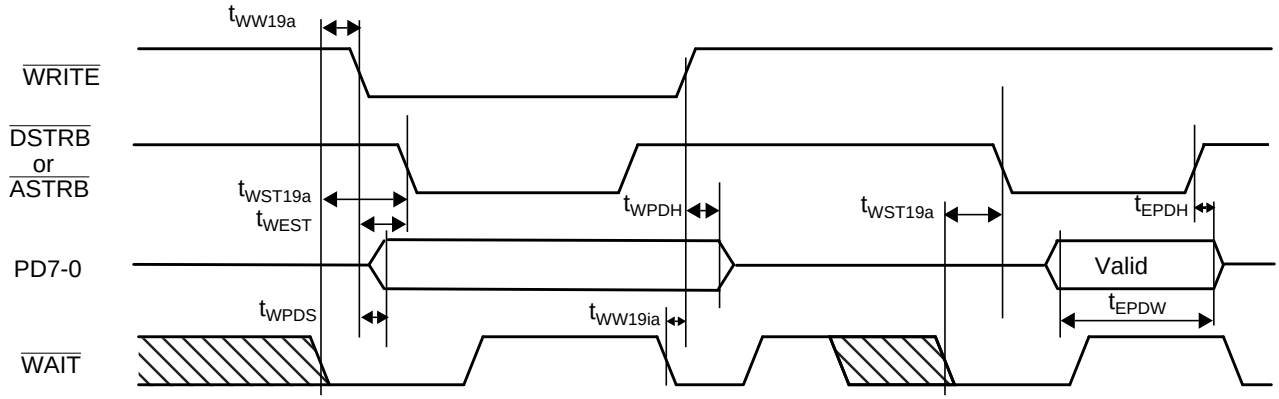
Symbol	Parameter	Conditions	Typ	Max	Unit
t_{PDH}	Port Data Hold	These times are system dependent and are therefore not tested.	500		ns
t_{PDS}	Port Data Setup	These times are system dependent and are therefore not tested.	500		ns
t_{SW}	Strobe Width	These times are system dependent and are therefore not tested.	500		ns

Typical Data Exchange



10.4.11 Enhanced Parallel Port Timing

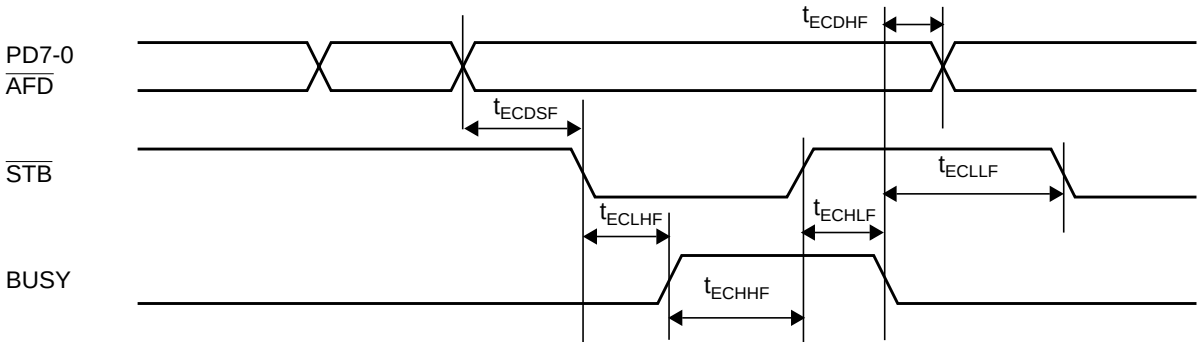
Symbol	Parameter	Min	Max	EPP 1.7	EPP 1.9	Unit
t_{WW19a}	$\overline{WRITE}$ Active from $\overline{WAIT}$ Low		45		✔	ns
t_{WW19ia}	$\overline{WRITE}$ Inactive from $\overline{WAIT}$ Low		45		✔	ns
t_{WST19a}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active from $\overline{WAIT}$ Low		65		✔	ns
t_{WEST}	$\overline{DSTRB}$ or $\overline{ASTRB}$ Active after $\overline{WRITE}$ Active	10		✔	✔	ns
t_{WPDH}	PD7-0 Hold after $\overline{WRITE}$ Inactive	0		✔	✔	ns
t_{WPDS}	PD7-0 Valid after $\overline{WRITE}$ Active		15	✔	✔	ns
t_{EPDW}	PD7-0 Valid Width	80		✔	✔	ns
t_{EPDH}	PD7-0 Hold after $\overline{DSTRB}$ or $\overline{ASTRB}$ Inactive	0		✔	✔	ns



10.4.12 Extended Capabilities Port (ECP) Timing

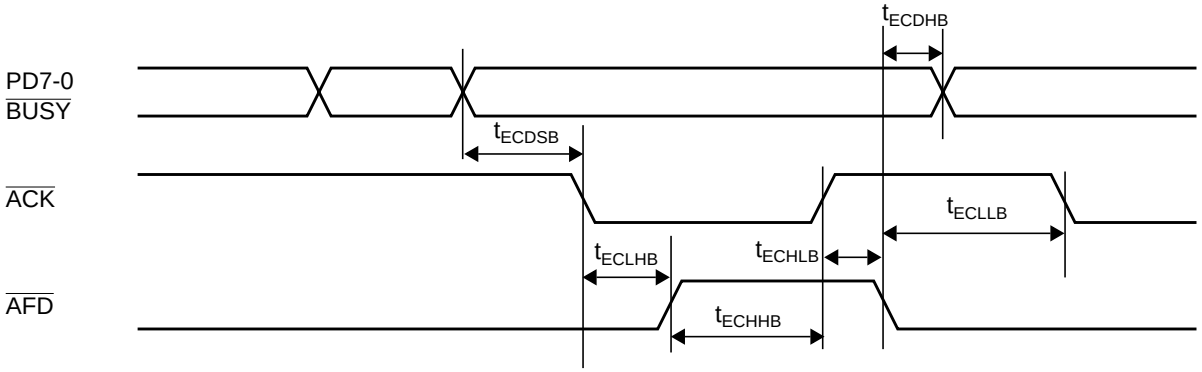
Forward Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSF}	Data Setup before $\overline{STB}$ Active	0		ns
t_{ECDHF}	Data Hold after BUSY Inactive	0		ns
t_{ECLHF}	BUSY Active after $\overline{STB}$ Active	75		ns
t_{ECHHF}	$\overline{STB}$ Inactive after BUSY Active	0	1	s
t_{ECHLF}	BUSY Inactive after $\overline{STB}$ Active	0	35	ms
t_{ECLLF}	$\overline{STB}$ Active after BUSY Inactive	0		ns



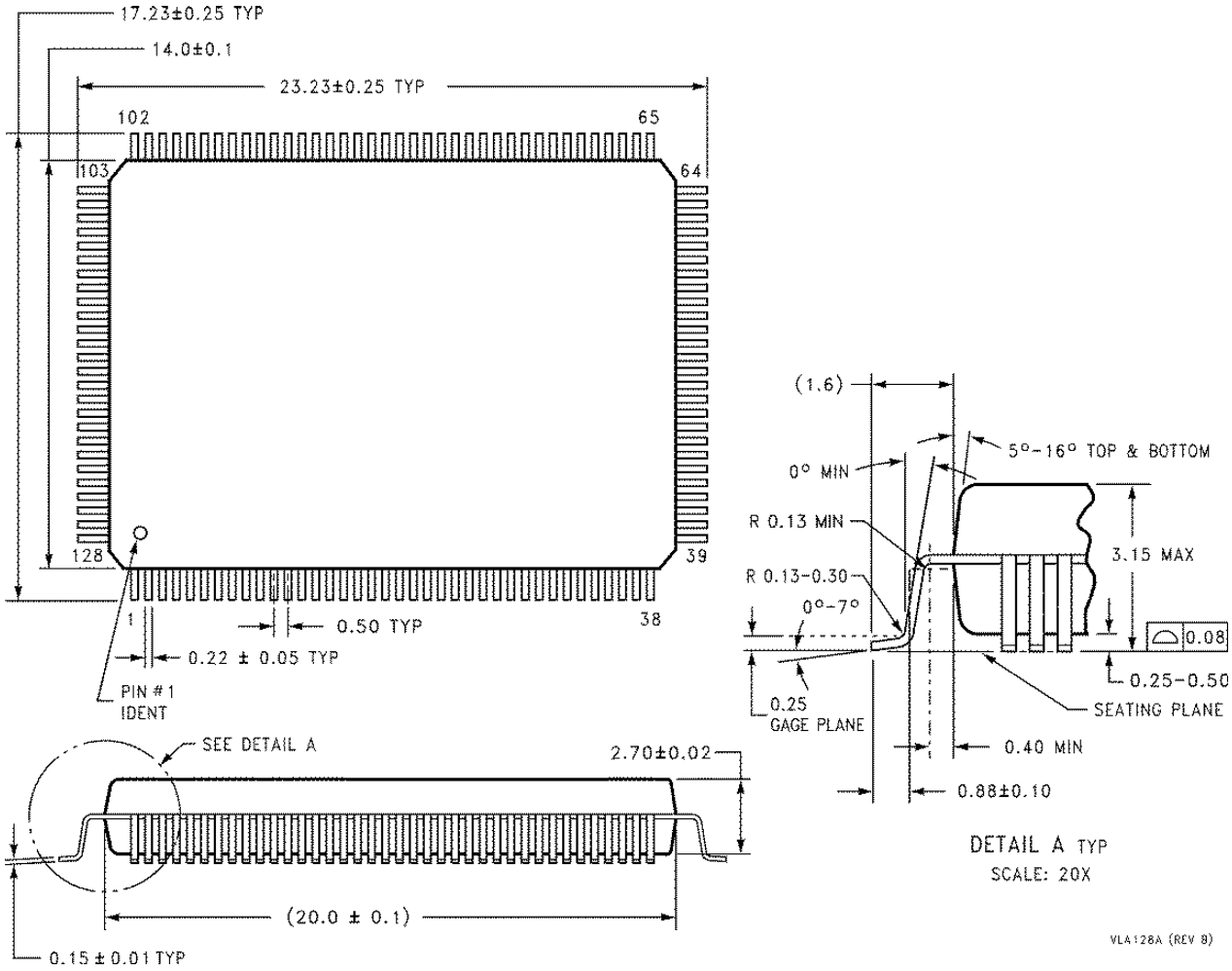
Reverse Mode

Symbol	Parameter	Min	Max	Unit
t_{ECDSR}	Data Setup before $\overline{ACK}$ Active	0		ns
t_{ECDHR}	Data Hold after $\overline{AFD}$ Active	0		ns
t_{ECLHR}	$\overline{AFD}$ Inactive after $\overline{ACK}$ Active	75		ns
t_{ECHHR}	$\overline{ACK}$ Inactive after $\overline{AFD}$ Inactive	0	35	ms
t_{ECHLR}	$\overline{AFD}$ Active after $\overline{ACK}$ Inactive	0	1	s
t_{ECLLR}	$\overline{ACK}$ Active after $\overline{AFD}$ Active	0		ns



Physical Dimensions

All dimensions are in millimeters.



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