National Semiconductor

MILITARY DATA SHEET

MNDS26LS31M-X REV 0A0

Original Creation Date: 01/24/96
Last Update Date: 11/15/96
Last Major Revision Date: 01/24/96

QUAD HIGH SPEED DIFFERENTIAL LINE DRIVER

General Description

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

The DS26LS31 features a power up/down protection circuit which keeps the output in a high impedance state (TRI-STATE) during power up or down preventing erroneous glitches on the transmission lines.

Industry Part Number

DS26LS31

NS Part Numbers

DS26LS31ME/883
DS26LS31MJ/883
DS26LS31MW/883

Prime Die

DS26LS31

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Operation from Single 5V Supply
- Outputs Won't Load Line When Vcc=0V
- Four Line Drivers in One Package For Maximum Package Density
- Output Short-Circuit Protection
- Complementary Outputs
- Meets the requirements of EIA Standard RS-422
- Pin Compatible with AM26LS31
- Glitch Free Power Up/Down

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5.5V
Output Voltage (Power OFF)	-0.25 to 6V
Maximum Power Dissipation @ 25 C (Note 2)	
Cavity Package	1400mW
LCC Package	1600mW
Flat Pack Package	850mW

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.
Note 2: Derate CDip = 11.5mW/C, CLCC = 13.0mW/C, CerPak = 7.4mW/C above 25C.

Recommended Operating Conditions

Supply Voltage, Vcc	4.5V to 5.5V
Temperature, TA	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	Logical "1" Input Voltage		1, 2		2		V	1, 2, 3
Vil	Logical "0" Input Voltage		1, 2			.8	V	1, 2, 3
Voh	Logical "1" Output Voltage	Vcc= 4.5V, Ioh= -20mA	2		2.5		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc= 4.5V, Iol= 20mA	2			.5	V	1, 2, 3
Iih	Logical "1" Input Current	Vcc= 5.5V, Vin=2.7V	2			20	uA	1, 2, 3
Iil	Logical "0" Input Current	Vcc= 5.5V, Vin= .4V	2			-200	uA	1, 2, 3
Ii	Input Reverse Current	Vcc=5.5V, Vin=7V	2			.1	mA	1, 2, 3
Io	TRI-STATE Output Current	Vcc=5.5V, Vo= .5V	2			-20	uA	1, 2, 3
		Vcc=5.5V, Vo=2.5V	2			20	uA	1, 2, 3
Vic	Input Clamp Voltage	Vcc=4.5V, Iin= -18mA	2			-1.5	V	1, 2, 3
Ios(min)	Output Short Circuit Current	Vcc=5.5V	2		-30		mA	1, 2, 3
Ios(max)	Output Short Circuit Current	Vcc=5.5V	2			-150	mA	1, 2, 3
Icc	Power Supply Current	Vcc=5.5V, All Outputs Disabled or Active	2			60	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: PROPAGATION DELAY TIME:

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc=5V, Cl=50pF or equivalent impedance provided by diode load.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH	Input to Output		2, 3			15	nS	9
			2, 3			30	nS	10, 11
tPHL	Input to Output		2, 3			15	nS	9
			2, 3			30	nS	10, 11
Skew	Output to Output		2, 3			6	nS	9
			2, 3			9	nS	10, 11
tLZ	Enable Time	S2 Open, Enable	2, 3			35	nS	9
			2, 3			53	nS	10, 11
		S2 Open, /Enable	2, 3			35	nS	9
			2, 3			53	nS	10, 11
tHZ	Enable Time	S1 Open, Enable	2, 3			25	nS	9
			2, 3			45	nS	10, 11
		S1 Open, /Enable	2, 3			25	nS	9
			2, 3			45	nS	10, 11
tZL	Disable Time	S2 Open, Enable	2, 3			30	nS	9
			2, 3			68	nS	10, 11
		S2 Open, /Enable	2, 3			30	nS	9
			2, 3			68	nS	10, 11
tZH	Disable Time	S1 Open, Enable	2, 3			30	nS	9
			2, 3			60	nS	10, 11
		S1 Open, /Enable	2, 3			30	nS	9
			2, 3			60	nS	10, 11

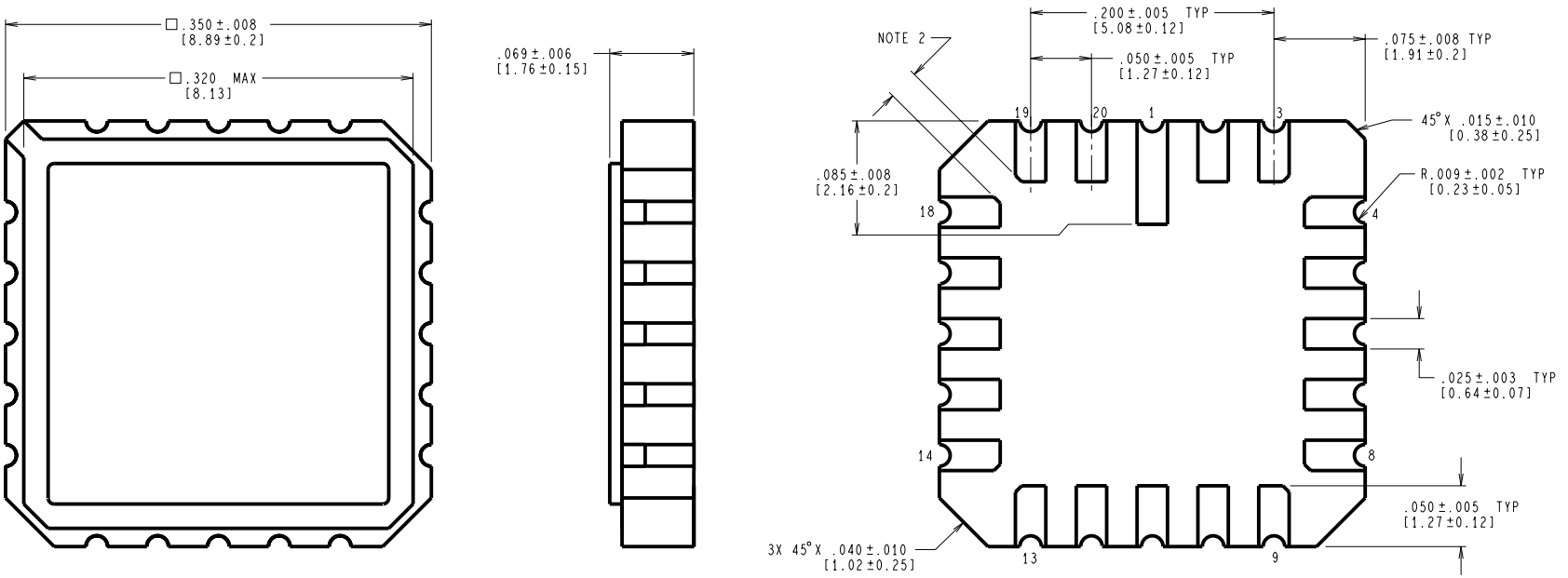
Note 1: Parameter tested go-no-go only.
Note 2: Subgroups 1,2 and 9,10: Power dissipation must be externally controlled at elevated temperatures.
Note 3: SBGRP 10 and 11 guaranteed but not tested.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LDLESS CHIP CARRIER, TYPE C 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
W16ARL	CERPAC (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION
INCH
[MM]

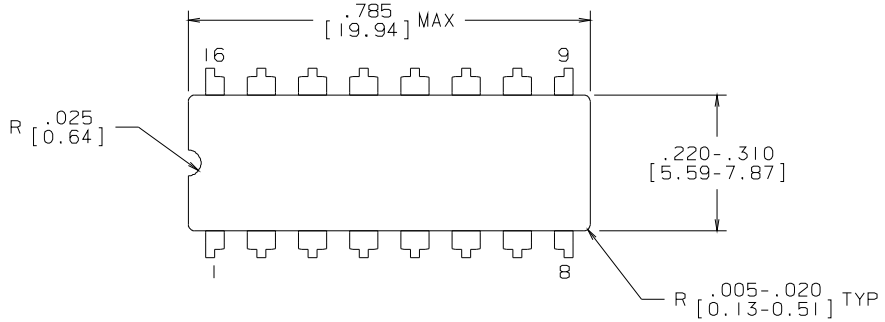
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

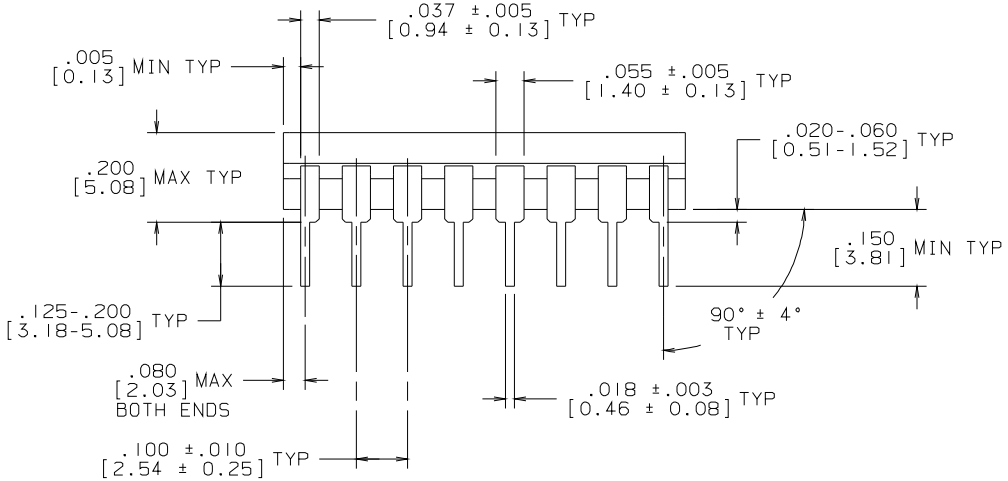
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

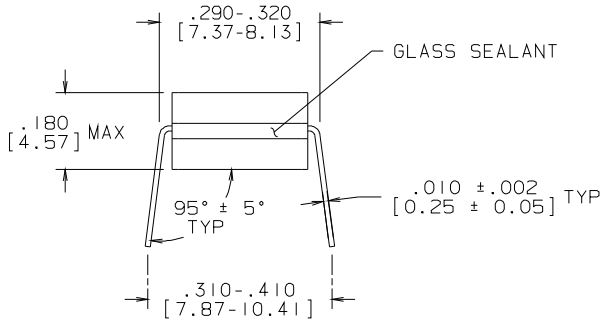
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

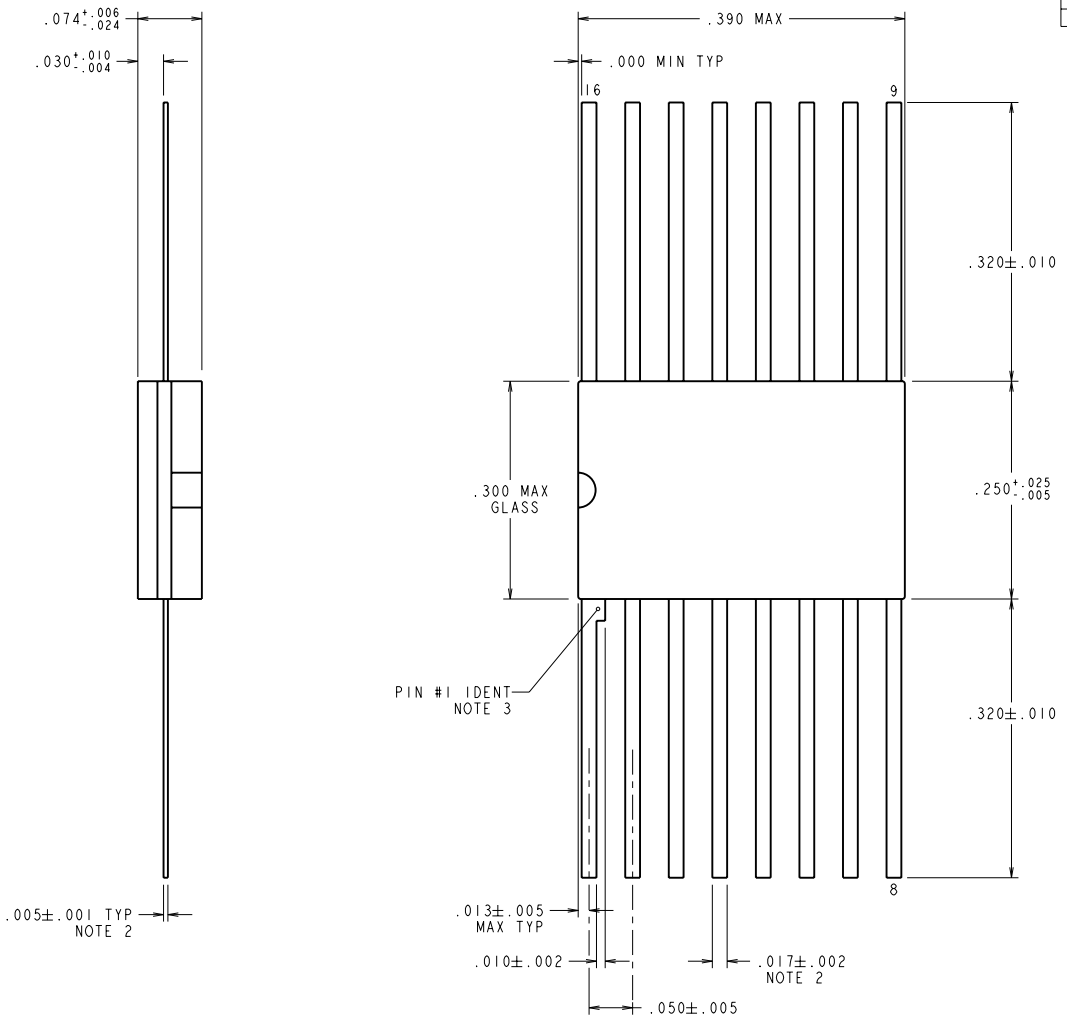
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-092, VARIATION AC, DATED 04/89.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

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2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD

PROJECTION

INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING | SHEET 1 of 1