

# LMX2377U

## PLLatinum™ Ultra Low Power Dual Frequency Synthesizer for RF Personal Communications

### 2.5 GHz/1.2 GHz

#### General Description

The LMX2377U device is a high performance frequency synthesizer with integrated dual modulus prescalers. The LMX2377U device is designed for use as a local oscillator for the first and second RF of a dual conversion radio transceiver.

A 16/17 or a 32/33 prescale ratio can be selected for the Main synthesizer. An 8/9 or a 16/17 prescale ratio can be selected for the Aux synthesizer. Using a proprietary digital phase lock technique, the LMX2377U device generates very stable, low noise control signals for UHF and VHF voltage controlled oscillators. Both the Main and Aux synthesizers include a two-level programmable charge pump. The Main synthesizer has dedicated Fastlock circuitry.

Serial data is transferred to the devices via a three-wire interface (Data, LE, Clock). The low voltage logic interface allows connection to 1.8V devices. Supply voltages from 2.7V to 5.5V are supported. The LMX2377U features ultra low current consumption, typically 3.5 mA at 3.0V.

The LMX2377U devices are available in 20-Pin TSSOP, 24-Pin CSP, and 20-Pin UTCSP surface mount plastic packages.

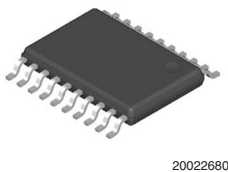
#### Features

- Ultra Low Current Consumption
- Upgrade and Compatible to the LMX2370
- 2.7V to 5.5V Operation
- 1.8V to 5.0V MICROWIRE Logic Interface
- Selectable Synchronous or Asynchronous Powerdown Mode:
  - $I_{CC-PWDN} = 1 \mu A$  typical
- Selectable Dual Modulus Prescaler:
  - Main: 16/17 or 32/33
  - Aux: 8/9 or 16/17
- Selectable Charge Pump TRI-STATE® Mode
- Programmable Charge Pump Current Levels
  - Main and Aux: 0.95 or 3.8 mA
- Selectable Fastlock™ Mode for the Main Synthesizer
- Open Drain Analog Lock Detect Output
- Available in 20-Pin TSSOP, 24-Pin CSP, and 20-Pin UTCSP

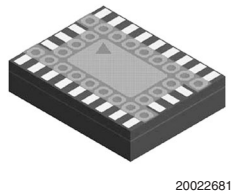
#### Applications

- Mobile Handsets (GSM, GPRS, W-CDMA, CDMA, PCS, AMPS, PDC, DCS)
- Cordless Handsets (DECT, DCT)
- Wireless Data
- Cable TV Tuners

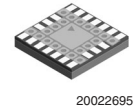
**Thin Shrink Small Outline Package (MTC20)**



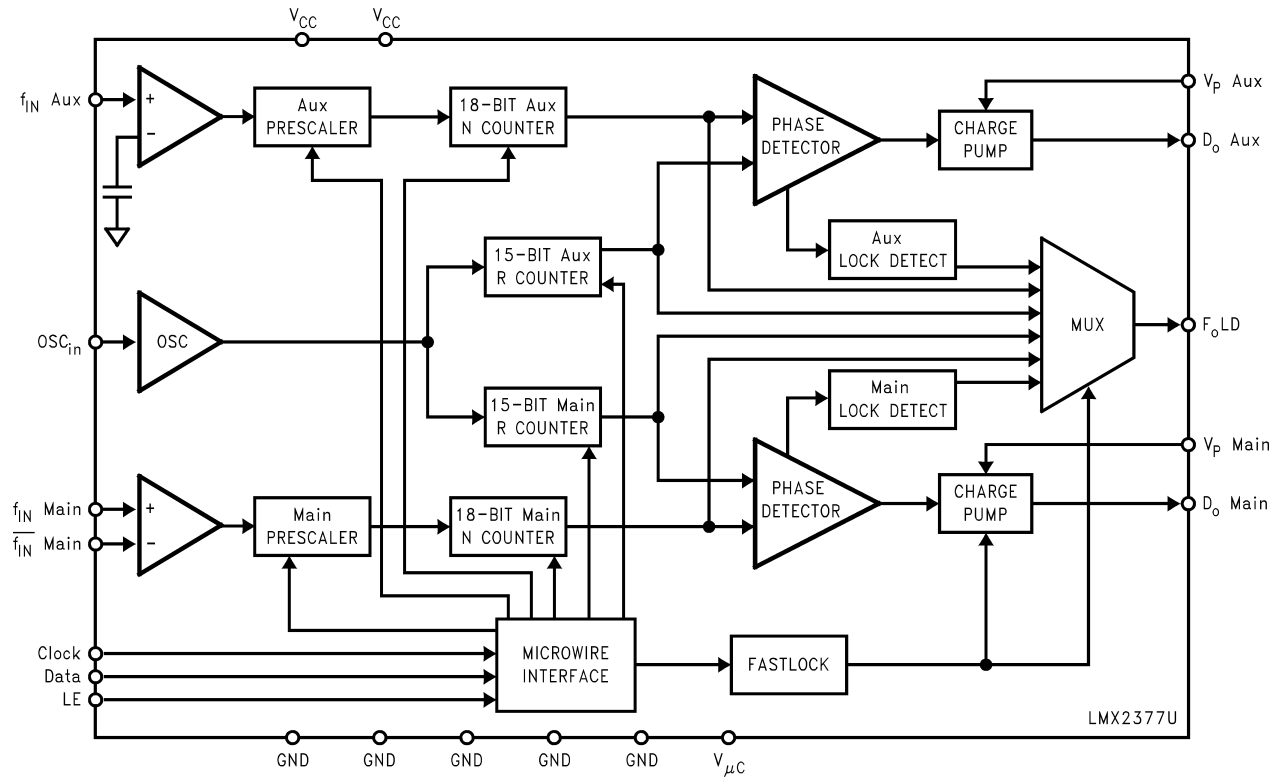
**Chip Scale Package (SLB24A)**



**Ultra Thin Chip Scale Package (SLE20A)**



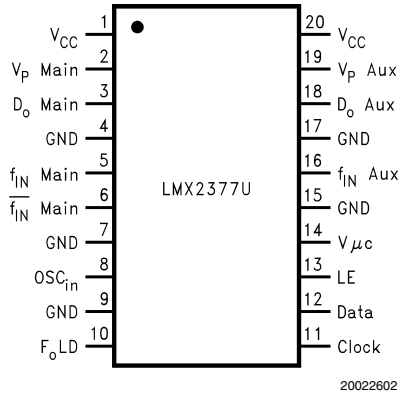
# Functional Block Diagram



20022604

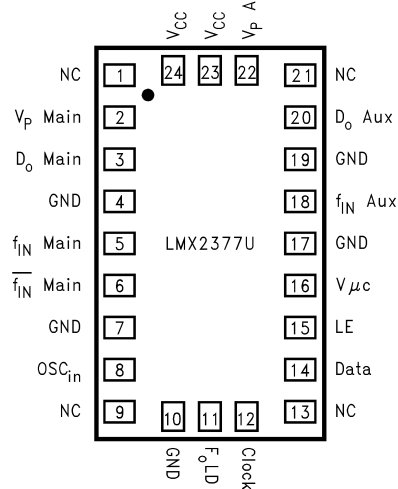
## Connection Diagrams

**Thin Shrink Small Outline Package (TM)  
(Top View)**



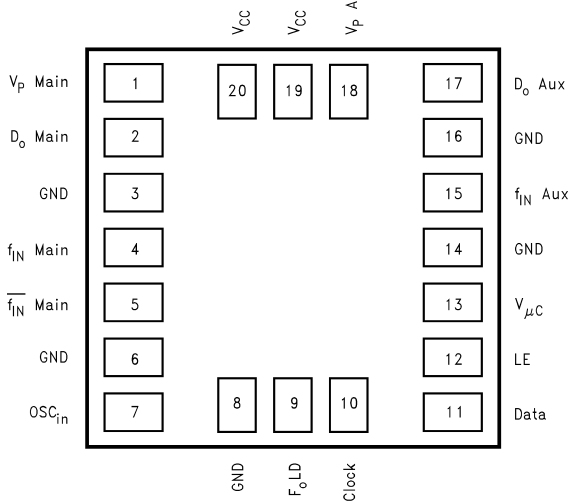
20022602

**Chip Scale Package (SLB)  
(Top View)**



20022603

**Ultra Thin Chip Scale Package (SLE)  
(Top View)**



20022696

## Pin Descriptions

Pin Name	Pin No. 20-Pin UTCSP	Pin No. 24-Pin CSP	Pin No. 20-Pin TSSOP	I/O	Description
V <sub>CC</sub>	20	24	1	—	Power supply bias for the Main PLL analog and digital circuits. V <sub>CC</sub> may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
V <sub>P</sub> Main	1	2	2	—	Main PLL charge pump power supply. Must be ≥ V <sub>CC</sub> .
D <sub>O</sub> Main	2	3	3	O	Main PLL charge pump output. The output is connected to the external loop filter, which drives the input of the VCO.
GND	3	4	4	—	Ground for the Main PLL digital circuitry.
f <sub>IN</sub> Main	4	5	5	I	Main PLL prescaler input. Small signal input from the VCO.

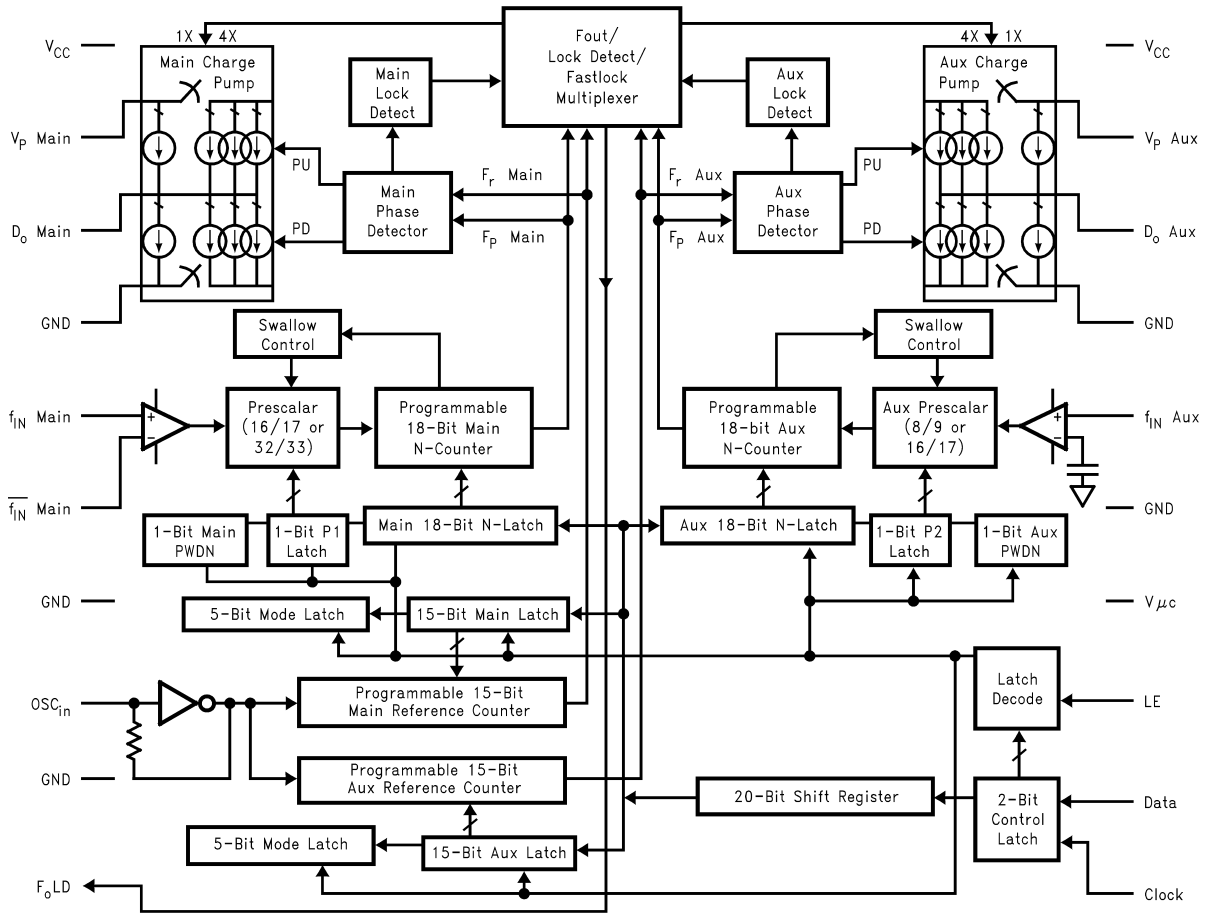
## Pin Descriptions (Continued)

Pin Name	Pin No. 20-Pin UTCSP	Pin No. 24-Pin CSP	Pin No. 20-Pin TSSOP	I/O	Description
$\overline{f_{IN}}$ Main	5	6	6	I	Main prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX2377U Main PLL can be driven differentially when the bypass capacitor is omitted.
GND	6	7	7	—	Ground for the Main PLL analog circuitry.
OSC <sub>in</sub>	7	8	8	I	Reference oscillator input. It has an approximate $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
GND	8	10	9	—	Ground for the Aux PLL digital circuitry, MICROWIRE, F <sub>o</sub> LD, and oscillator circuits.
F <sub>o</sub> LD	9	11	10	O	Programmable multiplexed output pin. Functions as a general purpose CMOS TRI-STATE output, Main/Aux PLL open drain analog lock detect output, N and R divider output or Fastlock output, which connects a parallel resistor to the external loop filter.
Clock	10	12	11	I	MICROWIRE Clock input. High impedance CMOS input. Data is clocked into the 22-bit shift register on the rising edge of Clock.
Data	11	14	12	I	MICROWIRE Data input. High impedance CMOS input. Binary serial data. The MSB of Data is shifted in first. The last two bits are the control bits.
LE	12	15	13	I	MICROWIRE Latch Enable input. High impedance CMOS input. When LE transitions HIGH, Data stored in the shift register is loaded into one of 4 internal control registers.
V <sub>μc</sub>	13	16	14	—	Power supply bias for the MICROWIRE circuitry. Must be $\leq V_{CC}$ . Typically connected to the same supply level as the microprocessor or baseband controller to enable programming at low voltages.
GND	14	17	15	—	Ground for the Aux PLL analog circuitry.
$f_{IN}$ Aux	15	18	16	I	Aux PLL prescaler input. Small signal input from the VCO.
GND	16	19	17	—	Ground for the Aux PLL digital circuitry, MICROWIRE, F <sub>o</sub> LD, and oscillator circuits.
D <sub>o</sub> Aux	17	20	18	O	Aux PLL charge pump output. the output is connected to an external loop filter, which drives the input of the VCO.
V <sub>P</sub> Aux	18	22	19	—	Aux PLL charge pump power supply. Must be $\geq V_{CC}$ .
V <sub>CC</sub>	19	23	20	—	Power supply bias for the Aux PLL analog and digital circuits, F <sub>o</sub> LD, and oscillator circuits. V <sub>CC</sub> may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
NC	—	1, 9, 13, 21	—	—	No Connect

## Ordering Information

Model	Temperature Range	Package Description	Packing	NS Package Number
LMX2377USLEX	-40°C to +85°C	Ultra Thin Chip Scale Package (UTCSP) Tape and Reel	2500 Units Per Reel	SLE20A
LMX2377USLBX	-40°C to +85°C	Chip Scale Package (CSP) Tape and Reel	2500 Units Per Reel	SLB24A
LMX2377UTM	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	73 Units Per Rail	MTC20
LMX2377UTMX	-40°C to +85°C	Thin Shrink Small Outline Package (TSSOP) Tape and Reel	2500 Units Per Reel	MTC20

# Detailed Block Diagram



20022608

**Notes:**

1.  $V_{CC}$  supplies power to the Main and Aux prescalers, Main and Aux feedback dividers, Main and Aux reference dividers, Main and Aux phase detectors, the  $OSC_{in}$  buffer, and  $F_0LD$  circuitry.
2.  $V_{\mu c}$  supplies power to the MICROWIRE circuitry.
3.  $V_P$  Main and  $V_P$  Aux supply power to the charge pumps. They can be run separately as long as  $V_P$  Main  $\geq V_{CC}$  and  $V_P$  Aux  $\geq V_{CC}$ .

**Absolute Maximum Ratings** (Notes 1,

2, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage

 $V_{CC}$  to GND -0.3V to +6.5V $V_P$  Main to GND -0.3V to +6.5V $V_P$  Aux to GND -0.3V to +6.5VVoltage on any pin to GND ( $V_I$ ) $V_I$  must be < +6.5V -0.3V to  $V_{CC}+0.3V$ Storage Temperature Range ( $T_S$ ) -65°C to +150°CLead Temperature (solder 4 s) ( $T_L$ ) +260°CTSSOP  $\theta_{JA}$  Thermal Impedance 114.5°C/WCSP  $\theta_{JA}$  Thermal Impedance 112°C/W**Recommended Operating****Conditions** (Note 1)

Power Supply Voltage

 $V_{CC}$  to GND +2.7V to +5.5V $V_P$  Main to GND  $V_{CC}$  to +5.5V $V_P$  Aux to GND  $V_{CC}$  to +5.5VOperating Temperature ( $T_A$ ) -40°C to +85°C

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, refer to the Electrical Characteristics section. The guaranteed specifications apply only for the conditions listed.

**Note 2:** This device is a high performance RF integrated circuit with an ESD rating <2 kV and is ESD sensitive. Handling and assembly of this device should only be done at ESD protected work stations.

**Note 3:** GND = 0V

**Electrical Characteristics**
 $V_{CC} = V_P \text{ Main} = V_P \text{ Aux} = V_{\mu c} = 3.0V, -40^\circ C \leq T_A \leq +85^\circ C$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
<b>I<sub>CC</sub> PARAMETERS</b>						
$I_{CC\text{Main} + \text{Aux}}$	Power Supply Current, Main + Aux Synthesizers	Clock, Data and LE = GND OSC <sub>in</sub> = GND PWDN Main Bit = 0 PWDN Aux Bit = 0		3.5	4.6	mA
$I_{CC\text{Main}}$	Power Supply Current, Main Synthesizer Only	Clock, Data and LE = GND OSC <sub>in</sub> = GND PWDN Main Bit = 0 PWDN Aux Bit = 1		2.3	3.0	mA
$I_{CC\text{Aux}}$	Power Supply Current, Aux Synthesizer Only	Clock, Data and LE = GND OSC <sub>in</sub> = GND PWDN Main Bit = 1 PWDN Aux Bit = 0		1.0	1.6	mA
$I_{CC\text{-PWDN}}$	Powerdown Current	Clock, Data and LE = GND OSC <sub>in</sub> = GND PWDN Main Bit = 1 PWDN Aux Bit = 1		1.0	10.0	μA
<b>MAIN SYNTHESIZER PARAMETERS</b>						
$f_{IN \text{ Main}}$	Main Operating Frequency		500		2500	MHz
$N_{\text{Main}}$	Main N Divider Range	Prescaler = 16/17 (Note 4)	48		131087	
		Prescaler = 32/33 (Note 4)	96		262143	
$R_{\text{Main}}$	Main R Divider Range		2		32767	
$F_{\phi\text{Main}}$	Main Phase Detector Frequency				10	MHz
$Pf_{IN \text{ Main}}$	Main Input Sensitivity	$2.7V \leq V_{CC} \leq 3.0V$ (Note 5)	-15		0	dBm
		$3.0V < V_{CC} \leq 5.5V$ (Note 5)	-10		0	dBm

**Electrical Characteristics** (Continued) $V_{CC} = V_P \text{ Main} = V_P \text{ Aux} = V_{\mu c} = 3.0V$ ,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
<b>MAIN SYNTHESIZER PARAMETERS</b>						
ID <sub>o</sub> Main SOURCE	Main Charge Pump Output Source Current	VD <sub>o</sub> Main = V <sub>P</sub> Main/2 ID <sub>o</sub> Main Bit = 0 (Note 6)		-0.95		mA
		VD <sub>o</sub> Main = V <sub>P</sub> Main/2 ID <sub>o</sub> Main Bit = 1 (Note 6)		-3.80		mA
ID <sub>o</sub> Main SINK	Main Charge Pump Output Sink Current	VD <sub>o</sub> Main = V <sub>P</sub> Main/2 ID <sub>o</sub> Main Bit = 0 (Note 6)		0.95		mA
		VD <sub>o</sub> Main = V <sub>P</sub> Main/2 ID <sub>o</sub> Main Bit = 1 (Note 6)		3.80		mA
ID <sub>o</sub> Main TRI-STATE	Main Charge Pump Output TRI-STATE Current	$0.5V \leq VD_o \text{ Main} \leq V_P \text{ Main} - 0.5V$ (Note 6)	-2.5		2.5	nA
ID <sub>o</sub> Main SINK Vs ID <sub>o</sub> Main SOURCE	Main Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch	VD <sub>o</sub> Main = V <sub>P</sub> Main/2 T <sub>A</sub> = 25°C (Note 7)		3	10	%
ID <sub>o</sub> Main Vs VD <sub>o</sub> Main	Main Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage	$0.5V \leq VD_o \text{ Main} \leq V_P \text{ Main} - 0.5V$ T <sub>A</sub> = 25°C (Note 7)		10	15	%
ID <sub>o</sub> Main Vs T <sub>A</sub>	Main Charge Pump Output Current Magnitude Variation Vs Temperature	VD <sub>o</sub> Main = V <sub>P</sub> Main/2 (Note 7)		10		%
<b>AUX SYNTHESIZER PARAMETERS</b>						
f <sub>IN</sub> Aux	Aux Operating Frequency		45		1200	MHz
N <sub>Aux</sub>	Aux N Divider Range	Prescaler = 8/9 (Note 4)	24		65559	
		Prescaler = 16/17 (Note 4)	48		131087	
R <sub>Aux</sub>	Aux R Divider Range		2		32767	
F <sub>φAux</sub>	Aux Phase Detector Frequency				10	MHz
Pf <sub>IN</sub> Aux	Aux Input Sensitivity	$2.7V \leq V_{CC} \leq 5.5V$ (Note 5)	-10		0	dBm



**Electrical Characteristics** (Continued)
 $V_{CC} = V_P \text{ Main} = V_P \text{ Aux} = V_{\mu C} = 3.0V$ ,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
<b>AUX SYNTHESIZER PARAMETERS</b>						
ID <sub>o</sub> Aux SOURCE	Aux Charge Pump Output Source Current	VD <sub>o</sub> Aux = V <sub>P</sub> Aux/2 ID <sub>o</sub> Aux Bit = 0 (Note 6)		-0.95		mA
		VD <sub>o</sub> Aux = V <sub>P</sub> Aux/2 ID <sub>o</sub> Aux Bit = 1 (Note 6)		-3.80		mA
ID <sub>o</sub> Aux SINK	Aux Charge Pump Output Sink Current	VD <sub>o</sub> Aux = V <sub>P</sub> Aux/2 ID <sub>o</sub> Aux Bit = 0 (Note 6)		0.95		mA
		VD <sub>o</sub> Aux = V <sub>P</sub> Aux/2 ID <sub>o</sub> Aux Bit = 1 (Note 6)		3.80		mA
ID <sub>o</sub> Aux TRI-STATE	Aux Charge Pump Output TRI-STATE Current	$0.5V \leq VD_o \text{ Aux} \leq V_P \text{ Aux} - 0.5V$ (Note 6)	-2.5		2.5	nA
ID <sub>o</sub> Aux SINK Vs ID <sub>o</sub> Aux SOURCE	Aux Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch	VD <sub>o</sub> Aux = V <sub>P</sub> Aux/2 T <sub>A</sub> = 25°C (Note 7)		3	10	%
ID <sub>o</sub> Aux Vs VD <sub>o</sub> Aux	Aux Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage	$0.5V \leq VD_o \text{ Aux} \leq V_P \text{ Aux} - 0.5V$ T <sub>A</sub> = 25°C (Note 7)		10	15	%
ID <sub>o</sub> Aux Vs T <sub>A</sub>	Aux Charge Pump Output Current Magnitude Variation Vs Temperature	VD <sub>o</sub> Aux = V <sub>P</sub> Aux/2 (Note 7)		10		%
<b>OSCILLATOR PARAMETERS</b>						
F <sub>OSC</sub>	Oscillator Operating Frequency		2		40	MHz
V <sub>OSC</sub>	Oscillator Sensitivity	(Note 8)	0.5		V <sub>CC</sub>	V <sub>PP</sub>
I <sub>OSC</sub>	Oscillator Input Current	V <sub>OSC</sub> = V <sub>CC</sub> = 5.5V			100	μA
		V <sub>OSC</sub> = 0V, V <sub>CC</sub> = 5.5V	-100			μA

**Electrical Characteristics** (Continued)
 $V_{CC} = V_P \text{ Main} = V_P \text{ Aux} = V_{\mu c} = 3.0V, -40^{\circ}C \leq T_A \leq +85^{\circ}C, \text{ unless otherwise specified}$ 

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
<b>DIGITAL INTERFACE (Data, LE, Clock, F<sub>o</sub>LD)</b>						
$V_{IH}$	High-Level Input Voltage	$1.72V \leq V_{\mu c} \leq 5.5V$	0.8 $V_{\mu c}$			V
$V_{IL}$	Low-Level Input Voltage	$1.72V \leq V_{\mu c} \leq 5.5V$			0.2 $V_{\mu c}$	V
$I_{IH}$	High-Level Input Current	$V_{IH} = V_{\mu c} = 5.5V$	-1.0		1.0	$\mu A$
$I_{IL}$	Low-Level Input Current	$V_{IL} = 0V, V_{\mu c} = 5.5V$	-1.0		1.0	$\mu A$
$V_{OH}$	High-Level Output Voltage	$I_{OH} = -500 \mu A$	$V_{CC} - 0.4$			V
$V_{OL}$	Low-Level Output Voltage	$I_{OL} = 500 \mu A$			0.4	V
<b>MICROWIRE INTERFACE</b>						
$t_{CS}$	Data to Clock Set Up Time	(Note 9)	50			ns
$t_{CH}$	Data to Clock Hold Time	(Note 9)	20			ns
$t_{CWH}$	Clock Pulse Width HIGH	(Note 9)	50			ns
$t_{CWL}$	Clock Pulse Width LOW	(Note 9)	50			ns
$t_{ES}$	Clock to Load Enable Set Up Time	(Note 9)	50			ns
$t_{EW}$	Latch Enable Pulse Width	(Note 9)	50			ns

**Electrical Characteristics** (Continued)
 $V_{CC} = V_P \text{ Main} = V_P \text{ Aux} = V_{\mu c} = 3.0V, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
<b>PHASE NOISE CHARACTERISTICS</b>						
$L_N(f)$ Main	Main Synthesizer Normalized Phase Noise Contribution (Note 10)	TCXO Reference Source $ID_o$ Main Bit = 1		-212.0		dBc/Hz
$L(f)$ Main	Main Synthesizer Single Side Band Phase Noise Measured	$f_{IN}$ Main = 2450 MHz $f$ = 1 kHz Offset $F_{\phi\text{Main}}$ = 200 kHz Loop Bandwidth = 7.5 kHz $N$ = 12250 $F_{OSC}$ = 10 MHz $V_{OSC}$ = 0.632 $V_{PP}$ $ID_o$ Main Bit = 1 PWDN Aux Bit = 1 $T_A$ = 25°C (Note 11)		-77.24		dBc/Hz
$L_N(f)$ Aux	Aux Synthesizer Normalized Phase Noise Contribution (Note 10)	TCXO Reference Source $ID_o$ Aux Bit = 1		-212.0		dBc/Hz
$L(f)$ Aux	Aux Synthesizer Single Side Band Phase Noise Measured	$f_{IN}$ Aux = 900 MHz $f$ = 1 kHz Offset $F_{\phi\text{Aux}}$ = 200 kHz Loop Bandwidth = 12 kHz $N$ = 4500 $F_{OSC}$ = 10 MHz $V_{OSC}$ = 0.632 $V_{PP}$ $ID_o$ Aux Bit = 1 PWDN Main Bit = 1 $T_A$ = 25°C (Note 11)		-85.94		dBc/Hz

**Note 4:** Some of the values in this range are illegal divide ratios ( $B < A$ ). To obtain continuous legal division, the Minimum Divide Ratio must be calculated. Use  $N \geq P * (P-1)$ , where P is the value of the prescaler selected.

**Note 5:** Refer to the LMX2377U  $f_{IN}$  Sensitivity Test Setup section

**Note 6:** Refer to the LMX2377U Charge Pump Test Setup section

**Note 7:** Refer to the Charge Pump Current Specification Definitions for details on how these measurements are made.

**Note 8:** Refer to the LMX2377U  $OSC_{in}$  Sensitivity Test Setup section

**Note 9:** Refer to the LMX2377U Serial Data Input Timing section

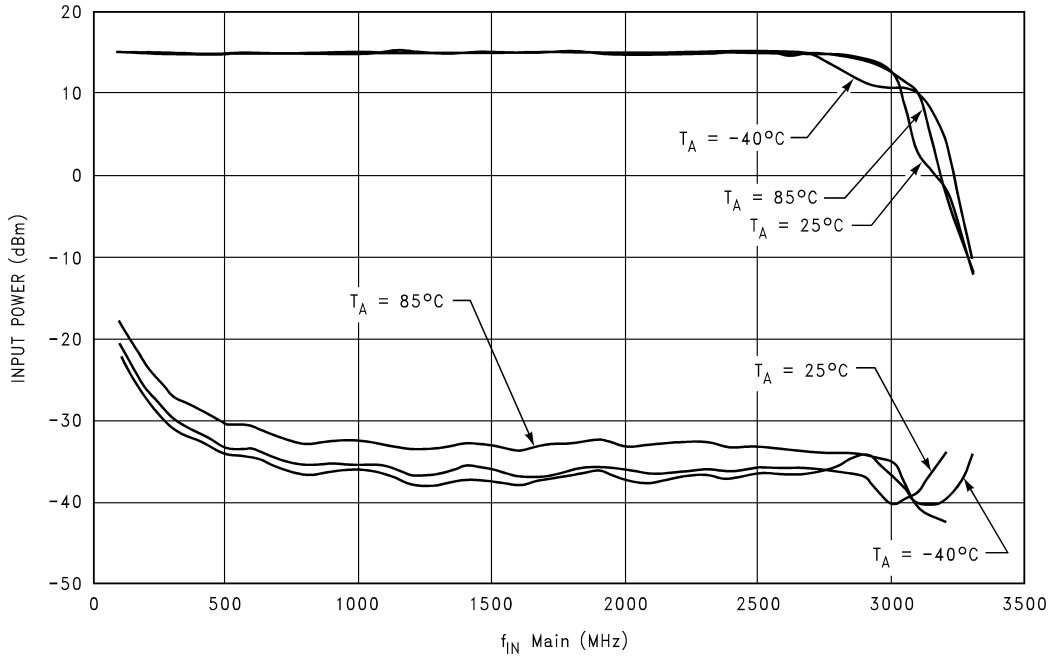
**Note 10:** Normalized Phase Noise Contribution is defined as :  $L_N(f) = L(f) - 20 \log(N) - 10 \log(F_\phi)$ , where  $L(f)$  is defined as the single side band phase noise measured at an offset frequency,  $f$ , in a 1 Hz bandwidth. The offset frequency,  $f$ , must be chosen sufficiently smaller than the PLL's loop bandwidth, yet large enough to avoid substantial phase noise contribution from the reference source.  $N$  is the value selected for the feedback divider and  $F_\phi$  is the Main/Aux phase detector comparison frequency..

**Note 11:** The synthesizer phase noise is measured with the LMX2370TMEB/LMX2370SLBEB/LMX2370SLEEB Evaluation boards and the HP8566B Spectrum Analyzer.

# Typical Performance Characteristics

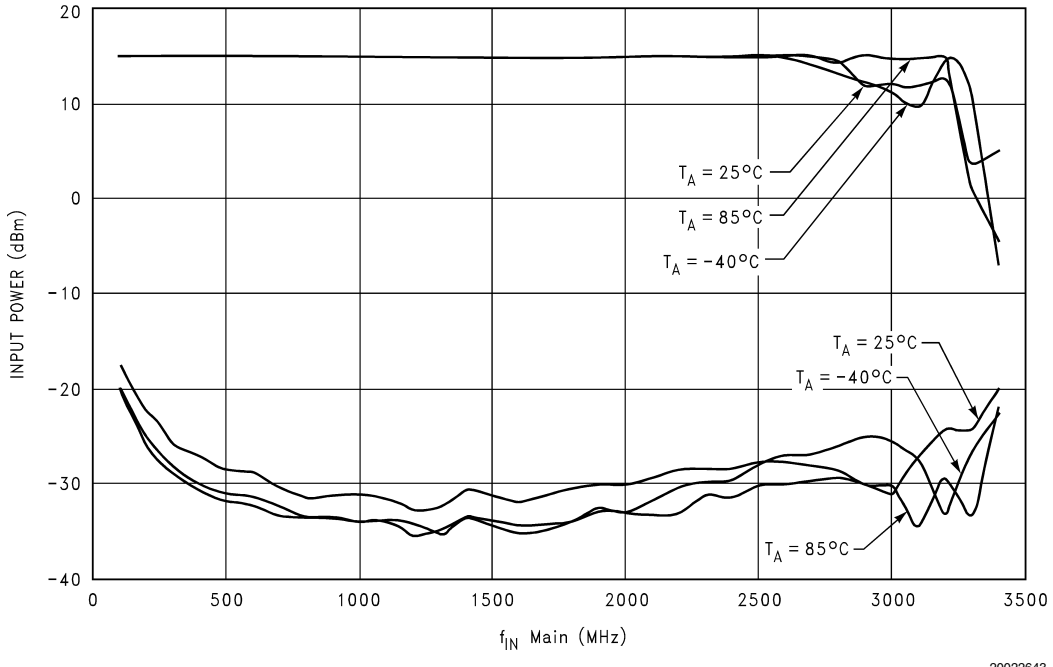
## Sensitivity

**LMX2377U  $f_{IN}$  Main Input Power Vs Frequency**  
 $V_{CC} = V_P \text{ Main} = V_{\mu c} = 3.0V$



20022642

**LMX2330U  $f_{IN}$  Main Input Power Vs Frequency**  
 $V_{CC} = V_P \text{ Main} = V_{\mu c} = 5.5V$

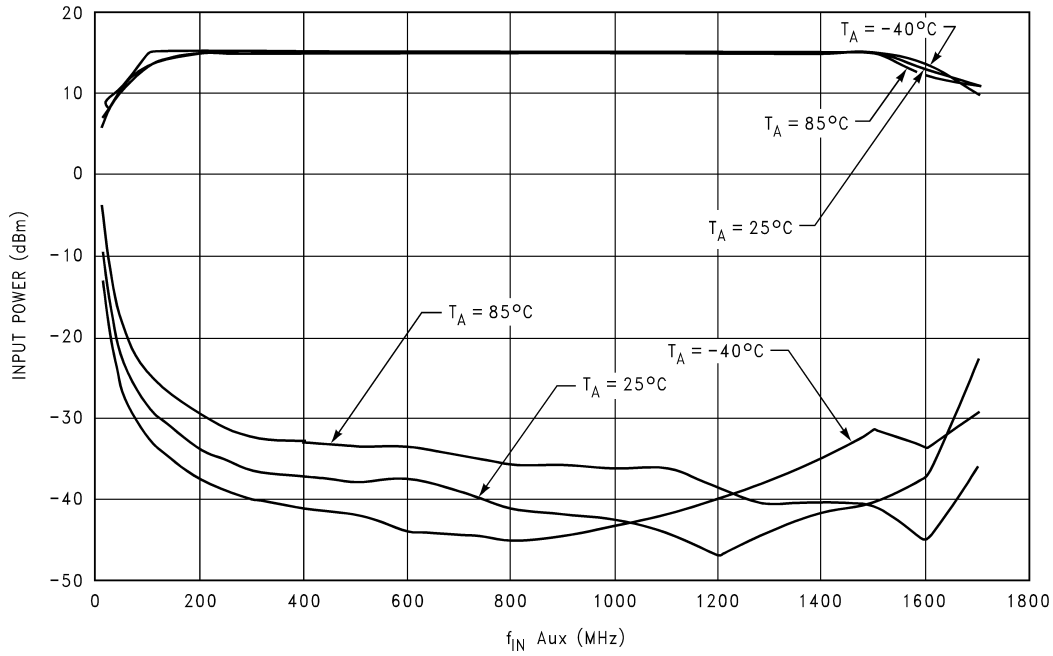


20022643

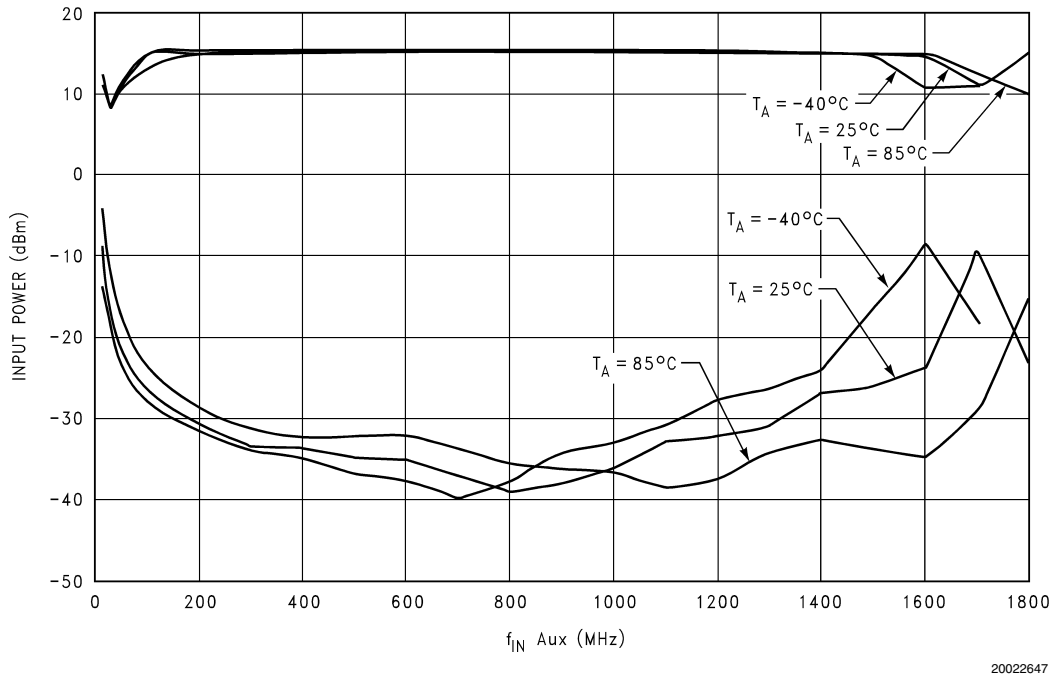
# Typical Performance Characteristics

## Sensitivity (Continued)

**LMX2377U  $f_{IN}$  Aux Input Power Vs Frequency**  
 $V_{CC} = V_P \text{ Aux} = V_{\mu C} = 3.0V$



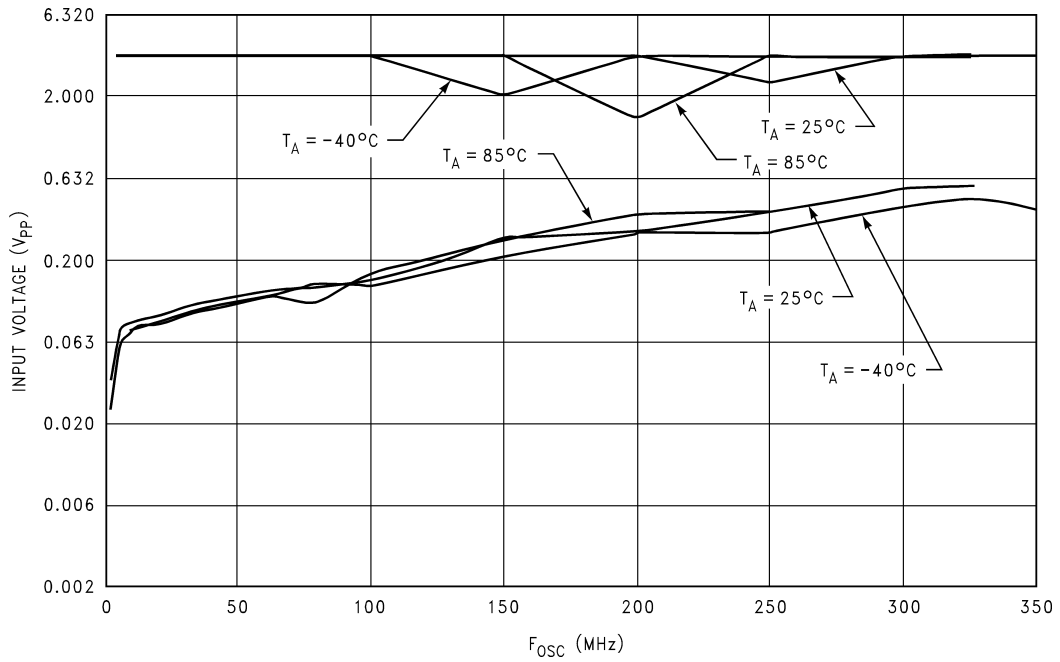
**LMX2377U  $f_{IN}$  Aux Input Power Vs Frequency**  
 $V_{CC} = V_P \text{ Aux} = V_{\mu C} = 5.5V$



# Typical Performance Characteristics

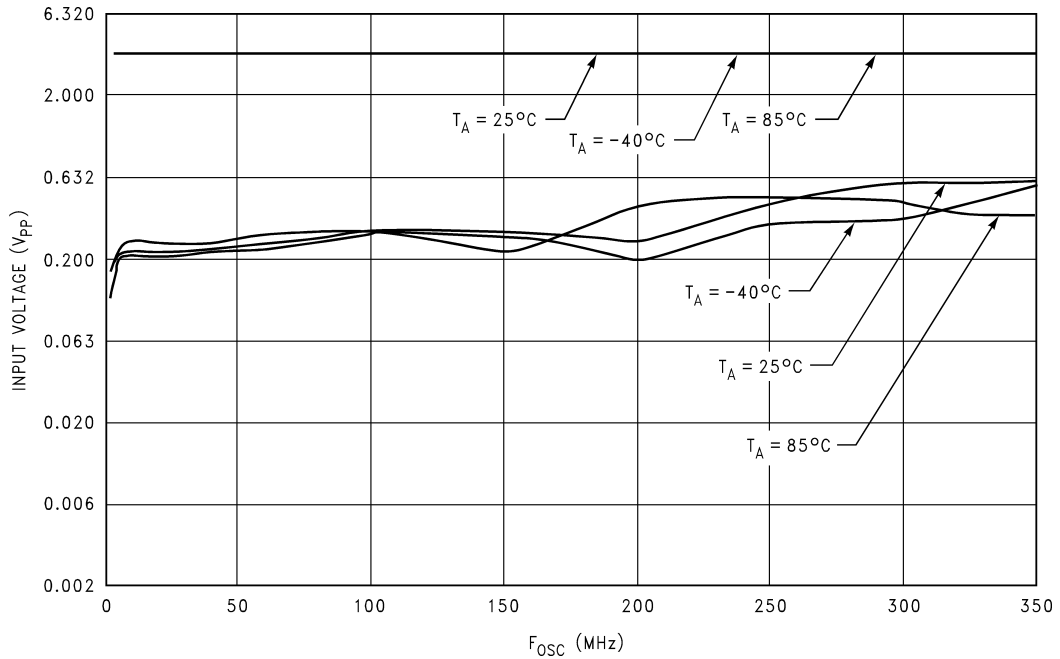
## Sensitivity (Continued)

LMX2377U OSC<sub>in</sub> Input Voltage Vs Frequency  
 $V_{CC} = V_{\mu C} = 3.0V$



20022652

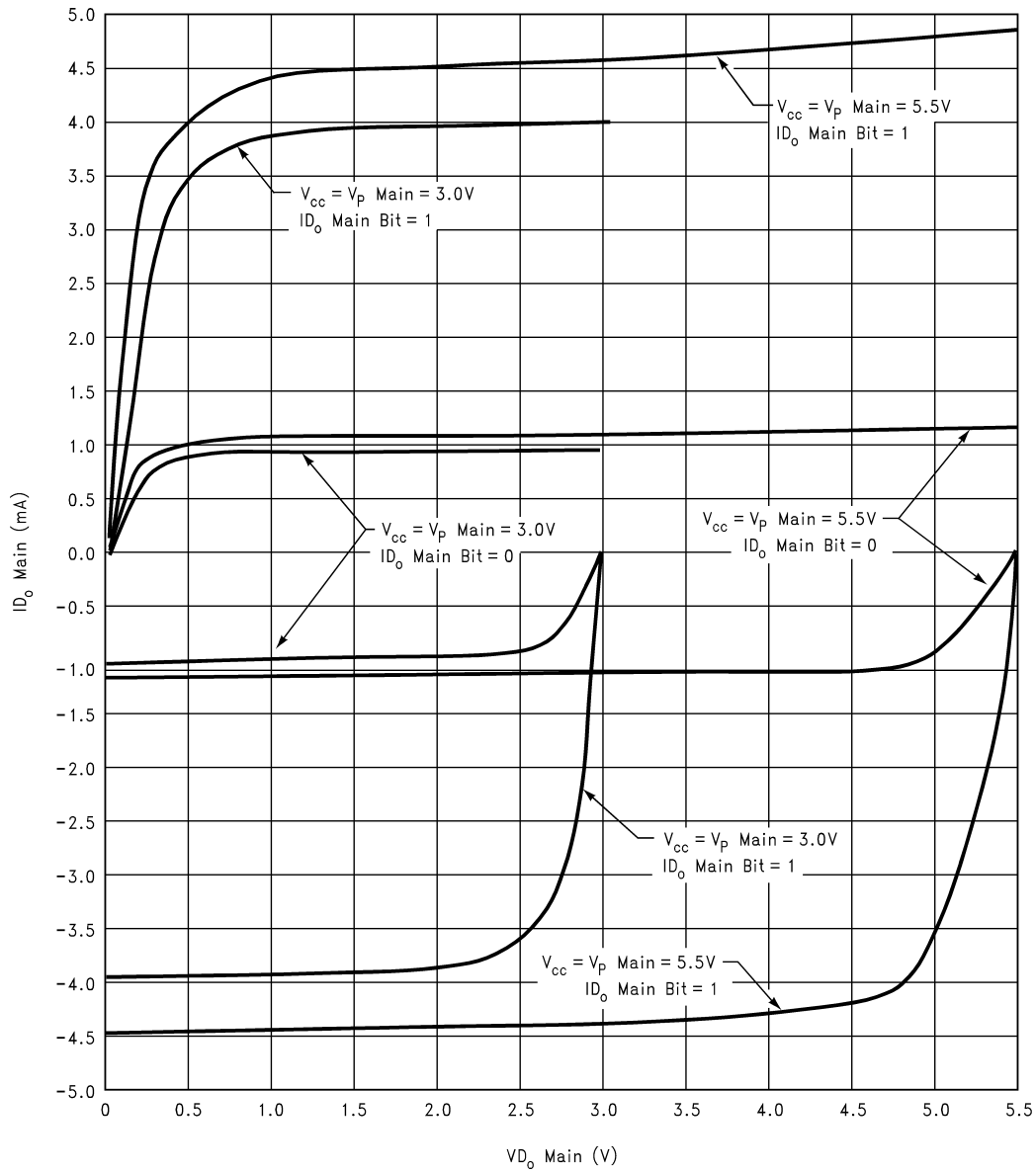
LMX2377U OSC<sub>in</sub> Input Voltage Vs Frequency  
 $V_{CC} = V_{\mu C} = 5.5V$



20022653

# Typical Performance Characteristics Charge Pump

LMX2377U Main Charge Pump Sweeps  
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ ,  $V_{\mu\text{C}} = V_{\text{CC}}$

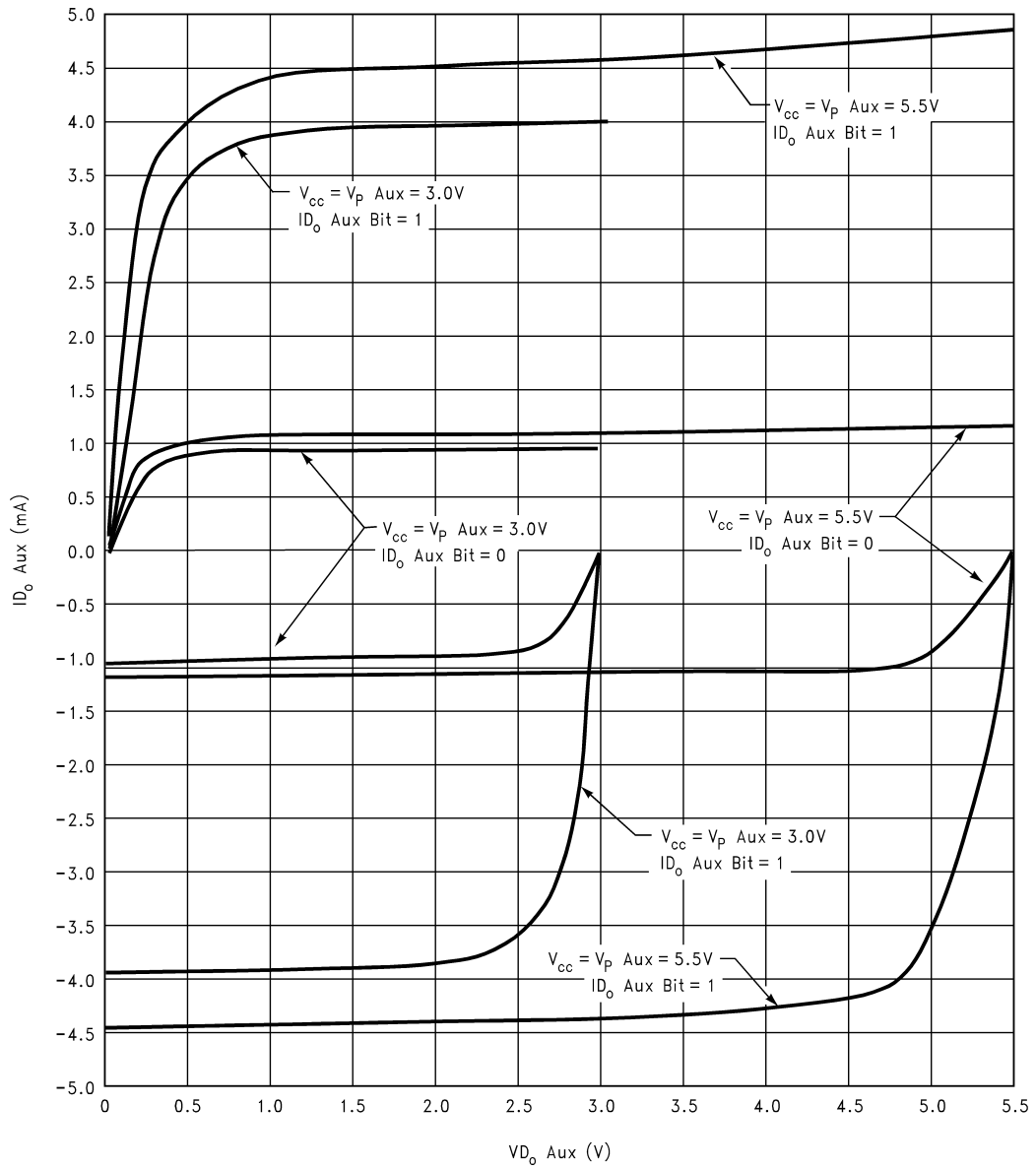


20022660

# Typical Performance Characteristics

## Charge Pump (Continued)

LMX2377U Aux Charge Pump Sweeps  
 $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ ,  $V_{\mu\text{C}} = V_{\text{CC}}$



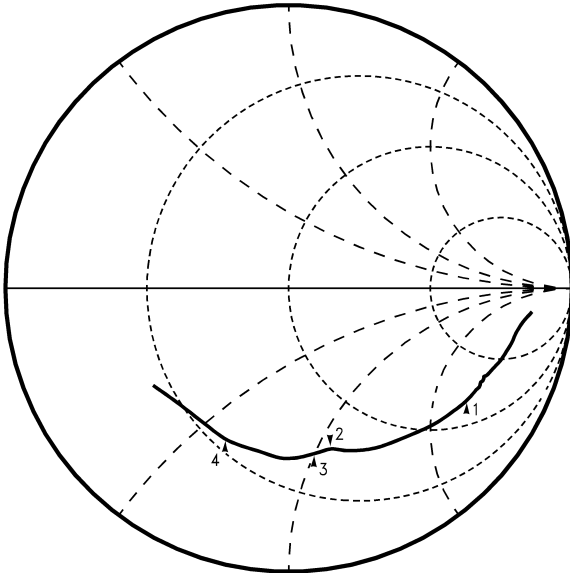
20022661



# Typical Performance Characteristics

## Input Impedance

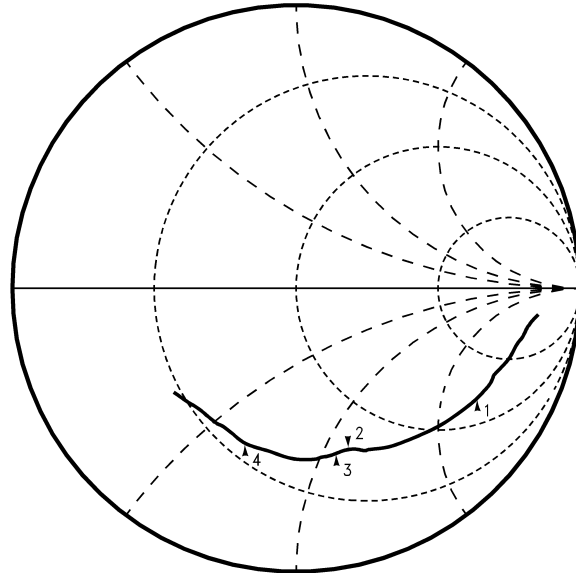
**LMX2377U TSSOP**  
 $f_{IN}$  Main and  $f_{IN}$  Aux Input Impedance  
 $V_{CC} = V_{\mu C} = 3.0V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

20022666

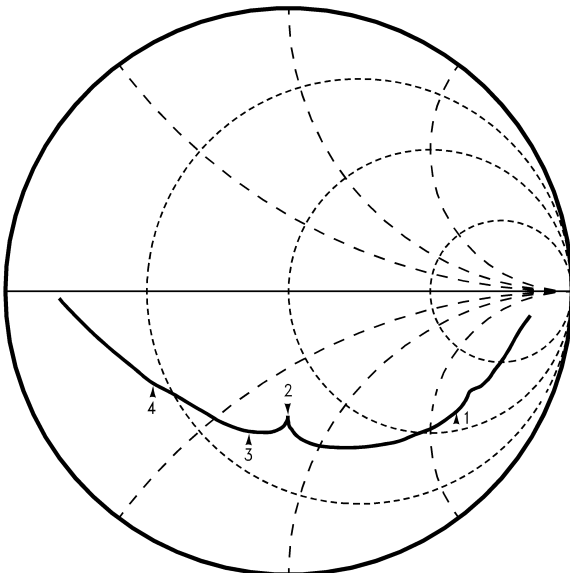
**LMX2377U TSSOP**  
 $f_{IN}$  Main and  $f_{IN}$  Aux Input Impedance  
 $V_{CC} = V_{\mu C} = 5.5V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

20022667

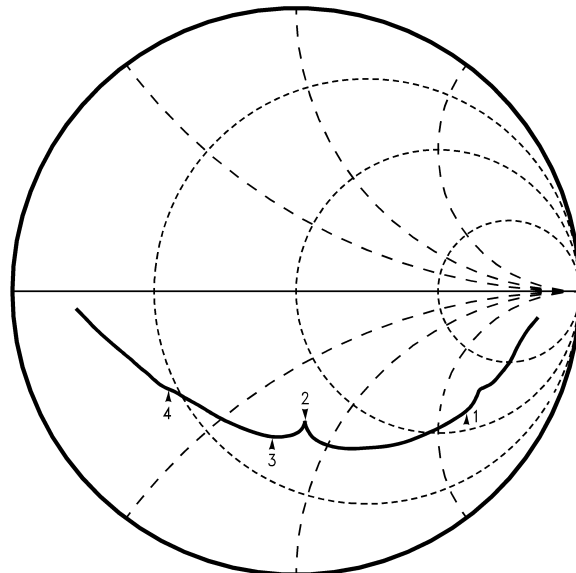
**LMX2377U CSP**  
 $f_{IN}$  Main and  $f_{IN}$  Aux Input Impedance  
 $V_{CC} = V_{\mu C} = 3.0V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

20022668

**LMX2377U CSP**  
 $f_{IN}$  Main and  $f_{IN}$  Aux Input Impedance  
 $V_{CC} = V_{\mu C} = 5.5V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

20022669

# Typical Performance Characteristics

## Input Impedance (Continued)

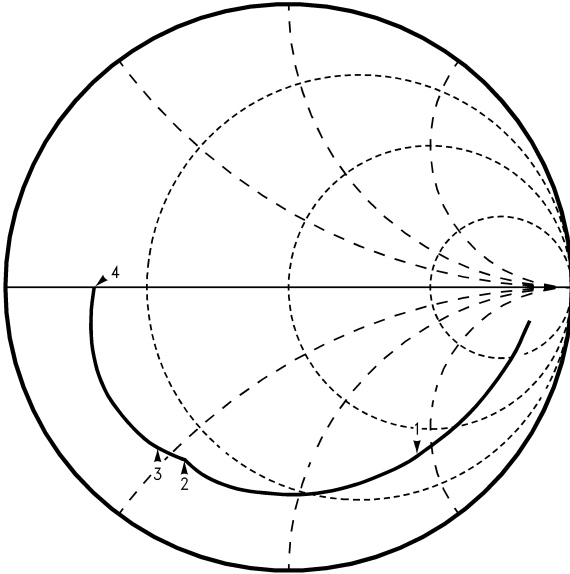
LMX2377U TSSOP and LMX2377U CSP  $f_{IN}$  Main and  $f_{IN}$  Aux Input Impedance Table

$f_{IN}$ (MHz)	LMX2377U TSSOP ( $Z_{f_{IN}}$ Main and $Z_{f_{IN}}$ Aux)										LMX2377U CSP ( $Z_{f_{IN}}$ Main and $Z_{f_{IN}}$ Aux)													
	$V_{CC} = V_P$ Main = $V_P$ Aux = $V_{IUC} = 3.0V$ ( $T_A = 25^\circ C$ )					$V_{CC} = V_P$ Main = $V_P$ Aux = $V_{IUC} = 5.5V$ ( $T_A = 25^\circ C$ )					$V_{CC} = V_P$ Main = $V_P$ Aux = $V_{IUC} = 3.0V$ ( $T_A = 25^\circ C$ )					$V_{CC} = V_P$ Main = $V_P$ Aux = $V_{IUC} = 5.5V$ ( $T_A = 25^\circ C$ )								
	$\angle \Gamma$	$ \Gamma $	$Z_{f_{IN}}$ ( $\Omega$ )	$R_{f_{IN}}$ ( $\Omega$ )	$X_{f_{IN}}$ ( $\Omega$ )	$ \Gamma $	$ \Gamma $	$Z_{f_{IN}}$ ( $\Omega$ )	$R_{f_{IN}}$ ( $\Omega$ )	$X_{f_{IN}}$ ( $\Omega$ )	$\angle \Gamma$	$ \Gamma $	$Z_{f_{IN}}$ ( $\Omega$ )	$R_{f_{IN}}$ ( $\Omega$ )	$X_{f_{IN}}$ ( $\Omega$ )	$\angle \Gamma$	$ \Gamma $	$Z_{f_{IN}}$ ( $\Omega$ )	$R_{f_{IN}}$ ( $\Omega$ )	$X_{f_{IN}}$ ( $\Omega$ )	$\angle \Gamma$	$ \Gamma $	$Z_{f_{IN}}$ ( $\Omega$ )	$R_{f_{IN}}$ ( $\Omega$ )
100	0.862	-6.23	439.774	-319.866	543.798	0.862	-6.07	448.230	-318.841	550.064	0.864	-6.44	431.004	-330.013	542.838	0.864	-6.30	438.240	-327.814	547.281				
200	0.834	-9.30	307.614	-272.274	410.803	0.834	-9.00	316.479	-271.581	417.031	0.836	-9.88	291.252	-277.923	402.577	0.836	-9.57	300.190	-277.552	408.838				
300	0.820	-12.11	237.700	-249.291	344.452	0.821	-11.66	247.264	-251.098	352.406	0.821	-13.24	215.318	-248.361	328.702	0.821	-12.76	224.624	-249.637	335.819				
400	0.808	-15.25	185.048	-227.171	293.001	0.808	-14.61	194.668	-229.054	300.601	0.808	-16.88	163.190	-219.893	273.832	0.808	-16.24	171.345	-222.518	280.844				
500	0.796	-18.51	147.785	-203.923	251.843	0.796	-17.66	156.935	-207.313	260.014	0.793	-20.90	126.193	-191.939	229.707	0.794	-20.00	133.885	-196.200	237.528				
600	0.781	-21.81	122.091	-181.461	218.710	0.782	-20.70	130.906	-185.850	227.325	0.775	-24.82	102.956	-168.026	197.060	0.777	-23.70	109.531	-172.887	204.663				
700	0.765	-24.72	106.107	-163.758	195.129	0.767	-23.45	113.780	-168.514	203.329	0.749	-28.29	90.820	-146.582	172.437	0.752	-27.02	96.279	-151.333	179.363				
800	0.760	-28.35	87.984	-150.524	174.352	0.762	-26.97	94.255	-155.481	181.819	0.742	-31.22	79.737	-136.782	158.327	0.746	-29.85	84.470	-141.473	164.772				
<b>900</b>	<b>0.747</b>	<b>-32.60</b>	<b>73.777</b>	<b>-134.500</b>	<b>153.406</b>	<b>0.750</b>	<b>-30.95</b>	<b>79.270</b>	<b>-139.668</b>	<b>160.596</b>	<b>0.739</b>	<b>-36.04</b>	<b>64.577</b>	<b>-123.951</b>	<b>139.764</b>	<b>0.742</b>	<b>-34.37</b>	<b>69.006</b>	<b>-128.610</b>	<b>145.954</b>				
1000	0.732	-36.68	64.122	-120.908	136.859	0.735	-34.73	69.215	-126.104	143.851	0.719	-41.44	55.019	-108.415	121.577	0.723	-39.46	58.684	-113.123	127.439				
1100	0.717	-41.25	55.780	-108.398	121.908	0.720	-39.12	60.041	-113.215	128.151	0.694	-47.27	48.056	-94.403	105.931	0.698	-45.08	51.159	-98.547	111.035				
1200	0.698	-46.24	49.180	-96.605	108.403	0.702	-43.84	52.848	-101.254	114.216	0.669	-53.59	42.269	-82.401	92.610	0.674	-51.01	45.061	-86.388	97.434				
1300	0.678	-51.43	43.982	-86.291	96.853	0.683	-48.77	47.173	-90.676	102.212	0.641	-60.42	37.856	-71.653	81.039	0.647	-57.50	40.230	-75.400	85.461				
1400	0.663	-56.68	39.397	-77.901	87.296	0.667	-53.71	42.317	-82.070	92.337	0.610	-68.33	34.108	-61.481	70.308	0.613	-64.90	36.477	-64.872	74.424				
1500	0.649	-62.08	35.566	-70.500	78.963	0.653	-58.74	38.281	-74.569	83.821	0.577	-77.01	31.049	-52.388	60.898	0.581	-73.18	33.064	-55.554	64.649				
1600	0.630	-67.58	32.912	-63.544	71.562	0.634	-63.96	35.335	-67.423	76.121	0.539	-84.86	29.732	-44.952	53.895	0.543	-80.36	31.654	-48.119	57.597				
1700	0.608	-72.22	31.565	-57.996	66.030	0.614	-68.51	33.590	-61.632	70.191	0.477	-97.97	26.359	-38.171	46.359	0.487	-94.99	33.106	-42.105	53.562				
<b>1800</b>	<b>0.596</b>	<b>-75.66</b>	<b>30.440</b>	<b>-54.462</b>	<b>62.392</b>	<b>0.601</b>	<b>-71.81</b>	<b>32.358</b>	<b>-57.943</b>	<b>66.366</b>	<b>0.455</b>	<b>89.90</b>	<b>32.829</b>	<b>-37.624</b>	<b>49.933</b>	<b>0.468</b>	<b>-85.87</b>	<b>33.886</b>	<b>-40.554</b>	<b>52.847</b>				
<b>1900</b>	<b>0.598</b>	<b>-80.06</b>	<b>27.915</b>	<b>-51.164</b>	<b>58.284</b>	<b>0.602</b>	<b>-76.22</b>	<b>29.678</b>	<b>-54.335</b>	<b>61.912</b>	<b>0.493</b>	<b>87.34</b>	<b>29.357</b>	<b>-38.214</b>	<b>48.189</b>	<b>0.500</b>	<b>-88.90</b>	<b>29.576</b>	<b>-39.369</b>	<b>49.241</b>				
2000	0.607	-85.31	24.914	-47.651	53.771	0.607	-81.32	26.675	-50.603	57.203	0.520	79.89	25.120	-35.225	43.264	0.521	84.05	26.396	-37.576	45.921				
2100	0.612	89.24	22.502	-43.994	49.414	0.611	-86.42	21.612	-42.064	47.292	0.529	70.97	22.177	-30.771	37.930	0.525	75.52	23.556	-33.043	40.580				
2200	0.605	84.09	21.289	-40.358	45.629	0.602	88.61	22.901	-43.251	48.940	0.531	61.99	20.155	-26.331	33.159	0.524	66.93	21.544	-28.595	35.802				
2300	0.594	78.44	20.367	-36.566	41.855	0.589	83.13	21.961	-39.298	45.018	0.533	52.71	18.533	-21.975	28.747	0.525	57.61	19.706	-24.119	31.146				
2400	0.590	72.27	19.111	-32.907	38.054	0.584	77.11	20.598	-35.536	41.074	0.550	43.18	16.578	-17.883	24.385	0.537	47.69	17.671	-19.749	26.501				
<b>2500</b>	<b>0.586</b>	<b>67.24</b>	<b>18.297</b>	<b>-30.064</b>	<b>35.194</b>	<b>0.576</b>	<b>72.09</b>	<b>19.792</b>	<b>-32.516</b>	<b>38.066</b>	<b>0.583</b>	<b>34.44</b>	<b>14.340</b>	<b>-14.328</b>	<b>20.272</b>	<b>0.566</b>	<b>38.69</b>	<b>15.416</b>	<b>-16.055</b>	<b>22.257</b>				

# Typical Performance Characteristics

## Input Impedance (Continued)

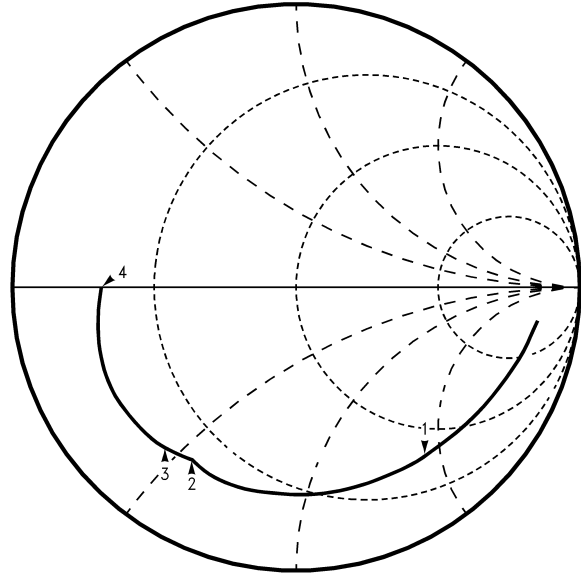
**LMX2377U UTCSP**  
 $f_{IN}$  Main and  $f_{IN}$  Aux Input Impedance  
 $V_{CC} = V_{\mu C} = 3.0V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

20022697

**LMX2377U UTCSP**  
 $f_{IN}$  Main and  $f_{IN}$  Aux Input Impedance  
 $V_{CC} = V_{\mu C} = 5.5V, T_A = +25^\circ C$



Marker 1 = 900 MHz  
 Marker 2 = 1800 MHz  
 Marker 3 = 1900 MHz  
 Marker 4 = 2500 MHz

20022697

# Typical Performance Characteristics

(Continued)

LMX2377U UTCSP  $f_{IN}$  Main and  $f_{IN}$  Aux Input Impedance Table

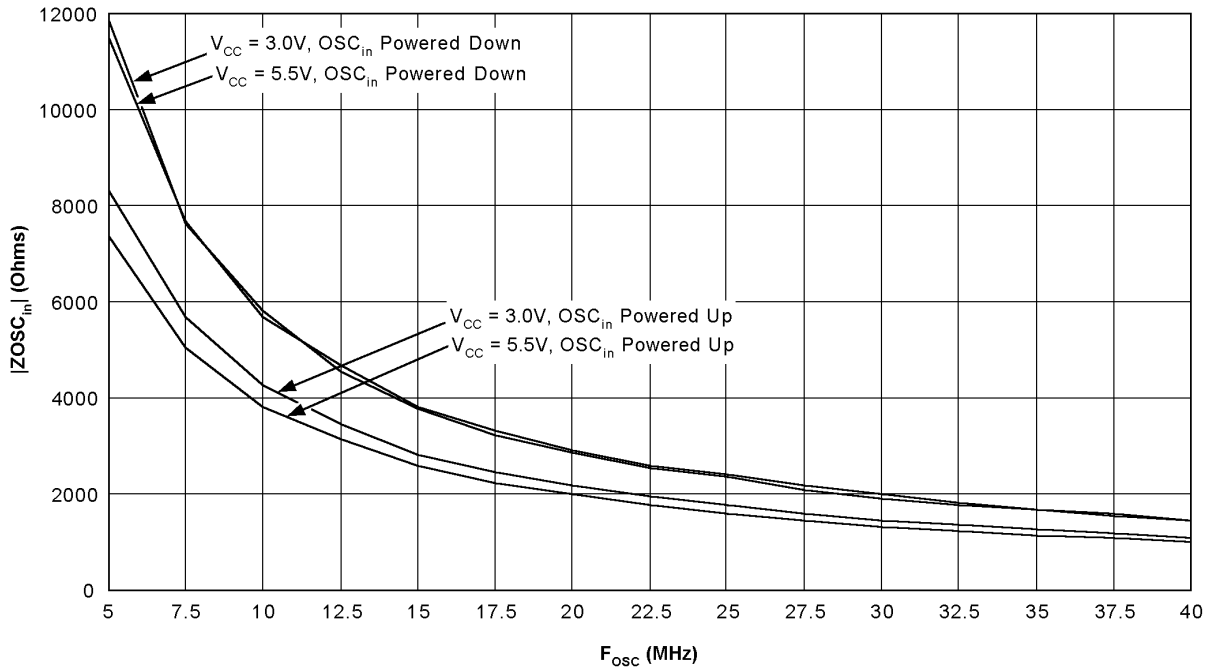
$f_{IN}$ (MHz)	LMX2377U UTCSP $Z_{f_{IN}}$ Main and $Z_{f_{IN}}$ Aux									
	$V_{CC} = V_P$ Main = $V_P$ , Aux = $V_{\mu C} = 3.0V$ ( $T_A = 25^\circ C$ )			$V_{CC} = V_P$ Main = $V_P$ , Aux = $V_{\mu C} = 5.5V$ ( $T_A = 25^\circ C$ )						
	$ T $	$\angle T$	$\frac{Re}{Z_{f_{IN}}}$ ( $\Omega$ )	$\frac{Im}{Z_{f_{IN}}}$ ( $\Omega$ )	$ Z_{f_{IN}} $ ( $\Omega$ )	$ T $	$\angle T$	$\frac{Re}{Z_{f_{IN}}}$ ( $\Omega$ )	$\frac{Im}{Z_{f_{IN}}}$ ( $\Omega$ )	$ Z_{f_{IN}} $ ( $\Omega$ )
100	0.86	-8.57	335.53	-330.26	470.80	0.86	-8.61	333.98	-330.26	469.70
200	0.83	-13.59	206.36	-258.74	330.95	0.83	-13.55	207.11	-258.92	331.57
300	0.81	-18.53	143.19	-214.36	257.79	0.81	-18.45	144.05	-214.75	258.59
400	0.80	-23.67	103.09	-183.95	210.86	0.80	-23.63	103.36	-184.12	211.15
500	0.79	-29.24	76.58	-157.24	174.89	0.79	-29.07	77.30	-157.87	175.78
600	0.77	-34.87	61.79	-133.64	147.24	0.77	-34.64	62.46	-134.31	148.12
700	0.76	-40.52	50.03	-116.97	127.23	0.76	-40.33	50.42	-117.43	127.80
800	0.76	-46.45	39.82	-103.86	111.24	0.76	-46.18	40.22	-104.42	111.89
<b>900</b>	<b>0.75</b>	<b>-53.27</b>	<b>32.87</b>	<b>-90.33</b>	<b>96.13</b>	<b>0.75</b>	<b>-52.89</b>	<b>33.27</b>	<b>-90.97</b>	<b>96.86</b>
1000	0.74	-60.04	27.98	-79.30	84.09	0.74	-59.70	28.24	-79.77	84.63
1100	0.73	-66.62	24.49	-70.27	74.42	0.73	-66.10	24.81	-70.90	75.11
1200	0.73	-74.07	20.63	-62.00	65.34	0.73	-73.57	20.85	-62.52	65.91
1300	0.73	-81.67	17.67	-54.66	57.45	0.73	-81.15	17.85	-55.13	57.95
1400	0.73	-89.59	15.34	-47.95	50.34	0.73	-88.94	15.51	-48.47	50.89
1500	0.73	-97.85	13.48	-41.75	43.87	0.73	-97.12	13.63	-42.27	44.41
1600	0.73	-106.72	11.96	-35.80	37.74	0.73	-105.87	12.09	-36.34	38.30
1700	0.72	-115.82	11.22	-30.21	32.22	0.72	-114.76	11.35	-30.82	32.84
<b>1800</b>	<b>0.70</b>	<b>-123.41</b>	<b>11.28</b>	<b>-25.85</b>	<b>28.20</b>	<b>0.70</b>	<b>-122.28</b>	<b>11.40</b>	<b>-26.45</b>	<b>28.80</b>
<b>1900</b>	<b>0.72</b>	<b>-130.68</b>	<b>9.80</b>	<b>-22.22</b>	<b>24.29</b>	<b>0.72</b>	<b>-129.92</b>	<b>9.86</b>	<b>-22.61</b>	<b>24.66</b>
2000	0.74	-140.55	8.41	-17.48	19.39	0.74	-139.88	8.44	-17.80	19.70
2100	0.74	-150.74	7.97	-12.74	15.03	0.74	-150.01	7.99	-13.07	15.32
2200	0.73	-160.86	8.02	-8.22	11.48	0.73	-160.03	8.04	-8.58	11.76
2300	0.71	-170.43	8.54	-4.06	9.46	0.71	-169.62	8.55	-4.41	9.62
2400	0.69	-179.08	9.17	-0.39	9.18	0.69	-178.32	9.17	-0.71	9.20
<b>2500</b>	<b>0.67</b>	<b>-172.38</b>	<b>9.92</b>	<b>3.20</b>	<b>10.43</b>	<b>0.67</b>	<b>-173.11</b>	<b>9.91</b>	<b>2.89</b>	<b>10.33</b>

20022688

# Typical Performance Characteristics

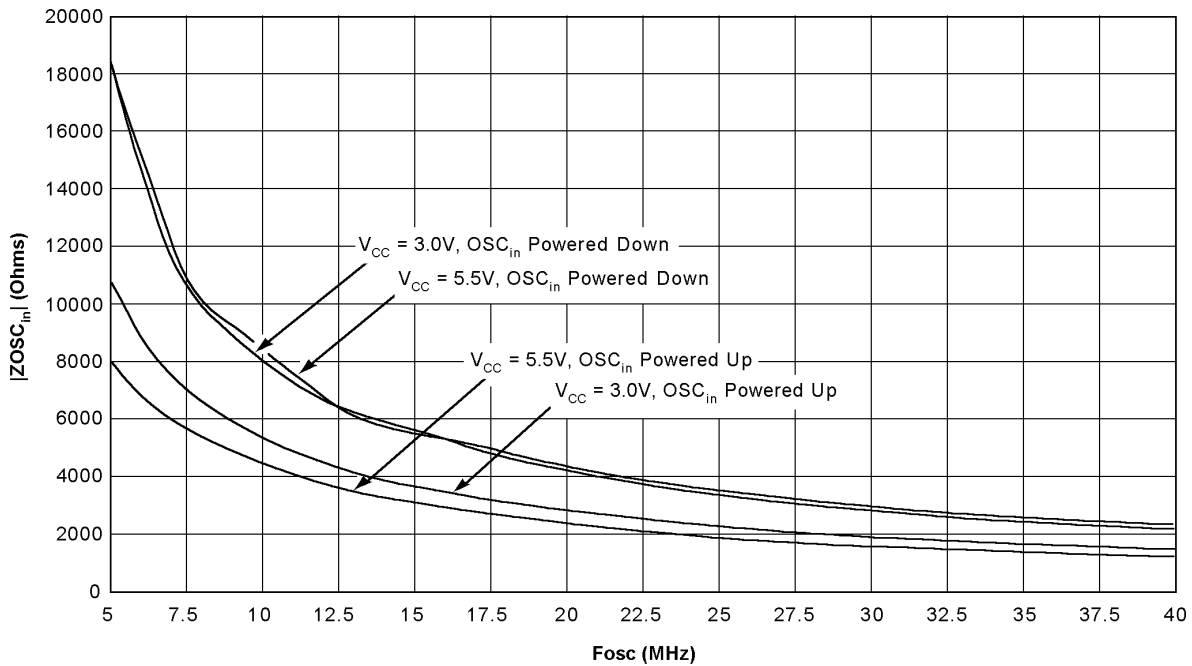
## Input Impedance (Continued)

LMX2377U TSSOP OSC<sub>in</sub> Input Impedance Vs Frequency  
T<sub>A</sub> = +25°C



20022676

LMX2377U CSP OSC<sub>in</sub> Input Impedance Vs Frequency  
T<sub>A</sub> = +25°C



20022677



# Typical Performance Characteristics

## Input Impedance (Continued)

LMX2377U TSSOP and LMX2377U CSP OSC<sub>in</sub> Input Impedance Table

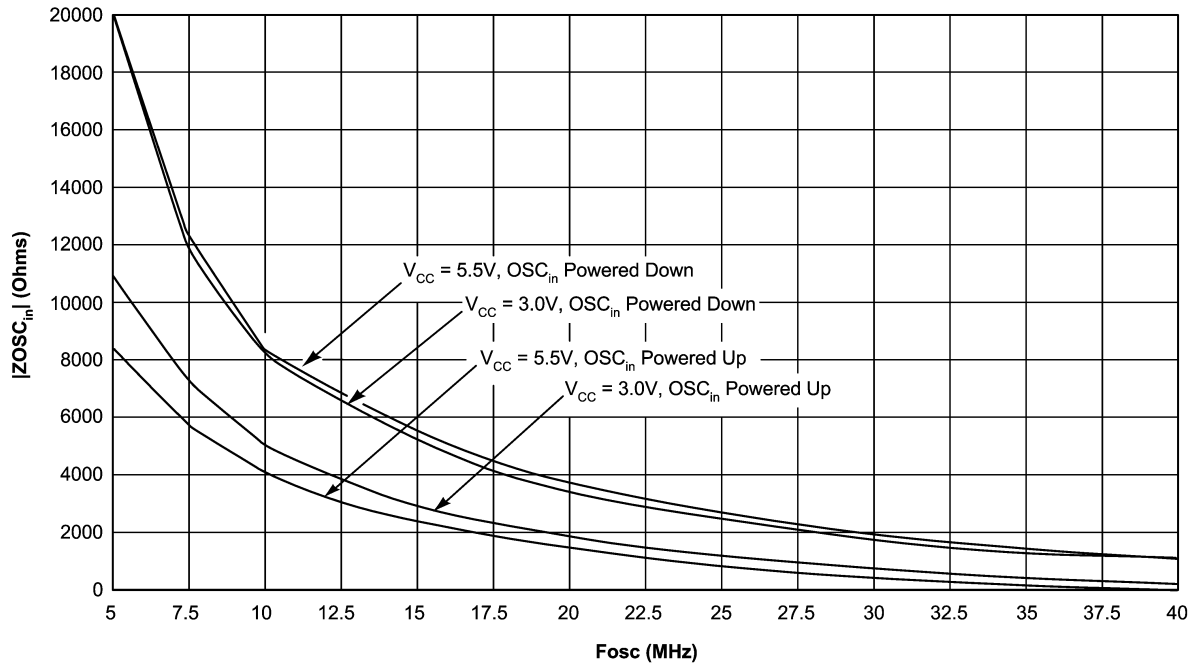
F <sub>osc</sub> (MHz)	LMX2377U TSSOP ZOSC <sub>n</sub>												LMX2377U CSP ZOSC <sub>n</sub>											
	V <sub>CC</sub> = V <sub>I<sub>A</sub></sub> = 3.0V (Γ <sub>A</sub> = 25°C)				V <sub>CC</sub> = V <sub>I<sub>A</sub></sub> = 5.5V (Γ <sub>A</sub> = 25°C)				V <sub>CC</sub> = V <sub>I<sub>A</sub></sub> = 3.0V (Γ <sub>A</sub> = 25°C)				V <sub>CC</sub> = V <sub>I<sub>A</sub></sub> = 5.5V (Γ <sub>A</sub> = 25°C)				V <sub>CC</sub> = V <sub>I<sub>A</sub></sub> = 5.5V (Γ <sub>A</sub> = 25°C)							
	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN	OSC <sub>n</sub> BUFFER POWERED UP	OSC <sub>n</sub> BUFFER POWERED DOWN						
	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)	Re ZOSC <sub>n</sub> (Ω)	Im ZOSC <sub>n</sub> (Ω)						
5.0	2291.113	-8000.376	8321.972	985.863	-11825.209	11866.234	2832.878	-6774.525	7342.982	1246.071	-11436.600	11504.282	5107.688	-9526.374	10809.27	4154.104	-18073.24	18544.50	4698.960	-6544.007	8056.318	4154.104	-18073.24	18544.50
7.5	1202.389	-5538.197	5667.218	294.460	-7640.322	7645.994	1267.479	-4861.053	5023.579	520.098	-7675.309	7692.910	2249.061	-6544.475	6920.146	1571.331	-10205.48	10325.74	2626.329	-4998.105	5646.119	1812.311	-10602.90	10756.68
10.0	791.970	-4218.658	4292.353	266.942	-5793.060	5799.207	739.926	-3754.673	3826.886	484.656	-5659.675	5680.388	1664.886	-5170.920	5432.335	1066.661	-8350.651	8418.499	1625.723	-4209.219	4512.261	976.808	-8800.590	8854.633
12.5	527.664	-3418.978	3459.456	197.874	-4547.094	4551.397	544.280	-3078.945	3126.584	196.239	-4865.169	4669.295	1048.750	-4245.537	4373.153	727.756	-6341.105	6382.730	1182.342	-3466.982	3663.045	899.697	-6248.932	6313.367
15.0	343.020	-2817.993	2838.794	161.801	-3761.566	3765.044	416.644	-2536.243	2570.238	160.236	-3799.626	3803.003	872.629	-3558.426	3663.861	442.319	-5658.273	5675.536	856.006	-2977.931	3098.519	436.542	-5712.786	5729.443
17.5	316.446	-2439.647	2460.085	141.326	-3203.351	3206.467	309.867	-2192.564	2214.372	196.400	-3305.741	3311.570	691.377	-3158.030	3232.825	296.061	-4799.917	4809.039	697.781	-2605.868	2697.692	309.618	-4985.007	4994.613
20.0	228.526	-2179.146	2191.096	83.505	-2879.931	2880.631	227.640	-1974.267	1987.347	73.816	-2917.281	2918.215	559.597	-2791.912	2847.441	194.872	-4242.475	4246.948	554.417	-2318.961	2384.315	303.378	-3445.597	3456.174
22.5	211.659	-1932.535	1944.091	98.108	-2543.330	2545.222	214.873	-1741.101	1754.310	103.131	-2608.411	2610.449	442.147	-2512.522	2551.129	186.123	-3777.847	3782.429	485.437	-2041.170	2098.100	168.163	-3935.873	3939.464
25.0	163.733	-1589.620	1598.030	69.675	-2106.253	2107.405	169.812	-1589.814	1598.857	67.246	-2388.967	2389.913	444.524	-2261.024	2304.307	170.072	-3402.400	3406.648	424.599	-1865.270	1912.986	174.460	-3506.895	3511.232
27.5	148.446	-1463.071	1470.583	81.310	-1926.889	1928.604	141.501	-1314.929	1322.520	69.823	-2161.702	2162.632	367.245	-2060.013	2092.491	191.739	-3114.867	3120.763	379.086	-1714.793	1756.195	159.273	-3213.478	3217.422
30.0	130.683	-1340.206	1346.562	46.548	-1750.824	1751.443	121.612	-1213.403	1219.482	37.610	-1812.700	1813.090	348.916	-1776.540	1810.480	188.280	-2837.317	2843.557	357.340	-1567.979	1608.182	157.424	-2834.223	2838.443
32.5	126.059	-1255.034	1261.349	38.046	-1662.230	1662.666	116.385	-1131.429	1137.399	45.646	-1689.748	1690.365	302.932	-1648.356	1675.961	95.424	-2471.170	2473.011	299.913	-1358.120	1390.940	125.530	-2600.472	2603.500
37.5	115.848	-1178.954	1184.632	37.202	-1547.816	1548.263	109.381	-1064.461	1070.066	36.346	-1591.439	1591.854	300.020	-1549.601	1578.377	117.732	-2331.694	2334.664	284.654	-1274.370	1305.774	144.727	-2419.904	2424.228
40.0	108.280	-1089.931	1095.296	36.351	-1439.460	1439.919	100.267	-985.544	990.631	39.180	-1470.482	1471.004	281.334	-1454.298	1481.260	81.318	-2182.473	2183.987	273.323	-1199.918	1230.654	152.283	-2302.913	2307.942

20022678

# Typical Performance Characteristics

## Input Impedance (Continued)

LMX2377U UTCSP OSC<sub>in</sub> Input Impedance Vs Frequency  
 T<sub>A</sub> = +25°C



200226A1

# Typical Performance Characteristics

## Input Impedance (Continued)

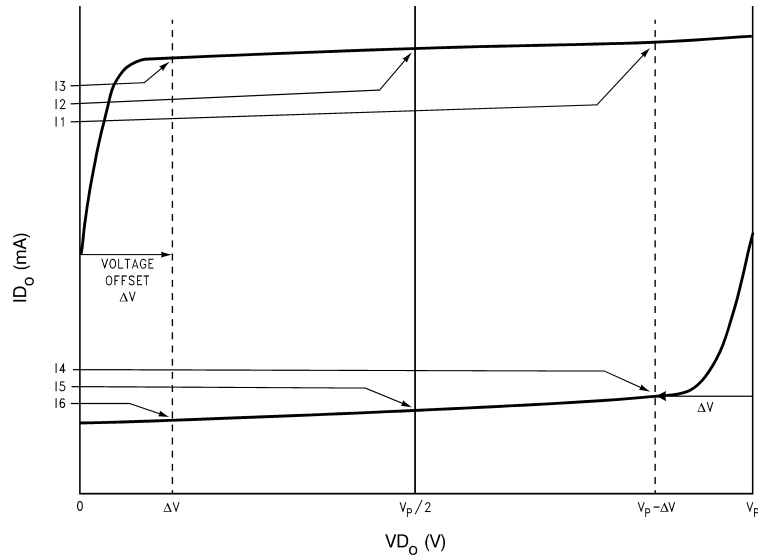
LMX2377U UTCSP OSC<sub>in</sub> Input Impedance Table

LMX2377U UTCSP ZOSC <sub>in</sub>												
V <sub>CC</sub> = 3.0V (T <sub>A</sub> = 25°C)												
F <sub>osc</sub> (MHz)	OSC <sub>in</sub> BUFFER POWERED UP			OSC <sub>in</sub> BUFFER POWERED DOWN			OSC <sub>in</sub> BUFFER POWERED UP			OSC <sub>in</sub> BUFFER POWERED DOWN		
	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	IZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	IZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	IZOSC <sub>in</sub> (Ω)	Re ZOSC <sub>in</sub> (Ω)	Im ZOSC <sub>in</sub> (Ω)	IZOSC <sub>in</sub> (Ω)
5.0	5918.57	-9897.80	11532.39	1822.62	-19947.73	20030.82	4982.73	-7668.32	9144.98	2478.02	-19591.11	19747.21
7.5	3097.46	-7441.43	8060.35	2238.93	-12114.22	12319.38	2742.97	-6082.16	6653.85	2483.54	-12531.99	12775.71
10.0	1695.22	-5720.83	5966.72	998.16	-9046.84	9101.74	1582.29	-4875.36	5125.70	1064.38	-9063.97	9126.25
12.5	1241.03	-4759.14	4918.29	660.39	-7338.93	7368.58	1150.39	-4034.66	4195.46	621.48	-7679.86	7704.97
15.0	820.55	-3955.33	4039.55	471.57	-6142.40	6160.48	861.48	-3448.80	3554.76	591.34	-6481.87	6508.79
17.5	646.18	-3417.20	3477.76	317.24	-5165.41	5175.14	599.49	-3009.04	3068.18	154.67	-5518.01	5520.17
20.0	520.20	-3006.22	3050.90	223.35	-4567.95	4573.41	491.78	-2647.38	2692.67	120.99	-4867.07	4868.57
22.5	459.63	-2666.05	2705.38	219.57	-4040.96	4046.92	396.64	-2342.62	2375.96	137.85	-4301.63	4303.84
25.0	391.21	-2398.19	2429.89	172.20	-3664.77	3668.81	323.46	-2108.25	2132.92	89.00	-3864.60	3865.62
27.5	348.79	-2210.66	2238.01	169.02	-3291.50	3295.84	312.14	-1920.70	1945.90	114.48	-3476.68	3478.56
30.0	285.07	-1996.71	2016.96	110.02	-3005.42	3007.43	260.59	-1763.82	1782.97	121.11	-3185.26	3187.56
32.5	267.83	-1847.30	1866.61	117.14	-2725.46	2727.97	239.41	-1612.35	1630.02	111.70	-2876.34	2878.50
35.0	252.27	-1719.32	1737.73	114.38	-2558.44	2561.00	222.16	-1503.76	1520.08	115.42	-2690.37	2692.84
37.5	224.94	-1639.80	1655.15	70.31	-2408.64	2409.67	191.46	-1422.88	1435.71	48.06	-2550.41	2550.86
40.0	208.96	-1512.91	1527.27	76.50	-2242.79	2244.09	180.75	-1329.24	1341.47	72.61	-2353.73	2354.85

20026A2



# Charge Pump Current Specification Definitions



20022637

11 = Charge Pump Sink Current at  $VD_o = V_p - \Delta V$

12 = Charge Pump Sink Current at  $VD_o = V_p/2$

13 = Charge Pump Sink Current at  $VD_o = \Delta V$

14 = Charge Pump Source Current at  $VD_o = V_p - \Delta V$

15 = Charge Pump Source Current at  $VD_o = V_p/2$

16 = Charge Pump Source Current at  $VD_o = \Delta V$

$\Delta V$  = Voltage offset from the positive and negative rails. Dependent on the VCO tuning range relative to  $V_{CC}$  and GND. Typical values are between 0.5V and 1.0V.

$V_p$  refers to either  $V_p$  Main or  $V_p$  Aux

$VD_o$  refers to either  $VD_o$  Main or  $VD_o$  Aux

$ID_o$  refers to either  $ID_o$  Main or  $ID_o$  Aux

## Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ID_o \text{ Vs } VD_o = \frac{(|I_{11}| - |I_{13}|)}{(|I_{11}| + |I_{13}|)} \times 100\%$$

$$= \frac{(|I_{14}| - |I_{16}|)}{(|I_{14}| + |I_{16}|)} \times 100\%$$

20022663

## Charge Pump Output Sink Current Vs Charge Pump Output Source Current Mismatch

$$ID_o \text{ SINK Vs } ID_o \text{ SOURCE} = \frac{|I_{12}| - |I_{15}|}{\frac{1}{2}(|I_{12}| + |I_{15}|)} \times 100\%$$

20022664

## Charge Pump Output Current Magnitude Variation Vs Temperature

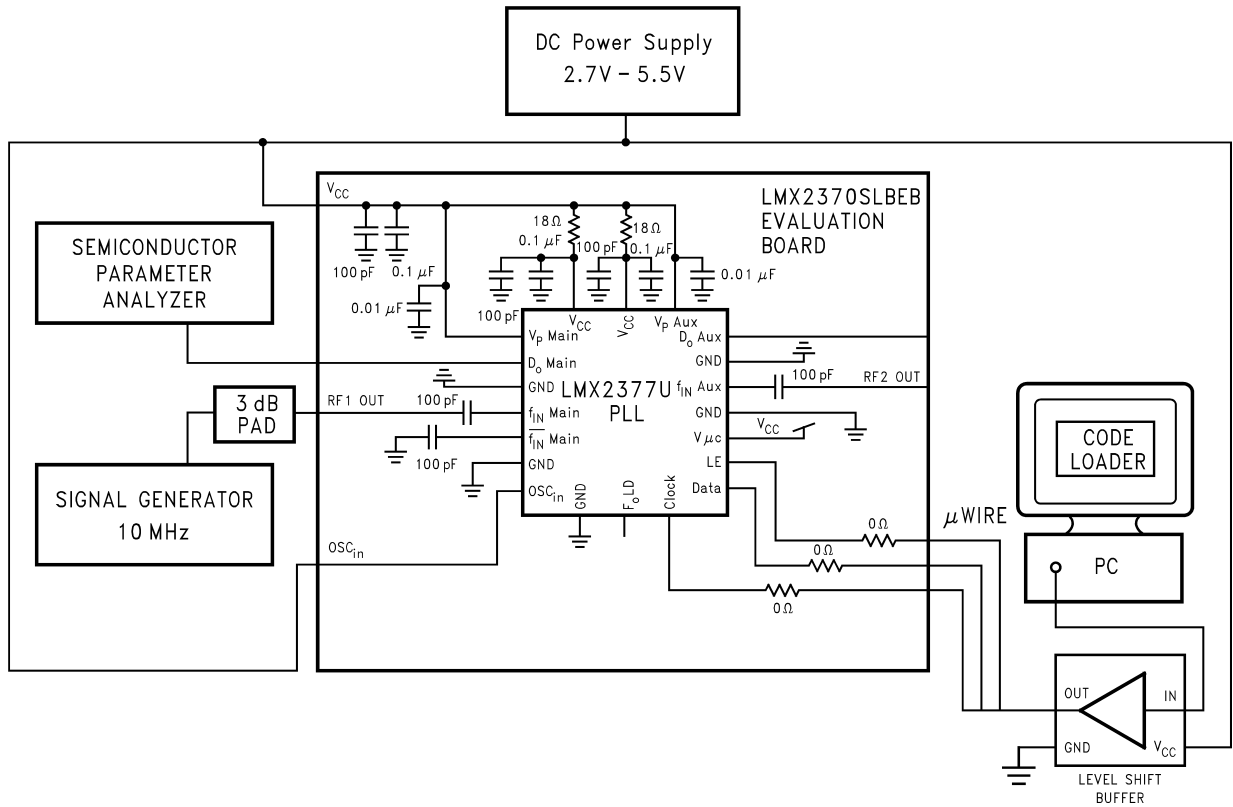
$$ID_o \text{ Vs } T_A = \frac{|I_{12}|_{T_A} - |I_{12}|_{T_A=25^\circ C}}{|I_{12}|_{T_A=25^\circ C}} \times 100\%$$

$$= \frac{|I_{15}|_{T_A} - |I_{15}|_{T_A=25^\circ C}}{|I_{15}|_{T_A=25^\circ C}} \times 100\%$$

20022665

## Test Setups

LMX2377U Charge Pump Test Setup



20022650

The block diagram above illustrates the setup required to measure the LMX2377U device's Main charge pump sink current. The same setup is used for the LMX2370TMEB/LMX2370SLEEB Evaluation Boards. The Aux charge pump measurement setup is similar to the Main charge pump measurement setup. The purpose of this test is to assess the functionality of the Main charge pump.

This setup uses an open loop configuration. A power supply is connected to  $V_{CC}$  and swept from 2.7V to 5.5V. The MICROWIRE power supply,  $V_{\mu c}$ , is tied to  $V_{CC}$ . By means of a signal generator, a 10 MHz signal is typically applied to the  $f_{IN}$  Main pin. The signal is one of two inputs to the phase detector. The 3 dB pad provides a 50  $\Omega$  match between the PLL and the signal generator. The  $OSC_{in}$  pin is tied to  $V_{CC}$ . This establishes the other input to the phase detector. Alternatively, this input can be tied directly to the ground plane. With the  $D_O$  Main pin connected to a Semiconductor Parameter Analyzer in this way, the sink, source, and TRI-STATE currents can be measured by simply toggling the **Phase Detector Polarity** and **Charge Pump State** states in Code

Loader. Similarly, the LOW and HIGH currents can be measured by switching the **Charge Pump Gain's** state between **1X** and **4X** in Code Loader.

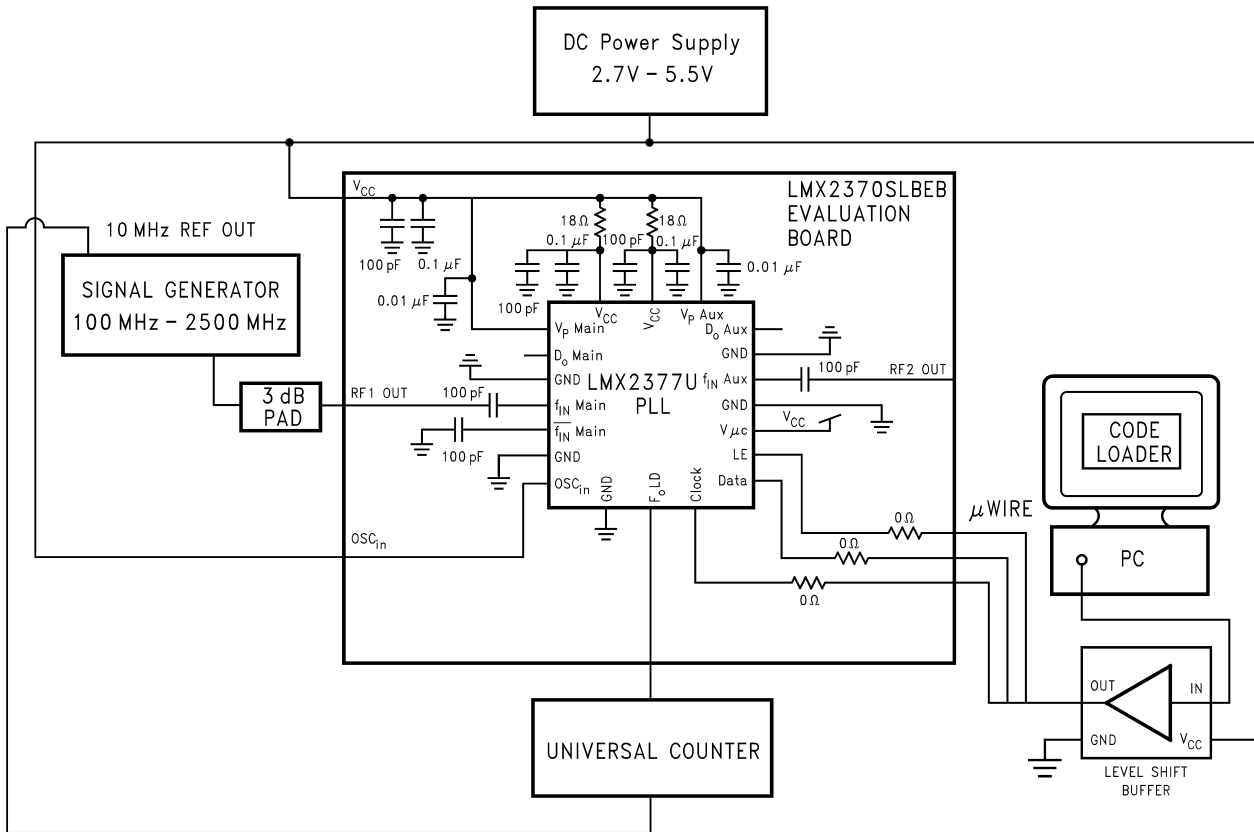
Let  $F_r$  represent the frequency of the signal applied to the  $OSC_{in}$  pin, which is simply zero in this case (DC), and let  $F_p$  represent the frequency of the signal applied to the  $f_{IN}$  Main pin. The phase detector is sensitive to the rising edges of  $F_r$  and  $F_p$ . Assuming positive VCO characteristics; the charge pump turns ON and sinks current when the first rising edge of  $F_p$  is detected. Since  $F_r$  has no rising edge, the charge pump continues to sink current indefinitely.

toggling the **Phase Detector Polarity** state to negative VCO characteristics allows the measurement of the Main charge pump source current. Likewise, selecting **TRI-STATE** (TRI-STATE  $ID_O$  Main Bit = 1) for **Charge Pump State** in Code Loader facilitates the measurement of the TRI-STATE current.

The measurements are repeated at different temperatures, namely  $T_A = -40^\circ C$ ,  $+25^\circ C$ , and  $+85^\circ C$ .

**Test Setups** (Continued)

**LMX2377U  $f_{IN}$  Sensitivity Test Setup**



20022640

The block diagram above illustrates the setup required to measure the LMX2377U device's Main input sensitivity level. The same setup is used for the LMX2370TMEB/LMX2370SLEEB Evaluation Boards. The Aux input sensitivity test setup is similar to the Main input sensitivity test setup. The purpose of this test is to measure the acceptable signal level to the  $f_{IN}$  Main input of the PLL chip. Outside the acceptable signal range, the feedback divider begins to divide incorrectly and miscount the frequency.

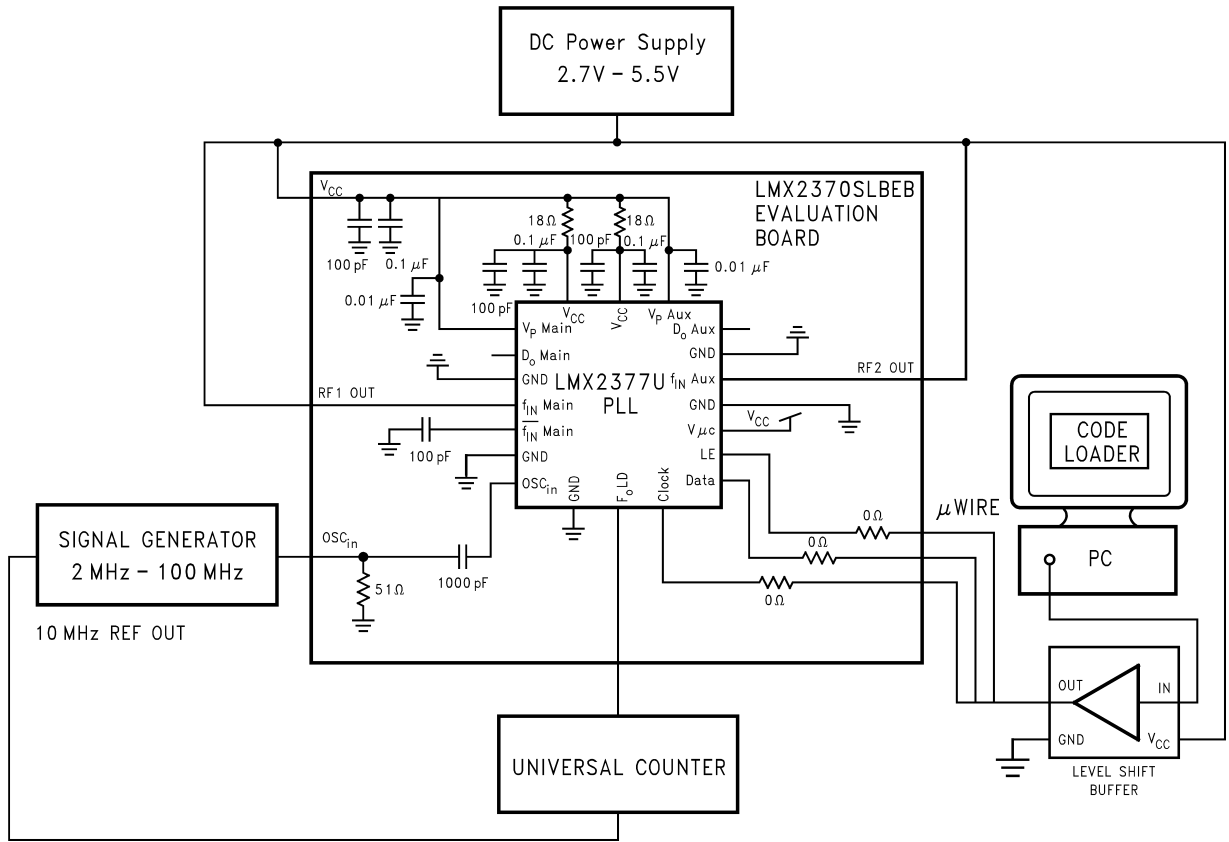
The setup uses an open loop configuration. A power supply is connected to  $V_{CC}$  and the bias voltage is swept from 2.7V to 5.5V. The MICROWIRE power supply,  $V_{\mu c}$ , is tied to  $V_{CC}$ . The Aux PLL is powered down (PWDN Aux Bit = 1). By means of a signal generator, an RF signal is applied to the  $f_{IN}$  Main pin. The 3 dB pad provides a 50  $\Omega$  match between the PLL and the signal generator. The  $OSC_{in}$  pin is tied to  $V_{CC}$ . The N value is typically set to 10000 in Code Loader, i.e. Main N\_CNTRB Word = 312 and Main N\_CNTRA Word = 16 for PRE Main Bit = 1. The feedback divider output is routed to the  $F_{oLD}$  pin by selecting the **Main PLL N Divider**

**Output** word ( $F_{oLD}$  Word = 6 or 14) in Code Loader. A Universal Counter is connected to the  $F_{oLD}$  pin and tied to the 10 MHz reference output of the signal generator. The output of the feedback divider is thus monitored and should be equal to  $f_{IN}$  Main/ N.

The  $f_{IN}$  Main input frequency and power level are then swept with the signal generator. The measurements are repeated at different temperatures, namely  $T_A = -40^\circ C$ ,  $+25^\circ C$ , and  $+85^\circ C$ . Sensitivity is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz. The power attenuation from the cable and the 3 dB pad must be accounted for. The feedback divider will actually miscount if too much or too little power is applied to the  $f_{IN}$  Main input. Therefore, the allowed input power level will be bounded by the upper and lower sensitivity limits. In a typical application, if the power level to the  $f_{IN}$  Main input approaches the sensitivity limits, this can introduce spurs and degradation in phase noise. When the power level gets even closer to these limits, or exceeds it, then the Main PLL loses lock.

**Test Setups** (Continued)

**LMX2377U OSC<sub>in</sub> Sensitivity Test Setup**



20022641

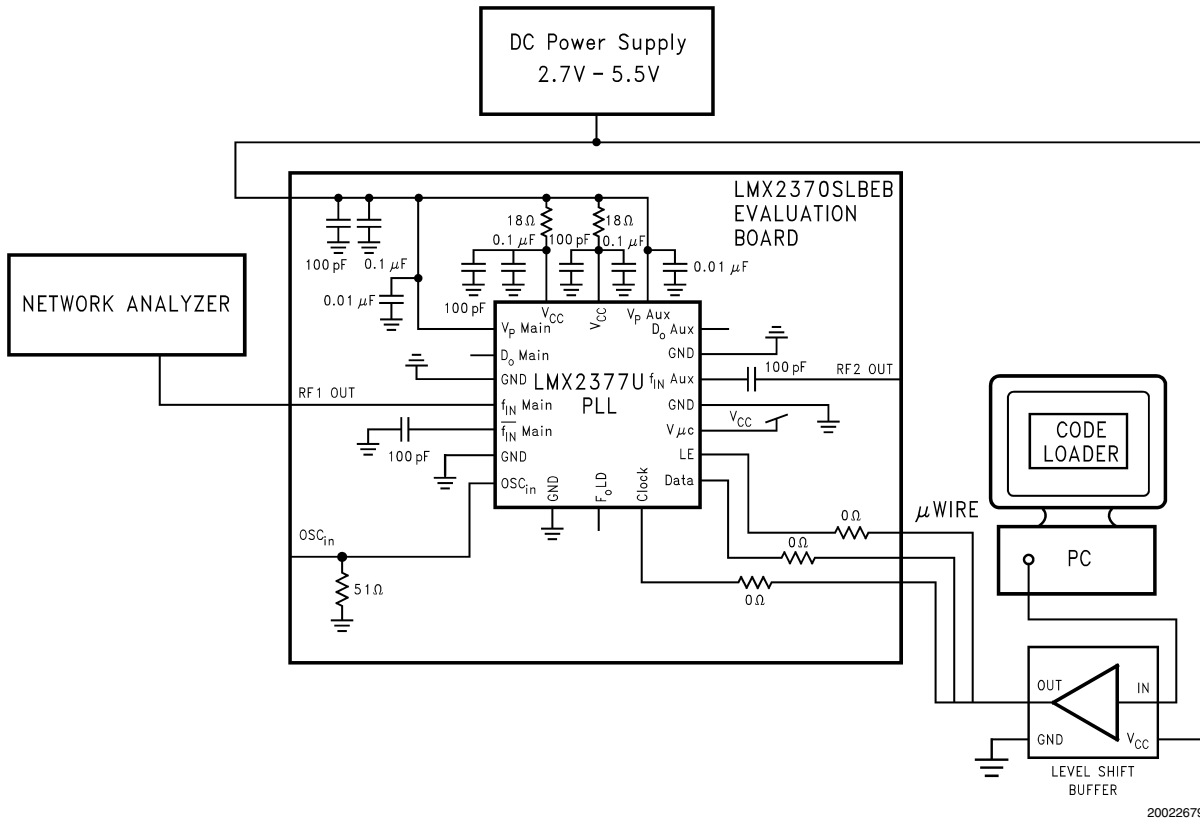
The block diagram above illustrates the setup required to measure the LMX2377U device's OSC<sub>in</sub> buffer sensitivity level. The same setup is used for the LMX2370TMEB/LMX2370SLEEB Evaluation Boards. This setup is similar to the f<sub>IN</sub> sensitivity setup except that the signal generator is now connected to the OSC<sub>in</sub> pin and both f<sub>IN</sub> pins are tied to V<sub>CC</sub>. The 51 Ω shunt resistor matches the OSC<sub>in</sub> input to the signal generator. The R counter is typically set to 1000, i.e. Main R\_CNTR Word = 1000 or Aux R\_CNTR Word = 1000. The reference divider output is routed to the F<sub>o</sub>LD pin by selecting the **Main PLL R Divider Output** word (F<sub>o</sub>LD Word = 2 or 10) or the **Aux PLL R Divider Output** word (F<sub>o</sub>LD Word = 1 or 9) in Code Loader. Similarly, a Universal

Counter is connected to the F<sub>o</sub>LD pin and is tied to the 10 MHz reference output from the signal generator. The output of the reference divider is monitored and should be equal to OSC<sub>in</sub>/ Main R\_CNTR or OSC<sub>in</sub>/ Aux R\_CNTR.

Again, V<sub>CC</sub> is swept from 2.7V to 5.5V. The MICROWIRE power supply, V<sub>mic</sub>, is tied to V<sub>CC</sub>. The OSC<sub>in</sub> input frequency and voltage level are then swept with the signal generator. The measurements are repeated at different temperatures, namely T<sub>A</sub> = -40°C, +25°C, and +85°C. Sensitivity is reached when the frequency error of the divided input signal is greater than or equal to 1 Hz.

Test Setups (Continued)

LMX2377U  $f_{IN}$  Impedance Test Setup



The block diagram above illustrates the setup required to measure the LMX2377U device's Main input impedance. The Aux input impedance and reference oscillator impedance setups are very much similar. The same setup is used for the LMX2370TMEB/ LMX2370SLEEB Evaluation Boards. Measuring the device's input impedance facilitates the design of appropriate matching networks to match the PLL to the VCO, or in more critical situations, to the characteristic impedance of the printed circuit board (PCB) trace, to prevent undesired transmission line effects.

Before the actual measurements are taken, the Network Analyzer needs to be calibrated, i.e. the error coefficients need to be calculated. Therefore, three standards will be used to calculate these coefficients: an **open**, **short** and a **matched load**. A 1-port calibration is implemented here.

To calculate the coefficients, the PLL chip is first removed from the PCB. The Network Analyzer port is then connected to the RF1 OUT connector of the evaluation board and the desired operating frequency is set. The typical frequency range selected for the LMX2377U device's Main synthesizer is from 100 MHz to 2500 MHz. The standards will be located down the length of the RF1 OUT transmission line. The transmission line adds electrical length and acts as an offset from the reference plane of the Network Analyzer; therefore,

it must be included in the calibration. Although not shown, 0 Ω resistors are used to complete the RF1 OUT transmission line (trace).

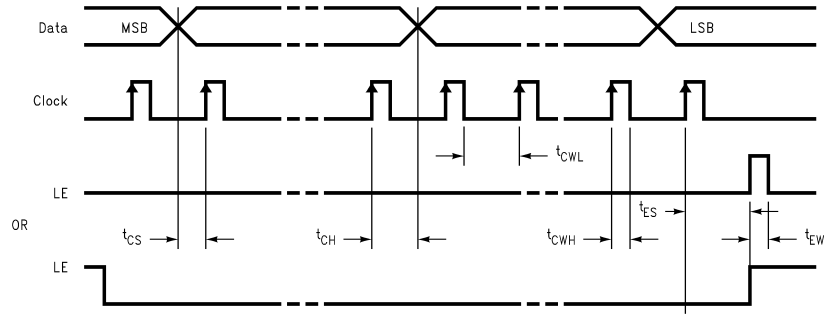
To implement an **open** standard, the end of the RF1 OUT trace is simply left open. To implement a **short** standard, a 0 Ω resistor is placed at the end of the RF1 OUT transmission line. Last of all, to implement a **matched load** standard, two 100 Ω resistors in parallel are placed at the end of the RF1 OUT transmission line. The Network Analyzer calculates the calibration coefficients based on the measured  $S_{11}$  parameters. With this all done, calibration is now complete.

The PLL chip is then placed on the PCB. A power supply is connected to  $V_{CC}$  and swept from 2.7V to 5.5V. The MICROWIRE power supply,  $V_{\mu c}$ , is tied to  $V_{CC}$ . The  $OSC_{in}$  pin is tied to the ground plane. Alternatively, the  $OSC_{in}$  pin can be tied to  $V_{CC}$ . In this setup, the complementary input ( $f_{IN}$  Main) is AC coupled to ground. With the Network Analyzer still connected to RF1 OUT, the measured  $f_{IN}$  Main impedance is displayed.

**Note:** The impedance of the reference oscillator is measured when the oscillator buffer is powered up (PWDN Main Bit = 0 or PWDN Aux Bit = 0), and when the oscillator buffer is powered down (PWDN Main Bit = 1 and PWDN Aux Bit = 1).

**Test Setups** (Continued)

**LMX2377U Serial Data Input Timing**



20022610

**Notes:**

1. Data is clocked into the 22-bit shift register on the rising edge of Clock
2. The MSB of Data is shifted in first.

## 1.0 Functional Description

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2377U, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, current mode charge pump, programmable reference R and feedback N frequency dividers. The VCO frequency is established by dividing the crystal reference signal down via the reference divider to obtain a comparison reference frequency. This reference signal,  $F_r$ , is then presented to the input of a phase/frequency detector and compared with the feedback signal,  $F_p$ , which was obtained by dividing the VCO frequency down by way of the feedback divider. The phase/frequency detector measures the phase error between the  $F_r$  and  $F_p$  signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The phase/frequency detector's function is to adjust the voltage presented to the VCO until the feedback signal's frequency and phase match that of the reference signal. When this "Phase-Locked" condition exists, the VCO frequency will be N times that of the comparison frequency, where N is the feedback divider ratio.

### 1.1 REFERENCE OSCILLATOR INPUT

The reference oscillator frequency for both the Main and Aux PLLs is provided from an external reference via the  $OSC_{in}$  pin. The reference buffer circuit supports input frequencies from 2 to 40 MHz with a minimum input sensitivity of  $0.5 V_{PP}$ . The reference buffer circuit has an approximate  $V_{CC}/2$  input threshold and can be driven from an external CMOS or TTL logic gate. Typically, the  $OSC_{in}$  pin is connected to the output of a crystal oscillator.

### 1.2 REFERENCE DIVIDERS (R COUNTERS)

The reference dividers divide the reference input signal,  $OSC_{in}$ , by a factor of R. The output of the reference divider circuits feeds the reference input of the phase detector. This reference input to the phase detector is often referred to as the comparison frequency. The divide ratio should be chosen such that the maximum phase comparison frequency ( $F_{\phi Main}$  or  $F_{\phi Aux}$ ) of 10 MHz is not exceeded.

The Main and Aux reference dividers are each comprised of 15-bit CMOS binary counters that support a continuous integer divide ratio from 2 to 32767. The Main and Aux reference divider circuits are clocked by the output of the reference buffer circuit which is common to both.

### 1.3 PRESCALERS

The  $f_{IN}$  Main and  $\overline{f_{IN}}$  Main input pins drive the input of a bipolar, differential-pair amplifier. The output of the bipolar, differential-pair amplifier drives a chain of ECL D-type

flip-flops in a dual modulus configuration. The output of the prescaler is used to clock the subsequent feedback dividers. The Main PLL complementary inputs can be driven differentially, or the negative input can be AC coupled to ground through an external capacitor for single ended configuration. A 16/17 or a 32/33 prescale ratio can be selected for the LMX2377U Main synthesizer. On the other hand, the Aux PLL is only intended for single ended operation. An 8/9 or a 16/17 prescale ratio can be selected for the LMX2377U Aux synthesizer.

### 1.4 PROGRAMMABLE FEEDBACK DIVIDERS (N COUNTERS)

The programmable feedback dividers operate in concert with the prescalers to divide the input signal  $f_{IN}$  by a factor of N. The output of the programmable reference divider is provided to the feedback input of the phase detector circuit. The divide ratio should be chosen such that the maximum phase comparison frequency ( $F_{\phi Main}$  or  $F_{\phi Aux}$ ) of 10 MHz is not exceeded.

The programmable feedback divider circuit is comprised of an A counter (swallow counter) and a B counter (programmable binary counter). The Main  $N_{CNTRA}$  and the Aux  $N_{CNTRA}$  counters are both 5-bit CMOS swallow counters, programmable from 0 to 31. The Main  $N_{CNTRB}$  and Aux  $N_{CNTRB}$  counters are both 13-bit CMOS binary counters, programmable from 3 to 8191. A continuous integer divide ratio is achieved if  $N \geq P * (P-1)$ , where P is the value of the prescaler selected. Divide ratios less than the minimum continuous divide ratio are achievable as long as the binary programmable counter value is greater than the swallow counter value ( $N_{CNTRB} \geq N_{CNTRA}$ ). Refer to **Sections 2.5.1, 2.5.2, 2.7.1 and 2.7.2** for details on how to program the  $N_{CNTRA}$  and  $N_{CNTRB}$  counters. The following equations are useful in determining and programming a particular value of N:

$$N = (P \times N_{CNTRB}) + N_{CNTRA}$$

$$f_{IN} = N \times F_{\phi}$$

#### Definitions:

$F_{\phi}$ :	Main or Aux phase detector comparison frequency
$f_{IN}$ :	Main or Aux input frequency
$N_{CNTRA}$ :	Main or Aux A counter value
$N_{CNTRB}$ :	Main or Aux B counter value
P:	Preset modulus of the dual modulus prescaler
	Main synthesizer: P = 16 or 32
	Aux synthesizer: P = 8 or 16

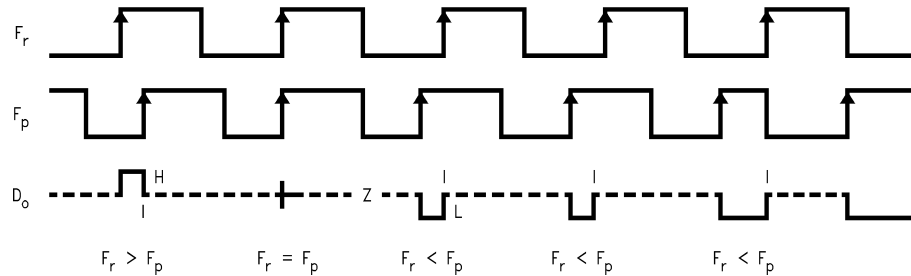
## 1.0 Functional Description (Continued)

### 1.5 PHASE/FREQUENCY DETECTORS

The Main and Aux phase/frequency detectors are driven from their respective N and R counter outputs. The maximum frequency for both the Main and Aux phase detector inputs is 10 MHz. The phase/frequency detector outputs control the respective charge pumps. The polarity of the pump-up or pump-down control signals are programmed using the **PD\_POL Main** or **PD\_POL Aux** control bits, de-

pending on whether the Main or Aux VCO characteristics are positive or negative. Refer to **Sections 2.4.2** and **2.6.2** for more details. The phase/frequency detectors have a detection range of  $-2\pi$  to  $+2\pi$ . The phase/frequency detectors also receive a feedback signal from the charge pump in order to eliminate dead zone.

#### PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



20022611

#### Notes:

1. The minimum width of the pump-up and pump-down current pulses occur at the  $D_o$  Main or  $D_o$  Aux pins when the loop is phase locked.
2. The diagram assumes positive VCO characteristics, i.e. **PD\_POL Main** or **PD\_POL Aux** = 1.
3.  $F_r$  is the phase detector input from the reference divider (R counter).
4.  $F_p$  is the phase detector input from the programmable feedback divider (N counter).
5.  $D_o$  refers to either the Main or Aux charge pump output.

### 1.6 CHARGE PUMPS

The charge pump directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of the VCO. The charge pump steers the VCO control voltage towards  $V_p$  Main or  $V_p$  Aux during pump-up events and towards GND during pump-down events. When locked,  $D_o$  Main or  $D_o$  Aux are primarily in a TRI-STATE mode with small corrections occurring at the phase comparator rate. The charge pump output current magnitude can be selected by toggling the **ID<sub>o</sub> Main** or **ID<sub>o</sub> Aux** control bits.

### 1.7 MICROWIRE SERIAL INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The supply for the MICROWIRE circuitry is separate from the rest of the IC to allow direct connection to 1.8V devices. The interface is comprised of three signal pins: Clock, Data and LE (Latch Enable). Serial data is clocked into the 22-bit shift register on the rising edge of Clock. The last two bits decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of four control registers depending on the state of the address bits. The MSB of Data is loaded in first. The synthesizers can be programmed even in power down mode. A complete programming description is provided in **Section 2.0 Programming Description**.

### 1.8 MULTI-FUNCTION OUTPUTS

The LMX2377U device's  $F_oLD$  output pin is a multi-function output that can be configured as the Main synthesizer Fast-Lock output, an open drain analog lock detect output, counter reset, or used to monitor the output of the various reference divider (R counter) or feedback divider (N counter) circuits. The  $F_oLD$  control word is used to select the desired output function. When the PLL is in powerdown mode, the  $F_oLD$  output is pulled to a LOW state. A complete programming description of the multi-function output is provided in **Section 2.8 F<sub>o</sub>LD**.

#### 1.8.1 Open Drain Analog Lock Detect Output

An analog lock detect status generated from the phase detector is available on the  $F_oLD$  output pin if selected. The lock detect output goes to a high impedance state when the charge pump is inactive. It goes low when the charge pump is active during a comparison cycle. When viewed with an oscilloscope, and when a pull-up resistor is used, narrow negative pulses are observed when the charge pump turns on. The lock detect output signal is an open drain configuration.

Three separate lock detect signals are routed to the multiplexer. Two of these monitor the 'lock' status of the individual synthesizers. The third detects the condition when both the Main and Aux synthesizers are in a 'locked state'. External circuitry however, is required to provide a steady DC signal to indicate when the PLL is in a locked state. Refer to **Section 2.8 F<sub>o</sub>LD** for details on how to program the different lock detect options.



## 1.0 Functional Description (Continued)

### 1.8.2 Open Drain FastLock Output

The LMX233xU Fastlock feature allows faster loop response time during lock acquisition. The loop response time (lock time) can be approximately halved if the loop bandwidth is doubled. In order to achieve this, the same gain/ phase relationship at twice the loop bandwidth must be maintained. This can be achieved by increasing the charge pump current from 0.95 mA ( $ID_0$  Main Bit = 0) in the steady state mode, to 3.8 mA ( $ID_0$  Main Bit = 1) in Fastlock. When the  $F_0LD$  output is configured as a FastLock output, an open drain device is enabled. The open drain device switches in a parallel resistor  $R2'$  to ground, of equal value to resistor  $R2$  of the external loop filter. The loop bandwidth is effectively doubled and stability is maintained. Once locked to the correct frequency, the PLL will return to a steady state condition. Refer to **Section 2.8  $F_0LD$**  for details on how to configure the  $F_0LD$  output to an open drain Fastlock output.

### 1.8.3 Counter Reset

Three separate counter reset functions are provided. When the  $F_0LD$  is programmed to **Reset Aux PLL Counters**, both the Aux feedback divider and the Aux reference divider are held at their load point. When the **Reset Main PLL Counters** is programmed, both the Main feedback divider and the Main reference divider are held at their load point. When the **Reset All Counters** mode is enabled, all feedback dividers and reference dividers are held at their load point. When the device is programmed to normal operation, both the feedback divider and reference divider are enabled and resume counting in 'close' alignment to each other. Refer to **Section 2.8  $F_0LD$**  for more details.

### 1.8.4 Reference Divider and Feedback Divider Output

The outputs of the various N and R divders can be monitored by selecting the appropriate  $F_0LD$  word. This is essential when performing  $OSC_{in}$  or  $f_{IN}$  sensitivity measurements. Refer to the **Test Setups** section for more details. Refer to **Section 2.8  $F_0LD$**  for details on how to route the appropriate divider output to the  $F_0LD$  pin.

## 1.9 POWER CONTROL

Each synthesizer in the LMX2377U device is individually power controlled by device powerdown bits. The powerdown word is comprised of the **PWDN Main (PWDN Aux)** bit, in conjunction with the **TRI-STATE  $ID_0$  Main (TRI-STATE  $ID_0$  Aux)** bit. The powerdown control word is used to set the operating mode of the device. Refer to **Sections 2.4.4, 2.5.4, 2.6.4, and 2.7.4** for details on how to program the Main or Aux powerdown bits.

When either the Main synthesizer or the Aux synthesizer enters the powerdown mode, the respective prescaler, phase detector, and charge pump circuit are disabled. The  $D_0$  Main ( $D_0$  Aux),  $f_{IN}$  Main ( $f_{IN}$  Aux), and  $\overline{f_{IN}}$  Main pins are all forced to a high impedance state. The reference divider and feedback divider circuits are held at the load point during powerdown. The oscillator buffer is disabled when both the Main and Aux synthesizers are powered down. The  $OSC_{in}$  pin is forced to a HIGH state through an approximate 100 k $\Omega$  resistance when this condition exists. When either synthesizer is activated, the respective prescaler, phase detector, charge pump circuit, and the oscillator buffer are all powered up. The feedback divider, and the reference divider are held at load point. This allows the reference oscillator, feedback divider, reference divider and prescaler circuitry to reach proper bias levels. After a finite delay, the feedback and reference dividers are enabled and they resume counting in 'close' alignment (the maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching data while in the powerdown mode.

### Synchronous Powerdown Mode

In this mode, the powerdown function is gated by the charge pump. When the device is configured for synchronous powerdown, the device will enter the powerdown mode upon completion of the next charge pump pulse event.

### Asynchronous Powerdown Mode

In this mode, the powerdown function is NOT gated by the completion of a charge pump pulse event. When the device is configured for asynchronous powerdown, the part will go into powerdown mode immediately.

TRI-STATE $ID_0$	PWDN	Operating Mode
0	0	PLL Active, Normal Operation
1	0	PLL Active, Charge Pump Output in High Impedance State
0	1	Synchronous Powerdown
1	1	Asynchronous Powerdown

#### Notes:

1. TRI-STATE  $ID_0$  refers to either the TRI-STATE  $ID_0$  Main or TRI-STATE  $ID_0$  Aux bit .
2. PWDN refers to either the PWDN Main or PWDN Aux bit.

## 2.0 Programming Description

### 2.1 MICROWIRE INTERFACE

The 22-bit shift register is loaded via the MICROWIRE interface. The shift register consists of a 20-bit Data[19:0] Field and a 2-bit Address[1:0] Field as shown below. The Address Field is used to decode the internal control register address. When LE transitions HIGH, data stored in the shift register is loaded into one of 4 control registers depending on the state of the address bits. The MSB of Data is loaded in first. The Data field assignments are shown in **Section 2.3 CONTROL REGISTER CONTENT MAP**.

MSB		LSB	
Data[19:0]		Address[1:0]	
21	2	1	0

### 2.2 CONTROL REGISTER LOCATION

The address bits Address[1:0] decode the internal register address. The table below shows how the address bits are mapped into the target control register.

Address[1:0] Field		Target Register
0	0	Aux R
0	1	Aux N
1	0	Main R
1	1	Main N

### 2.3 CONTROL REGISTER CONTENT MAP

The control register content map describes how the bits within each control register are allocated to specific control functions.

## 2.0 Programming Description (Continued)

### Control Register Content Map

Reg.	Most Significant Bit										SHIFR REGISTER BIT LOCATION										Least Significant Bit								
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
																						<i>Data Field</i>				<i>Address Field</i>			
<b>Aux R</b>	F <sub>o</sub> LD0	F <sub>o</sub> LD2	TRI-STATE ID <sub>o</sub> Aux	ID <sub>o</sub> Aux	PD <sub>-</sub> POL Aux	Aux R_CNTR[14:0]																0	0						
<b>Aux N</b>	PWDN Aux	PRE Aux	Aux N_CNTRB[12:0]																Aux N_CNTRA[4:0]	0	1								
<b>Main R</b>	F <sub>o</sub> LD1	F <sub>o</sub> LD3	TRI-STATE ID <sub>o</sub> Main	ID <sub>o</sub> Main	PD <sub>-</sub> POL Main	Main R_CNTR[14:0]																1	0						
<b>Main N</b>	PWDN Main	PRE Main	Main N_CNTRB[12:0]																Main N_CNTRA[4:0]	1	1								

## 2.0 Programming Description (Continued)

### 2.4 AUXILIARY R REGISTER

The Aux R register contains the Aux R\_CNTR, PD\_POL Aux, ID<sub>o</sub> Aux, and TRI-STATE ID<sub>o</sub> Aux control words, in addition to two bits that compose the F<sub>o</sub>LD control word. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	<i>Data Field</i>																			<i>Address Field</i>	
<b>Aux R</b>	F <sub>o</sub> LD0	F <sub>o</sub> LD2	TRI-STATE ID <sub>o</sub> Aux	ID <sub>o</sub> Aux	PD_POL Aux	Aux R_CNTR[14:0]														0	0

#### 2.4.1 Aux R\_CNTR[14:0] AUXILIARY SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) Aux R[2:16]

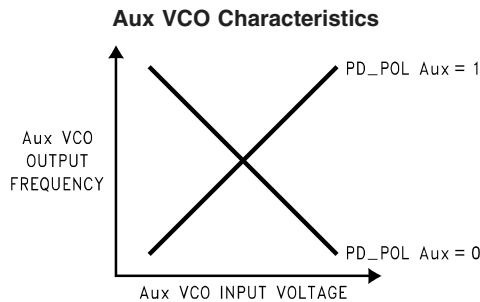
The Aux reference divider (Aux R\_CNTR) can be programmed to support divide ratios from 2 to 32767. Divide ratios less than 2 are prohibited.

Divide Ratio	Aux R_CNTR[14:0]															
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

#### 2.4.2 PD\_POL Aux AUXILIARY SYNTHESIZER PHASE DETECTOR POLARITY Aux R[17]

The PD\_POL Aux bit is used to control the Aux synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL Aux	Aux R[17]	Aux Phase Detector Polarity	Aux VCO Negative Tuning Characteristics	Aux VCO Positive Tuning Characteristics



#### 2.4.3 ID<sub>o</sub> Aux AUXILIARY SYNTHESIZER CHARGE PUMP CURRENT GAIN Aux R[18]

The ID<sub>o</sub> Aux bit controls the Aux synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID <sub>o</sub> Aux	Aux R[18]	Aux Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

## 2.0 Programming Description (Continued)

### 2.4.4 TRI-STATE ID<sub>o</sub> Aux AUXILIARY SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT Aux R[19]

The TRI-STATE ID<sub>o</sub> Aux bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID<sub>o</sub> Aux bit.

Furthermore, the TRI-STATE ID<sub>o</sub> Aux bit operates in conjunction with the PWDN Aux bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID <sub>o</sub> Aux	Aux R[19]	Aux Charge Pump TRI-STATE Current	Aux Charge Pump Normal Operation	Aux Charge Pump Output in High Impedance State

### 2.5 AUXILIARY N REGISTER

The Aux N register contains the Aux N\_CNTRA, Aux N\_CNTRB, PRE Aux, and PWDN Aux control words. The Aux N\_CNTRA and Aux N\_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																			Least Significant Bit	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	<i>Data Field</i>																			<i>Address Field</i>	
<b>Aux N</b>	PWDN Aux	PRE Aux	Aux N_CNTRB[12:0]												Aux N_CNTRA[4:0]				0	1	

### 2.5.1 Aux N\_CNTRA[4:0] AUXILIARY SYNTHESIZER SWALLOW COUNTER (A COUNTER) Aux N[2:6]

The Aux N\_CNTRA control word is used to setup the Aux synthesizer's A counter. The A counter is a 5-bit swallow counter used in the programmable feedback divider. The Aux N\_CNTRA control word can be programmed to values ranging from 0 to 31.

Divide Ratio	Aux N_CNTRA[4:0]				
	4	3	2	1	0
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

### 2.5.2 Aux N\_CNTRB[12:0] AUXILIARY SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER) Aux N[7:19]

The Aux N\_CNTRB control word is used to setup the Aux synthesizer's B counter. The B counter is a 13-bit programmable binary counter used in the programmable feedback divider. The Aux N\_CNTRB control word can be programmed to values ranging from 3 to 8191.

Divide Ratio	Aux N_CNTRB[12:0]												
	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

## 2.0 Programming Description (Continued)

### 2.5.3 PRE Aux AUXILIARY SYNTHESIZER PRESCALER SELECT

Aux N[20]

The Aux synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Function	
			0	1
PRE Aux	Aux N[20]	Aux Prescaler Select	8/9 Prescaler Selected	16/17 Prescaler Selected

### 2.5.4 PWDN Aux AUXILIARY SYNTHESIZER POWERDOWN

Aux N[21]

The PWDN Aux bit is used to switch the Aux PLL between a powered up and powered down mode.

Furthermore, the PWDN Aux bit operates in conjunction with the TRI-STATE ID<sub>0</sub> Aux bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN Aux	Aux N[21]	Aux Powerdown	Aux PLL Active	Aux PLL Powerdown

## 2.6 MAIN R REGISTER

The Main R register contains the Main R\_CNTR, PD\_POL Main, ID<sub>0</sub> Main, and TRI-STATE ID<sub>0</sub> Main control words, in addition to two bits that compose the F<sub>o</sub>LD control word. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																			Least Significant Bit	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	<i>Data Field</i>																			<i>Address Field</i>	
Main R	F <sub>o</sub> LD1	F <sub>o</sub> LD3	TRI-STATE ID <sub>0</sub> Main	ID <sub>0</sub> Main	PD_POL Main	Main R_CNTR[14:0]														1	0

### 2.6.1 Main R\_CNTR[14:0] MAIN SYNTHESIZER PROGRAMMABLE REFERENCE DIVIDER (R COUNTER) Main R[2:16]

The Main reference divider (Main R\_CNTR) can be programmed to support divide ratios from 2 to 32767. Divide ratios less than 2 are prohibited.

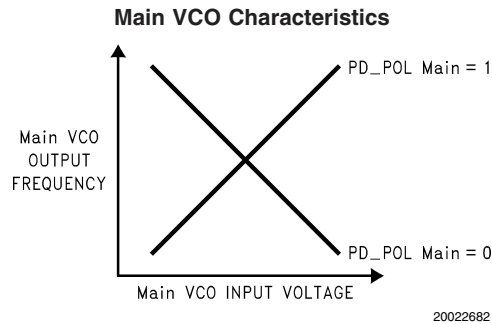
Divide Ratio	Main R_CNTR[14:0]															
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

## 2.0 Programming Description (Continued)

### 2.6.2 PD\_POL Main MAIN SYNTHESIZER PHASE DETECTOR POLARITY Main R[17]

The PD\_POL Main bit is used to control the Main synthesizer's phase detector polarity based on the VCO tuning characteristics.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL Main	Main R[17]	Main Phase Detector Polarity	Main VCO Negative Tuning Characteristics	Main VCO Positive Tuning Characteristics



### 2.6.3 ID<sub>o</sub> Main MAIN SYNTHESIZER CHARGE PUMP CURRENT GAIN Main R[18]

The ID<sub>o</sub> Main bit controls the Main synthesizer's charge pump gain. Two current levels are available.

Control Bit	Register Location	Description	Function	
			0	1
ID <sub>o</sub> Main	Main R[18]	Main Charge Pump Current Gain	LOW 0.95 mA	HIGH 3.80 mA

### 2.6.4 TRI-STATE ID<sub>o</sub> Main MAIN SYNTHESIZER CHARGE PUMP TRI-STATE CURRENT Main R[19]

The TRI-STATE ID<sub>o</sub> Main bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously with the change in the TRI-STATE ID<sub>o</sub> Main bit.

Furthermore, the TRI-STATE ID<sub>o</sub> Main bit operates in conjunction with the PWDN Main bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
TRI-STATE ID <sub>o</sub> Main	Main R[19]	Main Charge Pump TRI-STATE Current	Main Charge Pump Normal Operation	Main Charge Pump Output in High Impedance State

## 2.0 Programming Description (Continued)

### 2.7 MAIN N REGISTER

The Main N register contains the Main N\_CNTRA, Main N\_CNTRB, PRE Main, and PWDN Main control words. The Main N\_CNTRA and Main N\_CNTRB control words are used to setup the programmable feedback divider. The detailed description and programming information for each control word is discussed in the following sections.

Reg.	SHIFT REGISTER BIT LOCATION																					
	Most Significant Bit										Least Significant Bit											
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	<i>Data Field</i>																				<i>Address Field</i>	
Main N	PWDN Main	PRE Main	Main N_CNTRB[12:0]													Main N_CNTRA[4:0]				1	1	

#### 2.7.1 Main N\_CNTRA[4:0] MAIN SYNTHESIZER SWALLOW COUNTER (A COUNTER) Main N[2:6]

The Main N\_CNTRA control word is used to setup the Main synthesizer's A counter. The A counter is a 5-bit swallow counter used in the programmable feedback divider. The Main N\_CNTRA control word can be programmed to values ranging from 0 to 31.

Divide Ratio	Main N_CNTRA[4:0]				
	4	3	2	1	0
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

#### 2.7.2 Main N\_CNTRB[12:0] MAIN SYNTHESIZER PROGRAMMABLE BINARY COUNTER (B COUNTER) Main N[7:19]

The Main N\_CNTRB control word is used to setup the Main synthesizer's B counter. The B counter is a 13-bit programmable binary counter used in the programmable feedback divider. The Main N\_CNTRB control word can be programmed to values ranging from 3 to 8191.

Divide Ratio	Main N_CNTRB[12:0]												
	12	11	10	9	8	7	6	5	4	3	2	1	0
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8191	1	1	1	1	1	1	1	1	1	1	1	1	1

#### 2.7.3 PRE Main MAIN SYNTHESIZER PRESCALER SELECT Main N[20]

The Main synthesizer utilizes a selectable dual modulus prescaler.

Control Bit	Register Location	Description	Function	
			0	1
PRE Main	Main N[20]	Main Prescaler Select	16/17 Prescaler Selected	32/33 Prescaler Selected

#### 2.7.4 PWDN Main MAIN SYNTHESIZER POWERDOWN Main N[21]

The PWDN Main bit is used to switch the Main PLL between a powered up and powered down mode.

Furthermore, the PWDN Main bit operates in conjunction with the TRI-STATE ID<sub>0</sub> Main bit to set a synchronous or an asynchronous powerdown mode.

Control Bit	Register Location	Description	Function	
			0	1
PWDN Main	Main N[21]	Main Powerdown	Main PLL Active	Main PLL Powerdown



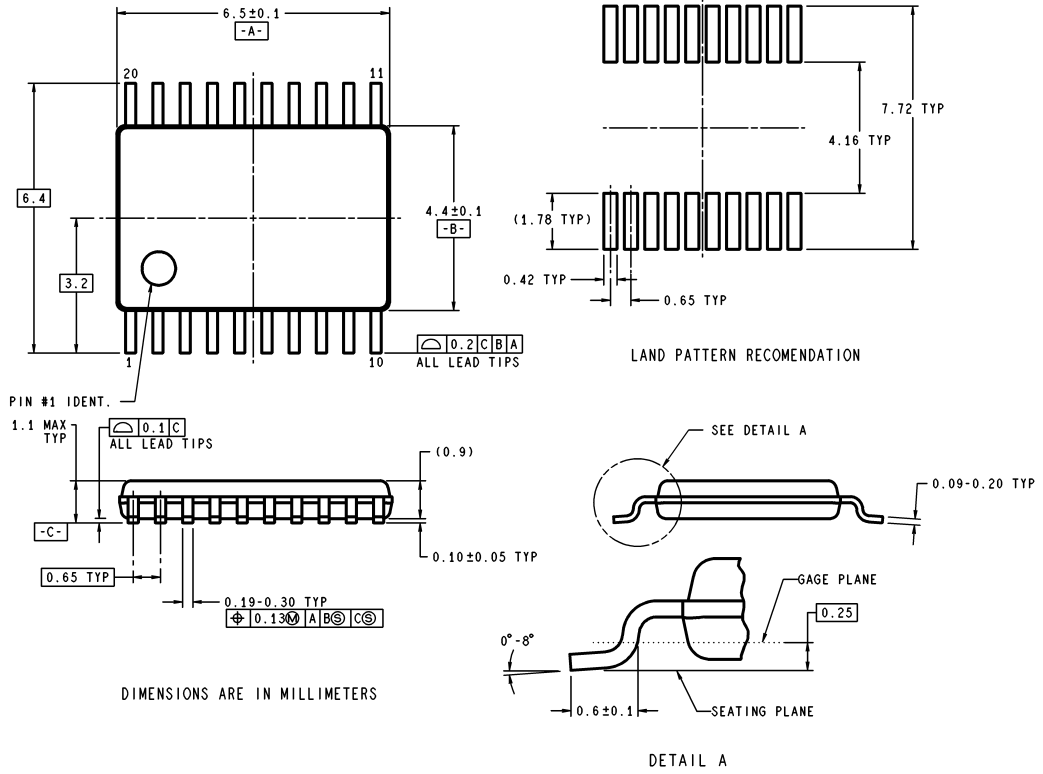
## 2.0 Programming Description (Continued)

### 2.8 F<sub>o</sub>LD[3:0] MULTI-FUNCTION OUTPUT SELECT [Main R[20], Aux R[20], Main R [21], Aux R[21]]

The F<sub>o</sub>LD control word is used to select which signal is routed to the F<sub>o</sub>LD pin.

F <sub>o</sub> LD3	F <sub>o</sub> LD2	F <sub>o</sub> LD1	F <sub>o</sub> LD0	F <sub>o</sub> LD Output State
0	0	0	0	LOW Logic State Output
0	0	0	1	Aux PLL R Divider Output, Push-Pull Output
0	0	1	0	Main PLL R Divider Output, Push-Pull Output
0	0	1	1	Open Drain Fastlock Output
0	1	0	0	Aux PLL Analog Lock Detect, Open Drain Output
0	1	0	1	Aux PLL N Divider Output, Push-Pull Output
0	1	1	0	Main PLL N Divider Output, Push-Pull Output
0	1	1	1	Reset Aux PLL Counters, LOW Logic State Output
1	0	0	0	Main PLL Analog Lock Detect, Open Drain Output
1	0	0	1	Aux PLL R Divider Output, Push-Pull Output
1	0	1	0	Main PLL R Divider Output, Push-Pull Output
1	0	1	1	Reset Main PLL Counters, LOW Logic State Output
1	1	0	0	Main and Aux Analog Lock Detect, Open Drain Output
1	1	0	1	Aux PLL N Divider Output, Push-Pull Output
1	1	1	0	Main PLL N Divider Output, Push-Pull Output
1	1	1	1	Reset All Counters, LOW Logic State Output

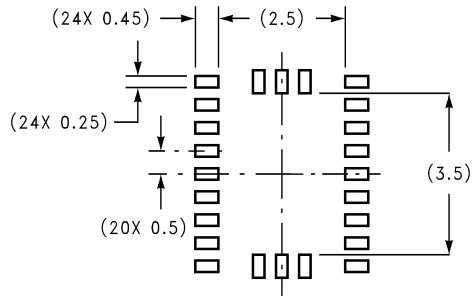
**Physical Dimensions** inches (millimeters) unless otherwise noted



MTC20 (Rev D)

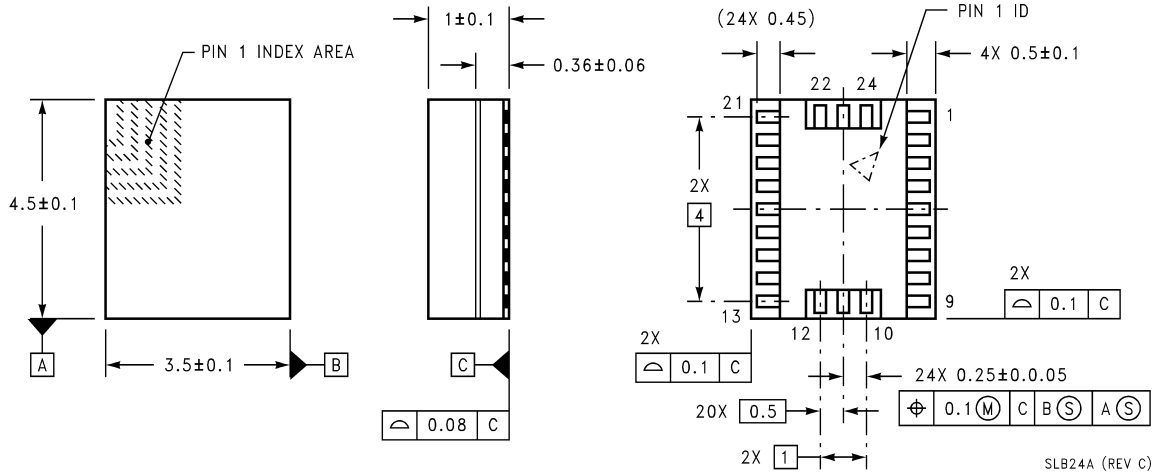
**20-Pin Thin Shrink Small Outline Package (TM)  
NS Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

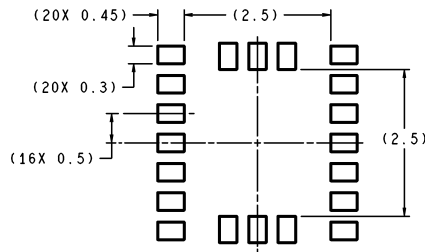
**RECOMMENDED LAND PATTERN**  
1:1 RATIO WITH PACKAGE SOLDER PADS



SLB24A (REV C)

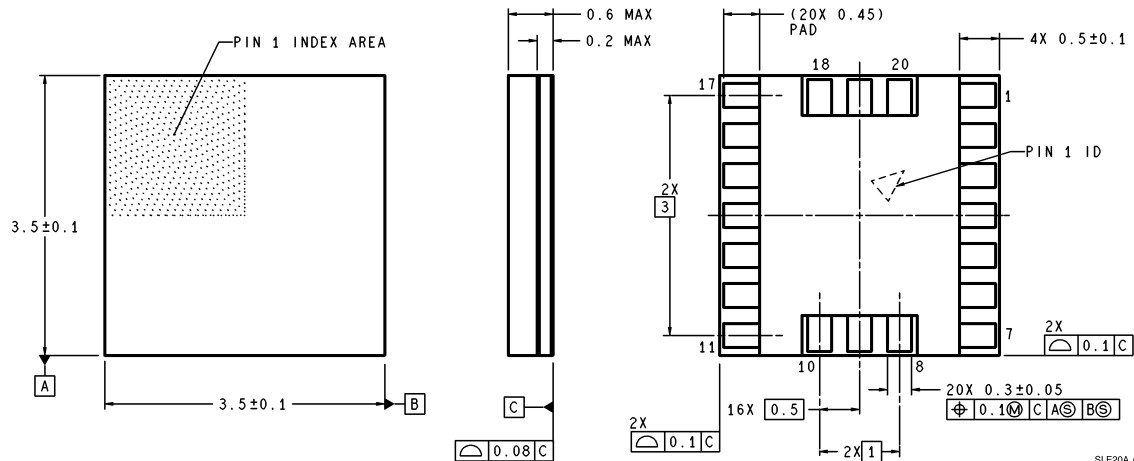
**24-Pin Chip Scale Package (SLB)**  
**NS Package Number SLB24A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



RECOMMENDED LAND PATTERN  
1:1 RATIO WITH PACKAGE SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



20-Pin Ultra Thin Chip Scale Package (SLE)  
NS Package Number SLE20A

SLE20A (Rev A)

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Email: support@nsc.com

www.national.com

**National Semiconductor Europe**

Fax: +49 (0) 180-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia Pacific Customer Response Group**

Tel: 65-2544466  
Fax: 65-2504466  
Email: ap.support@nsc.com

**National Semiconductor Japan Ltd.**

Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507