

# CD4046BM/CD4046BC Micropower Phase-Locked Loop

## General Description

The CD4046B micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO<sub>IN</sub> input, and the capacitor and resistors connected to pin C1<sub>A</sub>, C1<sub>B</sub>, R1 and R2.

The source follower output of the VCO<sub>IN</sub> (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

## Features

- Wide supply voltage range 3.0V to 18V
- Low dynamic power consumption 70 μW (typ.) at  $f_o = 10 \text{ kHz}$ ,  $V_{DD} = 5V$
- VCO frequency 1.3 MHz (typ.) at  $V_{DD} = 10V$
- Low frequency drift with temperature 0.06%/°C at  $V_{DD} = 10V$
- High VCO linearity 1% (typ.)

## Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

## Block & Connection Diagrams

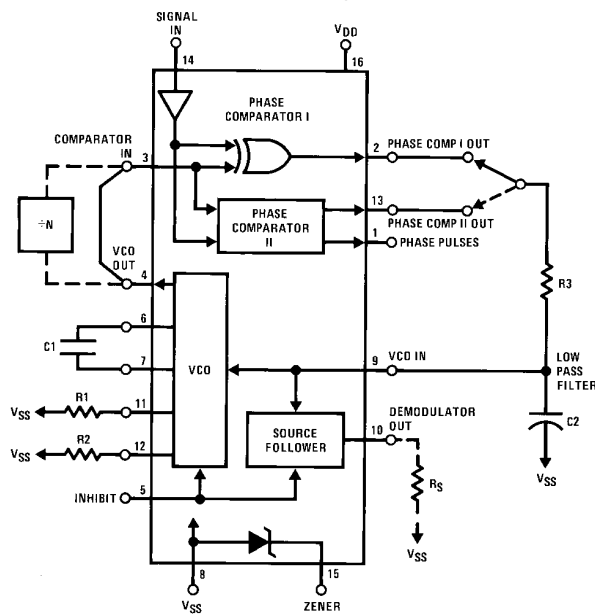
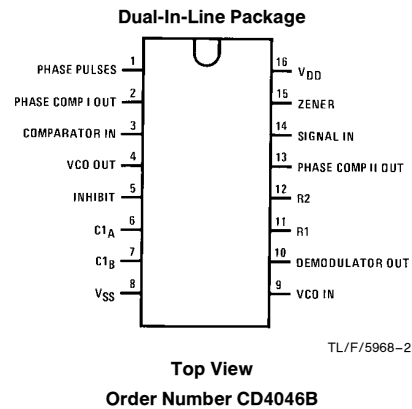


FIGURE 1

TL/F/5968-1



CD4046BM/CD4046BC Micropower Phase-Locked Loop

## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage ( $V_{DD}$ )	-0.5 to +18 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 to $V_{DD}$ + 0.5 $V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

## Recommended Operating Conditions (Note 2)

DC Supply Voltage ( $V_{DD}$ )	3 to 15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ $V_{DC}$
Operating Temperature Range ( $T_A$ )	
CD4046BM	-55°C to +125°C
CD4046BC	-40°C to +85°C

## DC Electrical Characteristics CD4046BM (Note 2)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	Pin 5 = $V_{DD}$ , Pin 14 = $V_{DD}$ , Pin 3, 9 = $V_{SS}$ $V_{DD}$ = 5V $V_{DD}$ = 10V $V_{DD}$ = 15V		5	0.005	5		150	$\mu A$	
				10	0.01	10		300	$\mu A$	
				20	0.015	20		600	$\mu A$	
		Pin 5 = $V_{DD}$ , Pin 14 = Open, Pin 3, 2 = $V_{SS}$ $V_{DD}$ = 5V $V_{DD}$ = 10V $V_{DD}$ = 15V		45	5	35		185	$\mu A$	
			450	20	350		650	$\mu A$		
			1200	50	900		1500	$\mu A$		
$V_{OL}$	Low Level Output Voltage	$V_{DD}$ = 5V		0.05	0	0.05		0.05	V	
		$V_{DD}$ = 10V		0.05	0	0.05		0.05	V	
		$V_{DD}$ = 15V		0.05	0	0.05		0.05	V	
$V_{OH}$	High Level Output Voltage	$V_{DD}$ = 5V	4.95		4.95	5		4.95	V	
		$V_{DD}$ = 10V	9.95		9.95	10		9.95	V	
		$V_{DD}$ = 15V	14.95		14.95	15		14.95	V	
$V_{IL}$	Low Level Input Voltage Comparator and Signal In	$V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V		1.5	2.25	1.5		1.5	V	
		$V_{DD}$ = 10V, $V_O$ = 1V or 9V		3.0	4.5	3.0		3.0	V	
		$V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V		4.0	6.25	4.0		4.0	V	
$V_{IH}$	High Level Input Voltage Comparator and Signal In	$V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V	3.5		3.5	2.75		3.5	V	
		$V_{DD}$ = 10V, $V_O$ = 1V or 9V	7.0		7.0	5.5		7.0	V	
		$V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V	11.0		11.0	8.25		11.0	V	
$I_{OL}$	Low Level Output Current (Note 4)	$V_{DD}$ = 5V, $V_O$ = 0.4V	0.64		0.51	0.88		0.36	mA	
		$V_{DD}$ = 10V, $V_O$ = 0.5V	1.6		1.3	2.25		0.9	mA	
		$V_{DD}$ = 15V, $V_O$ = 1.5V	4.2		3.4	8.8		2.4	mA	
$I_{OH}$	High Level Output Current (Note 4)	$V_{DD}$ = 5V, $V_O$ = 4.6V	-0.64		-0.51	-0.88		-0.36	mA	
		$V_{DD}$ = 10V, $V_O$ = 9.5V	-1.6		-1.3	-2.25		-0.9	mA	
		$V_{DD}$ = 15V, $V_O$ = 13.5V	-4.2		-3.4	-8.8		-2.4	mA	
$I_{IN}$	Input Current	All Inputs Except Signal Input $V_{DD}$ = 14V, $V_{IN}$ = 0V $V_{DD}$ = 15V, $V_{IN}$ = 15V		-0.1		-10 <sup>-5</sup>	-0.1		$\mu A$	
				0.1		10 <sup>-5</sup>	0.1		1.0	$\mu A$
$C_{IN}$	Input Capacitance	Any Input (Note 3)						7.5	pF	
$P_T$	Total Power Dissipation	$f_o$ = 10 kHz, $R_1$ = 1 M $\Omega$ $R_2$ = $\infty$ , $V_{CO_{IN}}$ = $V_{DD}/2$ $V_{DD}$ = 5V $V_{DD}$ = 10V $V_{DD}$ = 15V				0.07			mW	
						0.6			mW	
						2.4			mW	

## DC Electrical Characteristics CD4046BC (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I <sub>DD</sub>	Quiescent Device Current	Pin 5 = V <sub>DD</sub> , Pin 14 = V <sub>DD</sub> , Pin 3, 9 = V <sub>SS</sub> V <sub>DD</sub> = 5V		20		0.005	20		150	μA
		V <sub>DD</sub> = 10V		40		0.01	40		300	μA
		V <sub>DD</sub> = 15V		80		0.015	80		600	μA
		Pin 5 = V <sub>DD</sub> , Pin 14 = Open, Pin 3, 9 = V <sub>SS</sub> V <sub>DD</sub> = 5V		70		5	55		205	μA
		V <sub>DD</sub> = 10V		530		20	410		710	μA
		V <sub>DD</sub> = 15V		1500		50	1200		1800	μA
V <sub>OL</sub>	Low Level Output Voltage	V <sub>DD</sub> = 5V		0.05		0	0.05		0.05	V
		V <sub>DD</sub> = 10V		0.05		0	0.05		0.05	V
		V <sub>DD</sub> = 15V		0.05		0	0.05		0.05	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>DD</sub> = 5V	4.95		4.95	5		4.95		V
		V <sub>DD</sub> = 10V	9.95		9.95	10		9.95		V
		V <sub>DD</sub> = 15V	14.95		14.95	15		14.95		V
V <sub>IL</sub>	Low Level Input Voltage Comparator and Signal In	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1V or 9V		3.0		4.5	3.0		3.0	V
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V <sub>IH</sub>	High Level Input Voltage Comparator and Signal In	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1V or 9V	7.0		7.0	5.5		7.0		V
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I <sub>OL</sub>	Low Level Output Current (Note 4)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.4V	0.52		0.44	0.88		0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 0.5V	1.3		1.1	2.25		0.9		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V	3.6		3.0	8.8		2.4		mA
I <sub>OH</sub>	High Level Output Current (Note 4)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 13.5V	-3.6		-3.0	-8.8		-2.4		mA
I <sub>IN</sub>	Input Current	All Inputs Except Signal Input V <sub>DD</sub> = 15V, V <sub>IN</sub> = 0V		-0.3		-10 <sup>-5</sup>	-0.3		-1.0	μA
		V <sub>DD</sub> = 15V, V <sub>IN</sub> = 15V		0.3		10 <sup>-5</sup>	0.3		1.0	μA
C <sub>IN</sub>	Input Capacitance	Any Input (Note 3)					7.5			pF
P <sub>T</sub>	Total Power Dissipation	f <sub>o</sub> = 10 kHz, R1 = 1 MΩ, R2 = ∞, VCO <sub>IN</sub> = V <sub>DD</sub> /2								
		V <sub>DD</sub> = 5V				0.07				mW
		V <sub>DD</sub> = 10V				0.6				mW
		V <sub>DD</sub> = 15V				2.4				mW

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** V<sub>SS</sub> = 0V unless otherwise specified.

**Note 3:** Capacitance is guaranteed by periodic testing.

**Note 4:** I<sub>OH</sub> and I<sub>OL</sub> are tested one output at a time.

## AC Electrical Characteristics\* CD4046BM/CD4046BC $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>VCO SECTION</b>						
$I_{DD}$	Operating Current	$f_o = 10\text{ kHz}$ , $R1 = 1\text{ M}\Omega$ , $R2 = \infty$ , $V_{COIN} = V_{DD}/2$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		20 90 200		$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
$f_{MAX}$	Maximum Operating Frequency	$C1 = 50\text{ pF}$ , $R1 = 10\text{ k}\Omega$ , $R2 = \infty$ , $V_{COIN} = V_{DD}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$	0.4 0.6 1.0	0.8 1.2 1.6		MHz MHz MHz
	Linearity	$V_{COIN} = 2.5\text{V} \pm 0.3\text{V}$ , $R1 \geq 10\text{ k}\Omega$ , $V_{DD} = 5\text{V}$		1		%
		$V_{COIN} = 5\text{V} \pm 2.5\text{V}$ , $R1 \geq 400\text{ k}\Omega$ , $V_{DD} = 10\text{V}$		1		%
		$V_{COIN} = 7.5\text{V} \pm 5\text{V}$ , $R1 \geq 1\text{ M}\Omega$ , $V_{DD} = 15\text{V}$		1		%
	Temperature-Frequency Stability No Frequency Offset, $f_{MIN} = 0$	$\% / ^\circ\text{C} \propto 1/f$ , $V_{DD}$ $R2 = \infty$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		0.12–0.24 0.04–0.08 0.015–0.03		$\% / ^\circ\text{C}$ $\% / ^\circ\text{C}$ $\% / ^\circ\text{C}$
Frequency Offset, $f_{MIN} \neq 0$	$V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		0.06–0.12 0.05–0.1 0.03–0.06		$\% / ^\circ\text{C}$ $\% / ^\circ\text{C}$ $\% / ^\circ\text{C}$	
$V_{COIN}$	Input Resistance	$V_{DD} = 5\text{V}$		$10^6$		$\text{M}\Omega$
		$V_{DD} = 10\text{V}$		$10^6$		$\text{M}\Omega$
		$V_{DD} = 15\text{V}$		$10^6$		$\text{M}\Omega$
VCO	Output Duty Cycle	$V_{DD} = 5\text{V}$		50		%
		$V_{DD} = 10\text{V}$		50		%
		$V_{DD} = 15\text{V}$		50		%
$t_{THL}$	VCO Output Transition Time	$V_{DD} = 5\text{V}$		90	200	ns
$t_{THL}$		$V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		50 45	100 80	ns ns

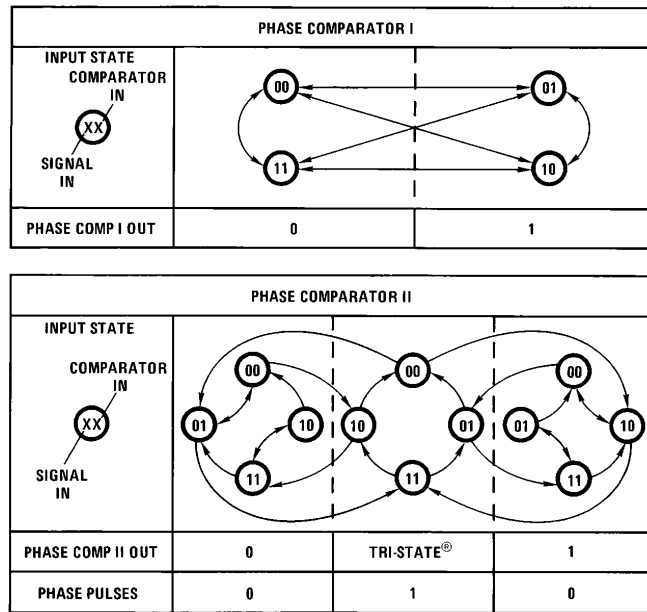
\*AC Parameters are guaranteed by DC correlated testing.

**AC Electrical Characteristics\*** CD4046BM/CD4046BC  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$  (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>PHASE COMPARATORS SECTION</b>							
$R_{IN}$	Input Resistance Signal Input	$V_{DD} = 5\text{V}$	1	3		$\text{M}\Omega$	
		$V_{DD} = 10\text{V}$	0.2	0.7		$\text{M}\Omega$	
		$V_{DD} = 15\text{V}$	0.1	0.3		$\text{M}\Omega$	
	Comparator Input	$V_{DD} = 5\text{V}$			$10^6$		$\text{M}\Omega$
		$V_{DD} = 10\text{V}$			$10^6$		$\text{M}\Omega$
		$V_{DD} = 15\text{V}$			$10^6$		$\text{M}\Omega$
AC-Coupled Signal Input Voltage Sensitivity	$C_{SERIES} = 1000\text{ pF}$ $f = 50\text{ kHz}$	$V_{DD} = 5\text{V}$		200	400	mV	
		$V_{DD} = 10\text{V}$		400	800	mV	
		$V_{DD} = 15\text{V}$		700	1400	mV	
<b>DEMODULATOR OUTPUT</b>							
$V_{COIN-}$ $V_{DEM}$	Offset Voltage	$R_S \geq 10\text{ k}\Omega$ , $V_{DD} = 5\text{V}$		1.50	2.2	V	
		$R_S \geq 10\text{ k}\Omega$ , $V_{DD} = 10\text{V}$		1.50	2.2	V	
		$R_S \geq 50\text{ k}\Omega$ , $V_{DD} = 15\text{V}$		1.50	2.2	V	
	Linearity	$R_S \geq 50\text{ k}\Omega$					
		$V_{COIN} = 2.5\text{V} \pm 0.3\text{V}$ , $V_{DD} = 5\text{V}$		0.1			%
	$V_{COIN} = 5\text{V} \pm 2.5\text{V}$ , $V_{DD} = 10\text{V}$		0.6			%	
	$V_{COIN} = 7.5\text{V} \pm 5\text{V}$ , $V_{DD} = 15\text{V}$		0.8			%	
<b>ZENER DIODE</b>							
$V_Z$	Zener Diode Voltage	$I_Z = 50\text{ }\mu\text{A}$	6.3	7.0	7.7	V	
$R_Z$	Zener Dynamic Resistance	$I_Z = 1\text{ mA}$		100		$\Omega$	

\*AC Parameters are guaranteed by DC correlated testing.

## Phase Comparator State Diagrams



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FIGURE 2

## Typical Waveforms

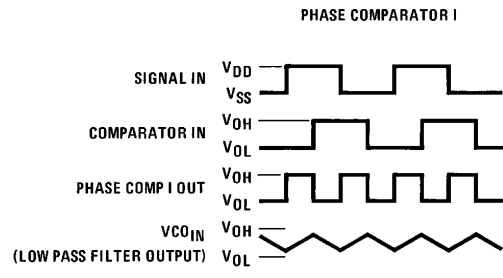


FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition

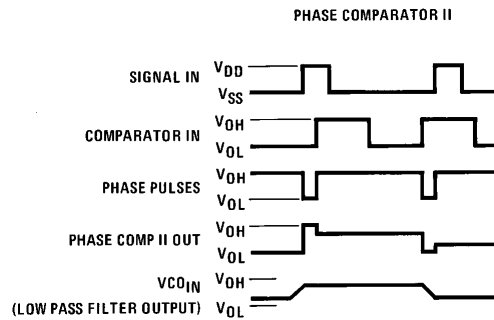
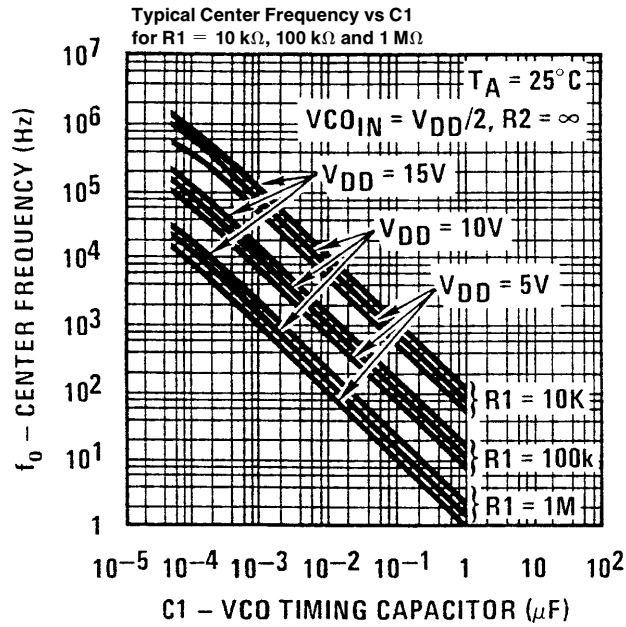


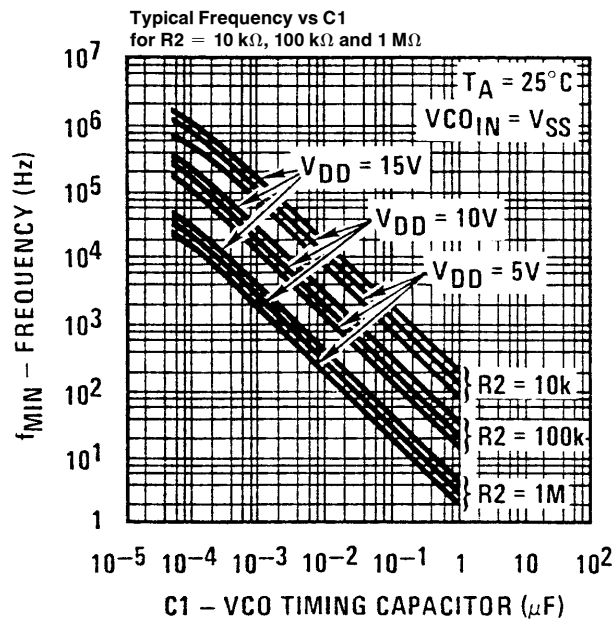
FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

## Typical Performance Characteristics



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FIGURE 5a



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FIGURE 5b

**Note:** To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I,  $P_D(\text{Total}) = P_D(f_0) + P_D(f_{MIN}) + P_D(R_S)$ ; Phase Comparator II,  $P_D(\text{Total}) = P_D(f_{MIN})$ .

Typical Performance Characteristics (Continued)

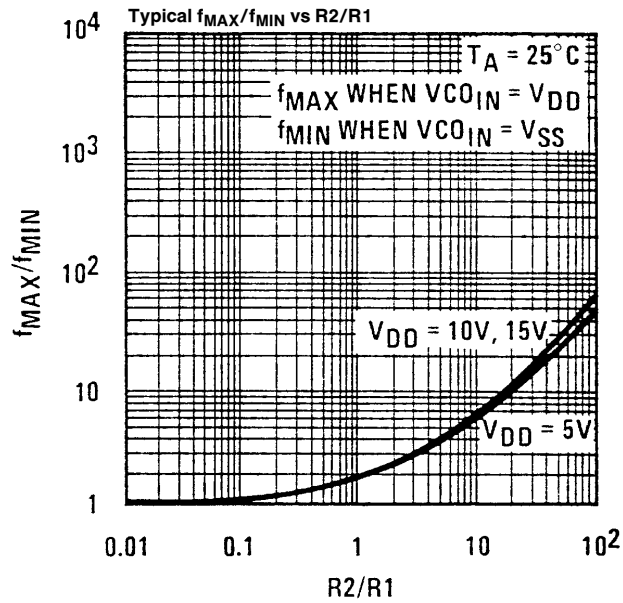


FIGURE 5C

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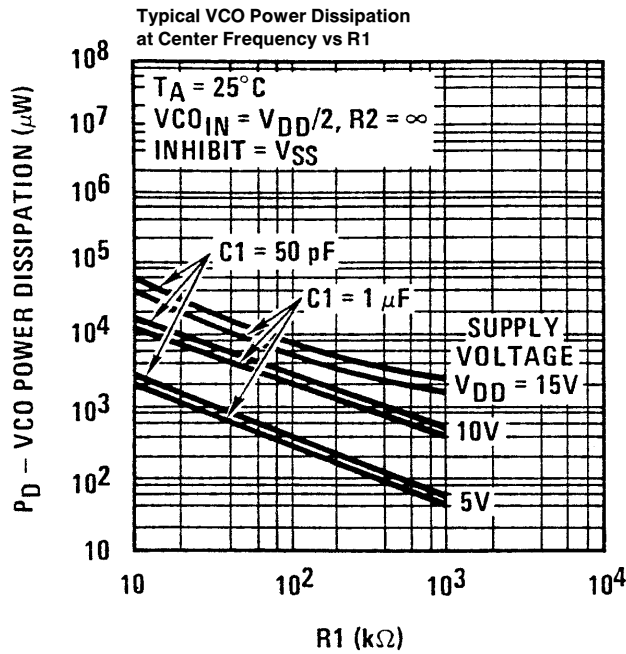


FIGURE 6a

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Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I,  $P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S)$ ; Phase Comparator II,  $P_D (Total) = P_D (f_{MIN})$ .



**Typical Performance Characteristics** (Continued)

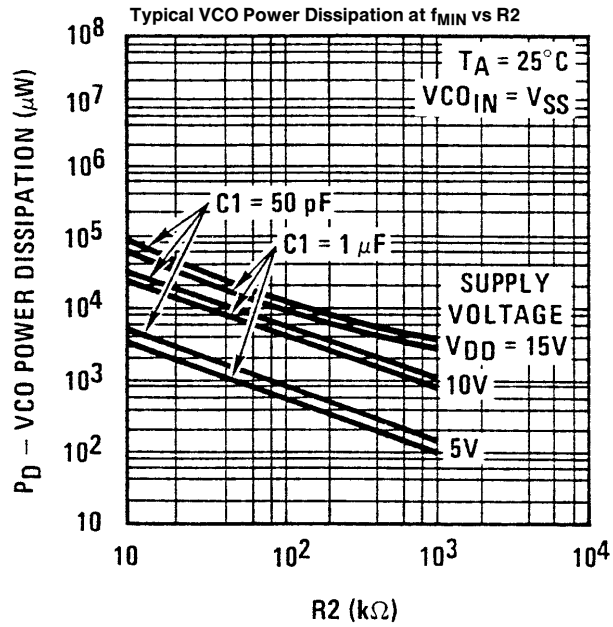


FIGURE 6b

TL/F/5968-16

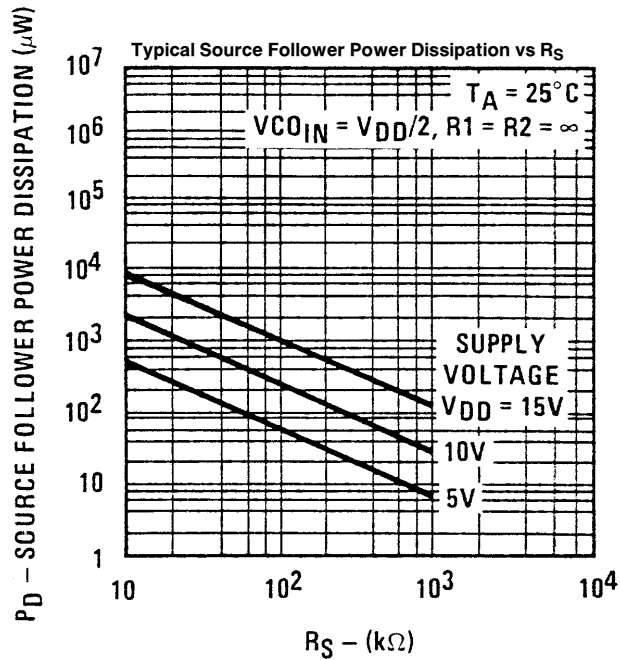
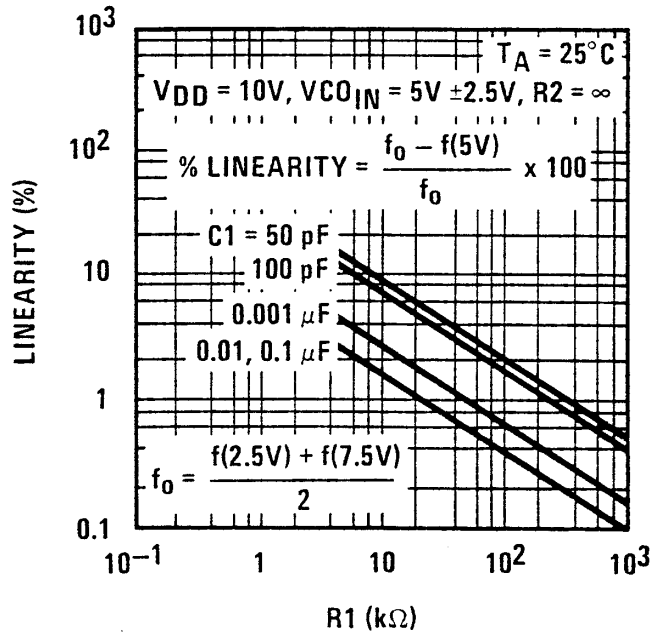


FIGURE 6c

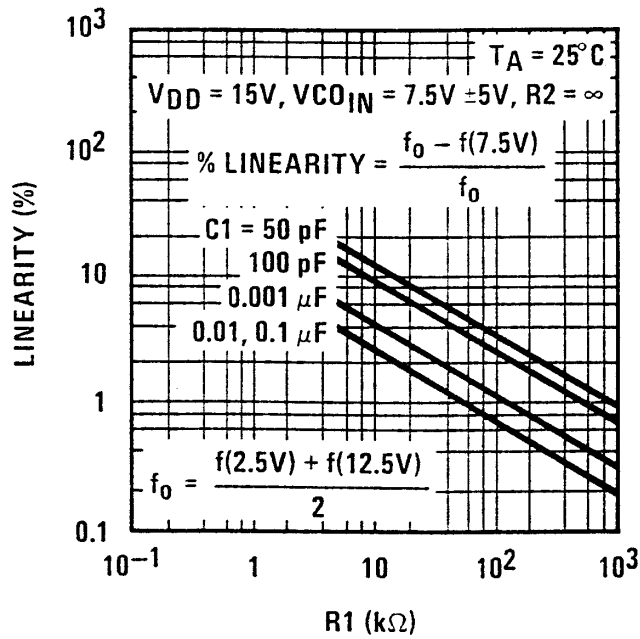
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**Note:** To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I,  $P_D(\text{Total}) = P_D(f_0) + P_D(f_{MIN}) + P_D(R_S)$ ; Phase Comparator II,  $P_D(\text{Total}) = P_D(f_{MIN})$ .

Typical Performance Characteristics (Continued)



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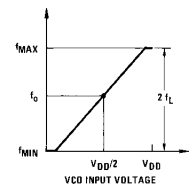
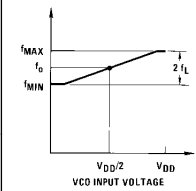
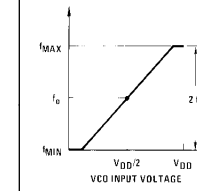
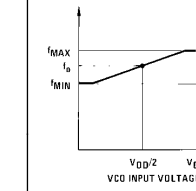
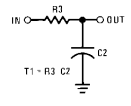
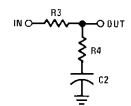
FIGURE 7. Typical VCO Linearity vs R1 and C1

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I,  $P_D(\text{Total}) = P_D(f_0) + P_D(f_{\text{MIN}}) + P_D(R_S)$ ; Phase Comparator II,  $P_D(\text{Total}) = P_D(f_{\text{MIN}})$ .

## Design Information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges:  $R_1, R_2 \geq 10 \text{ k}\Omega$ ,  $R_S \geq 10 \text{ k}\Omega$ ,  $C_1 \geq 50 \text{ pF}$ .

In addition to the given design information, refer to *Figure 5* for  $R_1, R_2$  and  $C_1$  component selections.

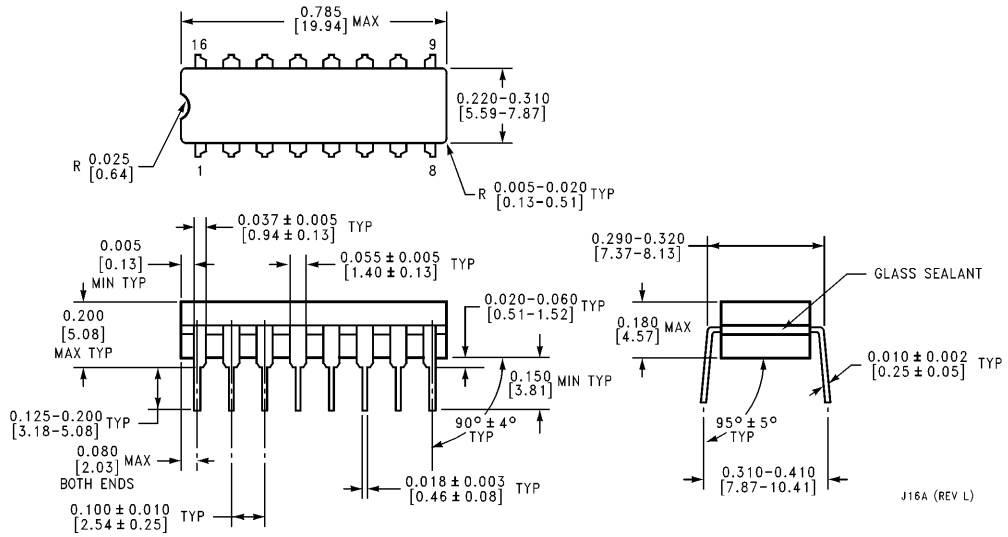
Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset $R_2 = \infty$	VCO With Offset	VCO Without Offset $R_2 = \infty$	VCO With Offset
VCO Frequency	 TL/F/5968-7	 TL/F/5968-8	 TL/F/5968-9	 TL/F/5968-10
For No Signal Input	VCO in PLL system will adjust to center frequency, $f_0$		VCO in PLL system will adjust to lowest operating frequency, $f_{\min}$	
Frequency Lock Range, $2 f_L$	$2 f_L = \text{full VCO frequency range}$ $2 f_L = f_{\max} - f_{\min}$			
Frequency Capture Range, $2 f_C$	 TL/F/5968-11		$2 f_C \approx \frac{1}{\pi} \sqrt{\frac{2 \pi f_L}{\tau_1}}$	
Loop Filter Component Selection	 TL/F/5968-12		$f_C = f_L$  For $2 f_C$ , see Ref.	
Phase Angle Between Single and Comparator	90° at center frequency ( $f_0$ ), approximating 0° and 180° at ends of lock range ( $2 f_L$ )		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	Given: $f_0$ . Use $f_0$ with <i>Figure 5a</i> to determine $R_1$ and $C_1$ .	Given: $f_0$ and $f_L$ . Calculate $f_{\min}$ from the equation $f_{\min} = f_0 - f_L$ . Use $f_{\min}$ with <i>Figure 5b</i> to determine $R_2$ and $C_1$ . Calculate $\frac{f_{\max}}{f_{\min}}$ from the equation $\frac{f_{\max}}{f_{\min}} = \frac{f_0 + f_L}{f_0 - f_L}$ . Use $\frac{f_{\max}}{f_{\min}}$ with <i>Figure 5c</i> to determine ratio $R_2/R_1$ to obtain $R_1$ .	Given: $f_{\max}$ . Calculate $f_0$ from the equation $f_0 = \frac{f_{\max}}{2}$ . Use $f_0$ with <i>Figure 5a</i> to determine $R_1$ and $C_1$ .	Given: $f_{\min}$ and $f_{\max}$ . Use $f_{\min}$ with <i>Figure 5b</i> to determine $R_2$ and $C_1$ . Calculate $\frac{f_{\max}}{f_{\min}}$ . Use $\frac{f_{\max}}{f_{\min}}$ with <i>Figure 5c</i> to determine ratio $R_2/R_1$ to obtain $R_1$ .

## References

- G.S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.  
 Floyd Gardner, "Phaselock Techniques", John Wiley & Sons, 1966.



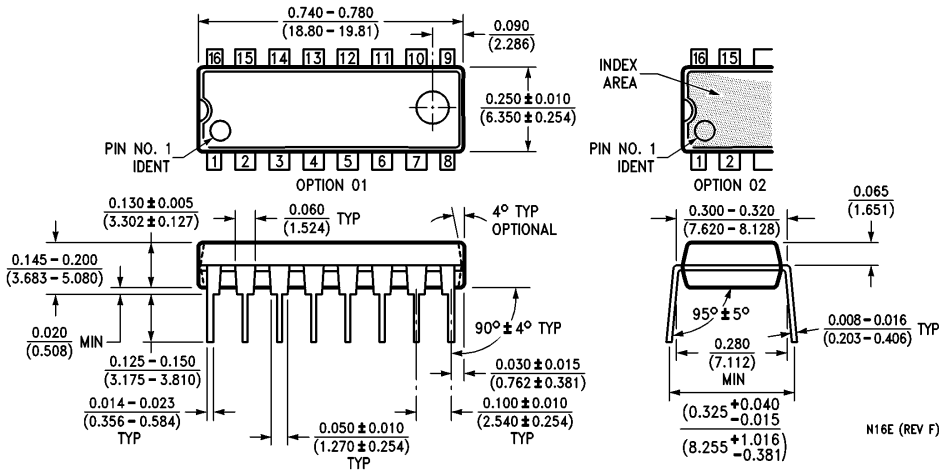
**Physical Dimensions** inches (millimeters)



**Order Number CD4046BMJ or CD4046BCJ**  
**NS Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) (Continued)



**Order Number CD4046BMN or CD4046BCN  
NS Package Number N16E**

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