

## 2-CHANNEL ELECTRONIC VOLUME WITH INPUT SELECTOR

### ■ GENERAL DESCRIPTION

NJW1154 is a two channel electronic volume with 6 in 1 out selector IC. It's suitable for Input signal trimmer of audio equipments such as DVD recorder and VCR. These functions are controlled by I<sup>2</sup>C Bus.

### ■ PACKAGE OUTLINE

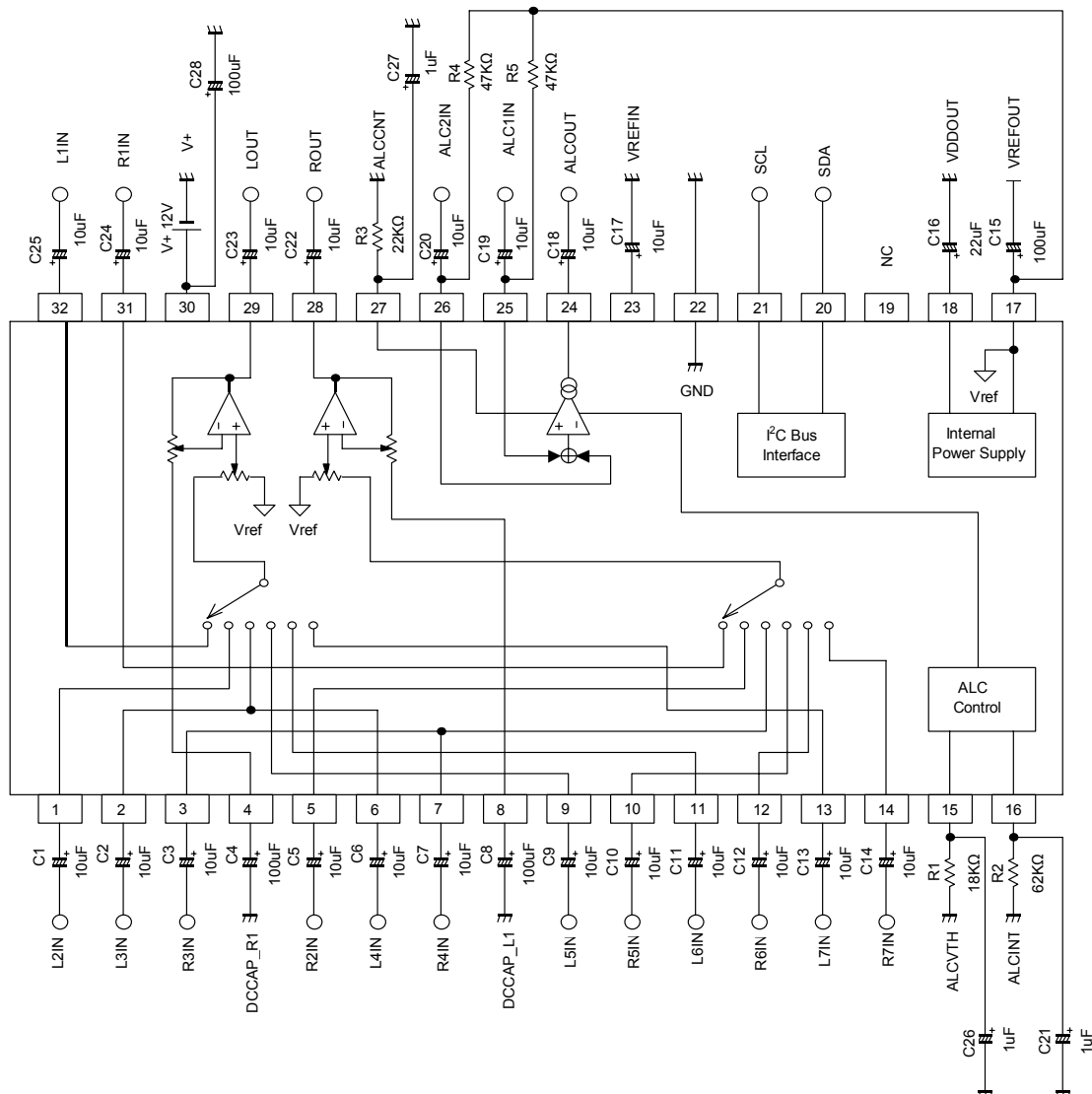


NJW1154V

### ■ FEATURES

- Operating Voltage 8 to 13V
- I<sup>2</sup>C Bus control
- 6in 1out Input Selector
- Volume +12 to -12dB/3dBstep, MUTE
- Bi-CMOS Technology
- Package Outline SSOP32

### ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V+	15	V
Power Dissipation	P <sub>D</sub>	800 NOTE: EIA/JEDEC STANDARD Test board (76.2x114.3x1.6mm, 2layer, FR-4) mounting	mW
Operating Temperature Range	Topr	-20 to +75	°C
Storage Temperature Range	Tstg	-40 to +125	°C

## ■ ELECTRICAL CHARACTERISTICS (Ta=25°C, V<sup>+</sup>=+12V, R<sub>L</sub>=47kΩ)

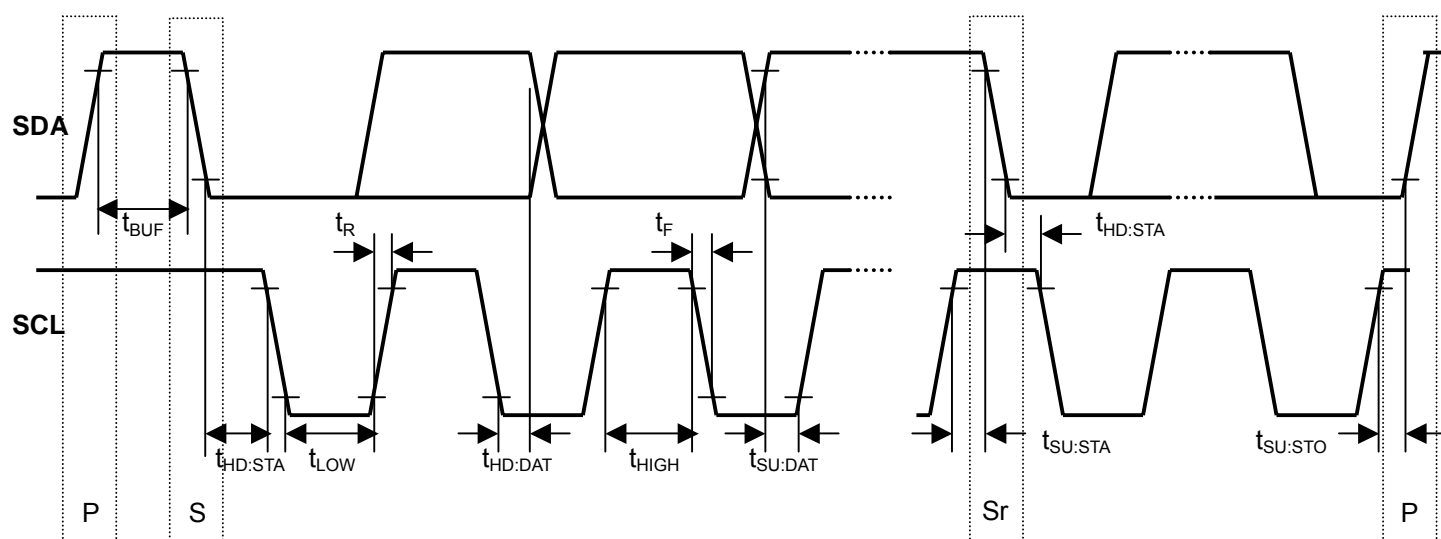
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
<b>◆ Power Supply</b>						
Operating Voltage	V+		8	12	13	V
Reference Voltage	V <sub>ref</sub>		5.5	6	6.5	V
Supply Current	I <sub>CC</sub>	No signal	-	7	9	mA
<b>◆ Input/Output Characteristics (Output)</b>						
Maximum Output Voltage	V <sub>OM</sub>	f=1KHz, THD=1% Volume=0dB	3.2	3.7	-	Vrms
Voltage Gain 1	G <sub>V1</sub>	V <sub>IN</sub> =1Vrms, f=1kHz Volume=0dB	-0.5	0	0.5	dB
Voltage Gain 2	G <sub>V2</sub>	V <sub>IN</sub> =0.25Vrms, f=1kHz Volume=+12dB	+11	+12	+13	dB
Voltage Gain 3	G <sub>V3</sub>	V <sub>IN</sub> =2.5Vrms, f=1kHz Volume=-12dB	-13	-12	-11	dB
Voltage Gain Error 1	ΔG <sub>V1</sub>	V <sub>IN</sub> =0.25Vrms, f=1kHz Volume=+12dB, Ach - Bch	-0.5	0	0.5	dB
Voltage Gain Error 2	ΔG <sub>V2</sub>	V <sub>IN</sub> =2.5Vrms, f=1kHz Volume=-12dB, Ach - Bch	-0.5	0	0.5	dB
Maximum Attenuation	A <sub>TT</sub>	f=1KHz, V <sub>IN</sub> =1Vrms Volume=Mute, A-weighted	-	-110	-	dB
Output Noise	V <sub>NO</sub>	Volume=0dB, R <sub>g</sub> =0, A-weighted	-	-114 (2μ)	-100 (10μ)	dBV (Vrms)
Total Harmonic Distortion	T.H.D	f=1KHz, V <sub>o</sub> =1Vrms, Volume=0dB, BW:400 – 30kHz	-	0.001	0.05	%
Cross Talk	CT	Selected Input : No signal R <sub>g</sub> =0Ω Unselected Input : Input signal A-weighted	-	-100	-	dB
Channel Separation	CS	f=1KHz, V <sub>o</sub> =1Vrms, A-weighted Volume=0dB	-	-100	-90	dB
<b>◆ ALC</b>						
Flat Level	ALC <sub>FLT</sub>	V <sub>in</sub> = 300mVrms	-	0	-	dB
ALC Cut Level	ALC <sub>CUT</sub>	V <sub>in</sub> = 2Vrms	-	-12	-	dB

## ■ I<sup>2</sup>C BUS BLOCK CHARACTERISTICS (SDA,SCL)

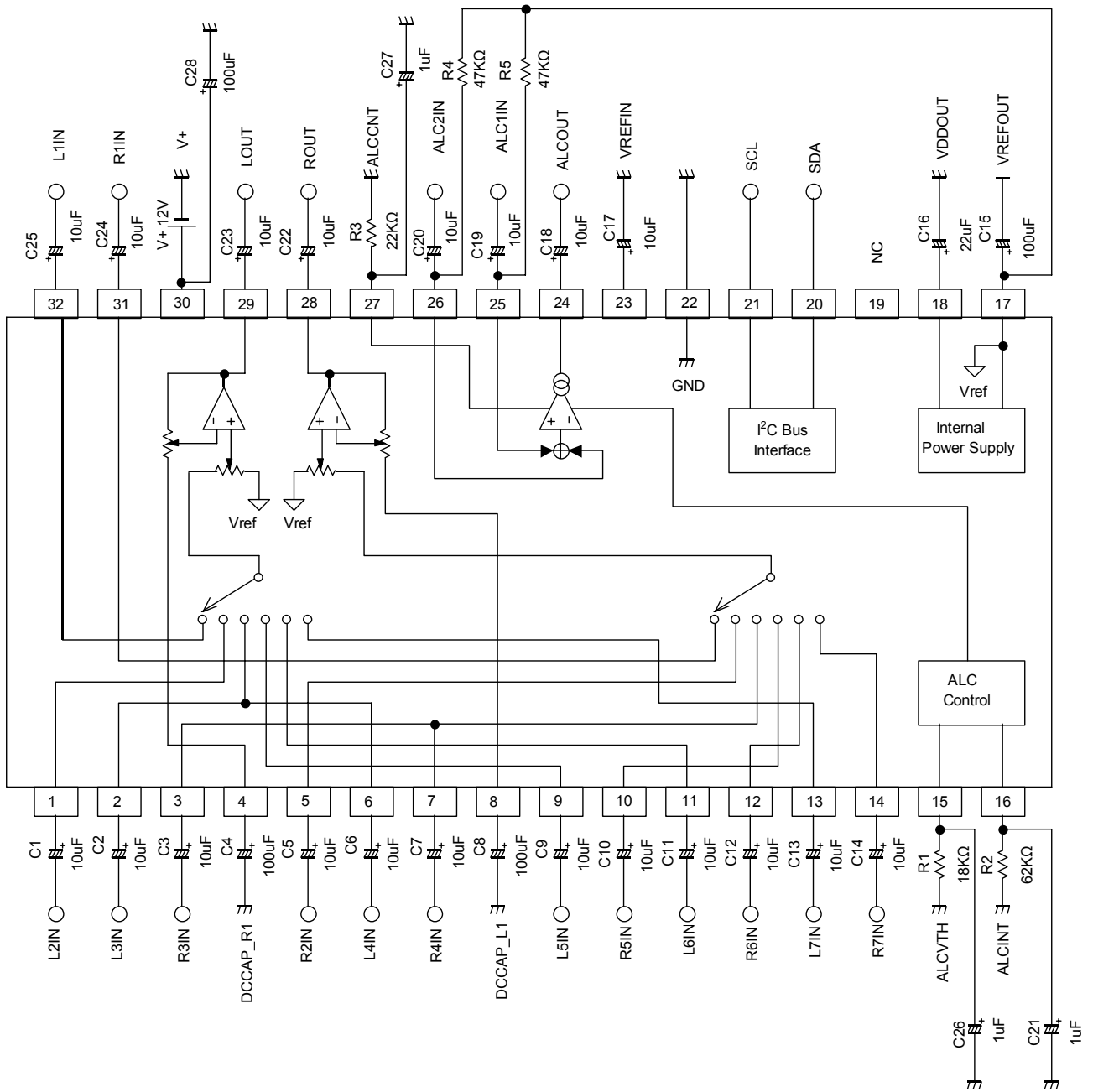
I<sup>2</sup>C BUS Load Conditions: Pull up resistance 4kΩ (Connected to +5V), Load capacitance 200pF (Connected to GND)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Low Level Input Voltage	V <sub>IL</sub>	0.0	-	1.5	V
High Level Input Voltage	V <sub>IH</sub>	3.0	-	5.0	V
Hysteresis of Schmitt trigger inputs	V <sub>hys</sub>	0.25	-	-	V
LOW level output voltage (3mA at SDA pin)	V <sub>OL</sub>	0	-	0.4	V
Output fall time from V <sub>IHmin</sub> to V <sub>ILmax</sub> with a bus capacitance from 10pF to 400pF	t <sub>of</sub>	20+0.1C <sub>b</sub>	-	250	ns
Pulse width of spikes which must be suppressed by the input filter	t <sub>SP</sub>	0	-	50	ns
Input current each I/O pin with an input voltage between 0.1V <sub>DD</sub> and 0.9V <sub>DDmax</sub>	I <sub>i</sub>	-10	-	10	μA
Capacitance for each I/O pin	C <sub>i</sub>	-	-	10	pF
SCL clock frequency	f <sub>SCL</sub>	-	-	400	kHz
Hold time (repeated) START condition.	t <sub>HD:STA</sub>	0.6	-	-	μs
LOW period of the SCL clock	t <sub>LOW</sub>	1.3	-	-	μs
HIGH period of the SCL clock	t <sub>HIGH</sub>	0.6	-	-	μs
Set-up time for a repeated START condition	t <sub>SU:STA</sub>	0.6	-	-	μs
Data hold time	t <sub>HD:DAT</sub>	0	-	0.9	μs
Data set-up time	t <sub>SU:DAT</sub>	100	-	-	ns
Rise time of both SDA and SCL signals	t <sub>r</sub>	-	-	300	ns
Fall time of both SDA and SCL signals	t <sub>f</sub>	-	-	300	ns
Set-up time for STOP condition	t <sub>SU:STO</sub>	0.6	-	-	μs
Bus free time between a STOP and START condition	t <sub>BUF</sub>	1.3	-	-	μs
Capacitive load for each bus line	C <sub>b</sub>	-	-	400	pF
Noise margin at the LOW level	V <sub>nL</sub>	0.5	-	-	V
Noise margin at the HIGH level	V <sub>nH</sub>	1	-	-	V

C<sub>b</sub> ; total capacitance of one bus line in pF.



## APPLICATION CIRCUIT



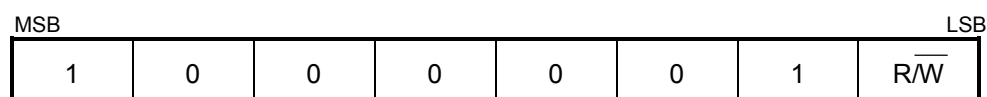
## ■ DEFINITION OF I<sup>2</sup>C REGISTER

### ◆ I<sup>2</sup>C BUS FORMAT



S: Starting Term  
A: Acknowledge Bit  
P: Ending Term

### ◆ SLAVE ADDRESS



R/W=0: Receive Only  
R/W=1: No Output Data

### ◆ CONTROL REGISTER TABLE

The select address sets each function (Volume, Selector).  
The auto increment function cycles the select address as follows.  
00H→01H→02H→00H

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	Don't Care				VOLa			
01H	Don't Care				VOLb			
02H	Don't Care					Selector		

### ◆ CONTROL REGISTER DEFAULT VALUE

Control register default values are as follows :

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	1	1	1	1	1	1	1	1
01H	1	1	1	1	1	1	1	1
02H	0	0	0	0	0	0	0	0

## ■ CONTROL COMMAND TABLE

### a) Master Volume

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	Don't Care				VOLa			
01H	Don't Care				VOLb			

•VOLa / VOLb : Ach and Bch volume level setting from +12dB to -12dB with 3dB step.

Gain (dB)	VOLa / VOLb			
	D3	D2	D1	D0
+12	0	0	0	0
+9	0	0	0	1
+6	0	0	1	0
+3	0	0	1	1
0	0	1	0	0
-3	0	1	0	1
-6	0	1	1	0
-9	0	1	1	1
-12	1	0	0	0
Mute	1	1	1	1

### b) Input Selector

Select Address	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
02H	Don't Care					Selector		

•Selector : Input signal selecting

Input	Selector		
	D2	D1	D0
L1IN / R1IN	0	0	0
L2IN / R2IN	0	0	1
L3IN, L4IN / R3IN, R4IN	0	1	0
L5IN / R5IN	0	1	1
L6IN / R6IN	1	0	0
L7IN / R7IN	1	0	1

[CAUTION]  
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