NEC

MOS INTEGRATED CIRCUIT

MC-242453

MCP (MULTI-CHIP PACKAGE) FLASH MEMORY AND MOBILE SPECIFIED RAM
32M-BIT FLASH MEMORY AND 16M-BIT CMOS MOBILE SPECIFIED RAM

Description

The MC-242453 is a stacked type MCP (Multi-Chip Package) of 33,554,432 bits (BYTE mode : 4,194,304 words by 8 bits, WORD mode : 2,097,152 words by 16 bits) flash memory and 16,777,216 bits (1,048,576 words by 16 bits) Mobile specified RAM.

★ The MC-242453 is packaged in a 77-pin TAPE FBGA and 71-pin TAPE FBGA.

Features

General Features

- Fast access time : t_{ACC} = 90 ns (MAX.), 85 ns (MAX.) ($V_{CC}f \geq 2.7$ V) (Flash Memory)
  t_{AA} = 80, 90, 100 ns (MAX.) (Mobile specified RAM)
- Supply voltage : $V_{CC}f$ / $V_{CC}m$ = 2.6 to 3.0 V
- Wide operating temperature : T_A = –20 to +70 °C

Flash Memory Features

- Two bank organization enabling simultaneous execution of erase / program and read
- Bank organization : 2 banks (8M bits + 24M bits)
- Memory organization : 4,194,304 words × 8 bits (BYTE mode)
  2,097,152 words × 16 bits (WORD mode)
- Sector organization : 71 sectors (8K bytes / 4K words × 8 sectors, 64K bytes / 32K words × 63 sectors)
- Boot sector allocated to the lowest address (sector)
- 3-state output
- Automatic program
  - Program suspend / resume
- Unlock bypass program
- Automatic erase
  - Chip erase
  - Sector erase (sectors can be combined freely)
  - Erase suspend / resume
- Program / Erase completion detection
  - Detection through data polling and toggle bits
  - Detection through RY (/BY) pin

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The mark ★ shows major revised points.

- Sector group protection
  - Any sector can be protected
  - Any protected sector can be temporary unprotected
- Sectors can be used for boot application
- Hardware reset and standby using /RESET pin
- Automatic sleep mode
- Boot block sector protect by /WP (ACC) pin
- Conforms to common flash memory interface (CFI)
- Extra One Time Protect Sector provided

Mobile specified RAM Features

- Memory organization : 1,048,576 words by 16 bits
- Supply current : At operating : 35 mA (MAX.)
  At Standby Mode 1 : 100 μA (MAX.)
  At Standby Mode 2 : 10 μA (MAX.)
- Chip Enable inputs : /CEm
- Byte data control : /LB, /UB
- Standby Mode input : MODE
- Standby Mode 1 : Normal standby (Memory cell data hold valid)
- Standby Mode 2 : Memory cell data hold invalid

★ Ordering Information

Part number	Flash Memory Boot sector	Flash Memory Access time ns (MAX.)	Mobile specified RAM Access time ns (MAX.)	Package
MC-242453F9-B90-BT3	Lowest address (sector) (B type)	90	80	77-pin TAPE FBGA (12 × 7)
MC-242453F9-B95-BT3[Note]		85 (V_{CCf} ≥ 2.7 V)	90	
MC-242453F9-B10-BT3			100	
MC-242453F9-B90-BS1[Note]			80	71-pin TAPE FBGA (11 × 7)
MC-242453F9-B95-BS1[Note]			90	
MC-242453F9-B10-BS1[Note]			100	

Note Under development

★ Pin Configurations

/xxx indicates active low signal.

77-pin TAPE FBGA (12 × 7)

Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	NC	NC	NC		A15	IC	IC	A16	CIOf	V_{SS}		NC	NC	NC
7		NC	NC	A11	A12	A13	A14	NC	I/O15, A-1	I/O7	I/O14	NC	NC	
6				A8	A19	A9	A10	I/O6	I/O13	I/O12	I/O5			
5				/WE	MODE	A20			I/O4	V_{CC}m	NC			
4				/WP(ACC)	/RESET	RY(/BY)			I/O3	V_{CC}f	I/O11			
3				/LB	/UB	A18	A17	I/O1	I/O9	I/O10	I/O2			
2		NC	NC	A7	A6	A5	A4	V_{SS}	/OE	I/O0	I/O8	NC	NC	
1	NC	NC	NC		A3	A2	A1	A0	/CEf	/CEm	NC	NC	NC	NC

71-pin TAPE FBGA (11 × 7)

Top View

	A	B	C	D	E	F	G	H	J	K	L	M
8	NC	NC		A15	NC	IC	A16	CIOf	Vss		NC	NC
7	NC	NC	A11	A12	A13	A14	NC	I/O15, A-1	I/O7	I/O14	NC	NC
6			A8	A19	A9	A10	I/O6	I/O13	I/O12	I/O5		
5			/WE	MODE	A20			I/O4	V_{CC}m	NC		
4			/WP(ACC)	/RESET	RY(/BY)			I/O3	V_{CC}f	I/O11		
3			/LB	/UB	A18	A17	I/O1	I/O9	I/O10	I/O2		
2	NC		A7	A6	A5	A4	Vss	/OE	I/O0	I/O8	NC	NC
1	NC	NC		A3	A2	A1	A0	/CEf	/CEm		NC	NC

Common Pins

A0 - A19	:	Address inputs
I/O0 - I/O15	:	Data inputs / outputs
/OE	:	Output Enable
/WE	:	Write Enable
V_{SS}	:	Ground
NC Note 1	:	No Connection
IC Note 2	:	Internal Connection

Flash Memory Pins

A20	:	Address inputs
I/O15, A–1	:	Data inputs / outputs 15 (WORD mode) LSB address input (BYTE mode)
/CEf	:	Chip Enable
RY (/BY)	:	Ready (Busy) output
/RESET	:	Hardware reset input
V_{CC}f	:	Supply Voltage
/WP(ACC)	:	Hardware Write Protect (Acceleration)
CIOf	:	Selects 8-bit or 16-bit mode

Mobile specified RAM Pins

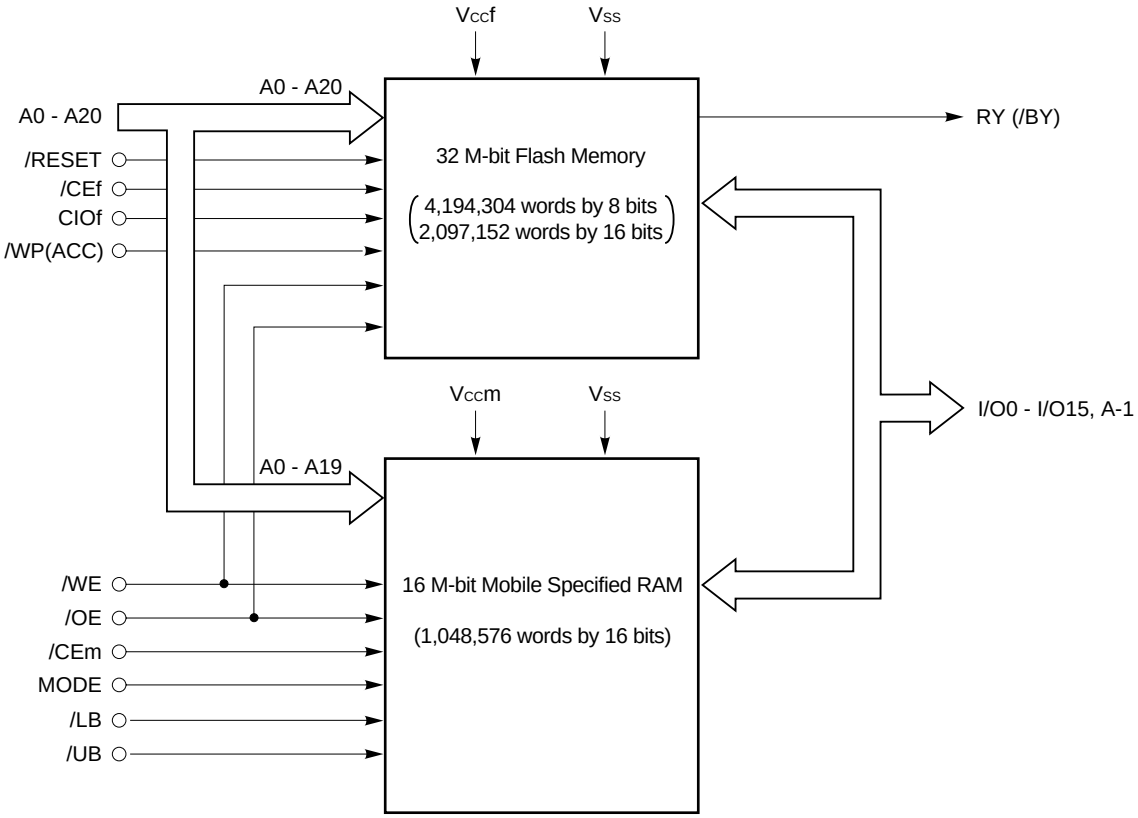
/CEm	:	Chip Enable
MODE	:	Standby mode select
V_{CC}m	:	Supply Voltage
/LB, /UB	:	Byte data select

Note 1. Some signals can be applied because this pin is not internally connected.

2. Leave this pin connected to V_{SS} or unconnected (Recommended to connected to V_{SS}).

Remark Refer to **Package Drawings** for the index mark.

Block Diagram



Bus Operations Table

Operation		Flash Memory				Mobile specified RAM				Common			
		/RESET	/CEf	CIOf	/WP(ACC)	/CEm	MODE	/LB	/UB	/OE	/WE	I/O0 - I/O7	I/O8-I/O15
Full standby	Standby Mode 1	H	H	×	×	H	H	×	×	×	×	Hi-Z	Hi-Z
	Standby Mode 2					H	L						
Output disable		H	L	×	×	L	H	×	×	H	H	Hi-Z	Hi-Z
Read (Flash Memory [Note 1])	BYTE mode	H	L	L	×	**Note 2**				L	H	Data Out	Hi-Z
	WORD mode			H								Data Out	Data Out
Write (Flash Memory)	BYTE mode	H	L	L	×	**Note 2**				H	L	Data In	Hi-Z
	WORD mode			H								Data In	Data In
Temporary sector group unprotect		V_{ID}	×	×	×	**Note 2**				×	×	Hi-Z or Data In/Out	Hi-Z or Data In/Out
Boot block sector protect		×	×	×	L	×	×	×	×	×	×	Hi-Z or Data In/Out	Hi-Z or Data In/Out
Flash Memory hardware reset		L	×	×	×	×	×	×	×	×	×	Hi-Z	Hi-Z
Read (Mobile specified RAM)		**Note 3**				L	H	L	L	L	H	Data Out	Data Out
									H				Hi-Z
								H	L			Hi-Z	Data Out
Write (Mobile specified RAM)		**Note 3**				L	H	L	L	×	L	Data In	Data In
									H				Hi-Z
								H	L			Hi-Z	Data In

Caution Other operations except for indicated in this table are inhibited.

Notes 1. When /OE = V_{IL}, V_{IL} can be applied to /WE. When /OE = V_{IH}, a write operation is started.

2. Mobile specified RAM should be Standby.

3. Flash Memory should be Standby or Hardware reset.

Remarks 1. H : V_{IH}, L : V_{IL}, × : V_{IH} or V_{IL}

2. Sector group protection and read the product ID are using a command.

3. MODE pin must be fixed to H during active operation.

★ **4.** Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)** for the flash memory bus operations.

Sector Organization / Sector Address Table (Flash Memory)

Flash Memory bottom boot **(1/2)**

Bank	Sector Organization	Address		Sectors Address	Sector Address Table								
					Bank Address Table								
	K bytes / K words	BYTE mode	WORD mode		A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank 2	64/32	3FFFFFH 3F0000H	1FFFFFH 1F8000H	FSA70	1	1	1	1	1	1	x	x	x
	64/32	3EFFFFH 3E0000H	1F7FFFH 1F0000H	FSA69	1	1	1	1	1	0	x	x	x
	64/32	3DFFFFH 3D0000H	1EFFFFH 1E8000H	FSA68	1	1	1	1	0	1	x	x	x
	64/32	3CFFFFH 3C0000H	1E7FFFH 1E0000H	FSA67	1	1	1	1	0	0	x	x	x
	64/32	3BFFFFH 3B0000H	1DFFFFH 1D8000H	FSA66	1	1	1	0	1	1	x	x	x
	64/32	3AFFFFH 3A0000H	1D7FFFH 1D0000H	FSA65	1	1	1	0	1	0	x	x	x
	64/32	39FFFFH 390000H	1CFFFFH 1C8000H	FSA64	1	1	1	0	0	1	x	x	x
	64/32	38FFFFH 380000H	1C7FFFH 1C0000H	FSA63	1	1	1	0	0	0	x	x	x
	64/32	37FFFFH 370000H	1BFFFFH 1B8000H	FSA62	1	1	0	1	1	1	x	x	x
	64/32	36FFFFH 360000H	1B7FFFH 1B0000H	FSA61	1	1	0	1	1	0	x	x	x
	64/32	35FFFFH 350000H	1AFFFFH 1A8000H	FSA60	1	1	0	1	0	1	x	x	x
	64/32	34FFFFH 340000H	1A7FFFH 1A0000H	FSA59	1	1	0	1	0	0	x	x	x
	64/32	33FFFFH 330000H	19FFFFH 198000H	FSA58	1	1	0	0	1	1	x	x	x
	64/32	32FFFFH 320000H	197FFFH 190000H	FSA57	1	1	0	0	1	0	x	x	x
	64/32	31FFFFH 310000H	18FFFFH 188000H	FSA56	1	1	0	0	0	1	x	x	x
	64/32	30FFFFH 300000H	187FFFH 180000H	FSA55	1	1	0	0	0	0	x	x	x
	64/32	2FFFFFH 2F0000H	17FFFFH 178000H	FSA54	1	0	1	1	1	1	x	x	x
	64/32	2EFFFFH 2E0000H	177FFFH 170000H	FSA53	1	0	1	1	1	0	x	x	x
	64/32	2DFFFFH 2D0000H	16FFFFH 168000H	FSA52	1	0	1	1	0	1	x	x	x
	64/32	2CFFFFH 2C0000H	167FFFH 160000H	FSA51	1	0	1	1	0	0	x	x	x
	64/32	2BFFFFH 2B0000H	15FFFFH 158000H	FSA50	1	0	1	0	1	1	x	x	x
	64/32	2AFFFFH 2A0000H	157FFFH 150000H	FSA49	1	0	1	0	1	0	x	x	x
	64/32	29FFFFH 290000H	14FFFFH 148000H	FSA48	1	0	1	0	0	1	x	x	x
	64/32	28FFFFH 280000H	147FFFH 140000H	FSA47	1	0	1	0	0	0	x	x	x
	64/32	27FFFFH 270000H	13FFFFH 138000H	FSA46	1	0	0	1	1	1	x	x	x
	64/32	26FFFFH 260000H	137FFFH 130000H	FSA45	1	0	0	1	1	0	x	x	x
	64/32	25FFFFH 250000H	12FFFFH 128000H	FSA44	1	0	0	1	0	1	x	x	x
	64/32	24FFFFH 240000H	127FFFH 120000H	FSA43	1	0	0	1	0	0	x	x	x
	64/32	23FFFFH 230000H	11FFFFH 118000H	FSA42	1	0	0	0	1	1	x	x	x
	64/32	22FFFFH 220000H	117FFFH 110000H	FSA41	1	0	0	0	1	0	x	x	x
	64/32	21FFFFH 210000H	10FFFFH 108000H	FSA40	1	0	0	0	0	1	x	x	x
	64/32	20FFFFH 200000H	107FFFH 100000H	FSA39	1	0	0	0	0	0	x	x	x
	64/32	1FFFFFH 1F0000H	0FFFFFH 0F8000H	FSA38	0	1	1	1	1	1	x	x	x
	64/32	1EFFFFH 1E0000H	0F7FFFH 0F0000H	FSA37	0	1	1	1	1	0	x	x	x
	64/32	1DFFFFH 1D0000H	0EFFFFH 0E8000H	FSA36	0	1	1	1	0	1	x	x	x
	64/32	1CFFFFH 1C0000H	0E7FFFH 0E0000H	FSA35	0	1	1	1	0	0	x	x	x

(2/2)

Bank	Sector Organization K bytes / K words	Address BYTE mode	Address WORD mode	Sectors Address	Sector Address Table: Bank Address Table A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank 2	64/32	1BFFFFH 1B0000H	0DFFFFH 0D8000H	FSA34	0	1	1	0	1	1	x	x	x
	64/32	1AFFFFH 1A0000H	0D7FFFH 0D0000H	FSA33	0	1	1	0	1	0	x	x	x
	64/32	19FFFFH 190000H	0CFFFFH 0C8000H	FSA32	0	1	1	0	0	1	x	x	x
	64/32	18FFFFH 180000H	0C7FFFH 0C0000H	FSA31	0	1	1	0	0	0	x	x	x
	64/32	17FFFFH 170000H	0BFFFFH 0B8000H	FSA30	0	1	0	1	1	1	x	x	x
	64/32	16FFFFH 160000H	0B7FFFH 0B0000H	FSA29	0	1	0	1	1	0	x	x	x
	64/32	15FFFFH 150000H	0AFFFFH 0A8000H	FSA28	0	1	0	1	0	1	x	x	x
	64/32	14FFFFH 140000H	0A7FFFH 0A0000H	FSA27	0	1	0	1	0	0	x	x	x
	64/32	13FFFFH 130000H	09FFFFH 098000H	FSA26	0	1	0	0	1	1	x	x	x
	64/32	12FFFFH 120000H	097FFFH 090000H	FSA25	0	1	0	0	1	0	x	x	x
	64/32	11FFFFH 110000H	08FFFFH 088000H	FSA24	0	1	0	0	0	1	x	x	x
	64/32	10FFFFH 100000H	087FFFH 080000H	FSA23	0	1	0	0	0	0	x	x	x
Bank 1	64/32	0FFFFFH 0F0000H	07FFFFH 078000H	FSA22	0	0	1	1	1	1	x	x	x
	64/32	0EFFFFH 0E0000H	077FFFH 070000H	FSA21	0	0	1	1	1	0	x	x	x
	64/32	0DFFFFH 0D0000H	06FFFFH 068000H	FSA20	0	0	1	1	0	1	x	x	x
	64/32	0CFFFFH 0C0000H	067FFFH 060000H	FSA19	0	0	1	1	0	0	x	x	x
	64/32	0BFFFFH 0B0000H	05FFFFH 058000H	FSA18	0	0	1	0	1	1	x	x	x
	64/32	0AFFFFH 0A0000H	057FFFH 050000H	FSA17	0	0	1	0	1	0	x	x	x
	64/32	09FFFFH 090000H	04FFFFH 048000H	FSA16	0	0	1	0	0	1	x	x	x
	64/32	08FFFFH 080000H	047FFFH 040000H	FSA15	0	0	1	0	0	0	x	x	x
	64/32	07FFFFH 070000H	03FFFFH 038000H	FSA14	0	0	0	1	1	1	x	x	x
	64/32	06FFFFH 060000H	037FFFH 030000H	FSA13	0	0	0	1	1	0	x	x	x
	64/32	05FFFFH 050000H	02FFFFH 028000H	FSA12	0	0	0	1	0	1	x	x	x
	64/32	04FFFFH 040000H	027FFFH 020000H	FSA11	0	0	0	1	0	0	x	x	x
	64/32	03FFFFH 030000H	01FFFFH 018000H	FSA10	0	0	0	0	1	1	x	x	x
	64/32	02FFFFH 020000H	017FFFH 010000H	FSA9	0	0	0	0	1	0	x	x	x
	64/32	01FFFFH 010000H	00FFFFH 008000H	FSA8	0	0	0	0	0	1	x	x	x
	8/4	00FFFFH 00E000H	007FFFH 007000H	FSA7	0	0	0	0	0	0	1	1	1
	8/4	00DFFFH 00C000H	006FFFH 006000H	FSA6	0	0	0	0	0	0	1	1	0
	8/4	00BFFFH 00A000H	005FFFH 005000H	FSA5	0	0	0	0	0	0	1	0	1
	8/4	009FFFH 008000H	004FFFH 004000H	FSA4	0	0	0	0	0	0	1	0	0
	8/4	007FFFH 006000H	003FFFH 003000H	FSA3	0	0	0	0	0	0	0	1	1
	8/4	005FFFH 004000H	002FFFH 002000H	FSA2	0	0	0	0	0	0	0	1	0
	8/4	003FFFH 002000H	001FFFH 001000H	FSA1	0	0	0	0	0	0	0	0	1
	8/4	001FFFH 000000H	000FFFH 000000H	FSA0	0	0	0	0	0	0	0	0	0

★ **Sector Group Address Table (Flash Memory)**

Sector group	A20	A19	A18	A17	A16	A15	A14	A13	A12	Size	Sector
SGA0	0	0	0	0	0	0	0	0	0	8 KB (1 Sector)	FSA0
SGA1	0	0	0	0	0	0	0	0	1	8 KB (1 Sector)	FSA1
SGA2	0	0	0	0	0	0	0	1	0	8 KB (1 Sector)	FSA2
SGA3	0	0	0	0	0	0	0	1	1	8 KB (1 Sector)	FSA3
SGA4	0	0	0	0	0	0	1	0	0	8 KB (1 Sector)	FSA4
SGA5	0	0	0	0	0	0	1	0	1	8 KB (1 Sector)	FSA5
SGA6	0	0	0	0	0	0	1	1	0	8 KB (1 Sector)	FSA6
SGA7	0	0	0	0	0	0	1	1	1	8 KB (1 Sector)	FSA7
SGA8	0	0	0	0	0	1	×	×	×	192 KB (3 Sectors)	FSA8–FSA10
					1	0					
					1	1					
SGA9	0	0	0	1	×	×	×	×	×	256 KB (4 Sectors)	FSA11–FSA14
SGA10	0	0	1	0	×	×	×	×	×	256 KB (4 Sectors)	FSA15–FSA18
SGA11	0	0	1	1	×	×	×	×	×	256 KB (4 Sectors)	FSA19–FSA22
SGA12	0	1	0	0	×	×	×	×	×	256 KB (4 Sectors)	FSA23–FSA26
SGA13	0	1	0	1	×	×	×	×	×	256 KB (4 Sectors)	FSA27–FSA30
SGA14	0	1	1	0	×	×	×	×	×	256 KB (4 Sectors)	FSA31–FSA34
SGA15	0	1	1	1	×	×	×	×	×	256 KB (4 Sectors)	FSA35–FSA38
SGA16	1	0	0	0	×	×	×	×	×	256 KB (4 Sectors)	FSA39–FSA42
SGA17	1	0	0	1	×	×	×	×	×	256 KB (4 Sectors)	FSA43–FSA46
SGA18	1	0	1	0	×	×	×	×	×	256 KB (4 Sectors)	FSA47–FSA50
SGA19	1	0	1	1	×	×	×	×	×	256 KB (4 Sectors)	FSA51–FSA54
SGA20	1	1	0	0	×	×	×	×	×	256 KB (4 Sectors)	FSA55–FSA58
SGA21	1	1	0	1	×	×	×	×	×	256 KB (4 Sectors)	FSA59–FSA62
SGA22	1	1	1	0	×	×	×	×	×	256 KB (4 Sectors)	FSA63–FSA66
SGA23	1	1	1	1	0	0	×	×	×	192 KB (3 Sectors)	FSA67–FSA69
					0	1					
					1	0					
SGA24	1	1	1	1	1	1	×	×	×	64 KB (1 Sector)	FSA70

Remark × : V_{IH} or V_{IL}

Command Sequence (Flash Memory)

Command sequence		Bus	1st bus Cycle		2nd bus Cycle		3rd bus Cycle		4th bus Cycle		5th bus Cycle		6th bus Cycle	
		Cycle	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read / Reset [Note1]		1	×××H	F0H	RA	RD	–	–	–	–	–	–	–	–
Read / Reset [Note1]	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	F0H	RA	RD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Program	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Program Suspend [Note 2]		1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Program Resume [Note 3]		1	BA	30H	–	–	–	–	–	–	–	–	–	–
Chip Erase	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
	WORD mode		555H		2AAH		555H		555H		2AAH		555H	
Sector Erase	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	FSA	30H
	WORD mode		555H		2AAH		555H		555H		2AAH			
Sector Erase Suspend [Note 4]		1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Sector Erase Resume [Note 5]		1	BA	30H	–	–	–	–	–	–	–	–	–	–
Unlock Bypass Set	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	20H	–	–	–	–	–	–
	WORD mode		555H		2AAH		555H							
Unlock Bypass Program [Note 6]		2	×××H	A0H	PA	PD	–	–	–	–	–	–	–	–
Unlock Bypass Reset [Note 6]		2	BA	90H	×××H	00H[Note11]	–	–	–	–	–	–	–	–
Product ID	BYTE mode	3	AAAH	AAH	555H	55H	(BA) AAAH	90H	IA	ID	–	–	–	–
	WORD mode		555H		2AAH		(BA) 555H							
Sector Group Protection [Note 7]		4	×××H	60H	SPA	60H	SPA	40H	SPA	SD	–	–	–	–
Sector Group Unprotect [Note 8]		4	×××H	60H	SUA	60H	SUA	40H	SUA	SD	–	–	–	–
Query [Note 9]	BYTE mode	1	AAH	98H	–	–	–	–	–	–	–	–	–	–
	WORD mode		55H											
Extra One Time Protect	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	88H	–	–	–	–	–	–
Sector Entry	WORD mode		555H		2AAH		555H							
Extra One Time Protect	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD	–	–	–	–
Sector Program [Note 10]	WORD mode		555H		2AAH		555H							
Extra One Time Protect	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	EOTPSA	30H
Sector Erase [Note 10]	WORD mode		555H		2AAH		555H		555H		2AAH			
Extra One Time Protect	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	90H	xxxH	00H	–	–	–	–
Sector Reset [Note 10]	WORD mode		555H		2AAH		555H							
Extra One Time Protect Sector Protection [Note 10]		4	×××H	60H	EOTPSA	60H	EOTPSA	40H	EOTPSA	SD	–	–	–	–

Notes 1. Both these read / reset commands reset the device to the read mode.

2. Programming is suspended if B0H is input to the bank address being programmed to in a program operation.

3. Programming is resumed if 30H is input to the bank address being suspended to in a program-suspend operation.

4. Erasure is suspended if B0H is input to the bank address being erased in a sector erase operation.

5. Erasure is resumed if 30H is input to the bank address being suspended in a sector-erase-suspend operation.

6. Valid only in the unlock bypass mode.

7. Valid only when /RESET = V_{ID} (except in the Extra One Time Protect Sector mode).

8. The command sequence that protects a sector group is excluded.

9. Only A0 to A6 are valid as an address.

10. Valid only in the Extra One Time Protect Sector mode.

11. This command can be used even if this data is F0H.

Remarks 1. Specify address 555H (A10 to A0) in the WORD mode, and AAAH (A10 to A0, A-1) in the BYTE mode.

2. RA : Read address

RD : Read data

IA : Address input

xx00H (to read the manufacturer code)

xx02H (to read the device code in the BYTE mode)

xx01H (to read the device code in the WORD mode)

ID : Code output. Refer to the **Product ID code (Manufacturer code / Device code) (Flash Memory)**.

PA : Program address

PD : Program data

FSA: Erase sector address. The sector to be erased is selected by the combination of this address. Refer to the **Sector Organization / Sector Address Table (Flash Memory)**.

BA : Bank address. Refer to the **Sector Organization / Sector Address Table (Flash Memory)**.

SPA : Sector group address to be protected. Set sector group address (SGA) and (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}). For the sector group address, refer to the **Sector Group Address Table (Flash Memory)**.

SUA : Unprotect sector group address. Set sector group address (SGA) and (A6, A1, A0) = (V_{IH}, V_{IH}, V_{IL}). For the sector group address, refer to the **Sector Group Address Table (Flash Memory)**.

SD : Data for verifying whether sector groups read from the address specified by SPA, SUA, and EOTPSA are protected.

EOTPSA : Extra One Time Protect Sector area addresses.

BYTE mode : 000000H to 00FFFFH, WORD mode : 000000H to 007FFFH

3. The sector group address is don't care except when a program / erase address or read address are selected.

4. For the operation of the bus, refer to **Bus Operations Table**.

5. × of address bit indicates V_{IH} or V_{IL}.

★ **6.** Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)** for the flash memory commands.

Product ID Code (Manufacturer Code / Device Code) (Flash Memory)

Product ID Code	Address inputs			Output
	A6	A1	A0	Hex
Manufacturer Code	L	L	L	10H
Device code	L	L	H	53H (BYTE mode), 2253H (WORD mode)

Product ID Code		Code outputs																
		I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0	Hex
Manufacturer Code		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	10H
Device code	BYTE mode	A-1	x	x	x	x	x	x	x	0	1	0	1	0	0	1	1	53H
	WORD mode	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	1	2253H

Remark H : V_{IH}, L : V_{IL}, x : Hi-Z

★ **Hardware Sequence Flags, Hardware Data Protection (Flash Memory)**

Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E).**

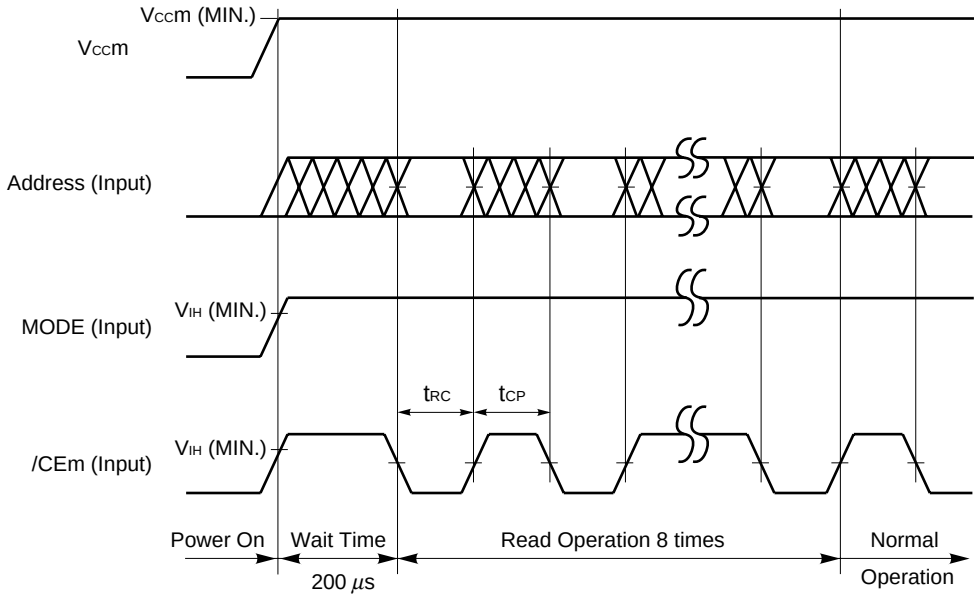
Initialization (Mobile specified RAM)

The MC-242453 is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, before turning on the power, a 200 μs or longer wait time must precede any signal toggling.

(2) After the wait time, read operation must be performed at least 8 times. After that, it can be normal operation.

Figure 1. Initialization Timing Chart



Cautions 1. Following power application, make MODE and /CEm high level during the wait time interval.

2. Following power application, make MODE high level during the wait time and eight read operations.

3. The read operation must satisfy the specs described on page 21 (Read Cycle (Mobile specified RAM)).

4. The address is don't care (V_{IH} or V_{IL}) during read operation.

5. Read operation must be executed with toggled the /CEm pin.

6. To prevent bus contention, it is recommended to set /OE to high level. However, do not input data to the I/O pins if /OE is low level during a read operation.

Standby Mode (Flash Memory)

Standby Mode 1 and Standby Mode 2 differ as shown below.

Table 1. Standby Mode Characteristics

Standby Mode	Memory Cell Data Hold	Standby Supply Current (μA)
Mode 1	Valid	100 (I_{SB1})
Mode 2	Invalid	10 (I_{SB2})

Standby Mode State Machine (Flash Memory)

(1) From Active

To shift from this state to Standby Mode 1, change /CEm from V_{IL} to V_{IH}.

To shift from this state to Standby Mode 2, change /CEm from V_{IL} to V_{IH} and change MODE from V_{IH} to V_{IL}.

(2) From Standby Mode 1

To shift from this state to Active, change /CEm from V_{IH} to V_{IL}.

To shift from this state to Standby Mode 2, change MODE from V_{IH} to V_{IL}.

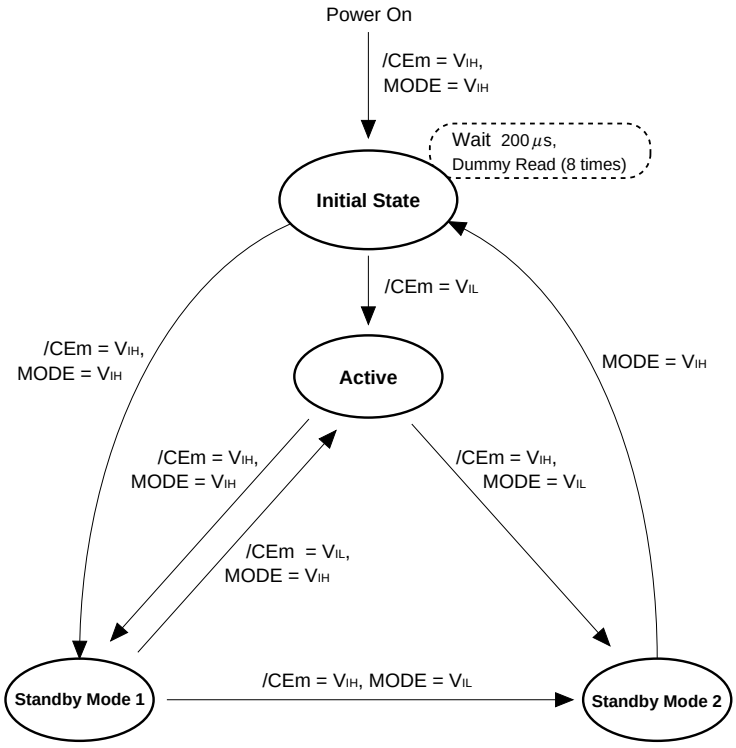
(3) From Standby Mode 2

When shifting from this state to the Active state or to Standby Mode 1, it is necessary to set MODE to V_{IH} and perform a Dummy Read operation 8 times after waiting for 200 μs, in the same way as at power application. Refer to **Figure 35. Standby Mode 2 entry and recovery Timing Chart (Mobile specified RAM)**.

After shifting to Active state, change /CEm to V_{IL}.

After shifting to Standby Mode 1, do not change either MODE or /CEm.

Figure 2. Standby Mode State Machine



Electrical Specifications

Before turning on power, input $V_{SS} \pm 0.2$ V to the /RESET pin until $V_{CCf} \geq V_{CCf}$ (MIN.).

Absolute Maximum Ratings

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{CCf}	with respect to V_{SS}		–0.5 to +4.0	V
	V_{CCm}	with respect to V_{SS}		–0.5 to +4.0	
Input / Output voltage	V_T	with respect to V_{SS}	/WP(ACC), /RESET	–0.5 Note 1 to +13.0	V
			except /WP(ACC), /RESET	–0.5 Note 1 to V_{CCf}, V_{CCm} + 0.4 (4.0 V MAX.) Note 2	
Ambient operation temperature	T_A			–20 to +70	°C
Storage temperature	T_{stg}			–55 to +125	°C

Notes 1. –1.0 V (MIN.) (pulse width ≤ 20 ns)

2. V_{CCf}, V_{CCm} + 0.5 V (MAX.) (pulse width ≤ 20 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Common

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CCf}, V_{CCm}		2.6		3.0	V
Ambient operation temperature	T_A		–20		+70	°C

Flash Memory

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.4		V_{CCf} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.5	V

Mobile specified RAM

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		V_{CCm} x 0.8		V_{CCm} + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		V_{CCm} x 0.2	V

Note –0.5 V (MIN.) (Pulse width: 30 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Common

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}		–1.0		+1.0	μA
Output leakage current	I_{LO}		–1.0		+1.0	μA

Flash Memory

Parameter			Symbol	Test condition		MIN.	TYP.	MAX.	Unit
High level output voltage			V_{OH}	I_{OH} = –500 μA, $V_{CC}f$ = $V_{CC}f$ (MIN.)		$V_{CC}f$–0.3			V
Low level output voltage			V_{OL}	I_{OL} = +1.0 mA, $V_{CC}f$ = $V_{CC}f$ (MIN.)				0.3	V
Power supply current	Read	BYTE mode	$I_{CC1}f$	$V_{CC}f$ = $V_{CC}f$ (MAX.), /CEf = V_{IL}, /OE = V_{IH}	t_{CYCLE} = 5 MHz		10	16	mA
					t_{CYCLE} = 1 MHz		2	4	
		WORD mode			t_{CYCLE} = 5 MHz		10	16	
					t_{CYCLE} = 1 MHz		2	4	
	Program, Erase		$I_{CC2}f$	$V_{CC}f$ = $V_{CC}f$ (MAX.), /CEf = V_{IL}, /OE = V_{IH}			15	30	mA
	Standby		$I_{CC3}f$	$V_{CC}f$ = $V_{CC}f$ (MAX.), /CEf = /RESET = /WP(ACC) = $V_{CC}f$ ± 0.3 V, /OE = V_{IL}			0.2	5	μA
	Standby / Reset		$I_{CC4}f$	$V_{CC}f$ = $V_{CC}f$ (MAX.), /RESET = V_{SS} ± 0.2 V			0.2	5	μA
	Automatic sleep mode		$I_{CC5}f$	V_{IH} = $V_{CC}f$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			0.2	5	μA
	Read during programming		$I_{CC6}f$	V_{IH} = $V_{CC}f$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			21	45	mA
	Read during erasing		$I_{CC7}f$	V_{IH} = $V_{CC}f$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			21	45	mA
	Programming during suspend		$I_{CC8}f$	/CEf = V_{IL}, /OE = V_{IH}, Automatic programming during suspend			17	35	mA
	Accelerated programming		I_{ACC}	/WP (ACC) pin			5	10	mA
				$V_{CC}f$			15	30	
/RESET high level input voltage			V_{ID}	High Voltage is applied		11.5		12.5	V
Accelerated programming voltage			V_{ACC}	High Voltage is applied		8.5		9.5	V
Low $V_{CC}f$ lock-out voltage [Note]			V_{LKO}					1.7	V

★ **Note** When $V_{CC}f$ is equal to or lower than V_{LKO}, the device ignores all write cycles. Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E)**.

Mobile specified RAM

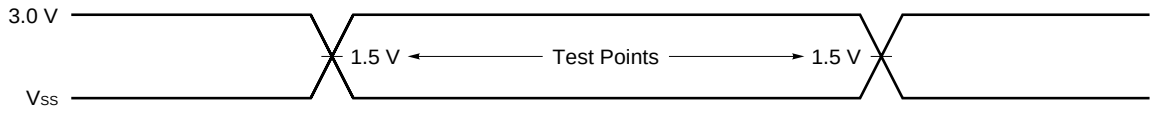
Parameter		Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High level output voltage		V_{OH}	I_{OH} = –0.5 mA	$V_{CC}m$ × 0.8			V
Low level output voltage		V_{OL}	I_{OL} = 1 mA			$V_{CC}m$ × 0.2	V
Operating supply current		I_{CCA}	/CEm = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA			35	mA
Standby supply current	Standby Mode 1	I_{SB1}	/CEm ≥ $V_{CC}m$ – 0.2 V, MODE ≥ $V_{CC}m$ – 0.2 V			100	μA
	Standby Mode 2	I_{SB2}	/CEm ≥ $V_{CC}m$ – 0.2 V, MODE ≤ 0.2 V			10	

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

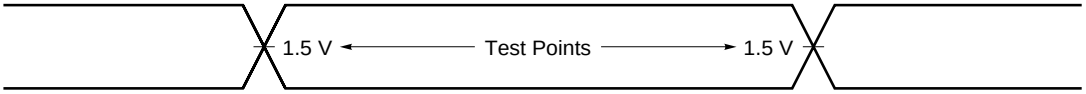
AC Test Conditions

Flash Memory

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

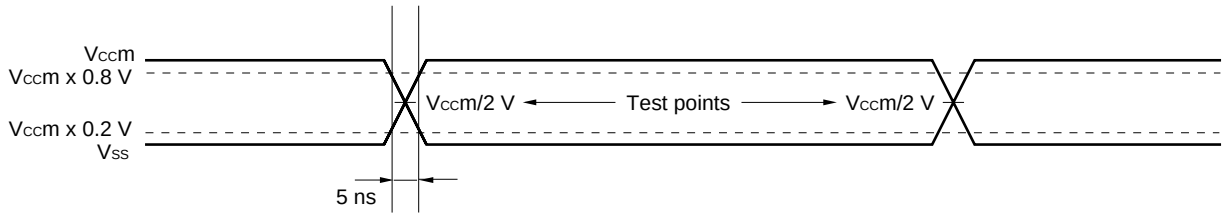


Output Load

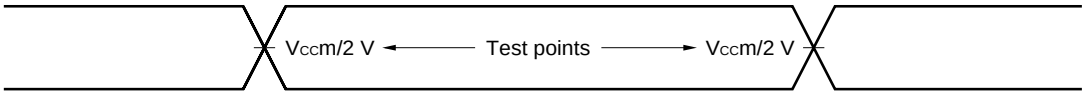
1 TTL + 30 pF

Mobile specified RAM

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

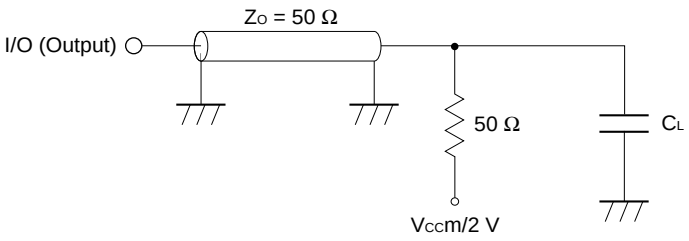


Output Load

AC characteristics directed with the note should be measured with the output load shown in Figure.

C_L: 50 pF

5 pF (t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ}, t_{OW})



/CEf, /CEm Timing

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Note
/CEf, /CEm recover time	t_{CCR}		0			ns	

Read Cycle (Flash Memory)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Note
Read cycle time	t_{RC}		90			ns	
$V_{CC}f \geq 2.7$ V			85				
Address access time	t_{ACC}	/CEf = /OE = V_{IL}			90	ns	
$V_{CC}f \geq 2.7$ V					85		
/CEf access time	t_{CEf}	/OE = V_{IL}			90	ns	
$V_{CC}f \geq 2.7$ V					85		
/OE access time	t_{OE}	/CEf = V_{IL}			40	ns	
Output disable time	t_{DF}	/OE = V_{IL} or /CEf = V_{IL}			30	ns	
Output hold time	t_{OH}		0			ns	
/RESET pulse width	t_{RP}		500			ns	
/RESET hold time before read	t_{RH}		50			ns	
/RESET low to read mode	t_{READY}				20	μs	
/CEf low to CIOf low, high	t_{ELFL}/t_{ELFH}				5	ns	
CIOf low output disable time	t_{FLQZ}				30	ns	
CIOf high access time	t_{FHQV}		90			ns	
$V_{CC}f \geq 2.7$ V			85				

Remark t_{DF} is the time from inactivation of /CEf or /OE to Hi-Z state output.

Write Cycle (Erase / Program) (Flash Memory)

Parameter		Symbol	MIN.	TYP.	MAX.	Unit	Note
Write cycle time		t_{WC}	90			ns	
	$V_{CC}f \geq 2.7$ V		85				
Address setup time (/WE to address)		t_{AS}	0			ns	
Address setup time (/CEf to address)		t_{AS}	0			ns	
Address hold time (/WE to address)		t_{AH}	45			ns	
Address hold time (/CEf to address)		t_{AH}	45			ns	
Input data setup time		t_{DS}	35			ns	
Input data hold time		t_{DH}	0			ns	
/OE hold time	Read	t_{OEH}	0			ns	
	Toggle bit, Data polling		10				
Read recovery time before write (/OE to /CEf)		t_{GHEL}	0			ns	
Read recovery time before write (/OE to /WE)		t_{GHWL}	0			ns	
/WE setup time (/CEf to /WE)		t_{WS}	0			ns	
/CEf setup time (/WE to /CEf)		t_{CS}	0			ns	
/WE hold time (/CEf to /WE)		t_{WH}	0			ns	
/CEf hold time (/WE to /CEf)		t_{CH}	0			ns	
Write pulse width		t_{WP}	35			ns	
/CEf pulse width		t_{CP}	35			ns	
Write pulse width high		t_{WPH}	30			ns	
/CEf pulse width high		t_{CPH}	30			ns	
Byte programming operation time		t_{BPG}		9	200	μs	
Word programming operation time		t_{WPG}		11	200	μs	
Sector erase operation time		t_{SER}		0.7	5	s	1
$V_{CC}f$ setup time		t_{VCS}	50			μs	
RY (/BY) recovery time		t_{RB}	0			ns	
/RESET pulse width		t_{RP}	500			ns	
/RESET high-voltage (V_{ID}) hold time from high of RY(/BY) when sector group is temporarily unprotect		t_{RRB}	20			μs	
/RESET hold time		t_{RH}	50			ns	
From completion of automatic		t_{EOE}			90	ns	
program / erase to data output time	$V_{CC}f \geq 2.7$ V				85		
RY (/BY) delay time from valid program or erase operation		t_{BUSY}			90	ns	
Address setup time to /OE low in toggle bit		t_{ASO}	15			ns	
Address hold time to /CEf or /OE high in toggle bit		t_{AHT}	0			ns	
/CEf pulse width high for toggle bit		t_{CEPH}	20			ns	
/OE pulse width high for toggle bit		t_{OEPH}	20			ns	
Voltage transition time		t_{VLHT}	4			μs	2
Rise time to V_{ID} (/RESET)		t_{VIDR}	500			ns	3
Rise time to V_{ACC} (/WP(ACC))		t_{VACCR}	500			ns	2
Erase timeout time		t_{TOW}	50			μs	4
Erase suspend transition time		t_{SPD}			20	μs	4

Notes 1. The preprogramming time prior to the erase operation is not included.

2. Sector group protection and accelerated mode only

3. Sector group protection only.

4. Table only.

Write operation (Erase / Program) Performance (Flash Memory)

Parameter	Description		MIN.	TYP.	MAX.	Unit
Sector erase time	Excludes programming time prior to erasure			0.7	5	s
Chip erase time	Excludes programming time prior to erasure			50		s
Byte programming time	Excludes system-level overhead			9	200	μs
Word programming time	Excludes system-level overhead			11	200	μs
Chip programming time	Excludes system-level overhead	BYTE mode		40		s
		WORD mode		25		
Accelerated programming time	Excludes system-level overhead			7	150	μs
Erase / Program cycle			100,000			cycles

Read Cycle (Mobile specified RAM)

Parameter	Symbol	MC-242453-B90		MC-242453-B95		MC-242453-B10		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	80	10,000	90	10,000	110	10,000	ns	1
Identical address read cycle time	t_{RC1}	80	10,000	90	10,000	110	10,000	ns	2
Address skew time	t_{SKEW}		10		15		20	ns	3
/CEm pulse width	t_{CP}	10		10		10		ns	
Address access time	t_{AA}		80		90		100	ns	4
/CEm access time	t_{ACS}		80		90		100	ns	
/OE to output valid	t_{OE}		35		40		50	ns	5
/LB, /UB to output valid	t_{BA}		35		40		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CEm to output in low impedance	t_{CLZ}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	5		5		5		ns	
/CEm to output in high impedance	t_{CHZ}		25		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25		25	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		25		25	ns	

Notes 1. One read cycle (t_{RC}) must satisfy the minimum value ($t_{RC(MIN.)}$) and maximum value ($t_{RC(MAX.)}$ = 10 μs). t_{RC} indicates the time from the /CEm low level input point or address determination point, whichever is later, to the /CEm high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{RC}.

1) Time from address determination point to /CEm high level input point (address access)
2) Time from address determination point to next address change start point (address access)
3) Time from /CEm low level input point to next address change start point (/CEm access)
4) Time from /CEm low level input point to /CEm high level input point (/CEm access)

2. The identical address read cycle time (t_{RC1}) is the cycle time of one read operation when performing continuous read operations toggling /OE , /LB, and /UB with the address fixed and /CEm low level. Perform settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CEm from high level to low level, t_{SKEW} is the time from the /CEm low level input point until the next address is determined.
2) When switching /CEm from low level to high level, t_{SKEW} is the time from the address change start point to the /CEm high level input point.
3) When /CEm is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CEm is active, t_{SKEW} is not subject to limitations when /CEm is switched from high level to low level following address determination, or when the address is changed after /CEm is switched from low level to high level.

4. Regarding t_{AA} and t_{ACS}, only t_{AA} is satisfied during address access (refer to 1) and 2) of **Note 1**), and only t_{ACS} is satisfied during /CEm access (refer to 3) of **Note 1**).

5. Regarding t_{BA} and t_{OE}, only t_{BA} is satisfied if /OE becomes active later than /UB and /LB, and only t_{OE} is satisfied if /UB and /LB become active before /OE.

Write Cycle (Mobile specified RAM)

Parameter	Symbol	MC-242453-B90		MC-242453-B95		MC-242453-B10		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	80	10,000	90	10,000	110	10,000	ns	1
Identical address write cycle time	t_{WC1}	80	10,000	90	10,000	110	10,000	ns	2
Address skew time	t_{SKEW}		10		15		20	ns	3
/CEm to end of write	t_{CW}	40		50		60		ns	4
/LB, /UB to end of write	t_{BW}	30		35		40		ns	
Address valid to end of write	t_{AW}	35		45		55		ns	
Write pulse width	t_{WP}	30		35		40		ns	
Write recovery time	t_{WR}	20		20		20		ns	5
/CEm pulse width	t_{CP}	10		10		10		ns	
Address setup time	t_{AS}	0		0		0		ns	
Byte write hold time	t_{BWH}	20		20		20		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/WE to output in high impedance	t_{WHZ}		25		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25		25	ns	
Output active from end of write	t_{OW}	5		5		5		ns	

Notes 1. One write cycle (t_{WC}) must satisfy the minimum value ($t_{WC(MIN.)}$) and the maximum value ($t_{WC(MAX.)}$ = 10 μs). t_{WC} indicates the time from the /CEm low level input point or address determination point, whichever is after, to the /CEm high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{WC}.

1) Time from address determination point to /CEm high level input point
2) Time from address determination point to next address change start point
3) Time from /CEm low level input point to next address change start point
4) Time from /CEm low level input point to /CEm high level input point

2. The identical address read cycle time (t_{WC1}) is the cycle time of one write cycle when performing continuous write operations with the address fixed and /CEm low level, changing /LB and /UB at the same time, and toggling /WE, as well as when performing a continuous write toggling /LB and /UB. Make settings so that the sum (t_{WC}) of the identical address write cycle times (t_{WC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CEm from high level to low level, t_{SKEW} is the time from the /CEm low level input point until the next address is determined.
2) When switching /CEm from low level to high level, t_{SKEW} is the time from the address change start point to the /CEm high level input point.
3) When /CEm is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CEm is active, t_{SKEW} is not subject to limitations when /CEm is switched from high level to low level following address determination, or when the address is changed after /CEm is switched from low level to high level.

4. Definition of write start and write end

	/CEm	/WE	/LB, /UB	Status
Write start pattern 1	H to L	L	L	If /WE, /LB, /UB are low level, time when /CEm changes from high level to low level
Write start pattern 2	L	H to L	L	If /CEm, /LB, /UB are low level, time when /WE changes from high level to low level
Write start pattern 3	L	L	H to L	If /CEm, /WE are low level, time when /LB or /UB changes from high level to low level
Write end pattern 1	L	L to H	L	If /CEm, /WE, /LB, /UB are low level, time when /WE changes from low level to high level
Write end pattern 2	L	L	L to H	When /CEm, /WE, /LB, /UB are low level, time when /LB or /UB changes from low level to high level

5. Definition of write end recovery time (t_{WR})

1) Time from write end to address change start point, or from write end to /CEm high level input point
2) When /CEm, /LB, /UB are low level and continuously written to the identical address, time from /WE high level input point to /WE low level input point
3) When /CEm, /WE are low level and continuously written to the identical address, time from /LB or /UB high level input point, whichever is later, to /LB or /UB low level input point, whichever is earlier.
4) When /CEm is low level and continuously written to the identical address, time from write end to point at which /WE , /LB, or /UB starts to change from high level to low level, whichever is earliest.

Read Write Cycle (Mobile specified RAM)

Parameter	Symbol	MC-242453-B90		MC-242453-B95		MC-242453-B10		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read write cycle time	t_{RWC}		10,000		10,000		10,000	ns	1, 2
Byte write setup time	t_{BWS}	20		20		20		ns	
Byte read setup time	t_{BRS}	20		20		20		ns	

Notes 1. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

2. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a read is performed at the identical address using /UB following a write using /LB with /CEm low level, or when a read is performed using /LB following a write using /UB.

Figure 3. Alternating Mobile specified RAM to Flash Memory Timing Chart

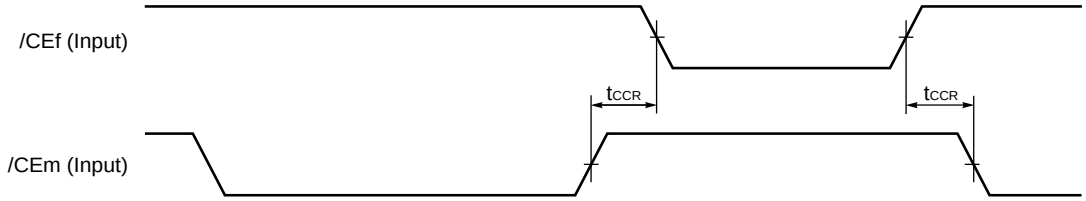


Figure 4. Read Cycle Timing Chart 1 (Flash Memory)

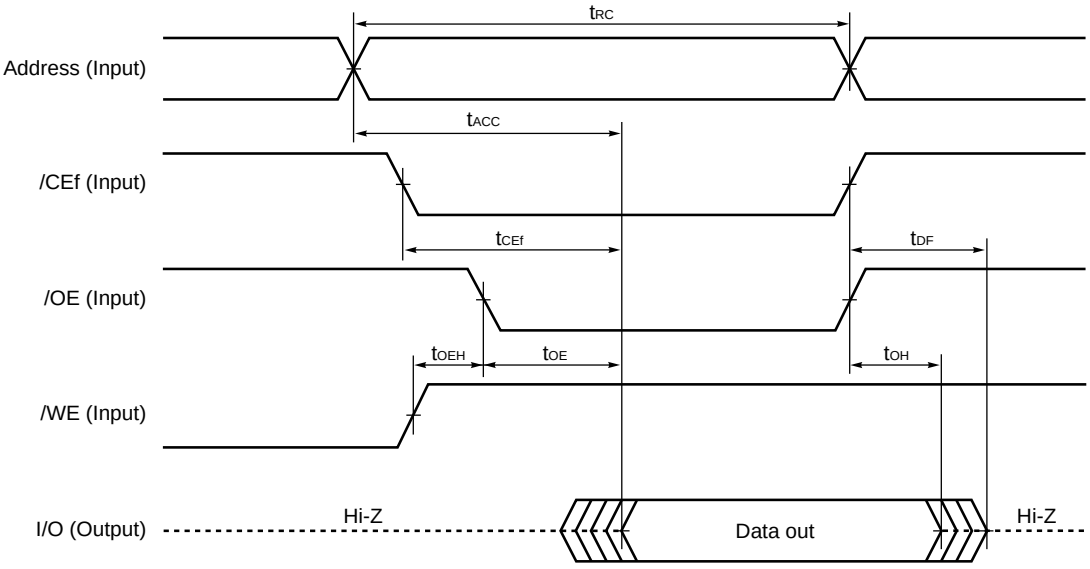


Figure 5. Read Cycle Timing Chart 2 (Flash Memory)

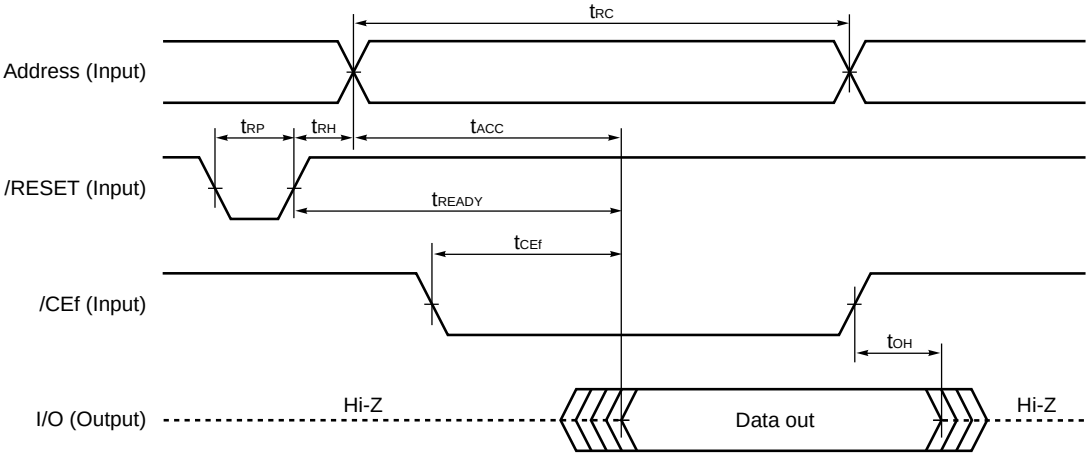
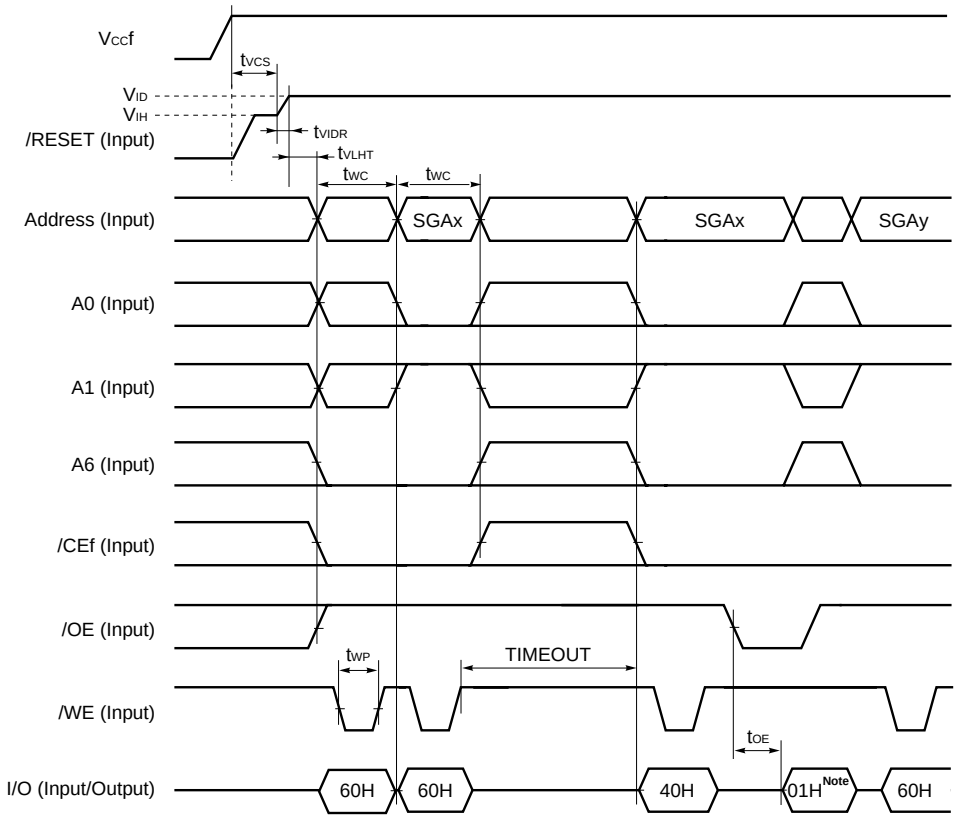


Figure 6. Sector Group Protection Timing Chart (Flash Memory)



Note The sector group protection verification result is output.

01H : The sector group is protected.

00H : The sector group is not protected.

Figure 7. Temporary Sector Group Unprotect Timing Chart (Flash Memory)

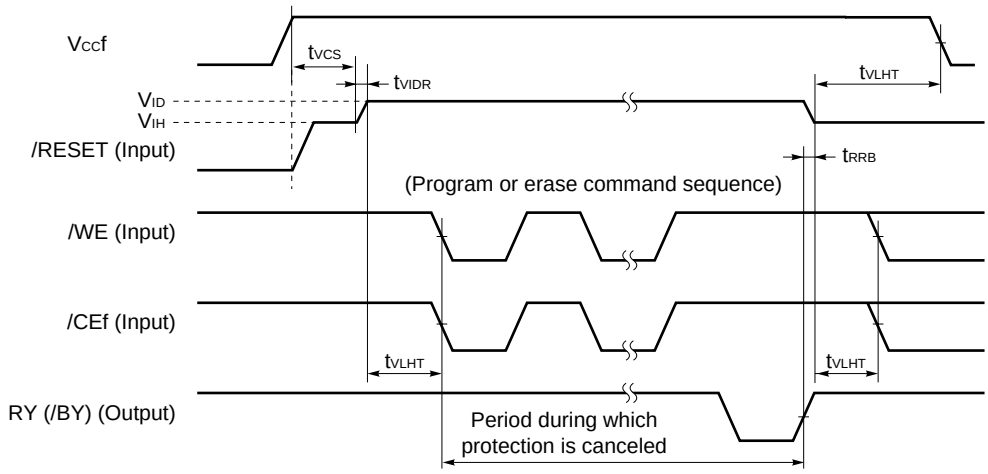


Figure 8. Accelerated Mode Timing Chart (Flash Memory)

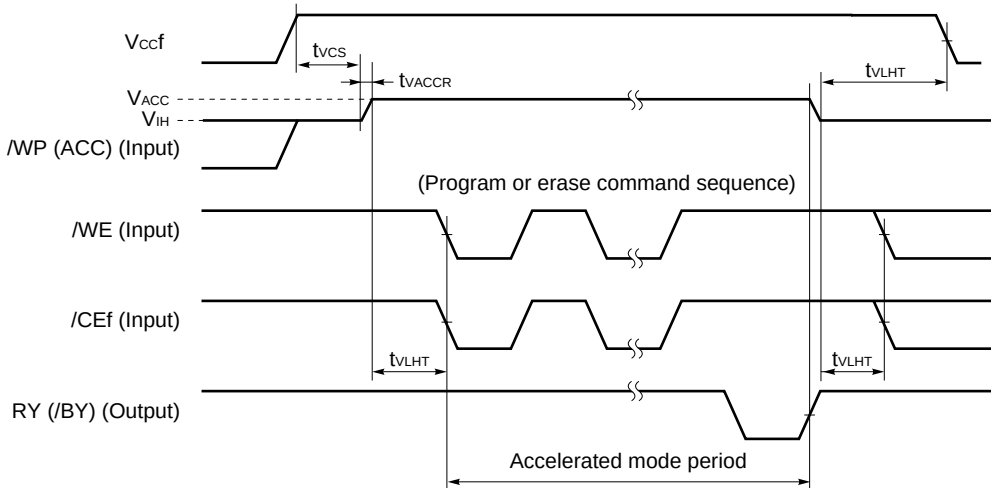


Figure 9. Dual Operation Timing Chart (Flash Memory)

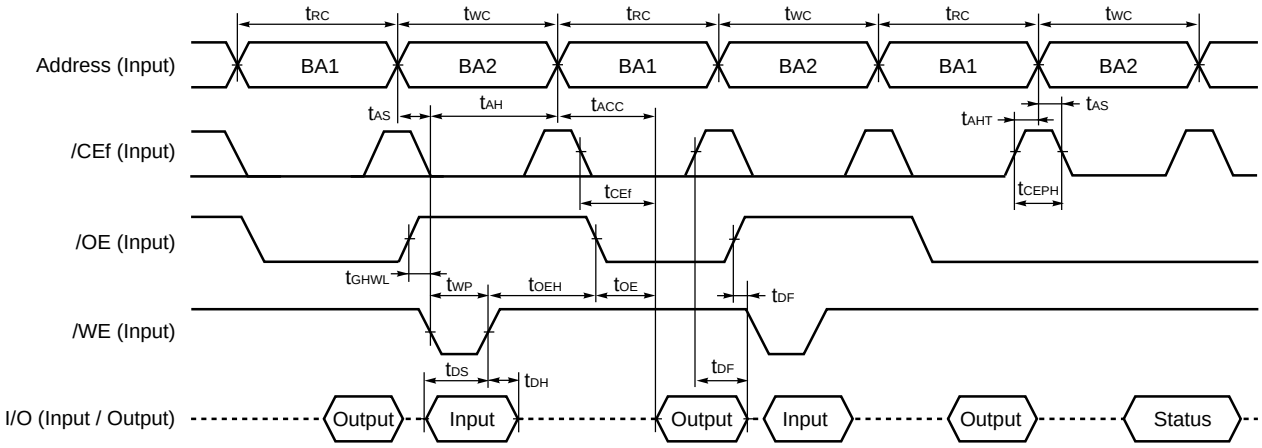
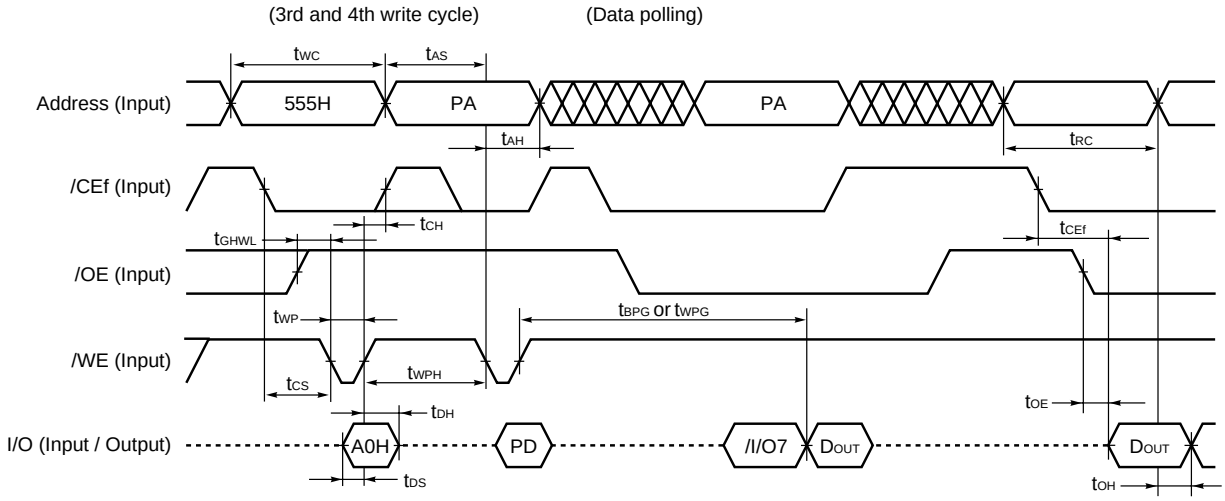


Figure 10. Write Cycle Timing Chart (/WE Controlled) (Flash Memory)

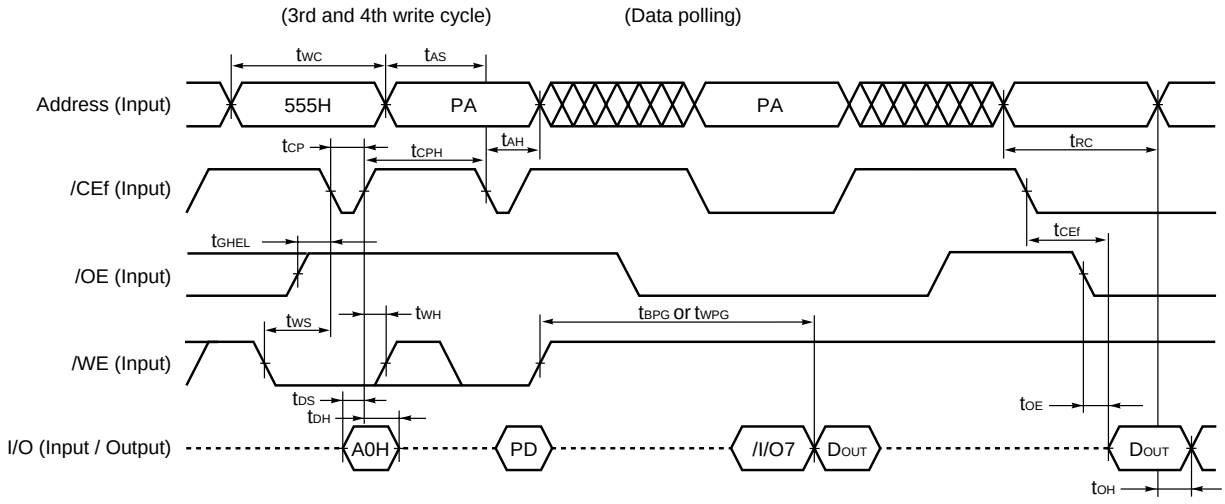


Remarks 1. This timing chart shows the last two write cycles among the program command sequence's four write cycles, and data polling.

2. This timing chart shows the WORD mode's case. In the BYTE mode, address to be input are different from the WORD mode. See **Command Sequence (Flash Memory)**.

3. PA : Program address
PD : Program data
/I/O7 : The output of the complement of the data written to the device.
DOUT : The output of the data written to the device.

Figure 11. Write Cycle Timing Chart (/CEf Controlled) (Flash Memory)

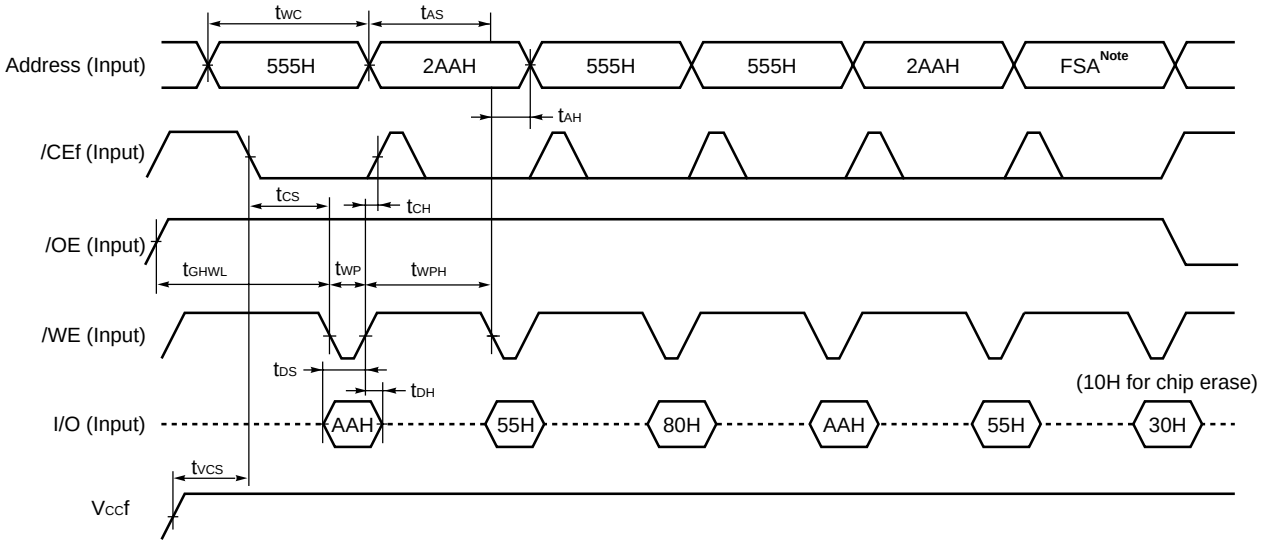


Remarks 1. This timing chart shows the last two write cycles among the program command sequence's four write cycles, and data polling.

2. This timing chart shows the WORD mode's case. In the BYTE mode, address to be input are different from the WORD mode. See **Command Sequence (Flash Memory)**.

3. PA : Program address
PD : Program data
/I/O7 : The output of the complement of the data written to the device.
DOUT : The output of the data written to the device.

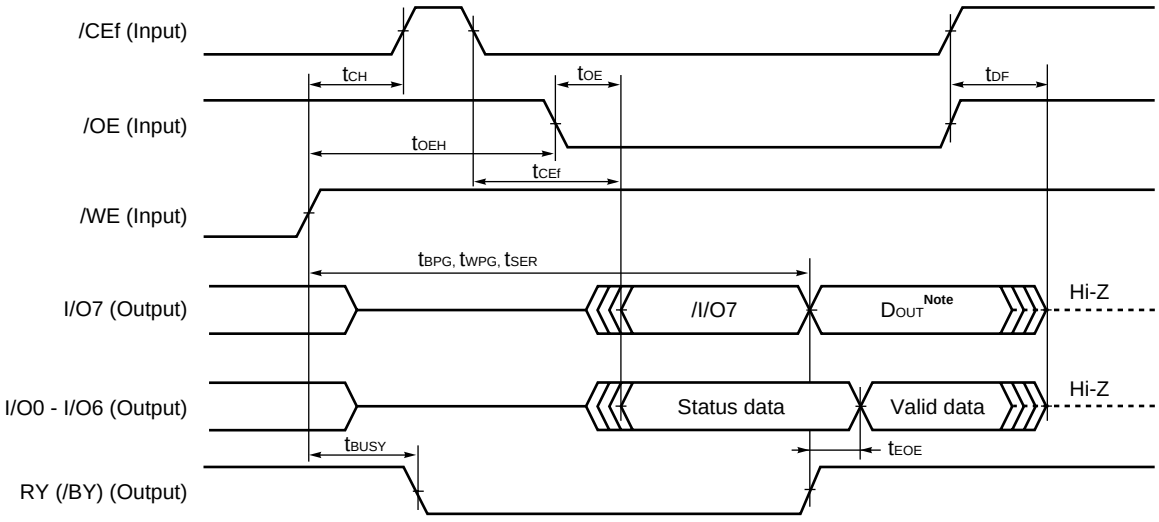
Figure 12. Sector / Chip Erase Timing Chart (Flash Memory)



Note FSA is the sector address to be erased. In the case of chip erase, input 555H (WORD mode), AAAH (BYTE mode).

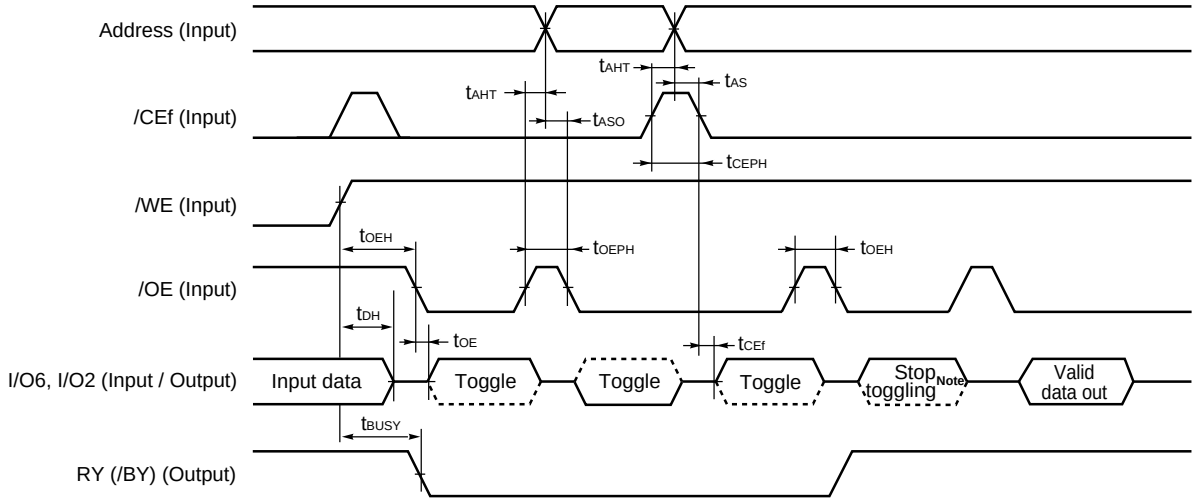
Remark This timing chart shows the WORD mode's case. In the BYTE mode, address to be input are different from the WORD mode. See **Command Sequence (Flash Memory)**.

Figure 13. Data Polling Timing Chart (Flash Memory)



Note I/O7 = D_{OUT} : True value of program data (indicates completion of automatic program / erase)

Figure 14. Toggle Bit Timing Chart (Flash Memory)



Note I/O6 stops the toggle (indicates automatic program / erase completion).

Figure 15. I/O2 vs. I/O6 Timing Chart (Flash Memory)

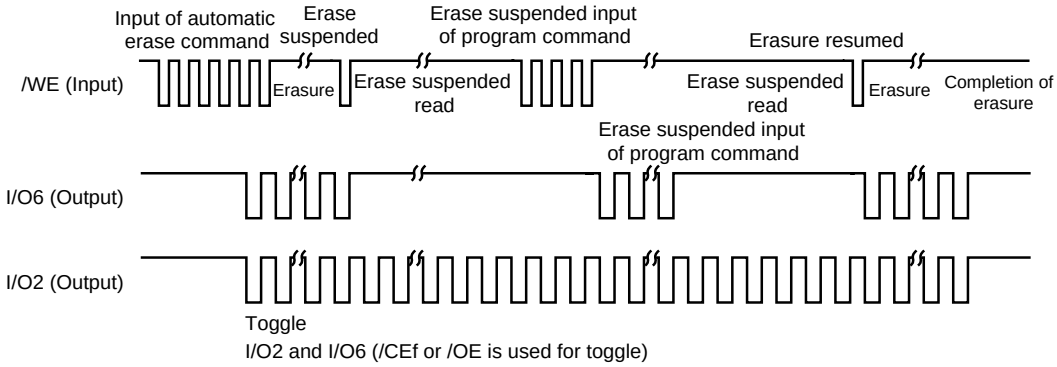


Figure 16. RY (/BY) (Ready / Busy) Timing Chart (Flash Memory)

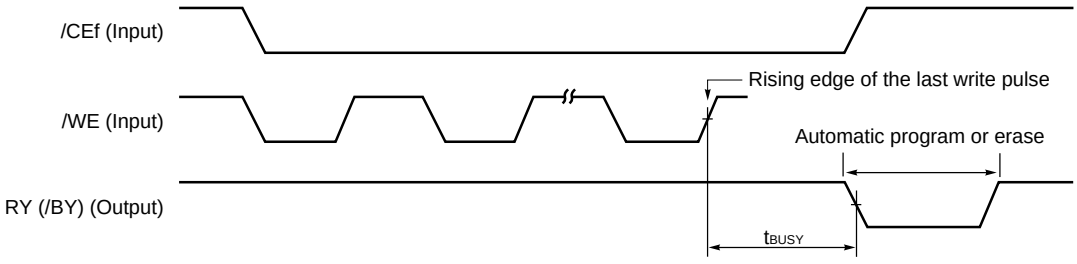


Figure 17. /RESET and RY (/BY) Timing Chart (Flash Memory)

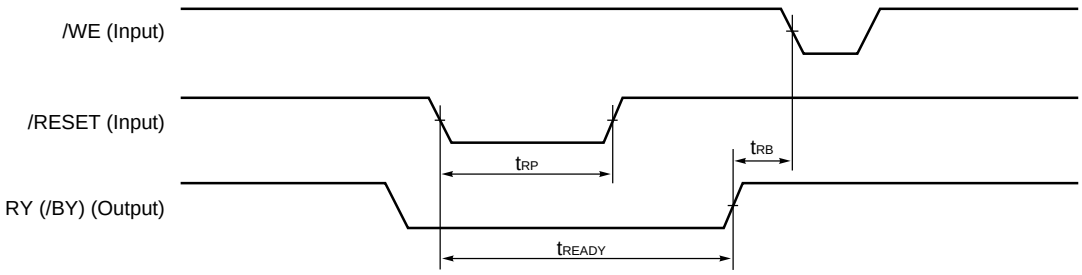


Figure 18. Write CIOf Timing Chart (Flash Memory)

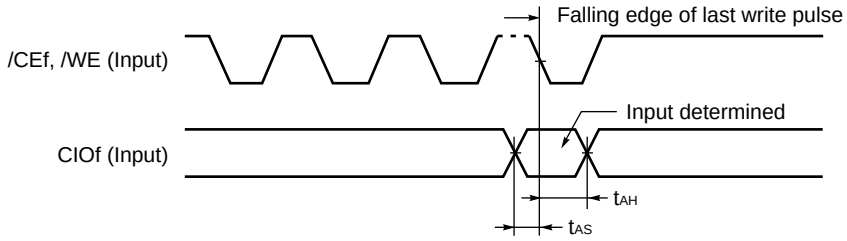


Figure 19. BYTE mode Switching Timing Chart (Flash Memory)

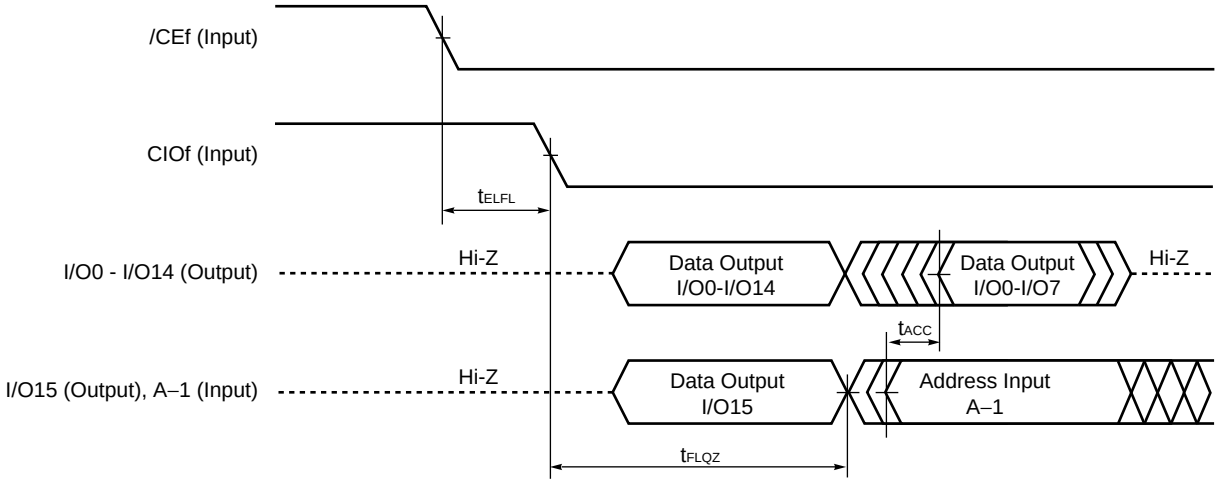


Figure 20. WORD mode Switching Timing Chart (Flash Memory)

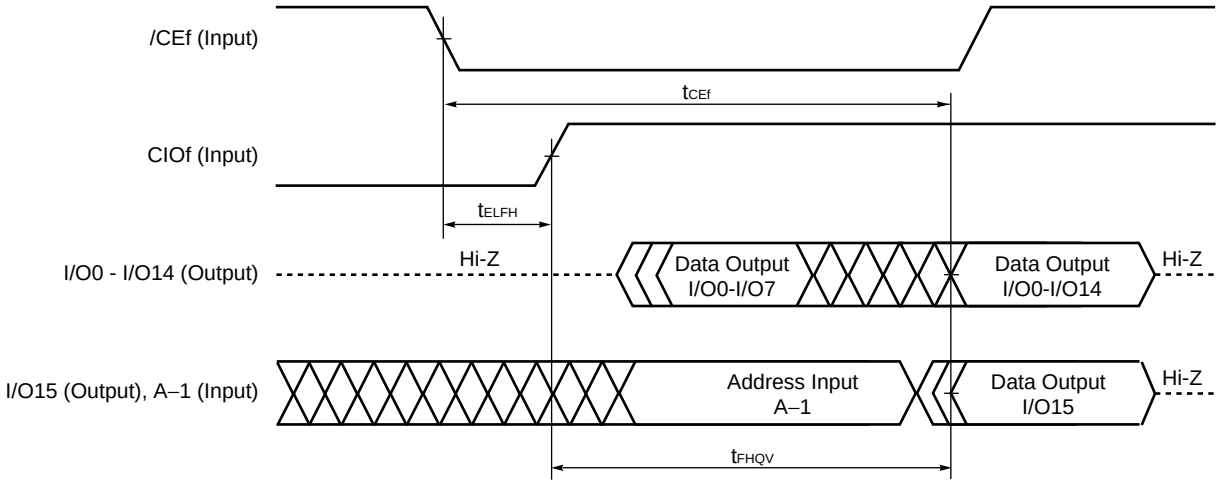
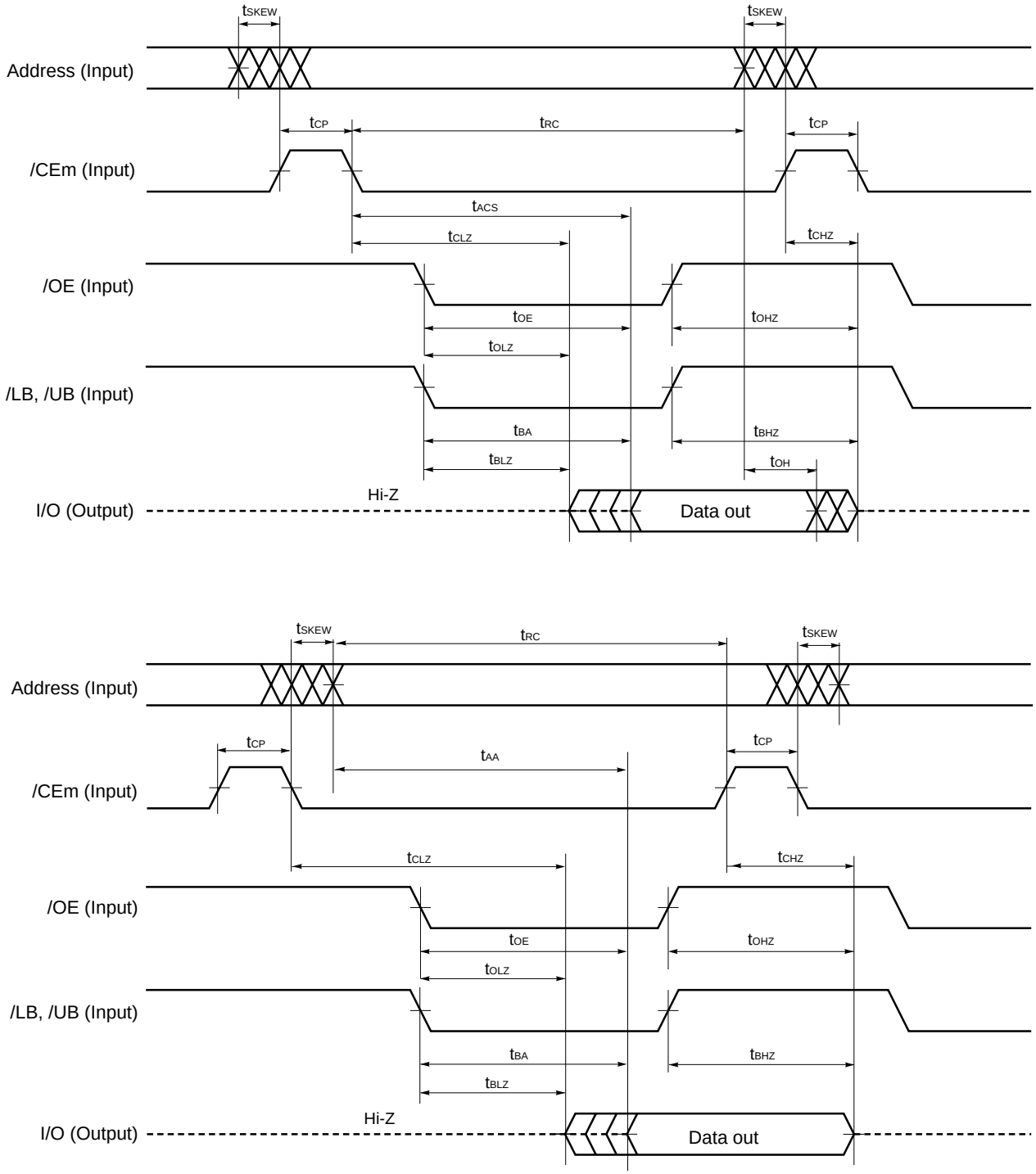


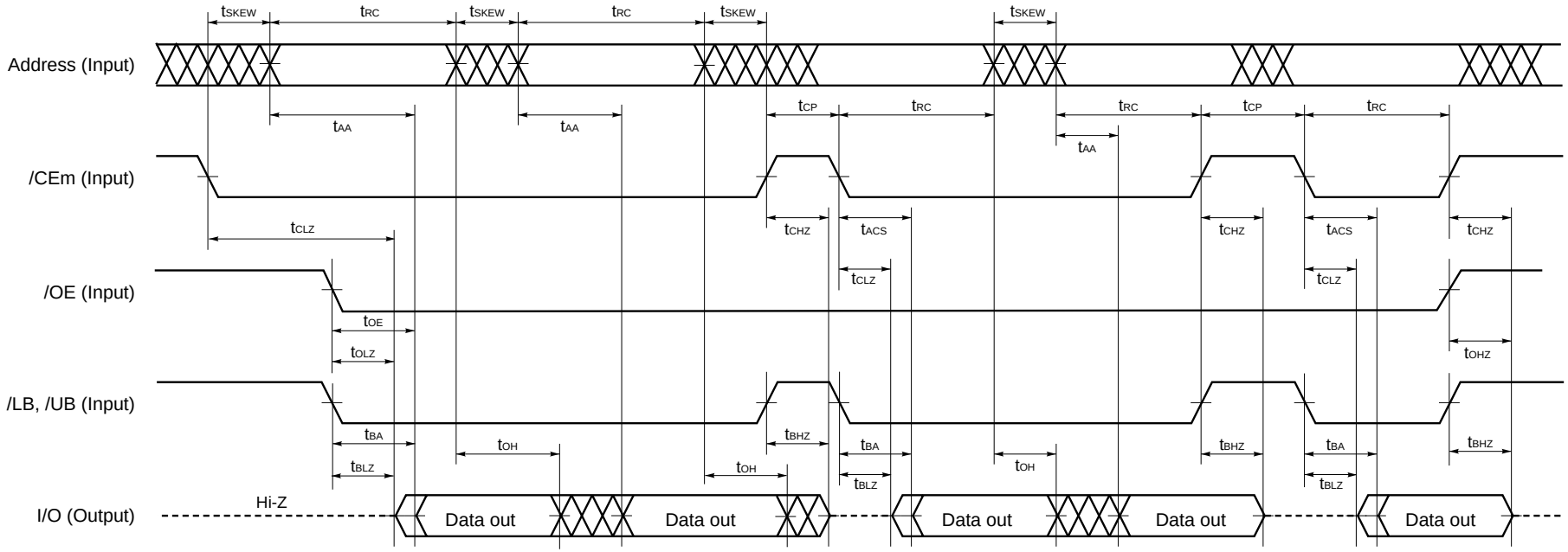
Figure 21. Read Cycle Timing Chart 1 (Mobile specified RAM)



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

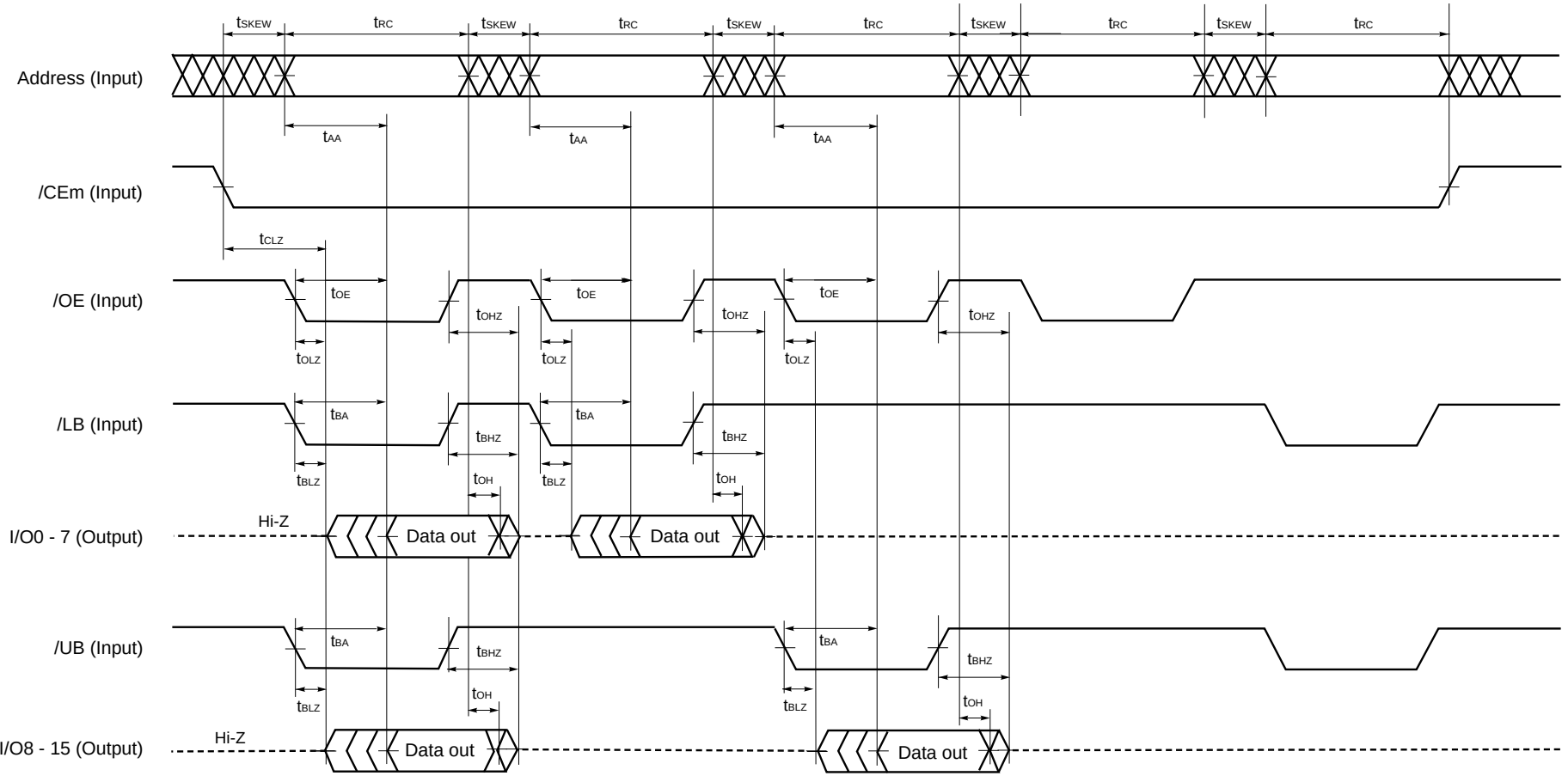
Figure 22. Read Cycle Timing Chart 2 (Mobile specified RAM)



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

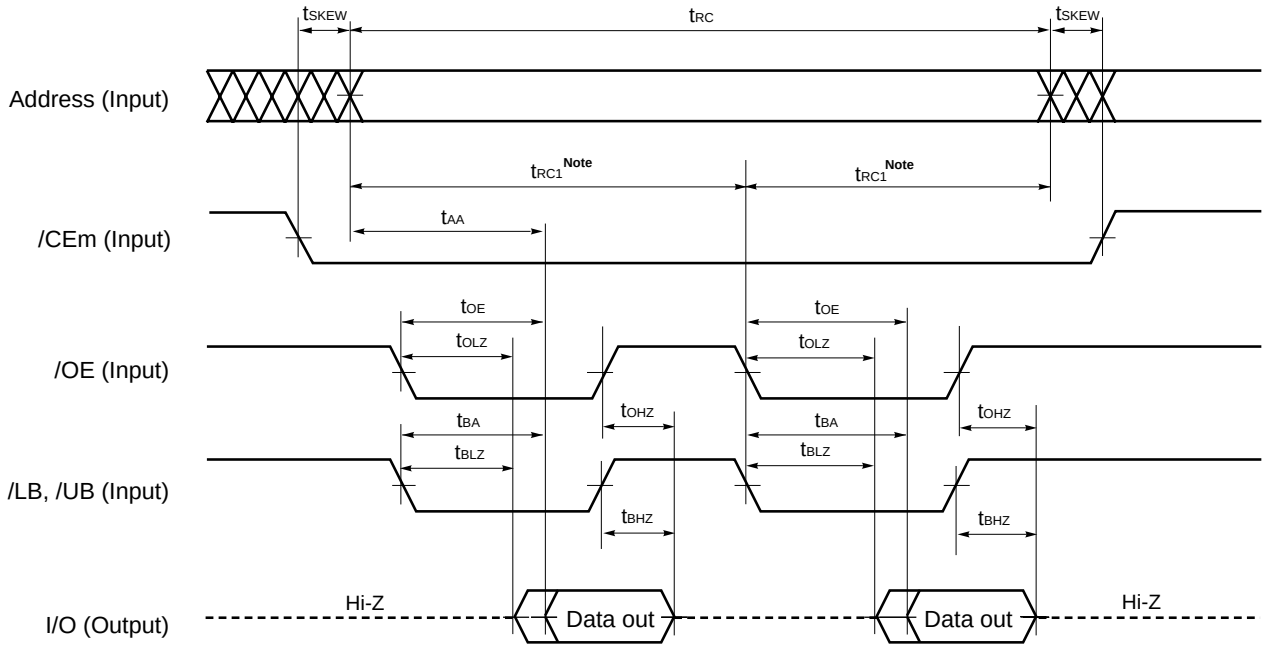
Figure 23. Read Cycle Timing Chart 3 (Mobile specified RAM)



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

Figure 24. Read Cycle Timing Chart 4 (Mobile specified RAM)

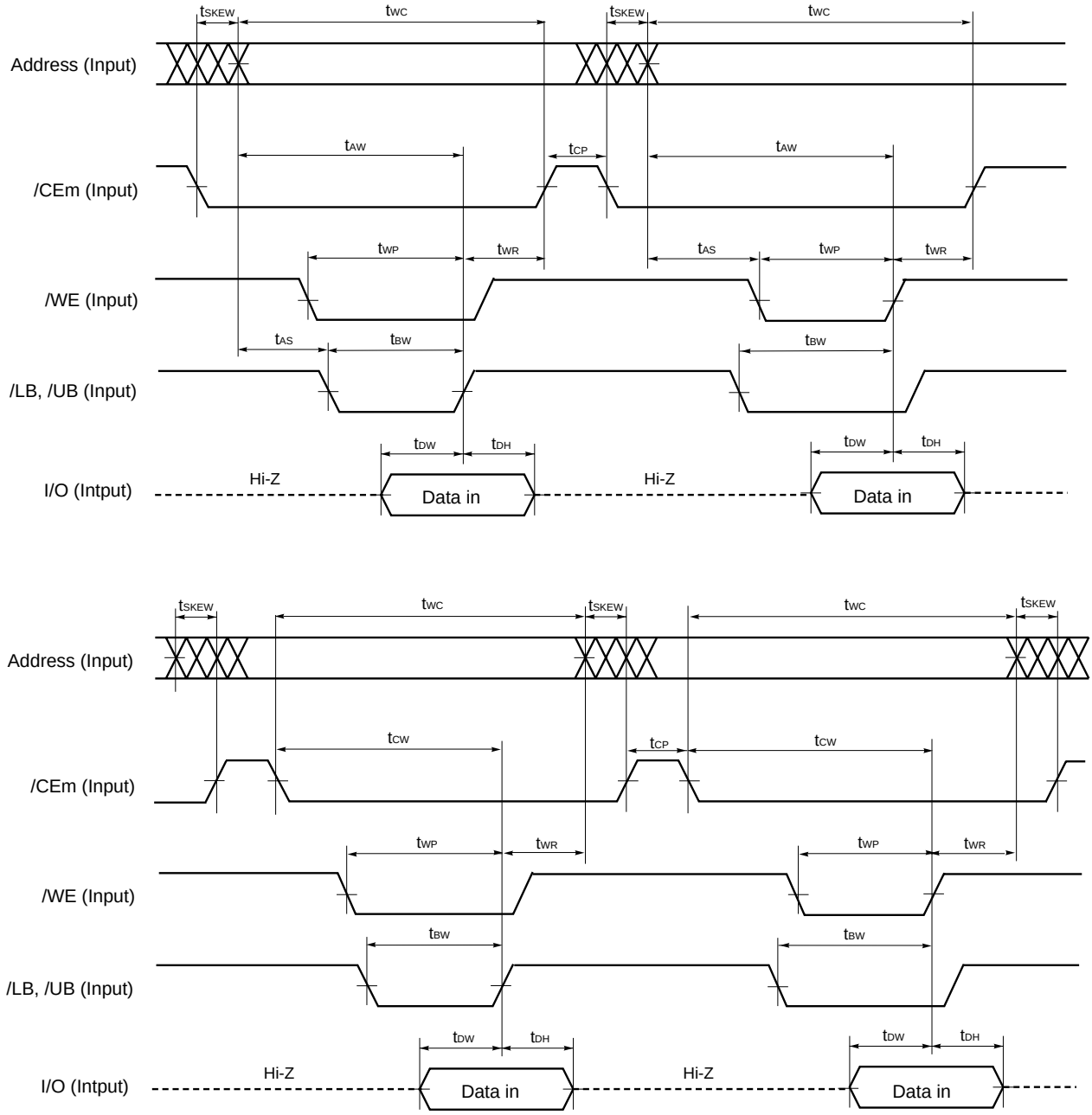


Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Note To perform a continuous read toggling /OE, /UB, and /LB with /CEm low level at an identical address, make settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

Remark In read cycle, /WE should be fixed to High.

Figure 25. Write Cycle Timing Chart 1 (Mobile specified RAM)



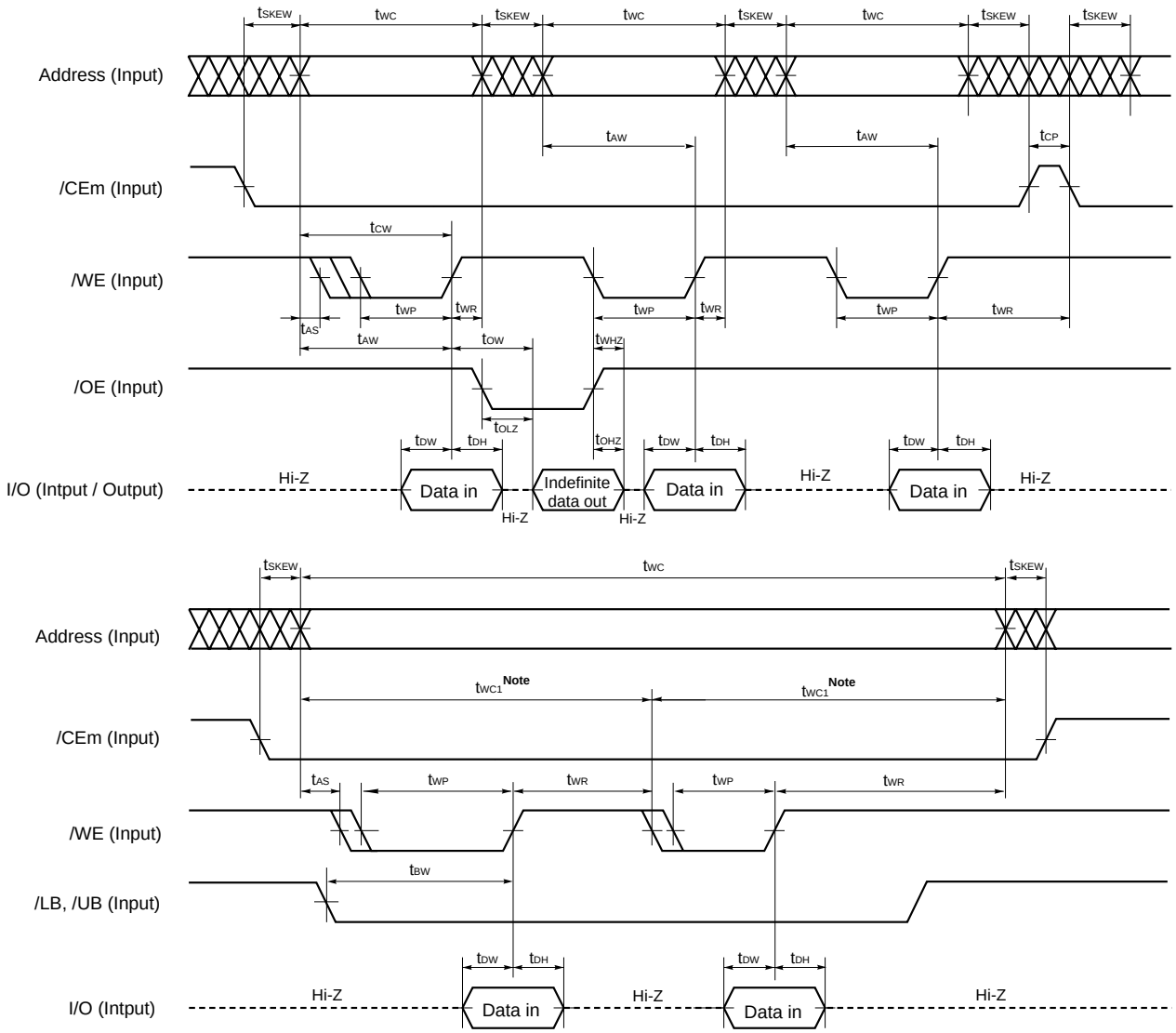
Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 26. Write Cycle Timing Chart 2 (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

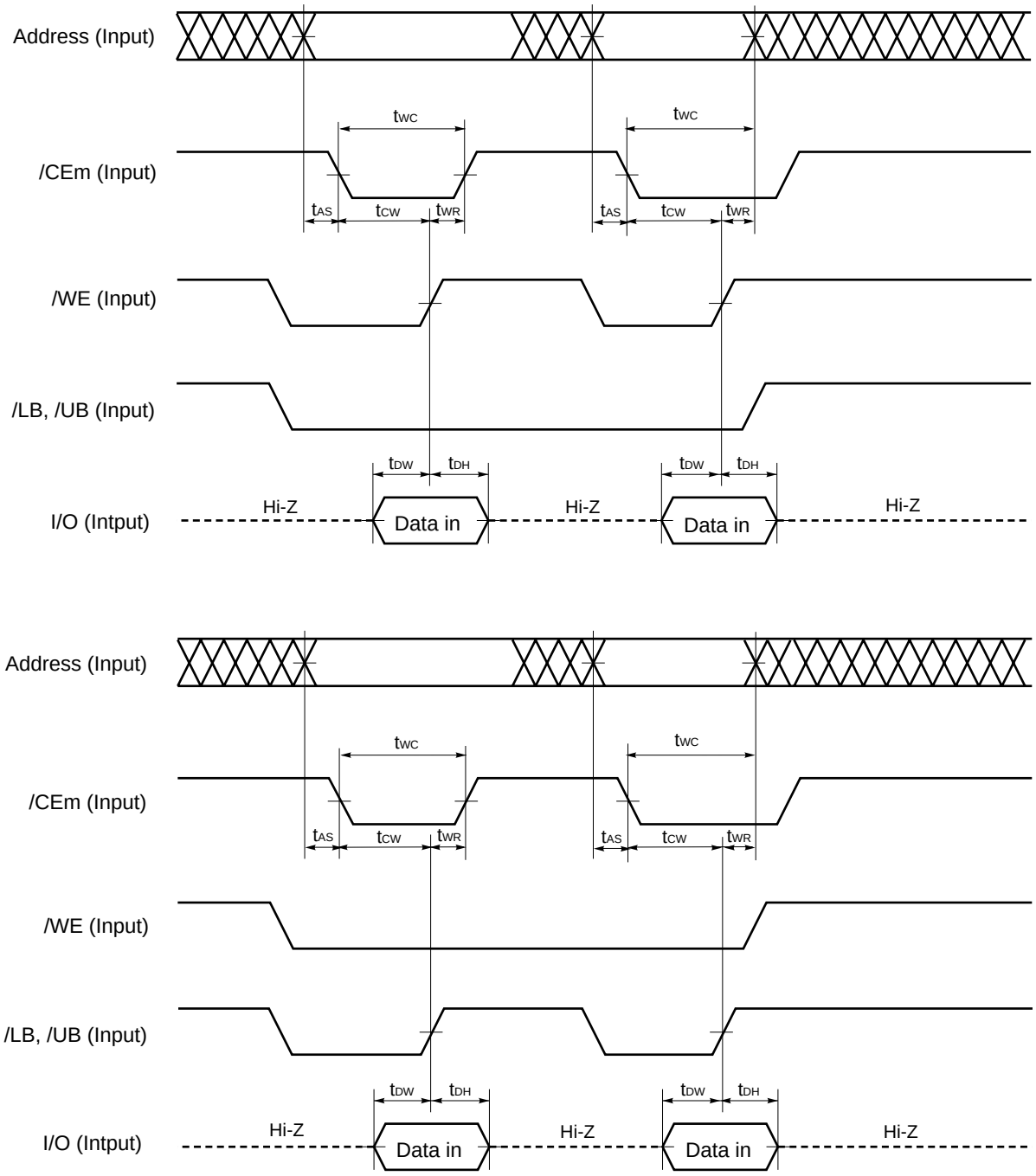
3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CEm low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remarks 1. Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

2. When /WE is at Low, the I/O pins are always high impedance. When /WE is at High, read operation is executed. Therefore /OE should be at High to make the I/O pins high impedance.

Figure 27. Write Cycle Timing Chart 3 (/CEm Controlled) (Mobile specified RAM)



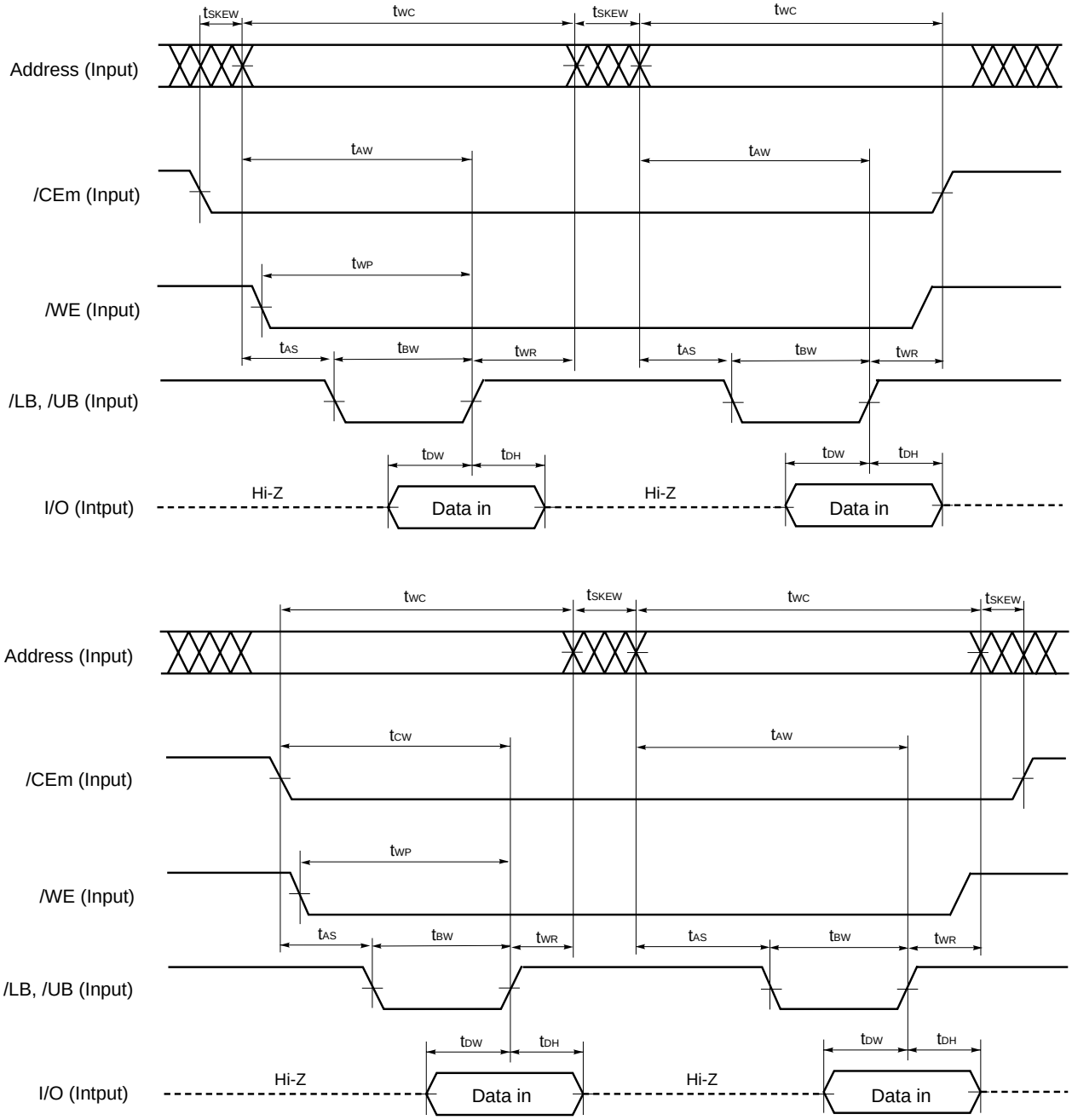
Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 28. Write Cycle Timing Chart 4 (/LB, /UB Controlled 1) (Mobile specified RAM)



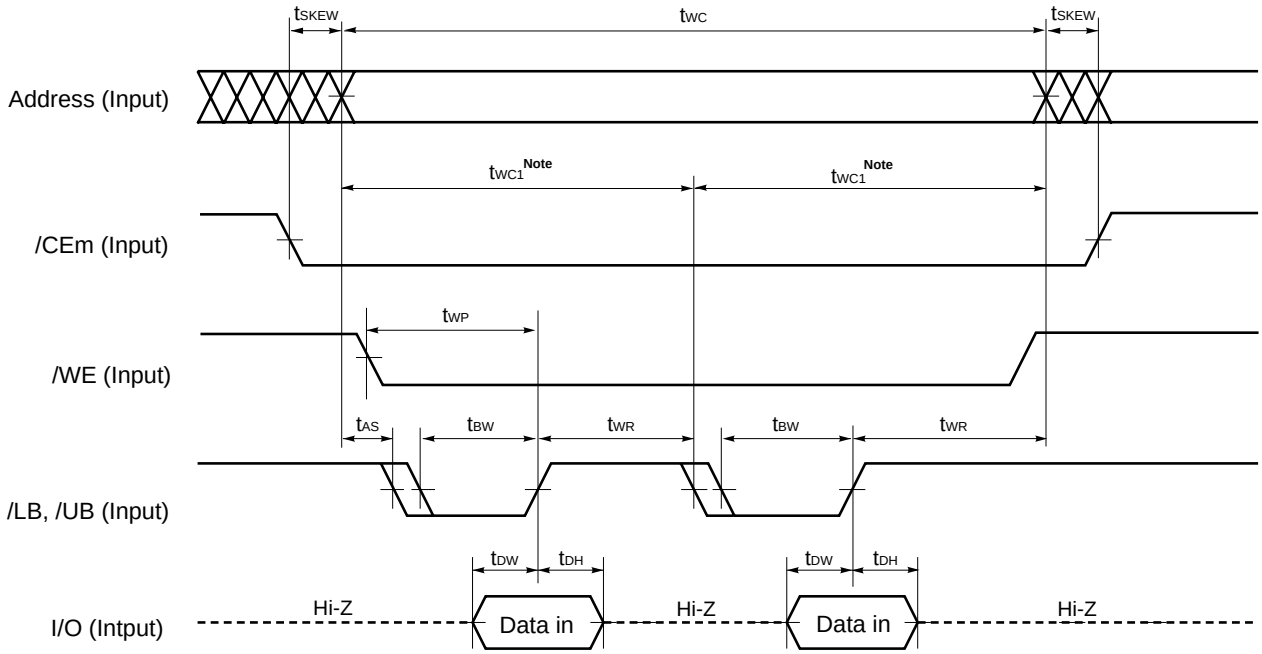
Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 29. Write Cycle Timing Chart 5 (/LB, /UB Controlled 2) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

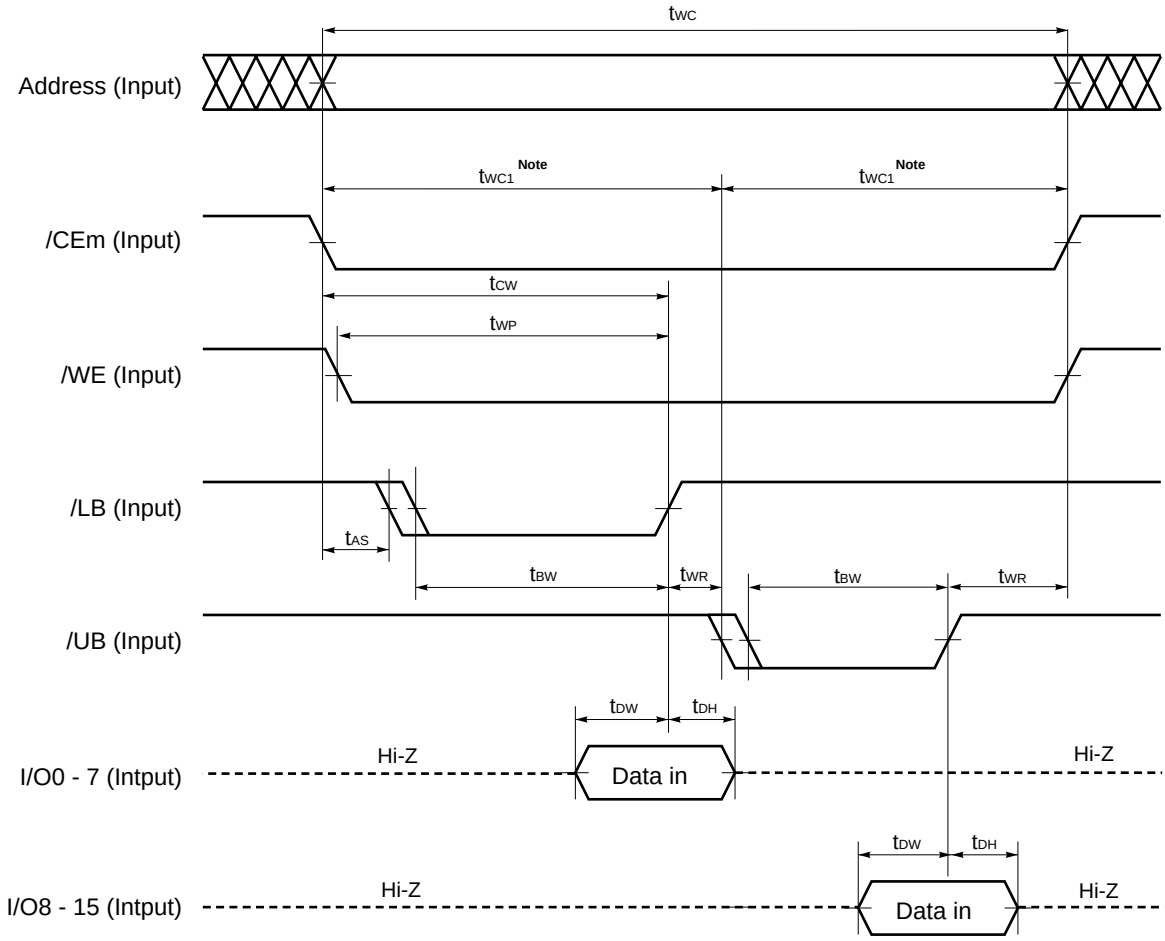
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CEm low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 30. Write Cycle Timing Chart 6 (/LB, /UB Independent Controlled 1) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

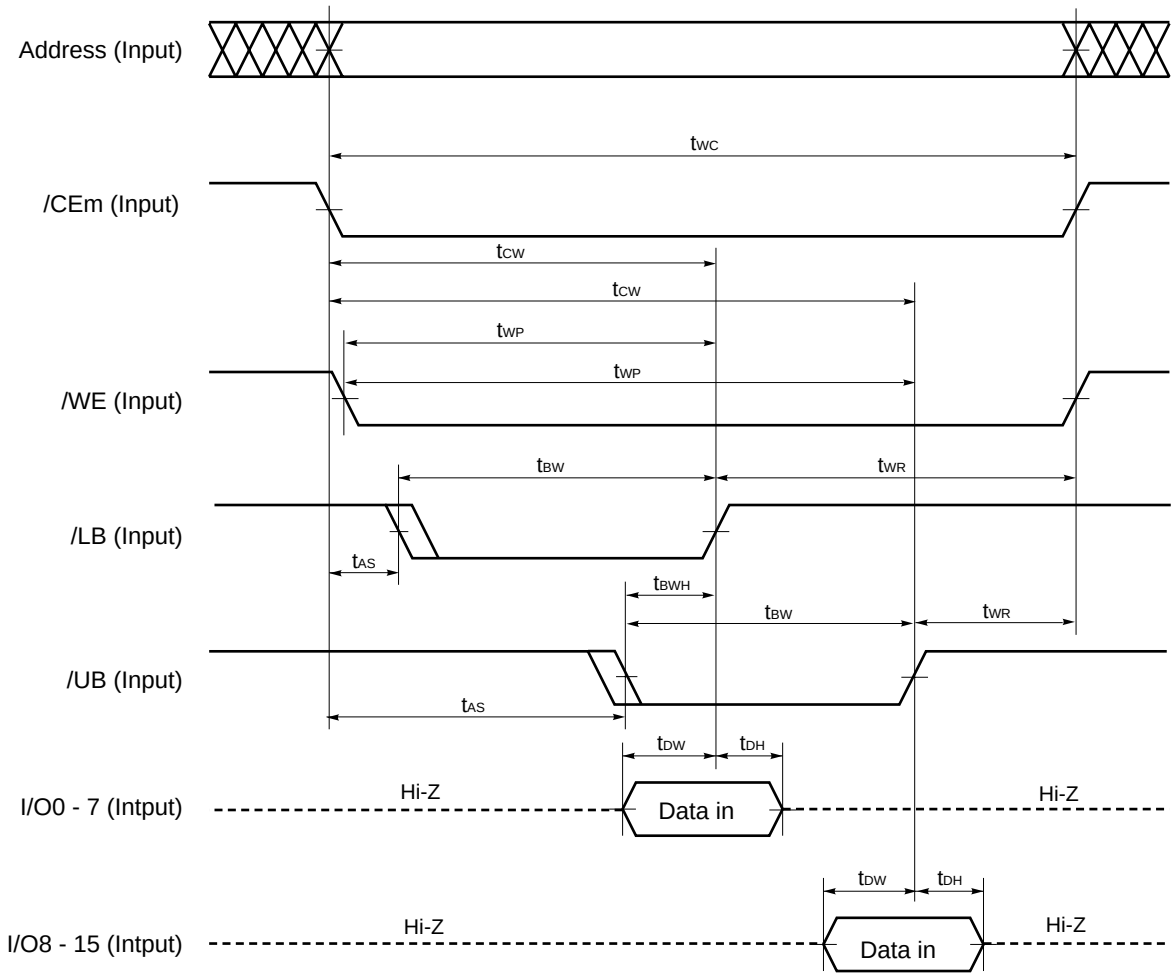
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CEm low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 31. Write Cycle Timing Chart 7 (/LB, /UB Independent Controlled 2) (Mobile specified RAM)



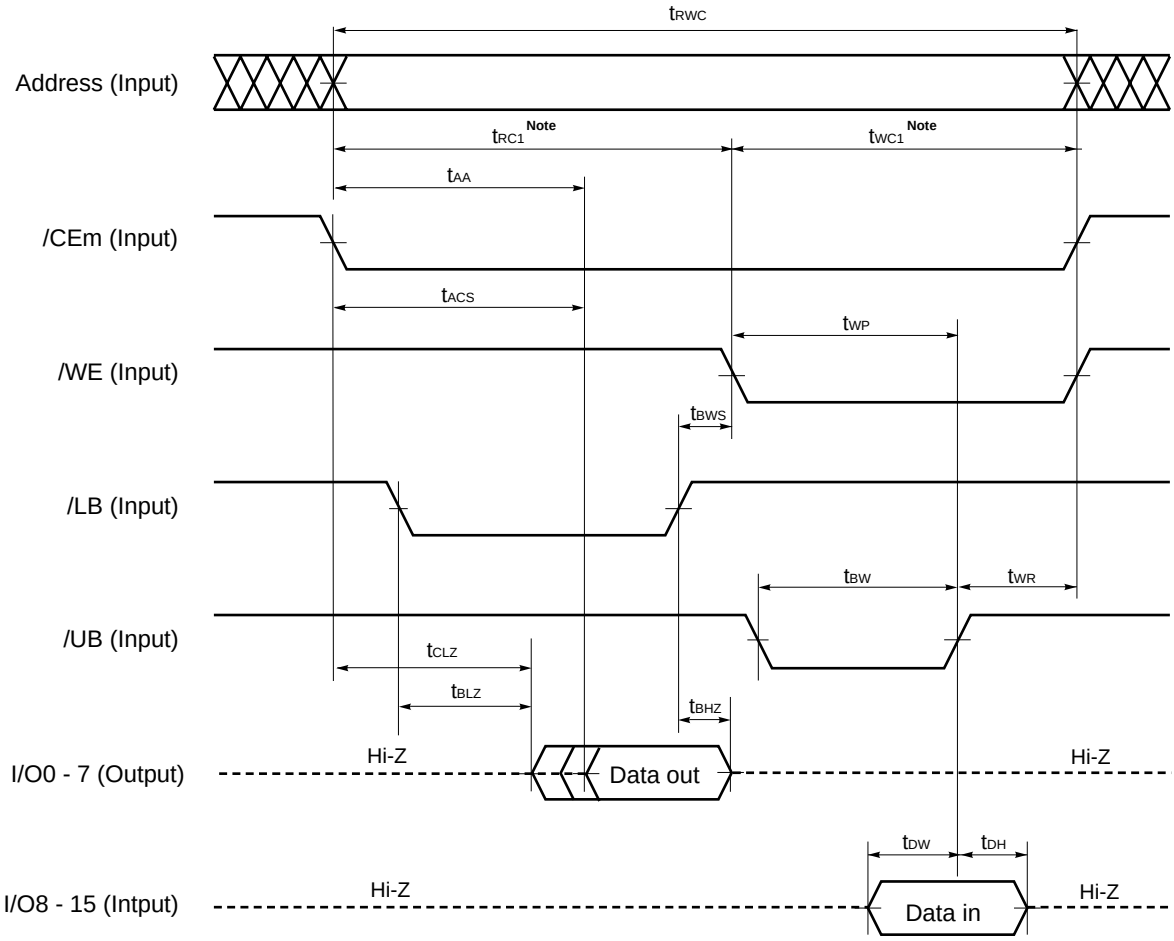
Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 32. Read Write Cycle Timing Chart 1 (/LB, /UB Independent Controlled 1) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

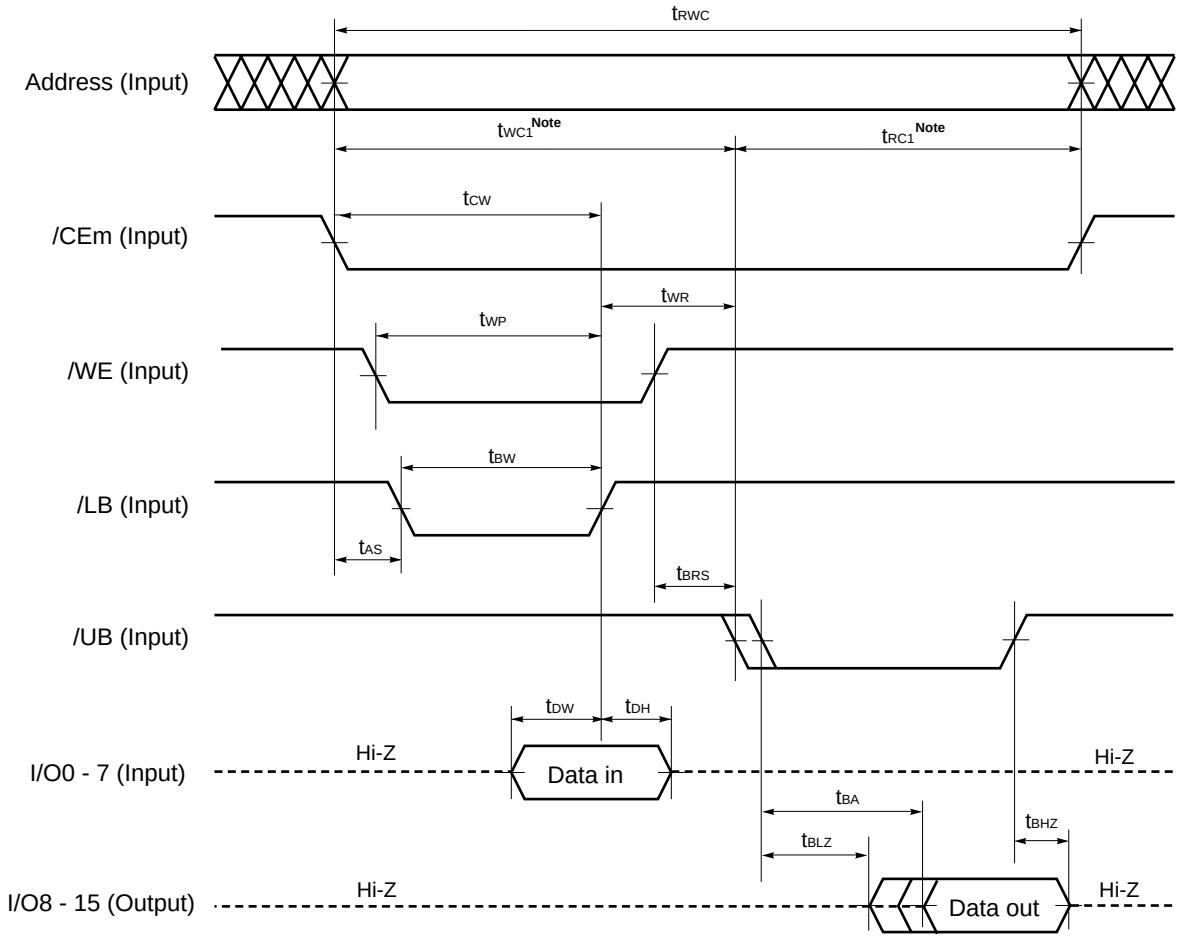
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 33. Read Write Cycle Timing Chart 2 (/LB, /UB Independent Controlled 2) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

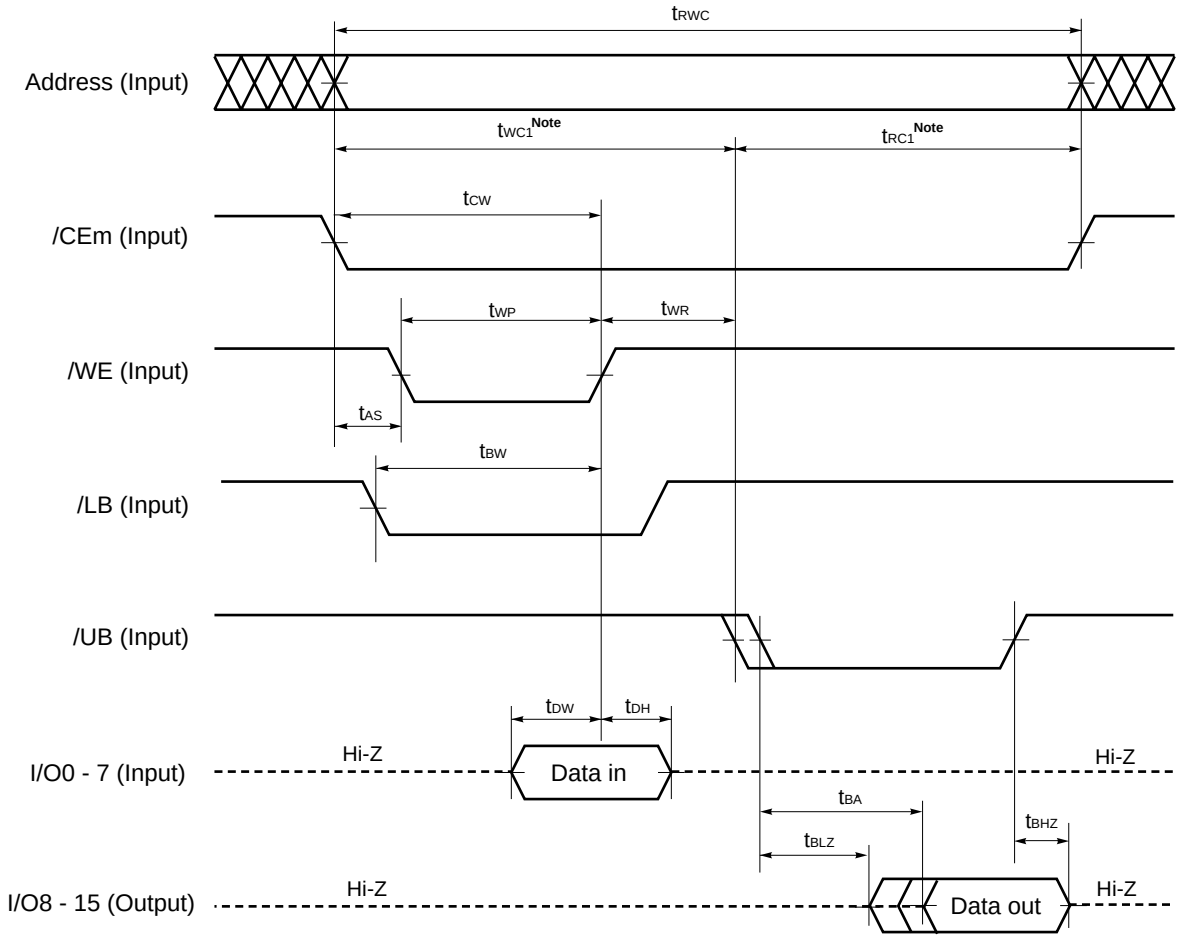
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 34. Read Write Cycle Timing Chart 3 (/LB, /UB Independent Controlled 3) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

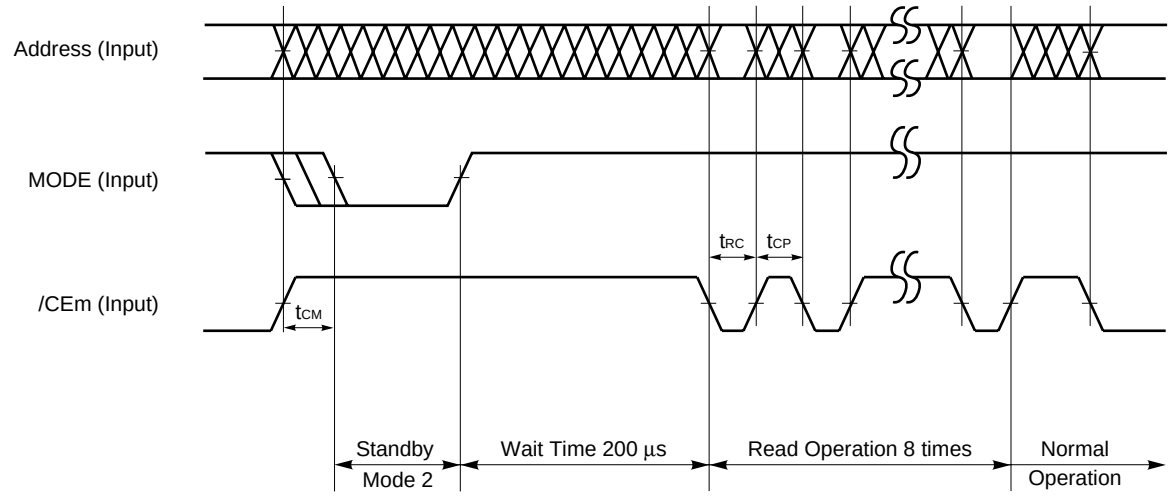
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 35. Standby Mode 2 entry and recovery Timing Chart (Mobile specified RAM)



Parameter	Symbol	MIN.	MAX.	Unit	Note
/CEm High to MODE Low	t_{CM}	0		ns	

Cautions 1. Make MODE and /CEm high level during the wait time.

2. Make MODE high level during the wait time and eight read operations.

3. The read operation must satisfy the specs described on page 21 (Read Cycle (Mobile specified RAM)).

4. The read operation address can be either V_{IH} or V_{IL}.

5. Perform reading by toggling /CEm.

6. To prevent bus contention, it is recommended to set /OE to high level. However, do not input data to the I/O pins if /OE is low level during a read operation.

★ **Flow Charts (Flash Memory)**

Refer to **DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information (M14914E).**

CFI Code List

(1/2)

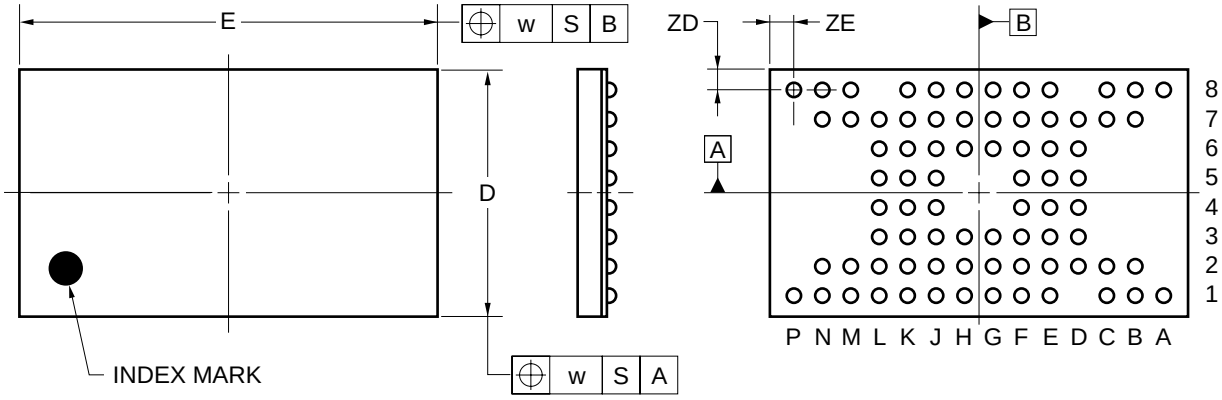
Address A6 to A0	Data I/O15 to I/O0	Description
10H	0051H	"QRY" (ASCII code)
11H	0052H	
12H	0059H	
13H	0002H	Main command set
14H	0000H	2 : AMD/FJ standard type
15H	0040H	Start address of PRIMARY table
16H	0000H	
17H	0000H	Auxiliary command set
18H	0000H	00H : Not supported
19H	0000H	Start address of auxiliary algorithm table
1AH	0000H	
1BH	0027H	Minimum V_{CC}f voltage (program / erase) I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
1CH	0036H	Maximum V_{CC}f voltage (program / erase) I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
1DH	0000H	Minimum V_{PP} voltage
1EH	0000H	Maximum V_{PP} voltage
1FH	0004H	Typical word program time (2^N μs)
20H	0000H	Typical buffer program time (2^N μs)
21H	000AH	Typical sector erase time (2^N ms)
22H	0000H	Typical chip erase time (2^N ms)
23H	0005H	Maximum word program time (typical time $\times$ 2^N)
24H	0000H	Maximum buffer program time (typical time $\times$ 2^N)
25H	0004H	Maximum sector erasing time (typical time $\times$ 2^N)
26H	0000H	Maximum chip erasing time (typical time $\times$ 2^N)
27H	0016H	Capacity (2^N Bytes)
28H	0002H	I/O information
29H	0000H	2 : $\times$8/$\times$16-bit organization
2AH	0000H	Maximum number of bytes when two banks are programmed (2^N)
2BH	0000H	
2CH	0002H	Type of erase block
2DH	0007H	Information about erase block 1
2EH	0000H	Bit0 to 15 : y = number of sectors
2FH	0020H	Bit16 to 31 : z = size
30H	0000H	(Z $\times$ 256 Bytes)

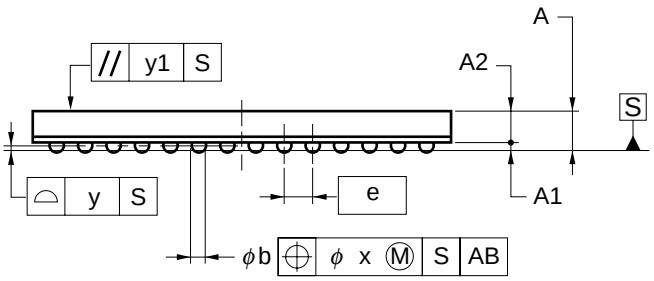
(2/2)

Address A6 to A0	Data I/O15 to I/O0	Description
31H	003EH	Information about erase block 2
32H	0000H	bit0 to 15 : y = number of sectors
33H	0000H	bit16 to 31 : z = size
34H	0001H	(z × 256 Bytes)
40H	0050H	"PRI" (ASCII code)
41H	0052H	
42H	0049H	
43H	0031H	Main version (ASCII code)
44H	0032H	Minor version (ASCII code)
45H	0000H	Address during command input 00H : Necessary 01H : Unnecessary
46H	0002H	Temporary erase suspend function 00H : Not supported 01H : Read only 02H : Read / Program
47H	0001H	Sector group protection 00H : Not supported 01H : Supported
48H	0001H	Temporary sector group protection 00H : Not supported 01H : Supported
49H	0004H	Sector group protection algorithm
4AH	00xxH	Number of sectors of bank 2 00H : Not supported 30H : MC-242453
4BH	0000H	Burst mode 00H : Not supported
4CH	0000H	Page mode 00H : Not supported
4DH	0085H	Minimum V_{ACC} voltage I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
4EH	0095H	Maximum V_{ACC} voltage I/O7 to I/O4 : 1 V/bit I/O3 to I/O0 : 100 mV/bit
4FH	00xxH	Boot organization 02H : Bottom boot
50H	0001H	Temporary program suspend function 00H : Not supported 01H : Supported

Package Drawings

77-PIN TAPE FBGA (12x7)

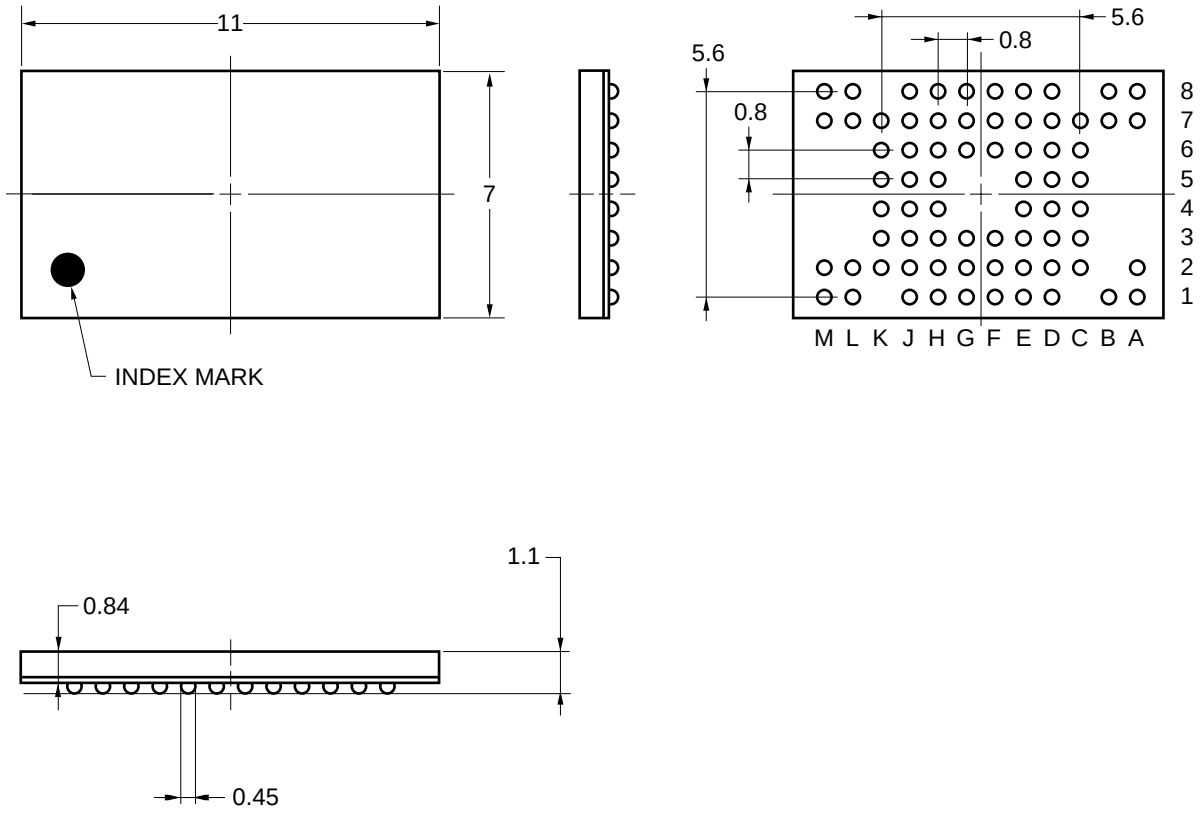




ITEM	MILLIMETERS
D	7.0±0.1
E	12.0±0.1
w	0.2
A	1.1±0.1
A1	0.26±0.05
A2	0.84
e	0.8
b	0.45±0.05
x	0.08
y	0.1
y1	0.1
ZD	0.7
ZE	0.8

P77F9-80-BT3

★ 71-PIN TAPE FBGA (11x7) (unit: mm)



These specifications are typical values.
This package drawing is a preliminary version. It may be changed in the future.

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the MC-242453.

★ **Types of Surface Mount Device**

MC-242453F9-B90-BT3 : 77-pin TAPE FBGA (12 × 7)

MC-242453F9-B95-BT3 : 77-pin TAPE FBGA (12 × 7)

MC-242453F9-B10-BT3 : 77-pin TAPE FBGA (12 × 7)

MC-242453F9-B90-BS1 : 71-pin TAPE FBGA (11 × 7)

MC-242453F9-B95-BS1 : 71-pin TAPE FBGA (11 × 7)

MC-242453F9-B10-BS1 : 71-pin TAPE FBGA (11 × 7)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related Documents

Document Name	Document Number
DUAL OPERATION FLASH MEMORY 32M BITS A SERIES Information	M14914E

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