

MPV5 Series

9x14 mm, 5.0 Volt, PECL, VCXO



- LVDS and PECL Output Logic With Good Integrated Jitter Performance (5 ps)
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation

Ordering Information

MPV5 1 0 R 1 P J 00.0000 MHz

Product Series _____

Temperature Range _____

1: 0°C to +70°C 2: -40°C to +85°C
 6: -20°C to +70°C 8: 0°C to +50°C

Stability _____

0: Nominal per APR selection

Output Type _____

R: Complementary, Tri-state Z: Complementary, Non Tri-state
 T: Single, Tri-state X: Single, Non Tri-state

Absolute Pull Range _____

1: ±50 ppm (±35 ppm typ. Stability) 2: ±100 ppm (±20 ppm typ. Stability)
 5: ±80 ppm (±25 ppm typ. Stability) 8: ±25 ppm (±50 ppm typ. Stability)

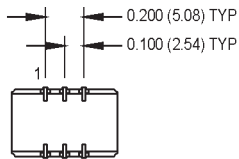
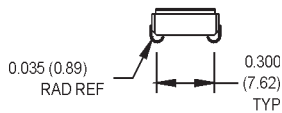
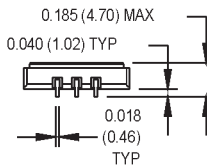
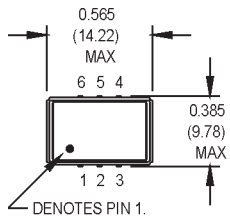
Symmetry/Output Logic Type _____

P: 45/55% PECL Q: 40/60% PECL

Package/Lead Configurations _____

J: J-lead

Frequency (customer specified) _____

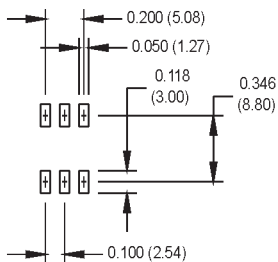


All dimensions in inches (mm).

Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Tri-state or N/C
3	Ground/Case
4	Output Q
5	Output \bar{Q} or N/C
6	+Vcc

SUGGESTED SOLDER PAD LAYOUT



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VCXO

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition	
Frequency Range	F	0.75		800	MHz	See Note 1	
Frequency Stability	$\Delta F/F$	(See Ordering Information)					See Note 2
Operating Temperature	Ts	-40		+85	°C	See ordering info.	
Storage Temperature	Ta	-55		+125	°C		
Input Voltage	Vcc	4.75	5.0	5.25	V		
Input Current	Idd						
0.75 MHz to 24 MHz				60	mA		
24 MHz to 160 MHz				100	mA		
160 MHz to 800 MHz				120	mA		
Symmetry (Duty Cycle)		40	50	60	%	@ Vcc -1.3 VDC	
Load						See Note 3	
Rise/Fall Time	Tr/Tf		.35	.55	ns	@ 20/80%	
Logic "1" Level	Voh	Vcc -1.02			V		
Logic "0" Level	Vol			Vcc -1.63	V		
Cycle to Cycle Jitter						1 Sigma	
@ 38.88 MHz			5.5	7	ps RMS		
@ 155.52 MHz			10	20	ps RMS		
@ 622.08 MHz			10	20	ps RMS		
Phase Jitter	ϕJ					Integrated 12 kHz - 20 MHz	
@ 38.88 MHz			.3	.5	ps RMS		
@ 155.52 MHz			3	5	ps RMS		
@ 622.08 MHz			3	5	ps RMS		
Peak to Peak Jitter (+/-)	Tj					@ BER 1E-12	
@ 38.88 MHz			2.1	3.5	ps RMS		
@ 155.52 MHz			21	35	ps RMS		
@ 622.08 MHz			21	35	ps RMS		
Phase Noise (Typical)						Offset from carrier	
@ 38.88 MHz	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	dBc/Hz	
@ 155.52 MHz	-65	-97	-127	-143	-153	dBc/Hz	
@ 622.08 MHz	-50	-80	-112	-128	-125	dBc/Hz	
						dBc/Hz	
Modulation Bandwidth	fm			10k	Hz	-3 dB bandwidth	
Input Impedance	Zin	50			K Ω		
Control Voltage	Vcc	0.5	2.5	5	V	Pin 1 voltage	
Center Frequency	Vc0		2.5		V		
Linearity			5	10	%		
Pullability	APR	(See Ordering Information)					See Note 4
Tri-state Output "On"	OE	2.8			V	Pin 2 voltage	
Tri-state Output "Off"	OE			0.6	V	Pin 2 voltage	
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C						
Vibration	Per MIL-STD-202, Method 201 & 204						
Reflow Solder Conditions	See "Figure 2" on page 147						
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 ⁻³ atm.cc/s of helium)						
Solderability	Per MIL-STD-883, Method 2003						

1. Frequencies above 70 MHz utilize a PLL design. Fundamental and PLL designs are available for other frequencies. Contact factory.
2. Stability is given for deviation over temperature.
3. PECL load - see load circuit diagram #3 on page 148.
4. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.

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